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ACPL-M60L

Small Outline, 5 Leads, High CMR, High-Speed, Logic Gate Optocouplers

Data Sheet

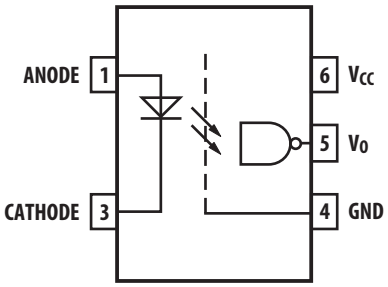
Description

The ACPL-M60L is an optically coupled gate that combines a GaAsP light emitting diode and an integrated high gain photo detector. The output of the detector IC is an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 15 kV/µs at 3.3V operation.

This unique design provides maximum AC and DC circuit isolation while achieving LVTTL/LVCMOS compatibility. The optocoupler AC and DC operational parameters are guaranteed from –40°C to +100°C, allowing trouble-free system performance.

These optocouplers are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Figure 1 Functional Diagram



CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Features

- Dual voltage operation (3.3V/5V)
- 15 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1000V (3.3V operating voltage)
- High speed: 15 MBd typical
- LVTTL/LVCMOS compatible
- Low input current capability: 5 mA
- Guaranteed AC and DC performance over temperature: –40°C to +100°C
- Safety approvals; UL, CSA, IEC/EN/DIN EN 60747-5-5 (Pending)
- Surface mountable
- Very small, low profile JEDEC Registered package outline

Applications

- Isolated line receiver
- Computer-peripheral interfaces
- Microprocessor system interfaces
- Digital isolation for A/D, D/A conversion
- Switching power supply
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement
- Field buses

Ordering Information

ACPL-M60L is UL Recognized with 3750 Vrms for 1 minute per UL1577 and is approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	Option	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant					
ACPL-M60L	-000E	SO-5	X			100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel

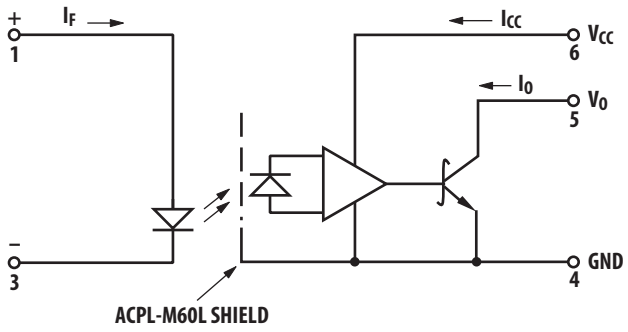
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-M60L-500E to order product of Surface Mount SO-5 in Tape and Reel packaging with RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Figure 2 Schematic

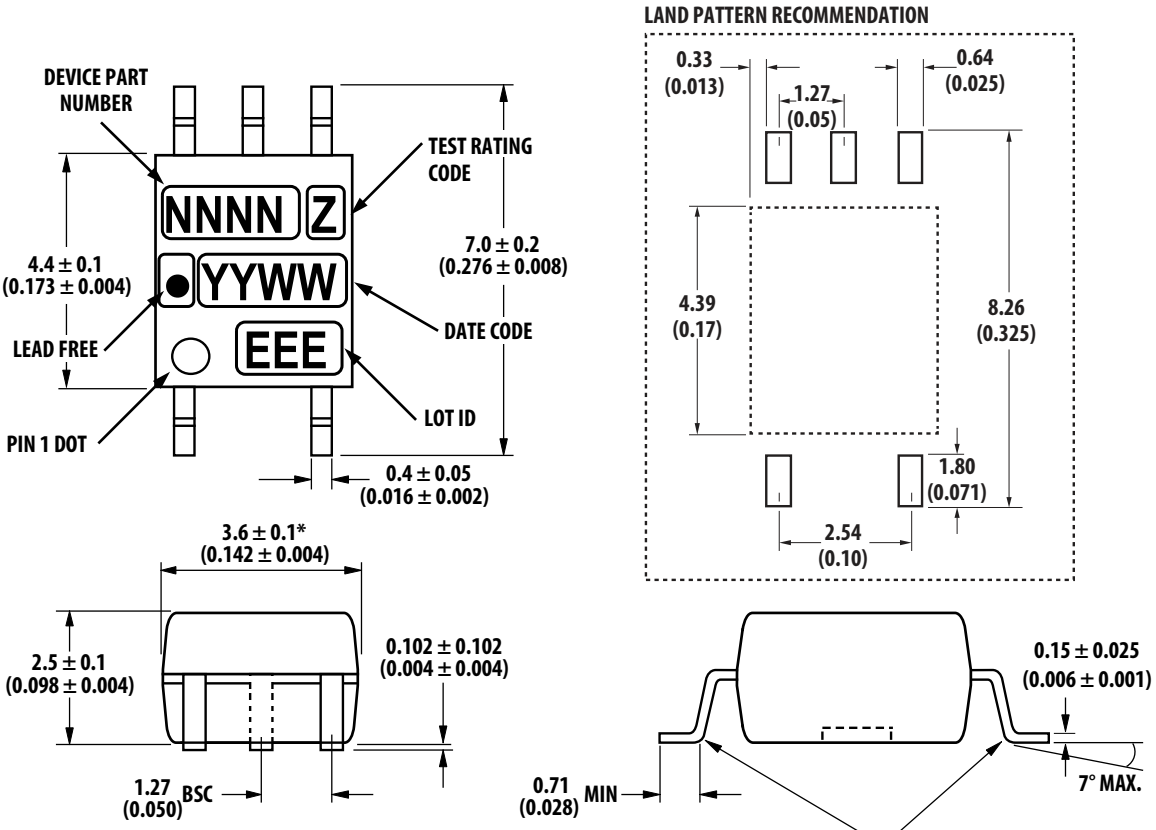


USE OF A 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 6 AND 4 (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

Figure 3 Package Outline Drawing



Dimensions in millimeters (inches).
Note: Foating Lead Protrusion is 0.15 mm (6 mils) max.
*** Maximum Mold flash on each side is 0.15 mm (0.006).**

Solder Reflow Profile

The recommended reflow soldering conditions are per JEDEC Standard J-STD-020 (latest revision). Non-halide flux should be used.

Insulation and Safety-Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L (I01)	5	mm	Measured from input terminals to output terminals
Minimum External Tracking Path (Creepage)	L (I02)	5	mm	Measured from input terminals to output terminals
Minimum Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance, conductor to conductor
Tracking Resistance	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics[a] (Option x60E)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage ≤150 V_{rms} for rated mains voltage ≤ 300 V_{rms} for rated mains voltage ≤ 600 V_{rms}		 I - IV I - IV I - III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	V_{peak}
Input to Output Test Voltage, Method b[a] $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m=1s, Partial discharge < 5 pC	V_{PR}	1063	V_{peak}
Input to Output Test Voltage, Method a[a] $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, t_m=10s, Partial discharge < 5 pC	V_{PR}	907	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60s)	V_{IOTM}	6000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure. Case Temperature Input Current Output Power	 T_S $I_{S, INPUT}$ $P_{S, OUTPUT}$	 175 150 600	 °C ms mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

NOTE These optocouplers are suitable for *safe electrical isolation* only within the safety limit data. Maintenance of the safety limit data shall be ensured by means of protective circuits.

Absolute Maximum Ratings (No Derating Required up to 85°C)

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	125	°C	
Operating Temperature†	T_A	–40	100	°C	
Average Forward Input Current	I_F	—	20	mA	a
Reverse Input Voltage	V_R	—	5	V	
Input Power Dissipation	P_I	—	40	mW	
Supply Voltage (1 minute maximum)	V_{CC}	—	7	V	
Output Collector Current	I_O	—	50	mA	
Output Collector Voltage	V_O	—	7	V	
Output Collector Power Dissipation	P_O	—	85	mW	
Solder Reflow Temperature Profile	See the Package Outline Drawing.				

a. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Conditions
Input Current, Low Level	I_{FL}[a]	0	250	µA	
Input Current, High Level[b]	I_{FH}[c]	5	15	mA	
		6		mA	$2.7V \le V_{CC} \le 3.6V$, $T_A = 85°C$ to 100°C
Power Supply Voltage	V_{CC}	2.7 4.5	3.6 5.5	V V	
Operating Temperature	T_A	–40	85	°C	
Fan Out (at R_L = 1 kΩ)[b]	N	—	5	TTL Loads	
Output Pull-up Resistor	R_L	330	4 k	Ω	

a. The off condition can also be guaranteed by ensuring that $V_{FL} \le 0.8V$.

b. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.

c. At T_A = –40°C to 85°C, the initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% LED degradation guardband.

Electrical Specifications

Over recommended operating condition (T_A = –40°C to +100°C, 2.7V ≤ V_{DD}≤ 3.6V) unless otherwise specified.
All Typical specifications at V_{CC} = 3.3V, T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}[a]	—	4.5	50	µA	V_{CC} = 3.3V, V_O = 3.3V, I_F = 250 µA	4	
Input Threshold Current	I_{TH}	—	3.0	5.0	mA	T_A =–40°C to 85°C V_{CC} = 3.3V, V_O = 0.6V, I_{OL} (Sinking) = 13 mA	6	
				6.0	mA	V_{CC} = 3.3V, V_O = 0.6V, I_{OL} (Sinking) = 13 mA	6	
Low Level Output Voltage	V_{OL}[a]	—	0.35	0.6	V	V_{CC} = 3.3 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	8, 10	
High Level Supply Current	I_{CCH}	—	4.7	7.0	mA	I_F = 0 mA, V_{CC} = 3.3V		
Low Level Supply Current	I_{CCL}	—	7.0	10.0	mA	I_F = 10 mA, V_{CC} = 3.3V		
Input Forward Voltage	V_F	1.4	1.5	1.75[a]	V	T_A = 25°C, I_F = 10 mA	12	
Input Reverse Breakdown Voltage	BV_R[a]	5	—	—	V	I_R = 10 µA		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	—	–1.6	—	mV/°C	I_F = 10 mA		
Input-Output Insulation	V_{ISO}	3750	—	—	V_{RMS}	R_H ≤ 50%, t = 1 min.		[b], [c]
Input Capacitance	C_{IN}	—	60	—	pF	f = 1 MHz, V_F = 0V		

a. The JEDEC Registration specifies 0°C to +70°C. Broadcom specifies –40°C to + 100°C.

b. Device considered a two terminal device: pins 1 and 3 shorted together, and pins 4, 5, and 6 shorted together.

c. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (Leakage detection current limit, I_{I-O} ≤ 5 µA).

Electrical Specifications

Over recommended temperature (T_A = –40°C to +100°, 4.5V≤ V_{DD} ≤ 5.5V) unless otherwise specified.
All Typical specifications at V_{CC} = 5V, T_A = 25°C.

Parameter	Symbol	Min.	Typ.[a]	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}	—	5.5	100	µA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250 µA	5	
Input Threshold Current	I_{TH}	—	2	5	mA	V_{CC} = 5.5V, I_O ≥ 13 mA, V_O = 0.6V	7	
Low Level Output Voltage	V_{OL}	—	0.4	0.6	V	V_{CC} = 5.5V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	9, 11	
High Level Supply Current	I_{CCH}	—	4	7.5	mA	V_{CC} = 5.5V, I_F = 0 mA		
Low Level Supply Current	I_{CCL}	—	6	10.5	mA	V_{CC} = 5.5V, I_F = 10 mA		
Input Forward Voltage	V_F	1.4	1.5	1.75	V	T_A = 25°C, I_F = 10 mA	12	
		1.3		1.85		I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	I_R = 10 µA		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	—	–1.6	—	mV/°C	I_F = 10 mA		
Input-Output Insulation	V_{ISO}	3750		—	V_{RMS}	RH ≤ 50%, t = 1 min.		b, c
Input Capacitance	C_{IN}	—	60	—	pF	V_F = 0V, f = 1 MHz		

a. All typicals at T_A = 25°C, V_{CC} = 5V.

b. Device considered a two terminal device: pins 1 and 3 shorted together, and pins 4, 5, and 6 shorted together.

c. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (Leakage detection current limit, I_{I-O} ≤ 5 µA).

Switching Specifications

Over recommended temperature (T_A = –40°C to +100°C), V_{CC} = 3.3V, I_F = 7.5 mA unless otherwise specified.
All Typical specifications at T_A = 25°C, V_{CC} = 3.3V.

Table 1 Switching Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	—	—	90	ns	T_A = –40°C to 85°C, R_L = 350Ω, C_L = 15 pF	13, 14	a, b
		—	—	95	ns	R_L = 350Ω, C_L = 15 pF		
Propagation Delay Time to Low Output Level	t_{PHL}	—	—	75	ns	T_A = –40°C to 85°C, R_L = 350Ω, C_L = 15 pF	13, 14	b, c
		—	—	90	ns	R_L = 350Ω, C_L = 15 pF		
Pulse Width Distortion	$\lvert t_{PHL} - t_{PLH} \rvert$	—	—	25	ns	T_A = –40°C to 85°C, R_L = 350Ω, C_L = 15 pF	16	b
		—	—	30	ns	R_L = 350Ω, C_L = 15 pF		
Propagation Delay Skew	t_{PSK}	—	—	40	ns	R_L = 350Ω, C_L = 15 pF		
Output Rise Time (10-90%)	t_r	—	45	—	ns	R_L = 350Ω, C_L = 15 pF		
Output Fall Time (90-10%)	t_f	—	20	—	ns	R_L = 350Ω, C_L = 15 pF		

a. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
b. See test circuit for measurement details.
c. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.

NOTE JEDEC registered data for the 6N137.

Switching Specifications

Over recommended temperature (T_A = –40°C to 100°C), V_{CC} = 5V, I_F = 7.5 mA unless otherwise specified.
All Typical specifications at T_A = 25°C, V_{CC} = 5V.

Table 2 Switching Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}	20	48	75	ns	T_A = 25°C, R_L=350Ω, CL=15 pF	13, 15	a, b
				100		R_L=350Ω, C_L=15 pF		
Propagation Delay Time to Low Output Level	tPHL	25	50	75	ns	T_A = 25°C, R_L=350Ω, C_L=15 pF	13, 15	b, c
				100		R_L= 350Ω, C_L = 15 pF		
Pulse Width Distortion	$\lvert t_{PHL} - t_{PLH} \rvert$	—	3.5	35	ns	R_L= 350Ω, C_L = 15 pF	17	b
Propagation Delay Skew	t_{PSK}	—	—	40	ns	R_L= 350Ω, C_L = 15 pF		
Output Rise Time (10%–90%)	t_{rise}	—	24	—	ns	R_L= 350Ω, C_L = 15 pF		
Output Fall Time (10%–90%)	t_{fall}	—	10	—	ns	R_L= 350Ω, C_L = 15 pF		

a. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
b. See test circuit for measurement details.
c. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.

Transient Immunity

Parameter	Sym.	Min.	Typ.	Units	Test Conditions		Figure	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	15,000	25,000	V/µs	$\|V_{CM}\|$ = 1000V	V_{CC} = 3.3V, I_F = 0 mA, $V_{O(MIN)}$ = 2V, R_L = 350Ω, T_A = 25°C	18	a, b
		10,000	15,000			V_{CC} = 5V, I_F = 0 mA, $V_{O(MIN)}$ = 2V, R_L = 350Ω, T_A = 25°C	18	a, b
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	15,000	25,000	V/µs	$\|V_{CM}\|$ = 1000V	V_{CC} = 3.3V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8V, R_L = 350Ω, TA = 25°C	18	b, c
		10,000	15,000			V_{CC} = 5V, I_F = 7.5 mA, $V_{O(MIN)}$ = 0.8V, R_L = 350Ω, T_A = 25°C	18	b, c

a. CM_H is the maximum tolerable rate of rise on the common mode voltage to assure that the output will remain in a high logic state (that is, V_o > 2.0V).

b. For sinusoidal voltages, $(|dV_{CM}| / dt)_{max} = \pi f_{CM} V_{CM}$ (p-p).

c. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (that is, V_o < 0.8V).

Figure 4 Typical High Level Output Current vs. Temperature

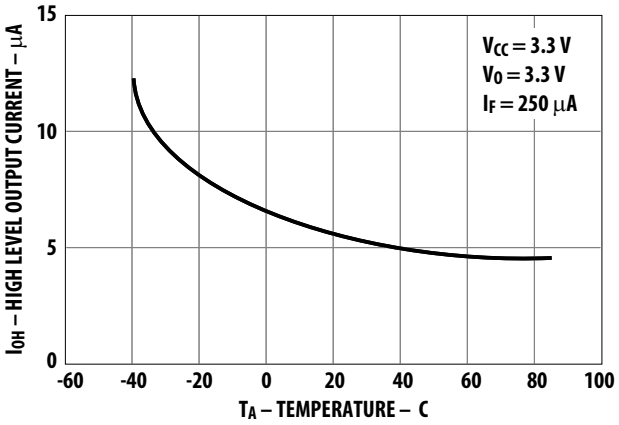


Figure 5 Typical High Level Output Current vs. Temperature

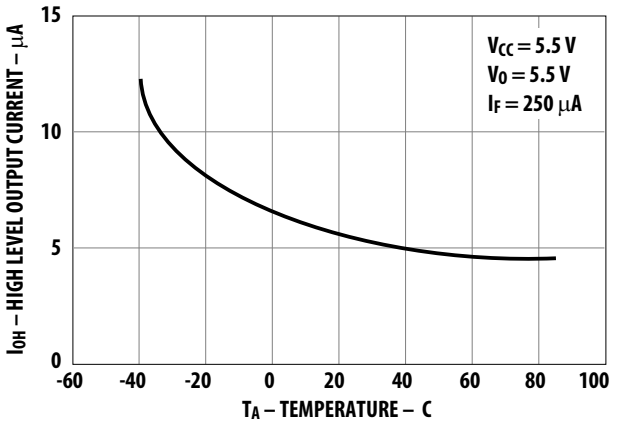


Figure 6 Typical Input Threshold Current vs. Temperature

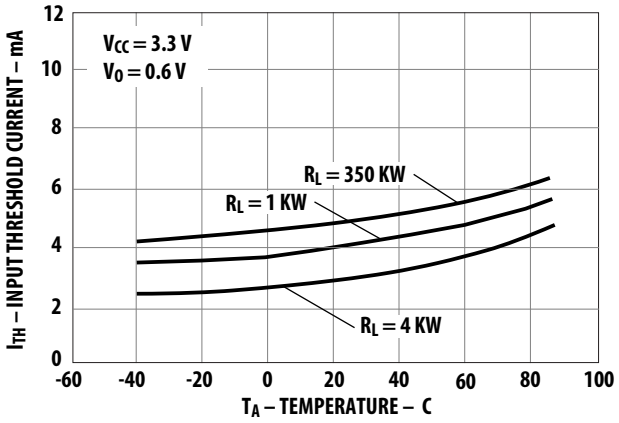


Figure 7 Typical Input Threshold Current vs. Temperature

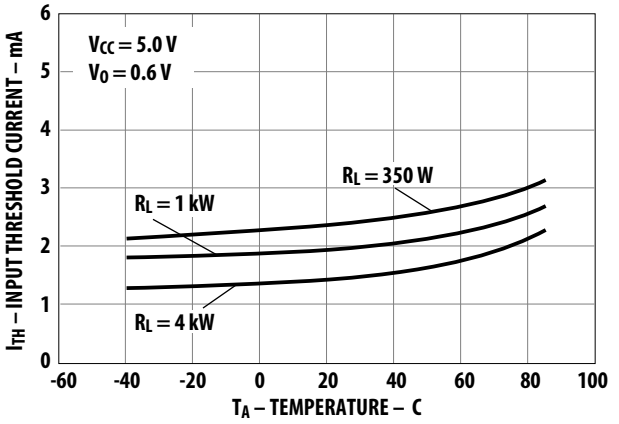


Figure 8 Typical Low Level Output Voltage vs. Temperature

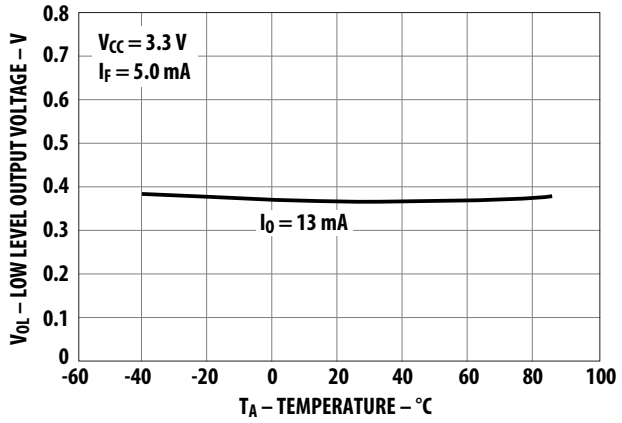


Figure 9 Typical Low Level Output Voltage vs. Temperature

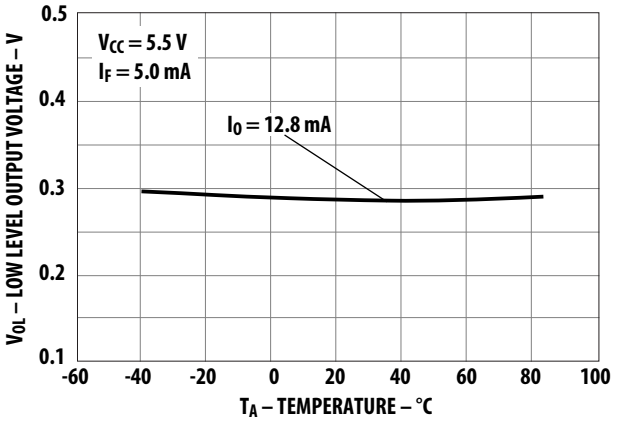


Figure 10 Typical Low Level Output Current vs. Temperature

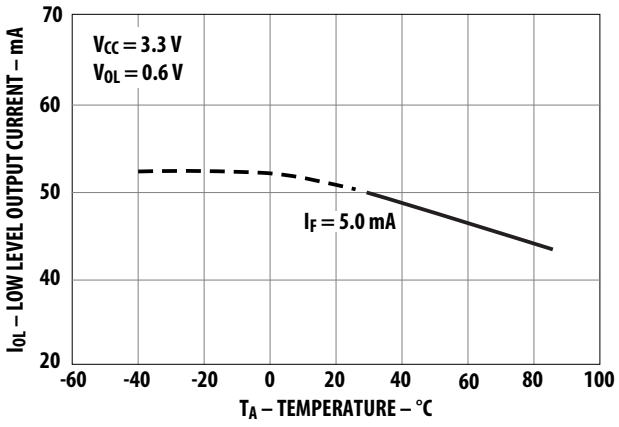


Figure 11 Typical Low Level Output Current vs. Temperature

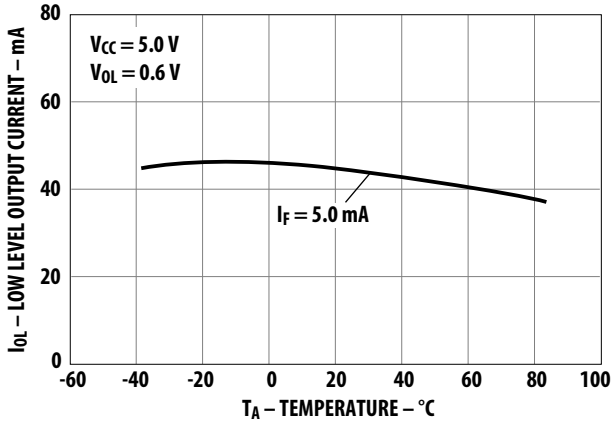


Figure 12 Typical Input Diode Forward Characteristic

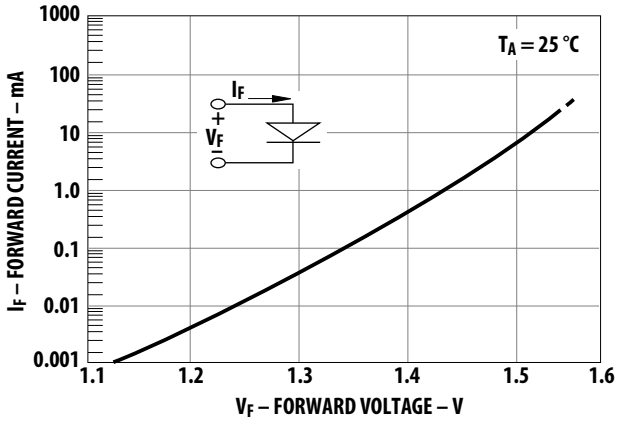
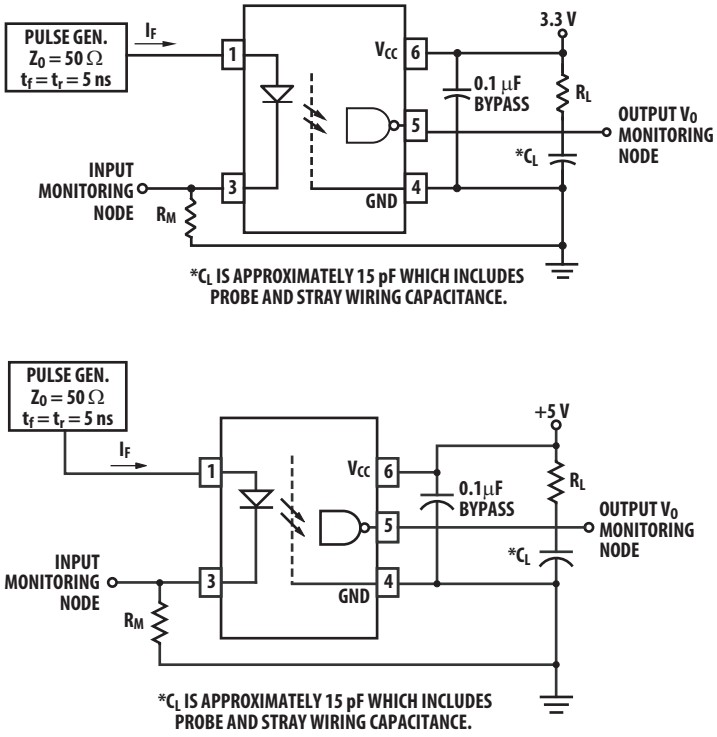


Figure 13 Test Circuit for t_{PHL} and t_{PLH}



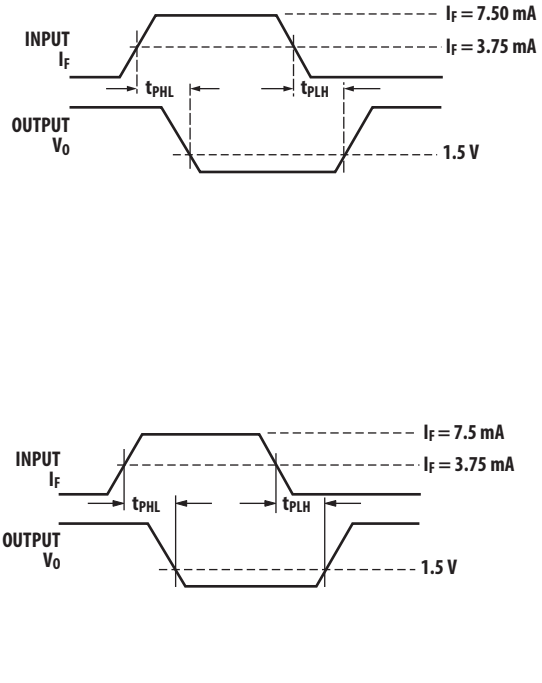


Figure 14 Typical Propagation Delay vs. Temperature

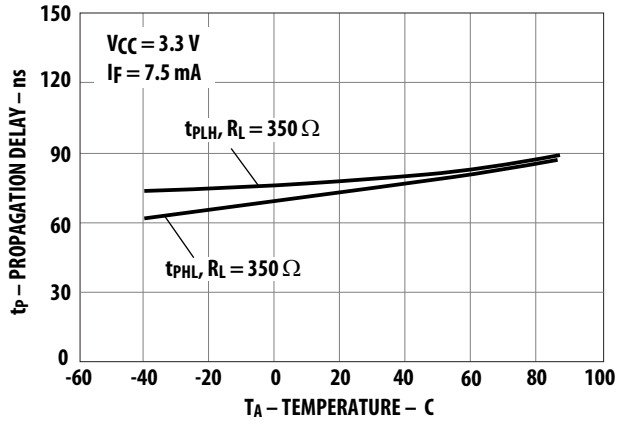


Figure 15 Typical Propagation Delay vs. Temperature

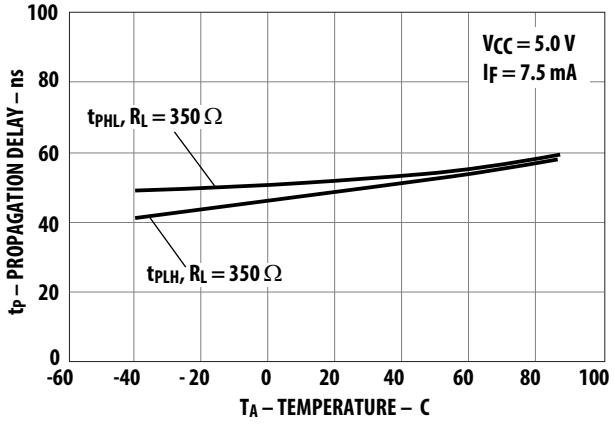


Figure 16 Typical Pulse Width Distortion vs. Temperature

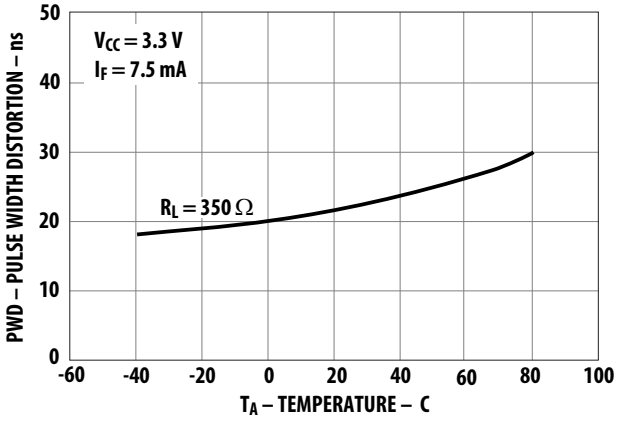


Figure 17 Typical Pulse Width Distortion vs. Temperature

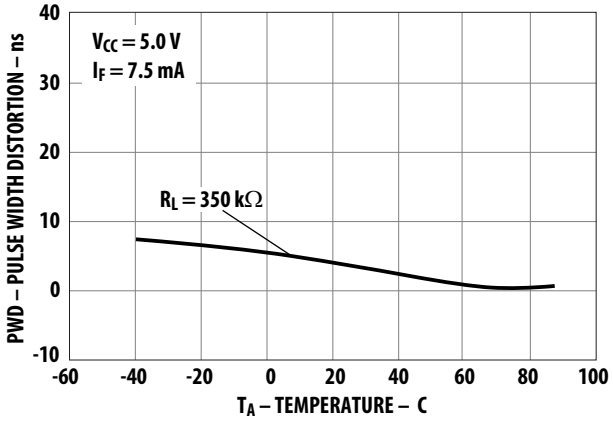
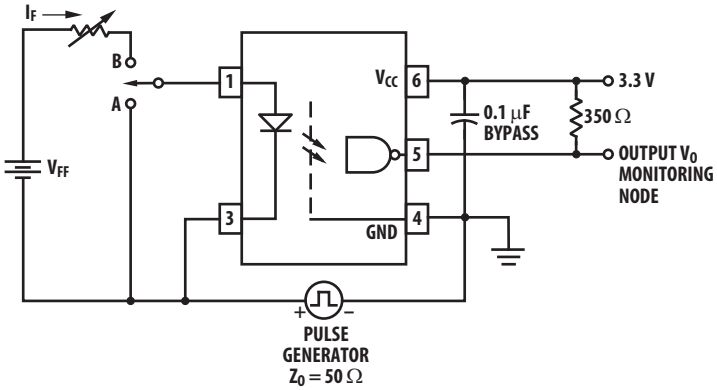
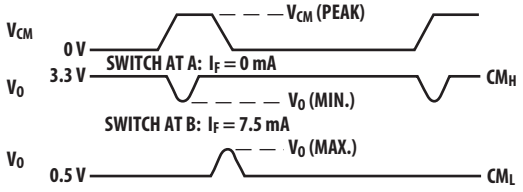
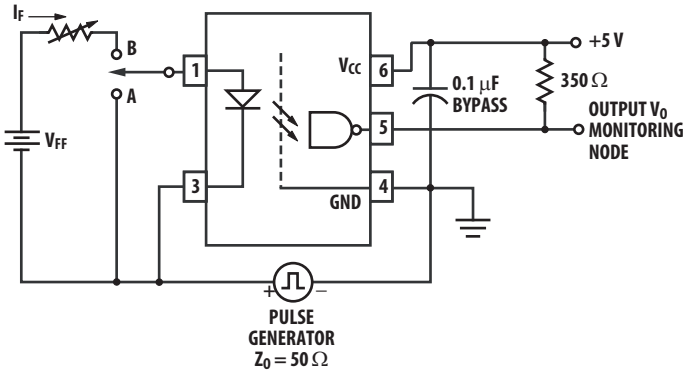
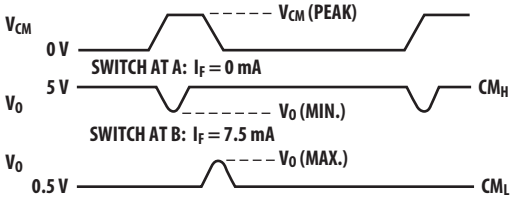


Figure 18 Test Circuit for Common Mode Transient Immunity and Typical Waveforms









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