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# ACPL-M62L

Ultra Low Power 10 MBd Digital Optocoupler

AVAGO TECHNOLOGIES

## Data Sheet

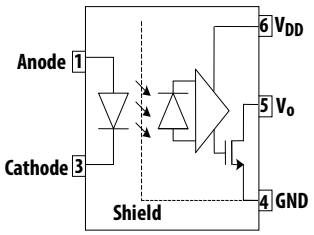
### Description

The ACPL-M62L is an optically-coupled optocoupler that combines an AlGaAs light-emitting diode and an integrated high-gain photo detector addresses the low power need. The optocoupler consumes low power at maximum 1.5 mA $I_{DD}$ across temperature. The forward current is as low as 2 mA, and so allows direct current drive by most microprocessors.

ACPL-M62L support both 3.3 V and 5 V supply voltage with guaranteed AC and DC operational parameters from -40 °C to +105 °C. The output of the detector IC is an open-drain type. The internal Faraday shield provides a guaranteed common mode transient immunity specification of 20 kV/µs.

This unique design provides maximum AC and DC circuit isolation while achieving TTL/CMOS compatibility. These optocouplers are suitable for high speed logic interfacing, while consuming extremely low power.

### Functional Diagram




**Truth table (Positive Logic)**

| LED | OUTPUT |
|---|---|
| ON | L |
| OFF | H |

A 0.1 µF bypass capacitor must be connected between pins $V_{DD}$ and GND.

### Features

- Ultra-low current $I_{DD}$ consumption: 1.5 mA max.
- Low input current capability: 2 mA
- Open-drain output
- SO-5 package
- 20 kV/µs minimum Common Mode Rejection (CMR) at $V_{CM}$ = 1000 V
- High Speed: 10 MBd min.
- Guaranteed AC and DC performance over wide temperature: -40 °C to +105 °C
- Safety and regulatory approval (pending):
  - UL 1577 recognized - 3750 $V_{rms}$ for 1 minute
  - CSA Approval
  - IEC/EN/DIN EN 60747-5-5 for Reinforced Insulation

### Applications

- Communication interface: $I^2C$-bus, CAN Bus
- Microprocessor system interfaces
- Digital isolation for A/D, D/A conversion

***CAUTION:*** *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD.*

## Ordering Information

ACPL-M62L is UL Recognized with 3750 $V_{rms}$ for 1 minute per UL1577.

| Part number | Option RoHS Compliant | Package | Surface Mount | Tape & Reel | IEC/EN/DIN EN 60747-5-5 | Quantity |
|---|---|---|---|---|---|---|
| ACPL-M62L | -000E | SO-5 | X | | | 100 per tube |
| | -060E | | X | | X | 100 per tube |
| | -500E | | X | X | | 1500 per reel |
| | -560E | | X | X | X | 1500 per reel |

To order, choose a part number from the Part number column and combine with the desired option from the Option column to form an order entry.

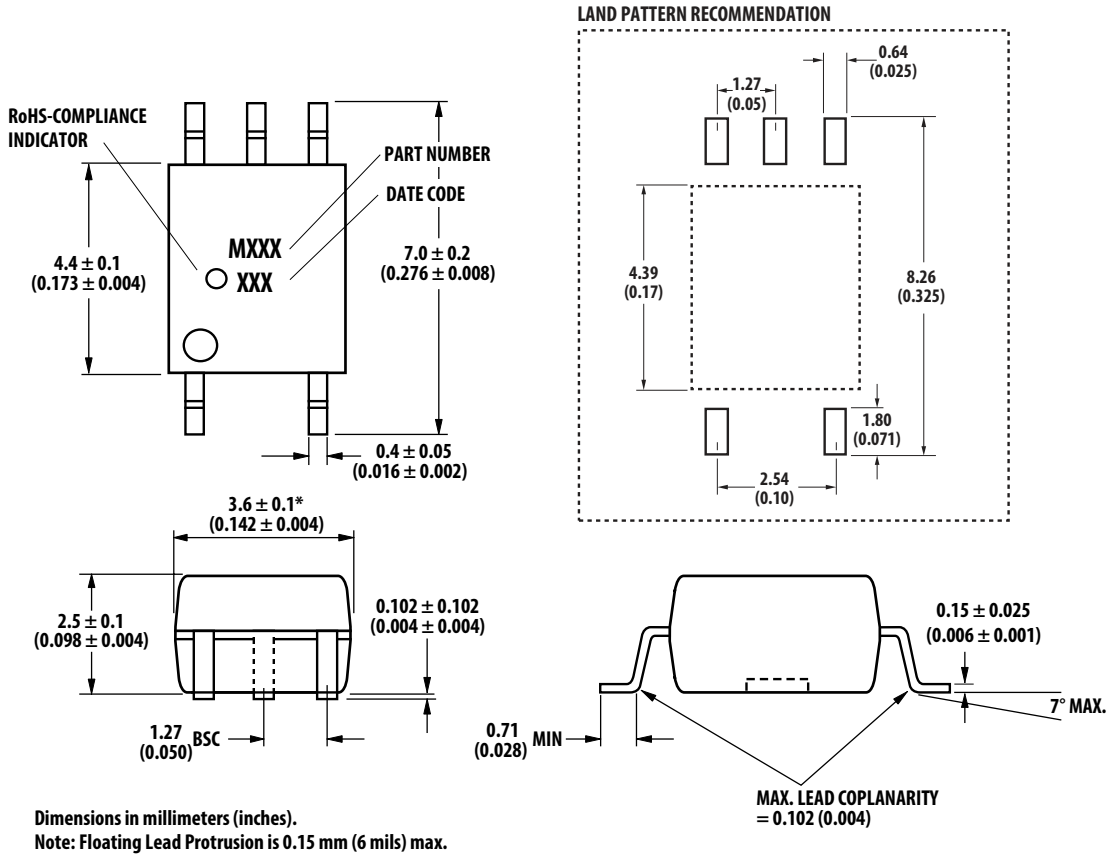
Example:

ACPL-M62L-560E: to order product of Small Outline SO-5 package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

## Package Outline Drawing

### ACPL-M62L SO-5 Package




**Dimensions in millimeters (inches).**
**Note: Floating Lead Protrusion is 0.15 mm (6 mils) max.**

*** Maximum Mold Flash on each side is 0.15 mm (0.006).**

## Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

## Regulatory Information

ACPL-M62L is pending approval by the following organizations:

| UL | CSA | IEC/EN/DIN EN 60747-5-5 |
|---|---|---|
| UL 1577, component recognition program up to $V_{ISO}$ = 3750 $V_{RMS}$ File E55361. | Approved under CSA Component Acceptance Notice #5, File CA 88324. | (Option 060E only) |

### Insulation and Safety Related Specifications

| Parameter | Symbol | ACPL-M62L | Units | Conditions |
|---|---|---|---|---|
| Minimum External Air Gap (External Clearance) | L(101) | 5 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (External Creepage) | L(102) | 5 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | | 0.08 | mm | Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector. |
| Tracking Resistance (Comparative Tracking Index) | CTI | 175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | IIIa | | Material Group (DIN VDE 0110, 1/89, Table 1) |

### IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (Option 060E)

| Description | Symbol | Characteristic | Unit |
|---|---|---|---|
| Installation classification per DIN VDE 0110/39, Table 1 | | | |
| for rated mains voltage ≤ 150 $V_{rms}$ | | I – IV | |
| for rated mains voltage ≤ 300 $V_{rms}$ | | I – IV | |
| for rated mains voltage ≤ 600 $V_{rms}$ | | I – III | |
| Climatic Classification | | 40/105/21 | |
| Pollution Degree (DIN VDE 0110/39) | | 2 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 567 | $V_{peak}$ |
| Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m$=1 sec, Partial discharge < 5 pC | $V_{PR}$ | 1063 | $V_{peak}$ |
| Input to Output Test Voltage, Method a* $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, $t_m$=10 sec, Partial discharge < 5 pC | $V_{PR}$ | 907 | $V_{peak}$ |
| Highest Allowable Overvoltage (Transient Overvoltage $t_{ini}$ = 60 sec) | $V_{IOTM}$ | 6000 | $V_{peak}$ |
| Safety-limiting values – maximum values allowed in the event of a failure | | | |
| Case Temperature | $T_S$ | 150 | °C |
| Input Current | $I_{S, INPUT}$ | 150 | mA |
| Output Power | $P_{S, OUTPUT}$ | 600 | mW |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | $R_S$ | $>10^9$ | Ω |

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

### Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units | Condition |
|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | -55 | 125 | °C | |
| Operating Temperature | $T_A$ | -40 | 105 | °C | |
| Reverse Input Voltage | $V_R$ | | 5 | V | |
| Supply Voltage | $V_{DD}$ | | 6.5 | V | |
| Average Forward Input Current | $I_F$ | | 8 | mA | |
| Output Current | $I_O$ | | 10 | mA | |
| Output Voltage | $V_O$ | –0.5 | $V_{DD}$ + 0.5 | V | |
| Input Power Dissipation | $P_I$ | | 14 | mW | |
| Output Power Dissipation | $P_O$ | | 20 | mW | |
| Lead Solder Temperature | $T_{LS}$ | | 260 °C for 10 sec., 1.6 mm below seating plane | | |
| Solder Reflow Temperature Profile | | | Refer to Solder Reflow Profile section | | |

### Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | -40 | 105 | °C |
| Input Current, Low Level | $I_{FL}$ | 0 | 250 | µA |
| Input Current, High Level | $I_{FH}$ | 2 | 6 | mA |
| Power Supply Voltage | $V_{DD}$ | 2.7 | 5.5 | V |
| Forward Input Voltage | $V_{F(OFF)}$ | | 0.8 | V |

### Electrical Specifications (DC)

Over recommended temperature ($T_A$ = –40 °C to +105 °C) and supply voltage (2.7 V ≤ $V_{DD}$ ≤ 3.6 V). All typical specifications are at $V_{DD}$ = 3.3 V, $T_A$ = 25 °C.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input Forward Voltage | $V_F$ | 0.95 | 1.3 | 1.7 | V | $I_F$ = 2.2 mA, Figure 1, Figure 2 |
| Input Reverse Breakdown Voltage | $BV_R$ | 3 | 5 | | V | $I_R$ = 10 µA |
| Logic High Output Current | $I_{OH}$ | | 4.5 | 50 | µA | $V_{DD}$ = 3.3 V, $I_F$ = 250 µA, $V_O$ = 3.3 V |
| Logic Low Output Voltage | $V_{OL}$ | | 0.3 | 0.6 | V | $I_F$= 2.2 mA, $I_O$ =10 mA, $R_L$=390 Ω |
| Input Threshold Current | $I_{TH}$ | | 0.7 | 1.5 | mA | Figure 3 |
| Logic Low Output Supply Current | $I_{DDL}$ | | 0.8 | 1.5 | mA | Figure 4 |
| Logic High Output Supply Current | $I_{DDH}$ | | 0.8 | 1.5 | mA | Figure 5 |
| Input Capacitance | $C_{IN}$ | | 60 | | pF | f = 1 MHz, $V_F$ = 0 V |
| Input Diode Temperature Coefficient | $\Delta V_F/\Delta T_A$ | | -1.6 | | mV/°C | $I_F$ = 2.2 mA |

Over recommended temperature ($T_A$ = –40 °C to +10 5°C) and supply voltage (4.5 V ≤ $V_{DD}$ ≤ 5.5 V). All typical specifications are at $V_{DD}$ = 5 V, $T_A$ = 25 °C.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input Forward Voltage | $V_F$ | 0.95 | 1.3 | 1.7 | V | $I_F$ = 2.2 mA, Figure 1, Figure 2 |
| Input Reverse Breakdown Voltage | $BV_R$ | 3 | 5 | | V | $I_R$ = 10 µA |
| Logic High Output Current | $I_{OH}$ | | 5.5 | 100 | µA | $V_{DD}$ = 5.5 V, $I_F$ = 250 µA, $V_O$ = 5.5 V |
| Logic Low Output Voltage | $V_{OL}$ | | 0.3 | 0.6 | V | $I_F$ = 2.2 mA, $I_O$ = 8.4 mA, $R_L$= 560 Ω |
| Input Threshold Current | $I_{TH}$ | | 0.7 | 1.5 | mA | Figure 3 |
| Logic Low Output Supply Current | $I_{DDL}$ | | 0.8 | 1.5 | mA | Figure 4 |
| Logic High Output Supply Current | $I_{DDH}$ | | 0.8 | 1.5 | mA | Figure 5 |
| Input Capacitance | $C_{IN}$ | | 60 | | pF | f = 1 MHz, $V_F$ = 0 V |
| Input Diode Temperature Coefficient | $\Delta V_F/\Delta T_A$ | | -1.6 | | mV/°C | $I_F$ = 2.2 mA |

## Switching Specifications (AC)

Over recommended temperature ($T_A$ = –40 °C to +105 °C), supply voltage (2.7 V ≤ $V_{DD}$ ≤ 3.6 V). All typical specifications are at $V_{DD}$ = 3.3 V, $T_A$ = 25 °C.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Propagation Delay Time to Logic Low Output [1] | $t_{PHL}$ | | 46 | 80 | ns | $I_F$ = 2.2 mA, $V_I$ = 5 V, $R_T$ = 1.5 kΩ, $C_L$= 15 pF<br>$I_F$ = 2.2 mA, $V_I$ = 3.3 V, $R_T$ = 700 Ω, $C_L$= 15 pF<br>$R_L$ = 390 Ω, Figure 6a, Figure 7a |
| Propagation Delay Time to Logic High Output [1] | $t_{PLH}$ | | 40 | 80 | ns | |
| Pulse Width | $t_{PW}$ | 100 | | | ns | |
| Pulse Width Distortion [2] | PWD | | 6 | 30 | ns | |
| Propagation Delay Skew [3] | $t_{PSK}$ | | | 30 | ns | |
| Output Rise Time (10% – 90%) | $t_R$ | | 12 | | ns | $I_F$ = 2.2 mA, $V_I$ = 5 V, $R_T$ = 1.5 kΩ, $C_L$= 15 pF, $R_L$ = 390 Ω |
| | | | 10 | | ns | $I_F$ = 2.2 mA, $V_I$ = 3.3 V, $R_T$ = 700 Ω, $C_L$ = 15 pF, $R_L$ =390Ω |
| Output Fall Time (90% - 10%) | $t_F$ | | 12 | | ns | $I_F$ = 2.2 mA, $V_I$ = 5 V, $R_T$ = 1.5 kΩ, $C_L$ = 15 pF, $R_L$= 390 Ω |
| | | | 10 | | ns | $I_F$ = 2.2 mA, $V_I$ = 3.3 V, $R_T$ = 700 Ω, $C_L$= 15 pF, $R_L$ =390 Ω |
| Static Common Mode Transient Immunity at Logic High Output [4] | $\lvert CM_H \rvert$ | 20 | 35 | | kV/µs | $V_{CM}$ = 1000 V, $T_A$ = 25 °C, $I_F$ = 0 mA, $C_L$= 15 pF, $R_L$ = 390 Ω, Figure 8 |
| Static Common Mode Transient Immunity at Logic Low Output [5] | $\lvert CM_L \rvert$ | 20 | 35 | | kV/µs | $V_{CM}$ = 1000 V, $T_A$ = 25 °C, $V_I$ = 5 V ($R_T$ =1.5 kΩ) or $V_I$ = 3.3 V (RT=700Ω), $I_F$ = 2.2 mA, $C_L$= 15 pF, $R_L$= 390 Ω, Figure 8 |
| Dynamic Common Mode Transient Immunity [6] | $CMR_D$ | | 35 | | kV/µs | $V_{CM}$ = 1000 V, $T_A$ = 25 °C, $I_F$ = 2.2 mA, $V_I$ = 5 V ($R_T$ =1.5 kΩ) or $V_I$ = 3.3 V ($R_T$=700 Ω), 10 MBd data rate, the absolute increase of PWD <10 ns, $R_L$= 390 Ω |

Over recommended temperature ($T_A$ = –40 °C to +105 °C), supply voltage (4.5 V ≤ $V_{DD}$ ≤ 5.5 V). All typical specifications are at $V_{DD}$ = 5 V, $T_A$ = 25 °C.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Propagation Delay Time to Logic Low Output [1] | $t_{PHL}$ | | 46 | 80 | ns | $I_F$ = 2.2 mA, $V_I$ = 5 V, $R_T$=1.5 kΩ, $C_L$= 15 pF<br>$I_F$ = 2.2 mA, $V_I$ = 3.3 V, $R_T$ = 700 Ω, $C_L$= 15 pF<br>$R_L$= 560 Ω, Figure 6b, Figure 7b |
| Propagation Delay Time to Logic High Output [1] | $t_{PLH}$ | | 40 | 80 | ns | |
| Pulse Width | $t_{PW}$ | 100 | | | ns | |
| Pulse Width Distortion [2] | PWD | | 6 | 30 | ns | |
| Propagation Delay Skew [3] | $t_{PSK}$ | | | 30 | ns | |
| Output Rise Time (10% – 90%) | $t_R$ | | 12 | | ns | $I_F$ = 2.2 mA, $V_I$ = 5 V, $R_T$ =1.5 kΩ, $C_L$ = 15 pF, $R_L$= 560 Ω |
| | | | 10 | | ns | $I_F$ = 2.2 mA, $V_I$ = 3.3 V, $R_T$ = 700 Ω, $C_L$= 15 pF, $R_L$ =560 Ω |
| Output Fall Time (90% - 10%) | $t_F$ | | 12 | | ns | $I_F$ = 2.2 mA, $V_I$= 5 V, $R_T$ = 1.5 kΩ, $C_L$ = 15 pF, $R_L$= 560 Ω |
| | | | 10 | | ns | $I_F$ = 2.2 mA, $V_I$ = 3.3 V, $R_T$ = 700 Ω, $C_L$= 15 pF, $R_L$= 560 Ω |
| Static Common Mode Transient Immunity at Logic High Output [4] | $\lvert CM_H \rvert$ | 20 | 35 | | kV/µs | $V_{CM}$ = 1000 V, $T_A$ = 25 °C, $I_F$ = 0 mA, $C_L$= 15 pF, $R_L$ = 560 Ω, Figure 8 |
| Static Common Mode Transient Immunity at Logic Low Output [5] | $\lvert CM_L \rvert$ | 20 | 35 | | kV/µs | $V_{CM}$ = 1000 V, $T_A$ = 25 °C, $V_I$ = 5 V ($R_T$ = 1.5 kΩ) or $V_I$ = 3.3 V ($R_T$ = 700 Ω), $I_F$ = 2.2 mA, $C_L$= 15 pF, $R_L$= 560 Ω, Figure 8 |
| Dynamic Common Mode Transient Immunity [6] | $CMR_D$ | | 35 | | kV/µs | $V_{CM}$ = 1000 V, $T_A$ = 25 °C, $I_F$ = 2.2 mA, $V_I$ = 5 V ($R_T$ = 1.5 kΩ) or $V_I$ = 3.3 V ($R_T$ =700 Ω), 10 MBd data rate, the absolute increase of PWD <10 ns, $R_L$ = 560 Ω |

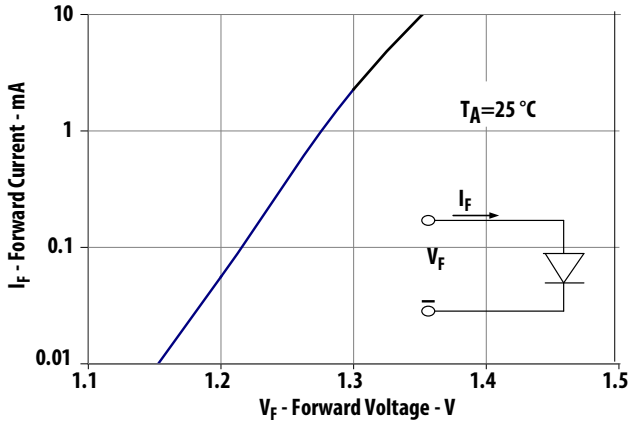



Figure 1. Typical input diode forward characteristic

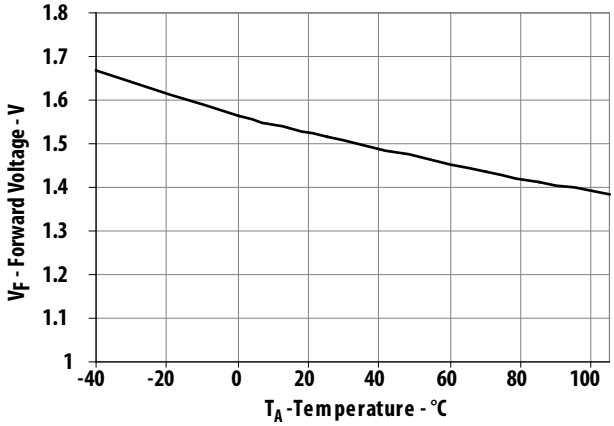



Figure 2. Typical $V_F$ vs. temperature

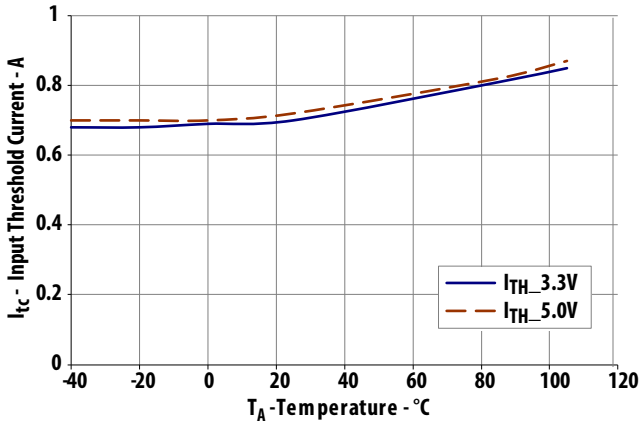



Figure 3. Typical input threshold current $I_{TH}$ vs. temperature

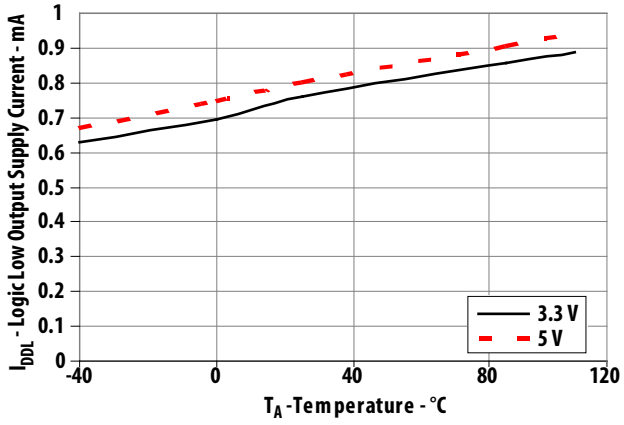



Figure 4. Typical logic low output supply current $I_{DDL}$ vs. temperature

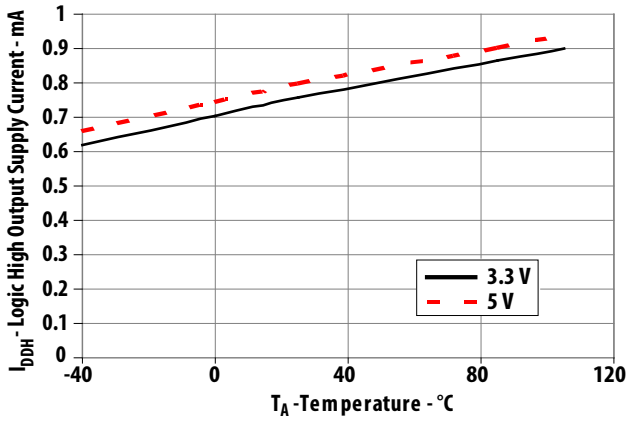



Figure 5. Typical logic high output supply current $I_{DDH}$ vs. temperature

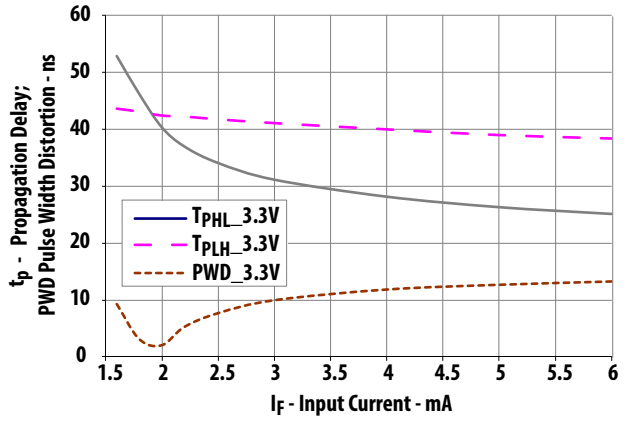



Figure 6a. Typical switching speed vs. input current at 3.3 V supply voltage

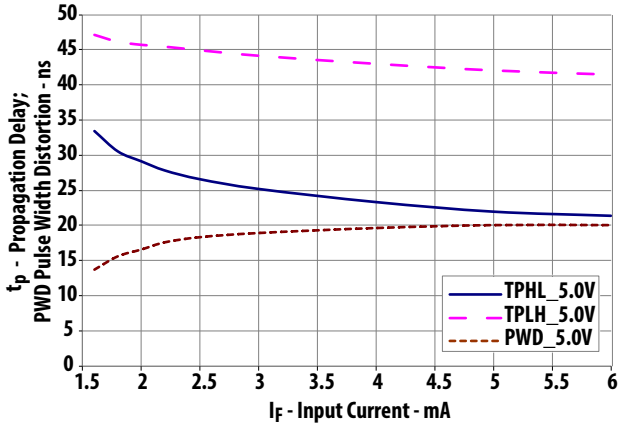



Figure 6b. Typical switching speed vs. input current at 5 V supply voltage

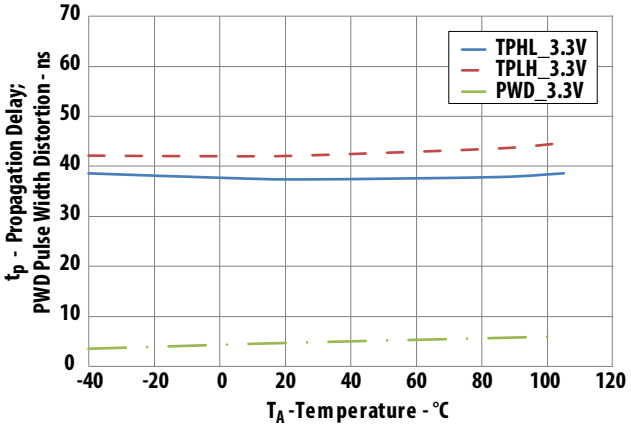



Figure 7a. Typical propagation delay v s. temperature at 3.3V supply voltage

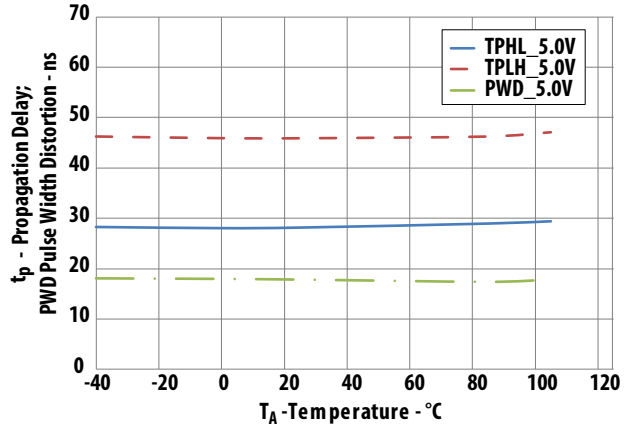



Figure 7b. Typical propagation delay v s. temperature at 5 V supply voltage

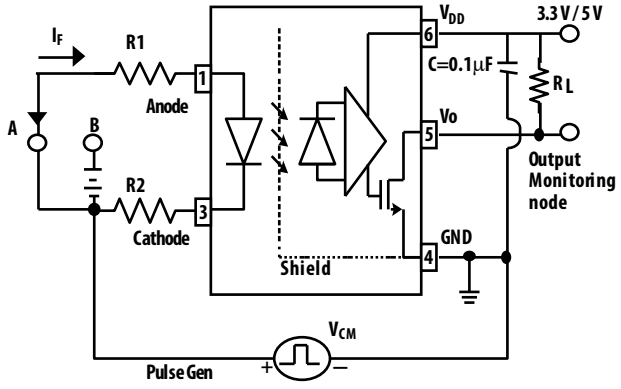
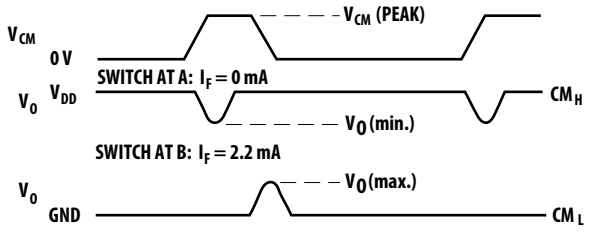



Figure 8. Common Mode Transient Immunity Test Setup



## Package Characteristics

All typical at $T_A$ = 25 °C.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input-Output Insulation | $V_{ISO}$ | 3750 | | | $V_{rms}$ | RH < 50% for 1 min. $T_A$ = 25 °C |
| Input-Output Resistance | $R_{I-O}$ | | $10^{12}$ | | Ω | $V_{I-O}$ = 500 V |
| Input-Output Capacitance | $C_{I-O}$ | | 0.6 | | pF | f =1 MHz, $T_A$ = 25 °C |

Notes:

1. $t_{PHL}$ propagation delay is measured from the 50% ($V_{in}$ or $I_F$) on the rising edge of the input pulse to the 50% $V_{DD}$ of the falling edge of the $V_O$ signal. $t_{PLH}$ propagation delay is measured from the 50% ($V_{in}$ or $I_F$) on the falling edge of the input pulse to the 50% level of the rising edge of the $V_O$ signal.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$.
3. $t_{PSK}$ is equal to the magnitude of the worst-case difference in $t_{PHL}$ and/or $t_{PLH}$ that will be seen between units at any given temperature within the recommended operating conditions.
4. $CM_H$ is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
5. $CM_L$ is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.
6. $CM_D$ is the maximum tolerable rate of the common mode voltage during data transmission to assure that the absolute increase of the PWD is less than 10 ns.

## Supply Bypassing, LED Bias Resistors and PC Board Layout

The ACPL-M62L optocouplers are extremely easy to use and feature high speed, open-drain outputs.

The external components required for proper operation are the input limiting resistors and the output bypass capacitor. Capacitor values should be 0.1 μF.

For each capacitor, the total lead length connecting the capacitor to the $V_{DD}$ and GND pins should not exceed 20 mm.

$V_{DD}$ = 3.3 V: R1 = 420 Ω ± 1%, R2 = 280 Ω ± 1%
$V_{DD}$ = 5.0 V: R1 = 900 Ω ± 1%, R2 = 600 Ω ± 1%
$R_T$ = R1 + R2; R1/R2 ≈ 1.5

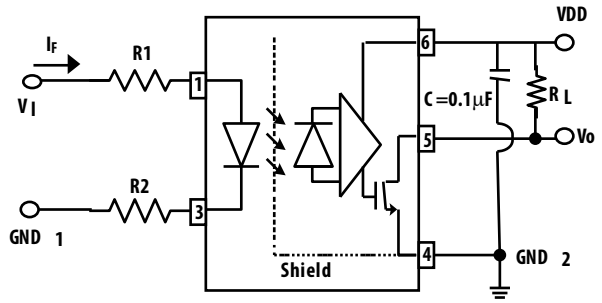



**Figure 9. Recommended printed circuit board layout and input current limiting resistor selection**

## Optocoupler CMR Performance

The principal protection against common mode noise, comes from the fundamental isolation properties of the optocoupler, and this in turn is directly related to the Input-Output leakage capacitance of the optocoupler.

To provide maximum protection to circuitry connected to the input or output of the optocoupler the leakage capac¬itance is minimized by having large separation distances at all points in the optocoupler construction, including the LED/photodiode interface.

In addition to the optocouplers basic physical construc¬tion, additional circuit design steps mitigate the effects of common mode noise. The most important of these is the Faraday shield on the photodetector stage.

A Faraday shield is effective in optocouplers because the internal modulation frequency (light) is many orders of magnitude higher than the common mode noise frequency.

## Improving CMR Performance at the Application Level

In an end application it desirable that the optocouplers common mode isolation be as close as possible to that indicated in the data sheet specifications. The first step in meeting this goal is to ensure maximum separation between PCB interconnects on either side of the opto-coupler is maintained and that PCB tracks beneath the optocoupler are avoided.

It is inevitable that a certain amount of CMR noise will be coupled into the inputs and this can potentially result in false-triggering of the input. This problem is frequently observed in devices with input high input impedance. In some cases this can cause momentary missing pulses and may even cause input circuitry to latch-up in some alternate technologies.

The ACPL-M62L optocoupler family does not have an input latch-up issue. Even at very high CMR levels such as those experienced in end equipment level tests (for example IEC61000-4-4) the ACPL-M62L series is immune to latch-up because of the simple diode structure of the LED.

In some cases achieving the rated data sheet CMR per¬formance level is not possible in an application. This is often because of the practical need to actually connect the isolator input to the output of a dynamically changing signal rather than tying the input statically to VDD or GND. A data sheet CMR "specmanship" issue is often seen with alternative technology isolators that are based on AC encoding techniques.

To address the need to define achievable end application performance on data sheets, the ACPL-M62L optocouplers include an additional typical performance specification for dynamic CMR in the electrical parameter table. The dynamic CMR specification indicates the typical achievable CMR performance as the input is being toggled on or off during a CMR transient.

The logic output the ACPL-M62L optocouplers is mainly controlled by LED current level, and since the LED current features very fast rise and fall times, dynamic noise immunity is essentially the same as static noise immunity.

Despite their immunity to input latch-up and the excellent dynamic CMR immunity, ACPL-M62L opto¬coupler devices are still potentially vulnerable to miss-operation caused by the LED being turned either on or off during a CMR disturbance. If the LED status could be ensured by design, the overall application level CMR performance would be that of the photodetector. To benefit from the inherently high CMR capabilities of the ACPL-M62L family, some simple steps about operating the LED at the application level should be taken.

In particular, ensure that the LED stays either on or off during a CMR transient. Some common design techniques to accomplish this are:

- Keep the LED on:
  - Overdrive the LED with a higher than required forward current.
- Keep the LED off:

  During the Off state:

  i) Reverse bias the LED.

  ii) Minimize the off-state impedance across the anode and cathode of the LED.

All these methods allow the full CMR capability of the ACPL-M62L family to be achieved, but they do have practical implementation issues or require a compromise on power consumption.

There is, however, an effective method to meet the goal of maintaining the LED status during a CMR event with no other design compromises other than adding a single resistor.

This CMR optimization takes advantage of the differential connection to the LED. By ensuring the common mode impedances at both the cathode and anode of the LED are equal, the CMR transient on the LED is effectively canceled. As shown in Figure 9, this is easily achieved by using two, instead of one, input bias resistors.




AV02-4059EN - April 19, 2013