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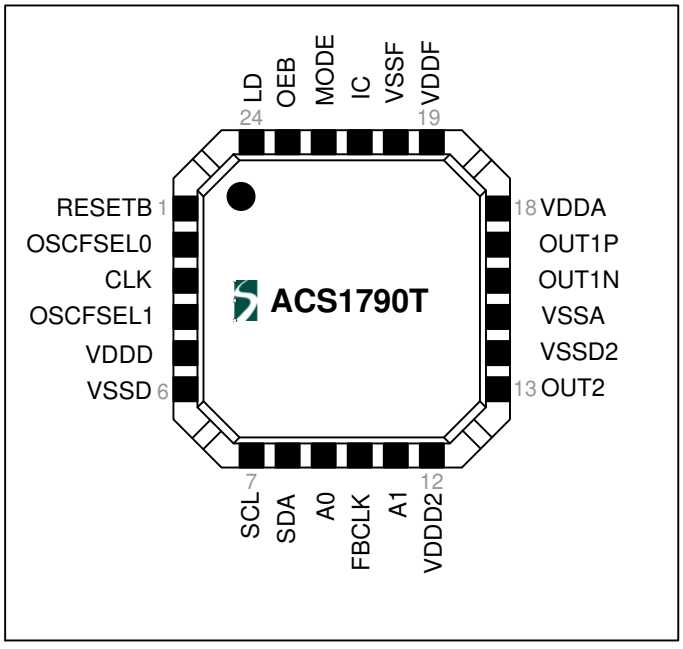
Introduction

The ACS1790T is a high-performance, low phase noise, programmable frequency synthesizer with ultra-fine dynamic output frequency control. It can be used as a companion to a compatible ToPSync™ device to generate outputs locked to an external reference source or standalone for standard frequency generation for common applications. The circuit includes an integrated VCO, loop filter, phase-and-frequency detector and output dividers. The default power-up mode is definable by pin settings and once operational the ACS1790T is fully-programmable via an I²C interface. The ACS1790T requires only a low-speed external clock input for operation.

When used in conjunction with a compatible ToPSync® device in a Synchronous Ethernet system the ACS1790T allows the Ethernet transmit clocks to be derived initially from the local reference oscillator and subsequently frequency-locked to an external reference source once the system is fully configured, simplifying system design and reducing component count and BOM cost.

Pin Diagram



Features

- Optimised for Synchronous Ethernet, SONET and SDH operation
- Meets RMS jitter requirements of Gigabit Ethernet, 10 Gigabit Ethernet and OC-48 / STM-16
- Default options for 25 MHz & 125 MHz or 25 MHz & 156.25 MHz outputs at reset
- High frequency LVPECL output:
  10 MHz – 200 MHz, 1 ppb step
- Low frequency LVCMOS output:
  2 kHz – 125 MHz
  1.8V, 2.5V and 3.3V operation
- Very-low frequency feedback clock output for connection to ToPSync® or external PFD
- Tunable over +/- 500 ppm range without loss of lock
- Integrated VCO, PFD and loop filter
- 2.3 – 2.7 GHz VCO frequency
- Typical RMS jitter performance for target application masks:
  OC-48, STM-16 (ANSI T1.105.03 & ITU-T G.813)
  0.56 ps (12 kHz – 20 MHz)
  1G Ethernet (IEEE 802.3-2008 38 & 39)
  0.15 ps (637 kHz – 20 MHz)
  XAUI (IEEE 802.3-2008 Clause 47)
  0.11 ps (1.875 MHz – 20 MHz)
  10G Ethernet (IEEE 802.3-2008 53 & 54)
  0.29 ps (4 MHz – 80 MHz)
- Reference spurs: < -67 dBc
- 10, 12.8, 20 or 25 MHz input clock
- Operating voltage: 3.0 - 3.6V
- I²C -bus interface
- Four selectable slave addresses to allow multiple devices to be used with a single controlling master
- Lock detect output
- Pin and register output enable control
- Temperature range: -40 to 85C
- 4 x 4 mm QFN 24 package
- Pb-Free, Halogen free, RoHS/WEEE compliant product

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Block Diagram

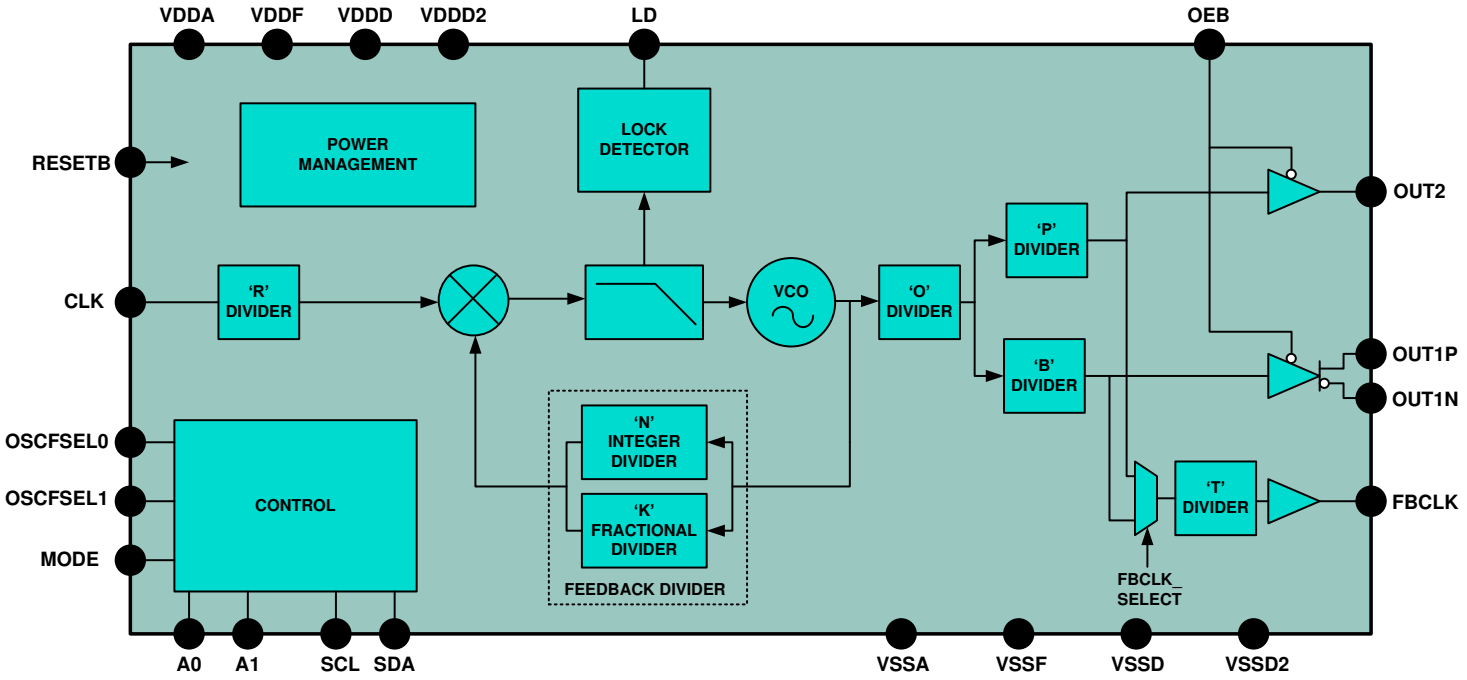

Figure 1 : ACS1790T Block Diagram

Pin Description

The ACS1790T uses a QFN 24 package with 24 device pins and a center thermal pad that is connected to the device ground. Table 1 shows the pin definitions.

Table 1 : ACS1790T Pin Description

Number	Name	Type	Description
1	RESETB	I	Active Low Reset
2	OSCFSEL0	I^{PD}	Input Clock Frequency Selection
3	CLK	I	Input Clock
4	OSCFSEL1	I^{PD}	Input Clock Frequency Selection
5	VDDD	Power	Digital Power Supply for Internal Logic and FBCLK Output
6	VSSD	Ground	Digital Ground for Internal Logic and FBCLK Output
7	SCL	I	I^2C Clock (requires external pull up resistor)
8	SDA	I/O	I^2C Data (requires external pull up resistor)
9	A0	I^{PD}	I^2C Address Selection
10	FBCLK	O	Feedback Clock to ToPSync (LVCMOS)
11	A1	I^{PD}	I^2C Address Selection
12	VDDD2	Power	Digital Power Supply for OUT2 Clock Output
13	OUT2	O	Single-ended Output Clock (LVCMOS)
14	VSSD2	Power	Digital Ground for OUT2 Clock Output
15	VSSA	Ground	Analogue Ground
16	OUT1N	O	Differential Output Clock (LVPECL)
17	OUT1P	O	Differential Output Clock (LVPECL)
18	VDDA	Power	Analogue Supply
19	VDDF	Power	RF Supply
20	VSSF	Ground	RF Ground
21	IC	-	Internally connected pin – do not connect
22	MODE	I^{PD}	Initial Mode Select
23	OEB	I	Output Enable
24	LD	O	Lock Detect (Open Drain)
25	GND	Ground	Center Body Contact. Connect to ground

I – Input
O – Output
I/O – Bidirectional pin
I^{PD} – Input with internal pull-down

Device Operation

Figure 1 shows the internal architecture of the ACS1790T. The ACS1790T can be divided into a number of main blocks – the voltage-controlled oscillator phase-locked-loop (VCO PLL) block, the output divider block, the output stage and the control block.

The VCO PLL block

The VCO PLL block is a fully self-contained phase-locked loop that generates an output frequency of between 2.3 and 2.7 GHz that is phase-locked to the clock input. This block is shown in Figure 2.

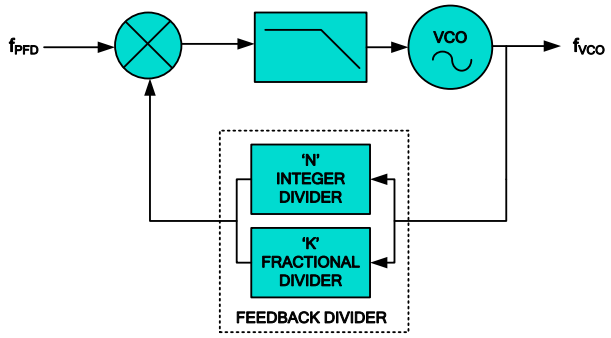

Figure 2 : ACS1790T VCO PLL

The VCO frequency, f_{VCO} is determined by a divider in the feedback path that supports fractional division ratios and that locks the VCO output to a multiple of the reference frequency, f_{PFD}, which is the input frequency after passing through the R-divider shown in Figure 1. For input frequencies of 10 and 12.8 MHz the R-divider is in bypass mode, making f_{PFD} equal to 10 or 12.8 MHz respectively. For input frequencies of 20 and 25 MHz the R-divider is set to divide by two, making f_{PFD} equal to 10 or 12.5 MHz respectively. The high resolution of the fractional feedback divider provides ultra-fine control of the VCO output. Any frequency within the VCO operating range can be achieved with an accuracy of better than 1 ppb. The design of the VCO and the corresponding phase-and-frequency detector ensure that the output has very low jitter and is not adversely affected by noise and jitter on the input clock that falls above the ACS1790T's PLL bandwidth.

Locking of the VCO to an arbitrary frequency, including immediately after reset, is a two stage process. Firstly, the ACS1790T performs a calibration operation to select the optimal VCO operating point for the selected frequency. When this operation is complete the ACS1790T transitions to a "fine-lock" state in which the VCO output frequency is tuned until it is phase-locked to the reference clock. Once in the fine-lock state, the output frequency of the ACS1790T can be adjusted by up to +/- 500 ppm from the frequency at which the calibration operation was performed without requiring further calibration. However, if the frequency is moved outside of this range then a new calibration cycle must be initiated. At reset the VCO frequency is set to 2.5 GHz. Therefore, once calibrated, the actual output frequency can be set to any value between 2.49875 GHz and 2.50125 GHz without needing to reinitiate the calibration process. This +/- 500 ppm adjustment range should be adequate for any application in which the output frequency is set and subsequently fine-tuned. Refer to the *Applications Information* section for further details of setting the VCO output frequency and initiating recalibration.

The VCO PLL block provides a lock detect signal, LD, to indicate when lock has been achieved after a recalibration cycle. This is an open-drain pin that is pulled low until lock is established, at which time it is released and pulled high by an external pull-up resistor. This allows the LD pins of multiple ACS1790T devices to be connected together to provide a single overall lock indication.

The output divider block

The output of the VCO PLL block drives the divider block that consists of a number of cascaded dividers, and a multiplexer, as shown in Figure 3.

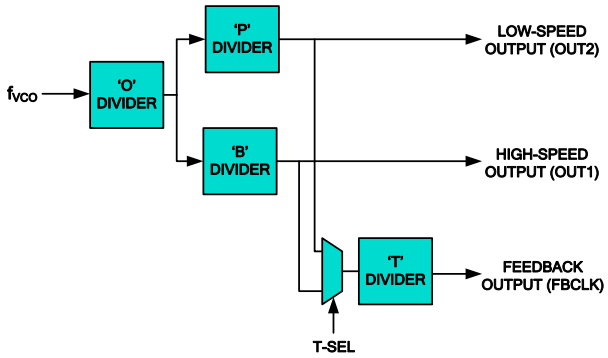

Figure 3 : ACS1790T Output Divider Structure

The O-divider is a shared prescaler whereas the B- and P-dividers are specific to the OUT1 and OUT2 outputs respectively. The T-divider further divides down either the OUT1 or OUT2 output to generate the feedback clock that is used when the ACS1790T forms the controllable oscillator portion of an external phase-locked loop, such as when the ACS1790T is used in conjunction with a suitable ToPSync device.

The O, P, B and T-dividers are individually programmable, and together with the frequency of the VCO, determine the ACS1790T output frequencies. Additionally, the P and B-dividers can be individually disabled in the case that only a single output is being used to reduce power consumption and device noise. The T-divider, which is responsible for generating the low-speed feedback output, FBCLK, can be driven from the output of either the P or B-divider through the multiplexer shown in Figure 3.

Refer to the *Using the ACS1790T* section for further information on the output dividers.

The output stage

The ACS1790T provides a total of three clock outputs – a high-speed LVPECL output, OUT1; a low-speed LVCMOS output, OUT2 and; a low-speed LVCMOS feedback clock, FBCLK.

The OUT2 output features a separate power supply pin for the output buffer, allowing operation at 1.8V, 2.5V or 3.3V. There is also a slew-rate limiting option on the OUT2 output to slow the edge-rate of the output clock. The FBCLK output operates at a fixed 3.3V level.

An active-low output enable signal, OEB, is provided to disable the OUT1 and OUT2 outputs, and these outputs can also be disabled under software control.

The control block

The control block is responsible for control of the other parts of the ACS1790T and includes a set of registers accessible to an external device through a standard I²C interface. These registers allow configuration of the VCO PLL, output dividers and output stage, as well as monitoring of the ACS1790T's status. The registers are fully documented in the section entitled *Register-based Device Configuration*.

Reset

The control block is also responsible for handling device reset. The ACS1790T includes a power monitor to reset the device automatically at power-up, and an external, active-low, reset pin, RESETB.

During reset, all the registers are reset to their default values, the I²C interface is reset and the clock outputs are held inactive. Immediately after reset, the registers are loaded with default values dependent on the state of the MODE and OSCFSEL[1:0] pins (see the section entitled *Hardware Device Configuration*) to enable generation of frequencies for 1G or 10G Ethernet designs. The VCO will automatically enter a calibration cycle during which the lock-detect pin, LD, is driven low. Once the calibration cycle is complete the LD pin is released and the outputs are activated (unless disabled). The ACS1790T is now fully functional and can be programmed under software control.

Using the ACS1790T

There are two methods of programming the ACS1790T. The initial operating mode is determined by the state of various device pins that are sampled at power-up and reset. Subsequent control, and status monitoring, is provided through a set of registers accessible to an external microprocessor through an I²C-compatible interface.

Hardware device configuration

There are three device pins that determine the initial operating state at power-up and reset – OSCFSEL0, OSCFSEL1 and MODE.

The state of these pins is sampled during reset and the pins have internal pull-down mechanisms to ensure that valid inputs are sensed even if the pin is left floating. In a typical application these configuration pins would be connected to a static level, either by tying them directly to ground or 3.3V as appropriate, or connecting them to ground or 3.3V through a pull-up/pull-down resistor. The presence of the internal pull-down means that care needs to be taken when using an external pull-up resistor to ensure that the voltage at the pin exceeds the minimum V_{IH} threshold. A single 4.7Kohm resistor per pin, or a 1Kohm resistor shared between up to three pins, is recommended to ensure this requirement is met.

Should dynamic control of the hardware configuration pins be required then they can be actively driven from logic. However, since the state of these pins is only sampled at reset, it is necessary to reset the ACS1790T, by asserting RESETB, whenever the state of the configuration pins is changed.

Input clock frequency selection

The two OSCFSEL pins determine the frequency of the ACS1790T's input clock. Table 2 shows the acceptable frequencies.

Table 2 : Input Clock Frequency Selection

OSCFSEL1	OSCFSEL0	Input Frequency of CLK
0	0	20 MHz
0	1	10 MHz
1	0	12.8 MHz
1	1	25 MHz

The 10, 12.8 and 20 MHz options correspond to the supported reference clock frequencies of the ToPSync family allowing a single oscillator and OSCFSEL setting to be shared between the two parts when the ACS1790T is used as a companion to a ToPSync device. The 25 MHz input frequency is not supported by the ToPSync but is a frequency commonly found in Ethernet applications and easily generated using very-low cost oscillators.

Default output frequency selection

The MODE pin determines the initial output frequencies from the ACS1790T as shown in Table 3.

Table 3 : Default Output Frequency Selection

MODE	OUT1	OUT2	Typical Application
0	125 MHz	25 MHz	Gigabit Ethernet
1	156.25 MHz	25 MHz	10 Gigabit Ethernet

When the ACS1790T is used in a Synchronous Ethernet application the MODE pin will typically be set to generate the appropriate output frequencies for the desired Ethernet speed. This allows the ACS1790T's outputs to provide clocks to the Ethernet circuitry immediately after reset prior to any additional configuration being performed.

When the ACS1790T is used for an application other than Synchronous Ethernet, for example as a Sonet clock generator, it is unlikely that either setting of the MODE pin will provide the desired output frequency. In this case, the MODE pin setting is arbitrary and the ACS1790T output frequency must be set via the I²C interface, either from a microprocessor or a companion ToPSync, prior to the output clocks being used.

Register-based device configuration

The ACS1790T incorporates eleven user-accessible registers accessed by a microprocessor or companion ToPSync through an industry-standard I²C interface. This section documents these registers and the method of accessing them. Since the I²C bus is a widely-adopted standard, non-ACS1790T specific details, such as the general I²C protocol, are not included here. For this information refer to the I²C specification, which can be obtained from NXP Semiconductors.

The ACS1790T I²C interface meets the requirements of an F/S-mode I²C device as defined in the I²C specification. The ACS1790T is able to complete register accesses faster than the I²C bus and therefore cycle-stretching is unnecessary and SCL is an input only to the ACS1790T. For full electrical and timing characteristics of the I²C interface refer to the *Electrical Specifications* section.

I²C slave address selection

The ACS1790T provides two address selection pins, A0 and A1, to allow one of four different I²C slave addresses to be selected as shown in Table 4. This allows a single device, such as a ToPSync, to control up to four associated ACS1790T devices.

Table 4 : I²C Interface Slave Address Selection

A1	A0	I²C Slave Address (0x0)
0	0	C0 (b'1100 000x)
0	1	C2 (b'1100 001x)
1	0	C4 (b'1100 010x)
1	1	C6 (b'1100 011x)

The A0 and A1 address pins should be connected to static levels on the PCB – either directly to power or ground or through 4.7K-ohm, or lower, resistors. The state of these pins should not be changed during operation.

I²C Write

Figure 4 shows the process used to write one or more registers. The operation is initiated by the host generating a start, or repeated start, condition and then writing the appropriate slave address (with bit 0 clear) followed immediately by the eight bit address of the first register to be written and then one or more data bytes containing the desired register contents. After each register write the register address pointer is automatically incremented unless it has reached the address of the highest register, 0x0A. This allows multiple consecutive registers to be written simply by sending additional data bytes. The host must generate either a stop or a repeated start condition to terminate the write operation. The ACS1790T acknowledges the slave address, and all subsequent bytes written, in accordance with the I²C specification.

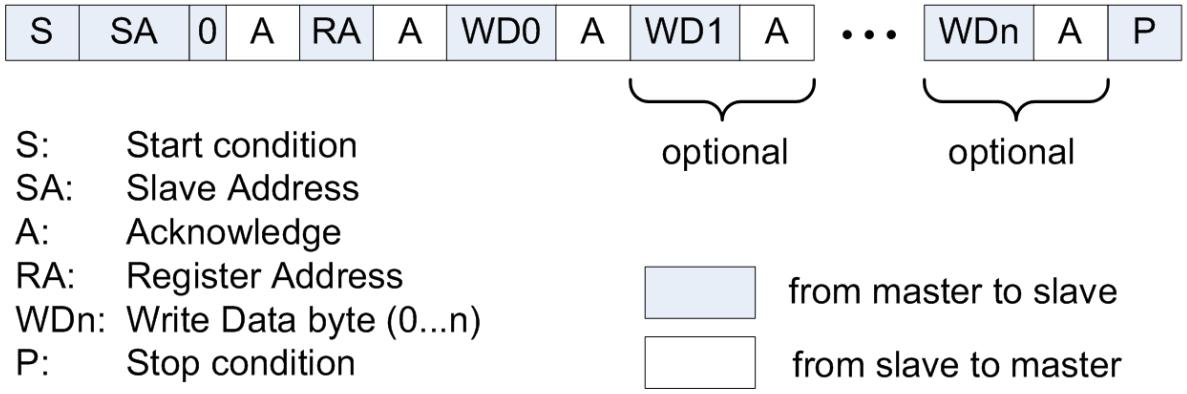

Figure 4 : I²C Write Operation

I²C Read

Figure 5 shows the process used to read one or more registers. It starts off in the same way as a register write operation, with the host writing the slave address (with bit 0 clear) followed by the address of the register to access. However, the host must then issue a repeated start condition, or optionally a stop followed by a start, followed by a write of the slave address with bit 0 set to initiate a read operation. The host can then read consecutive registers as required until generating a final stop condition. As for write operations, the auto-increment of the address stops at the last register, allowing this register to be polled with repeated reads without needing to re-write the register address. In accordance with the I²C specification, the host must acknowledge receipt of each byte read, by driving SDA low during the ninth bit time of the byte, except for the last byte that must not be acknowledged (by allowing SDA to float). This signals the ACS1790T to not drive SDA during the next bit time so that the host can generate the stop condition.

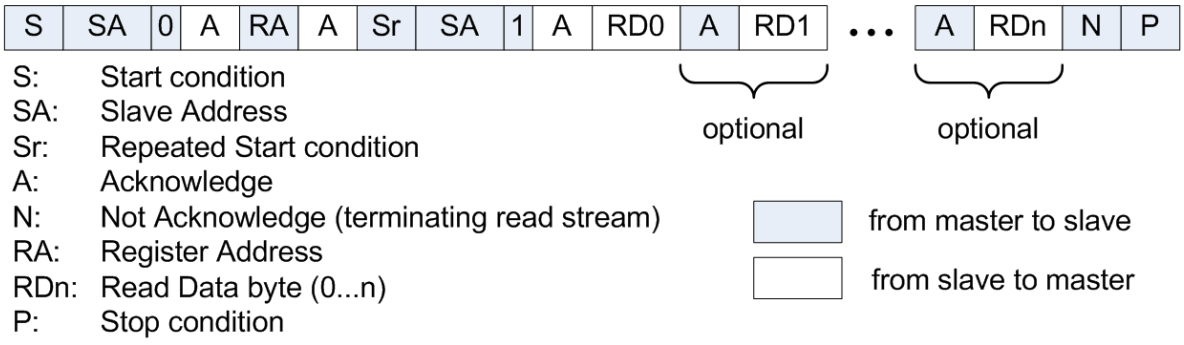

Figure 5 : I²C Read Operation

Register map

Table 5 shows the ACS1790T register map.

Table 5 : ACS1790T Register Map

Register name	Address	Default	Bit significance							
			7 (MSB)	6	5	4	3	2	1	0 (LSB)
reg_status	00	*		mode	oscfsel1	oscfsel0	a0	a1	oeb	lock
reg_output	01	6C		fbclk_ auto_ squelch	out1/2_ auto_ squelch	fbclk_ enable	out1_ enable	out2_ enable	out2_ slew-rate	out2_ drive
reg_n_div	02	*	integer portion of VCO feedback divider							
reg_k_div_hi	03	*	bits [23:16] of fractional portion of VCO feedback divider							
reg_k_div_med	04	00	bits [15:8] of fractional portion of VCO feedback divider							
reg_k_div_lo	05	00	bits [7:0] of fractional portion of VCO feedback divider							
reg_o_div	06	*					prescaler division ratio			
reg_b_div	07	*						out1 division ratio		
reg_t_div	08	00	fbclk_ select				feedback divider ratio			
reg_p_div	09	*				out2 division ratio				
reg_vco	0A	01								vco_ calibrate
reg_dither	1B	*	(preserve)		dither	(preserve)				

Address and default values are in hexadecimal

** indicates that the default value of this register is determined by the state of the hardware configuration pins at reset*

Other register addresses are reserved for factory test purposes. For correct operation undocumented addresses must not be read or written.

Register Descriptions

Status Register

Software name	Address (0x0)	Access	Default value
reg_status	00	Read-only	0*** ***0
Description	Status register		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	-	not used	-	-	0
6	mode	Indicates the state of the MODE pin as sampled at power-up or last reset	0 1	MODE is low (gigabit Ethernet mode) MODE is high (10-gigabit Ethernet mode)	*
5	oscfsel1	Indicates the state of the OSCFSEL1 pin as sampled at power-up or last reset	0 1	OSCFSEL1 is low OSCFSEL1 is high	*
4	oscfsel0	Indicates the state of the OSCFSEL0 pin as sampled at power-up or last reset	0 1	OSCFSEL0 is low OSCFSEL0 is high	*
3	a0	Indicates the state of the A0 I²C address pin as sampled at power-up or last reset	0 1	A0 is low A0 is high	*
2	a1	Indicates the state of the A1 I²C address pin as sampled at power-up or last reset	0 1	A1 is low A1 is high	*
1	oeb	Indicated the current state of the output enable pin	0 1	OEB is low (outputs are enabled) OEB is high (outputs are disabled)	*
0	lock	VCO PLL lock status	0 1	VCO PLL is not locked VCO PLL is locked	0

Output control register

Software name	Address (0x0)	Access	Default value
reg_output	01	Read-write	0110 1100
Description	Output control register		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	-	not used	-	-	0
6	fbclk_auto_squelch	Controls whether the feedback clock output is deactivated (held low) when the VCO PLL is out not locked	0 1	FBCLK toggling when VCO PLL not locked FBCLK low when VCO PLL not locked	1
5	out1/2_auto_squelch	Controls whether the OUT1 and OUT2 clock outputs are deactivated (held low) when the VCO PLL is out not locked	0 1	OUT1/2 toggling when VCO PLL not locked OUT1/2 low when VCO PLL not locked	1
4	fbclk_enable	Controls whether the feedback clock output is enabled	0 1	FBCLK is held low FBCLK is driven by output of T-divider	0

3	out1_ enable	Controls whether the OUT1 clock output is enabled	0 1	OUT1 is held low OUT1 is driven by output of B-divider	1
2	out2_ enable	Controls whether the OUT2 clock output is enabled	0 1	OUT2 is held low OUT2 is driven by output of P-divider	1
1	out2_slew_ rate	Controls the OUT2 pin slew rate	0 1	Fast OUT2 edge rate Slow OUT2 edge rate	0
0	out2_ drive	Controls the OUT2 pin drive strength	0 1	Low OUT2 drive (2.5V and 3.3V) High OUT2 drive (1.8V)	0

VCO PLL feedback divider registers

Software name	Address (0x0)	Access	Default value
reg_n_div	02	Read-write	**** ****
Description	VCO PLL feedback divider (integer portion)		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	n_div[7:0]	Holds the integer portion of the VCO PLL feedback divider – 67 For correct operation, division ratios that result in the VCO frequency being outside the range 2.3 – 2.7 GHz must not be programmed	0x00 0x01 : 0xF7 0xF8	Integer division ratio = 67 Integer division ratio = 68 : Integer division ratio = 314 Integer division ratio = 315 (Do not program values 0xF9– 0xFF)	

Software name	Address (0x0)	Access	Default value
reg_k_div_hi	03	Read-write	**** ****
Description	Bits [23:16] of the VCO PLL feedback divider (fractional part)		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	k_div [23:16]	Bits [23:16] of the fractional part of the VCO PLL feedback divider * 2^{24} (Bit 23 corresponds to a value of 0.5)			

Software name	Address (0x0)	Access	Default value
reg_k_div_med	04	Read-write	0000 0000
Description	Bits [15:8] of the VCO PLL feedback divider (fractional part)		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	k_div [15:8]	Bits [15:8] of the fractional part of the VCO PLL feedback divider * 2^{24} (Bit 15 corresponds to a value of 2^{-9})			

Software name	Address (0x0)	Access	Default value
reg_k_div_lo	05	Read-write	0000 0000
Description	Bits [7:0] of the VCO PLL feedback divider (fractional part)		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	k_div [7:0]	Bits [7:0] of the fractional part of the VCO PLL feedback divider * 2^{24} (Bit 0 corresponds to a value of 2^{-24}) A write to this register forces the VCO PLL feedback divider to by updated with the values programmed into the *n_div* and *k_div* registers			

Output divider control registers

Software name	Address (0x0)	Access	Default value
reg_o_div	06	Read-write	0000 ****
Description	The O-divider (prescaler) division ratio		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	-	not used	-	-	0000
[3:0]	o_div [3:0]	Sets the division ratio of the O-divider, which is the VCO PLL prescaler shared between the OUT1 and OUT2 outputs	0000	Prescaler divides by 4	****
			0001	Prescaler divides by 6	
			0010	Prescaler divides by 8	
			0011	Prescaler divides by 10	
			0100	Prescaler divides by 12	
			0101	Prescaler divides by 14	
			0110	Prescaler divides by 16	
			0111	Prescaler divides by 18	
			1000	Prescaler divides by 20	
			1001	Prescaler divides by 22	
			1010	Prescaler divides by 24	
			1011	Prescaler divides by 26	
			1100	Prescaler divides by 28	
			1101	Prescaler divides by 30	
			1110	Do not use	
			1111	Do not use	

Software name	Address (0x0)	Access	Default value
reg_b_div	07	Read-write	0000 0***
Description	The B-divider (OUT1) division ratio		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:3]	-	not used	-	-	00000
[2:0]	b_div [2:0]	Sets the division ratio of the B-divider, which is used to drive the OUT1 output	000	Disable B-divider (OUT1 is held low)	***
			001	Bypass divider	
			010	Divide by 2	
			011	Divide by 4	
			100	Divide by 8	
			101	Divide by 16	
			110	Do not use	
			111	Do not use	

Software name	Address (0x0)	Access	Default value
reg_t_div	08	Read-write	0000 0000
Description	The T-divider (FBCLK) division ratio		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	fbclk_ select	T-divider clock source select	0	The T-divider is driven with the OUT1 clock frequency	0
			1	The T-divider is driven with the OUT2 clock frequency	
[6:4]	-	not used	-	-	000
[3:0]	t_div [2:0]	Sets the division ratio of the T-divider, which divides either the OUT1 or OUT2 output frequency to generate the FBCLK output	0000	T-divider is disabled (FBCLK is held low)	0000
			0001	Bypass divider	
			0010	Divide by 2	
			0011	Divide by 4	
			0100	Divide by 8	
			0101	Divide by 16	
			0110	Divide by 32	
			0111	Divide by 64	
			1000	Divide by 128	
			1001	Divide by 256	
			1010	Divide by 512	
			1011	Divide by 1024	
			1100	Divide by 2048	
			1101	Divide by 4096	
			1110	Divide by 8192	
			1111	Divide by 16384	

Software name	Address (0x0)	Access	Default value
reg_p_div	09	Read-write	000* ****
Description	The P-divider (OUT1) division ratio		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:5]	-	not used	-	-	000
[4:0]	p_div [4:0]	Sets the division ratio of the P-divider, which is used to drive the OUT2 output	00000	Disable P-divider (OUT2 is held low)	*****
			00001	Divide by 2	
			00010	Divide by 4	
			00011	Divide by 5	
			00100	Divide by 8	
			00101	Divide by 10	
			00110	Divide by 16	
			00111	Divide by 25	
			01000	Divide by 32	
			01001	Divide by 64	
			01010	Divide by 128	
			01011	Divide by 256	
			01100	Divide by 512	
			01101	Divide by 1024	
			01110	Divide by 2048	
			01111	Divide by 4096	
			10000	Divide by 8192	
			10001	Divide by 16384	
			10010	Divide by 32768	
			10011	Divide by 65536	
			10100 : 11111	Do not use values 10100 - 11111	

VCO calibration request register

Software name	Address (0x0)	Access	Default value
reg_vco	0A	Read-write	0000 0001
Description	Controls the VCO calibration process		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:1]	-	not used	-	-	0
0	vco_ calibrate	Setting this bit forces the VCO to recalibrate to its optimum operating point after a large frequency change (Bit is cleared automatically)	0	No action (write) / Calibration complete (read)	1
			1	Force calibration (write) / Calibration in process (read)	

Software name	Address (0x0)	Access	Default value
reg_dither	1B	Read-write	**0* ****

Description Status register

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:6]	-	Reserved[1]	-	-	*
5	dither	Enable fractional divider dithering	0 1	K-divider value is used as programmed K-divider value is extended with one additional fractional bit forced to 1	0
[4:0]	-	Reserved[1]	-	-	*

[1] For correct operation the current value of these bits must be preserved when changing the dither setting. Therefore, to change the dither setting software must read this register, and rewrite the value read with bit 5 set or cleared as needed.

VCO calibration and lock detection

The VCO can generate any frequency between 2.3 and 2.7 GHz, with an ultra-fine resolution of less than 1 ppb. However, locking to an arbitrary frequency requires the VCO to be calibrated to select its optimal operating point. The VCO calibration process is initiated automatically at power-up or reset to set the VCO to its default frequency of 2.5 GHz, and can be retriggered at any time by writing a '1' to the *vco_calibrate* bit (bit 0 of *reg_vco*). This bit will remain set while the calibration process is executed and will be automatically cleared once it is complete and the VCO PLL is locked.

Once the VCO PLL has been calibrated for a given frequency, the actual frequency can be adjusted by up to 500 ppm either side of the original frequency without needing to reinitiate a calibration cycle. However, if it is desired to change the output frequency by more than this amount then a recalibration cycle must be initiated once the new frequency has been programmed.

The active low, open-drain, lock-detect pin, LD, indicates the lock state of the VCO PLL. Whenever an out-of-lock condition is detected LD is pulled low to indicate that the output frequency cannot be relied on. If the auto-squelch option is enabled then the corresponding output is automatically held low until lock is established. Initiating a recalibration cycle causes the LD pin to be driven low immediately.

Fractional divider dithering

By default, the programmed K-divider value is used directly to determine the ratio of the VCO output frequency to the reference clock frequency (after scaling by the R-divider). This allows the output frequency to be determined precisely, subject to the resolution of the K-divider. However, for K-divider values in which the fractional portion is $1/2^n$ (0.5, 0.25, 0.125 etc.), the nature of fractional division can result in excessive deterministic jitter being generated on the output. To avoid this, the *dither* bit (bit 5 of *reg_dither*) can be set to append a fixed '1' bit to the fractional portion of the K-divider, effectively adding $1/2^{-25}$ to the programmed value.

Using this dither feature can significantly reduce the deterministic jitter for certain K-divider settings. However, it will also result in a fixed error in the output frequency of the order of 0.25 ppb. In applications where the ACS1790T is operated as part of a closed loop system, such as when being controlled by a ToPSync device with the output frequency monitored through the FBCLK pin, the control loop will remove this fixed error over time so the average output frequency will be correct. However, when the ACS1790T is operated in an open-loop mode, either to generate a non-disciplined output frequency or when the reference clock itself is disciplined, for example when ToPSync is tuning a VCXO, then the fixed error will not be removed and the resultant output frequency will show a corresponding inaccuracy resulting in an unbounded Maximum Time Interval Error (MTIE) measurement. Whether this fixed error is acceptable or not will depend on the application, and therefore the overall system requirements should be considered before enabling the dithering feature in open-loop operation.

Output enable control and squelching

OUT1 and OUT2

The behavior of the OUT1 and OUT2 outputs is determined by a number of factors which control whether the pins are actively driven with the corresponding output frequency, held inactive or tri-stated. Table 6 indicates the behavior of the outputs under various conditions.

The automatic squelch capability shown in Table 6 allows the outputs to be forced inactive at any time the VCO is unlocked, as indicated by the LD pin being pulled low. This capability is enabled by setting the *out1/2_Auto_Squelch* bit (bit 5 of *reg_output*).

Table 6 : OUT1 and OUT2 Output Control

	Input Pin Setting		*Power-on reset*	*Lock State*	*Register Settings*			*Clock Output State*
	RESETB	*OEB*			*out1/2_ Auto_ Squelch*	*outn_ Enable*	*B (OUT1) or P (OUT2) Divider Disabled*	*OUTn*
	X	X	Yes	Not locked	1	1	X	Hi-impedance
Reset	0	0	No	Not locked	1	1	X	Driven Low
	0	1	No	Not locked	1	1	X	Hi-impedance
Hardware Control	1	1	No	X	X	X	X	Hi-impedance
	1	0	No	Not locked	0	0	X	Hi-impedance
Unlocked	1	0	No	Not locked	0	1	No	Active (Toggling)
Operation	1	0	No	Not locked	1	0	X	Hi-impedance
	1	0	No	Not locked	1	1	X	Driven Low
	1	0	No	Not locked	X	1	Yes	Driven Low
	1	0	No	Locked	0	0	X	Hi-impedance
Normal	1	0	No	Locked	0	1	No	Active (Toggling)
Operation	1	0	No	Locked	1	0	X	Hi-impedance
	1	0	No	Locked	1	1	No	Active (Toggling)
	1	0	No	Locked	X	1	Yes	Driven Low

FBCLK

The low-speed feedback clock output pin, FBCLK, is simpler in operation than the OUT1 and OUT2 clocks since it doesn't support a tri-state option, and therefore is unaffected by the state of the OEB pin. Table 7 summarizes the behavior of the FBCLK output under various conditions.

The FBCLK output also features an auto-squelch feature with the same functionality as that of the OUT1 and OUT2 outputs. However, it is controlled by a separate bit – *fbclk_auto_squelch* in the *reg_output* register.

Table 7 : FBCLK Output Control

	Input Pin Setting	Power-on reset	Lock State	Register Settings			Clock Output State
	RESETB			FBCLK_Auto_Squelch	FBCLK_Enable	T-Divider Disabled	FBCLK
Reset	X	Yes	Not locked	1	0	X	Driven Low
	0	No	Not locked	1	0	X	Driven Low
Unlocked Operation	1	No	Not locked	0	0	X	Driven Low
	1	No	Not locked	0	1	No	Active (Toggling)
	1	No	Not locked	1	0	X	Driven Low
	1	No	Not locked	1	1	X	Driven Low
	1	No	Not locked	X	1	Yes	Driven Low
Normal Operation	1	No	Locked	0	0	X	Driven Low
	1	No	Locked	0	1	No	Active (Toggling)
	1	No	Locked	1	0	X	Driven Low
	1	No	Locked	1	1	No	Active (Toggling)
	1	No	Locked	X	1	Yes	Driven Low

OUT2 slew-rate and voltage control

The OUT2 CMOS clock output is capable of operating at 1.8V, 2.5V and 3.3V LVCMOS standards. It also supports a slew-rate limiting capability which can improve signal quality in some circumstances, such as when the output is driving a lengthy PCB trace, by reducing the rise and fall times of the clock edges.

The OUT2 pin has a separate dedicated power supply pin – VDDD2. This pin must be connected to 1.8V, 2.5V or 3.3V to set the OUT2 pin signalling level as required. Additionally, when operating at 1.8V it is necessary to set the *out2_drive* bit in the *reg_output* register to increase the drive strength of the output buffer. Failure to do so will result in reduced signal quality on the OUT2 output.

Table 8 summarises the requirements for each output standard on the OUT2 pin.

Table 8 : OUT2 Drive-Type Setting

OUT2 I/O Standard	Maximum Voltage Swing	VDDD2 Voltage	out2_drive Bit Setting
LVCMOS18	1.8V	1.8V	1
LVCMOS25	2.5V	2.5V	0
LVCMOS33	3.3V	3.3V	0

The slew-rate of the OUT2 pin is controlled by the *out2_slew_rate* bit in the *reg_output* register. When this bit is clear the OUT2 signal is driven with fast rise and fall times. Setting the *out2_slew_rate* bit increases the rise and fall times of the OUT2 signal. This in turn allows the OUT2 pin to drive considerably longer PCB traces (as long as several inches) without needing any termination. The *out2_slew_rate* bit is set by default.

Electrical Specifications

Maximum Ratings

Important Note: The Absolute Maximum Ratings, in the table below, are stress ratings only, and functional operation of the device at conditions other than those indicated in the Operating Conditions sections of this specification are not implied. Exposure to the absolute maximum ratings, where different to the operating conditions, for an extended period may reduce the reliability or useful lifetime of the product.

Table 9 : Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage VDDA, VDDD, VDDD2, VDDF	V_{DD}	-0.5	3.7	V
Input Voltage (non-supply pins)	Vin	-	3.7	V
Operating Junction Temperature	T_{JCT}	-	125	°C
Reflow Temperature	T_{RE}	-	260	°C
Storage Temperature	T_{stor}	-50	150	°C
ESD (Human Body Model)	ESD_{HBM}	-	2	kV
ESD (Charged Device Model)	ESD_{CDM}	-	1	kV
Latchup	I_{LU}	-100	100	mA

Operating Conditions

Table 10 : Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supply VDDA, VDDD, VDDF	V_{DD}	3.0	3.3	3.6	V
Power Supply VDDD2 (1.8V operation)	V_{DDD2}	1.71	1.8	1.89	V
Power Supply VDDD2 (2.5V operation)	V_{DDD2}	2.375	2.5	2.625	V
Power Supply VDDD2 (3.3V operation)	V_{DDD2}	3.0	3.3	3.6	V
Ambient Temperature Range	T_A	-40	-	+85	°C
Supply Current Inputs & digital	I_{DDD}	-	5	8	mA
Supply Current Synthesizer only	I_{DDF}	-	52	60	mA

Supply Current HF output[1]	I_{DDA}	-	19	28	mA
Supply Current LF output[2]	I_{DDD2}	-	12	15	mA
Total Power Dissipation[1,2]	P_{TOT}	-	290	400	mW
Package Thermal Resistance – still air	Θ_{JA}	-	-	32.2	c/w
Package Thermal Resistance – 1 m/s	Θ_{JA}	-	-	29.9	c/w
Package Thermal Resistance – 2 m/s	Θ_{JA}	-	-	28.1	c/w

Notes:
1. Assumes 200 MHz OUT1 output into 50 ohm LVPECL load terminated as shown in Figure 21.
2. Assumes 125 MHz OUT2 output driving 10 pF unterminated load.

DC Characteristics

Across all operating conditions, unless otherwise stated

Table 11 : DC Characteristics

DC Input Characteristics: CLK, OEB, A0, A1, OSCFSEL0, OSCFSEL1, MODE, RESETB pins

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2.0	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Pull-down Resistor (A0, A1, MODE, OSCFSEL0, OSCFSEL1)	R_{PD}	28	36	44	kΩ
Input Low Current (V_{IN} = VSSD)	I_{IL}	-	-	1	µA
Input High Current (V_{IN} = VDDD)	I_{IH}	-	-	130	µA

DC Input Characteristics: SDA and SCL pins

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	0.7 * VDDD	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.3 * VDDD	V
Input Low Current (V_{IN} = VSSD)	I_{IL}	-	-	1	µA
Input High Current (V_{IN} = VDDD)	I_{IH}	-	-	1	µA
Noise margin at low level	V_{nL}		200		mV
Noise margin at high level	V_{nH}		200		mV

DC Output Characteristics: FBCLK pin

Parameter	Symbol	Minimum	Typical	Maximum	Units
Vout *Low* (Iol = 4mA)	V_{OL}	0	-	0.3	V
Vout *High* (Ioh = -4mA)	V_{OH}	2.4	-	-	V
Output Low Current	I_{OL}	-	-	4	mA
Output High Current	I_{OH}	-	-	-4	mA

DC Output Characteristics: SDA, LD pins

Parameter	Symbol	Minimum	Typical	Maximum	Units
Vout *Low* (Iol = 4mA)	V_{OL}	0	-	0.4	V
Output Low Current	I_{OL}	-	-	4	mA

DC Output Characteristics: OUT2 pin

Parameter	Symbol	Minimum	Typical	Maximum	Units
Vout *Low* (VDDD2 = 1.8V, Iol = 1mA)	V_{OL}	0	-	0.3	V
Vout *High* (VDDD2 = 1.8V, Ioh = -1mA)	V_{OH}	1.3	-	-	V
Vout *Low* (VDDD2 = 2.5V, Iol = 2mA)	V_{OL}	0	-	0.3	V
Vout *High* (VDDD2 = 2.5V, Ioh = -2mA)	V_{OH}	1.7	-	-	V
Vout *Low* (VDDD2 = 3.3V, Iol = 4mA)	V_{OL}	0	-	0.3	V
Vout *High* (VDDD2 = 3.3V, Ioh = -4mA)	V_{OH}	2.4	-	-	V
Output Low Current	I_{OL}	-	-	4	mA
Output High Current	I_{OH}	-	-	-4	mA

DC Characteristics: OUT1P, OUT1N pins

Parameter	Symbol	Minimum	Typical	Maximum	Units
Vout *Low*[1]	V_{OL}	VDD – 2.1	-	VDD – 1.62	V
Vout *High*[1]	V_{OH}	VDD – 1.45	-	VDD – 1.0	V
Differential Output Voltage[1]	V_{OD}	550	-	900	mV

Notes:
1) Driving into a LVPECL 50Ω load biased to VDD – 2V

RF Characteristics

Across all operating conditions, unless otherwise stated

Table 12 : RF Characteristics

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
CLK Input Frequency	F_{REF}	External Clock Source	10	12.8	25	MHz
PFD Update Frequency[1]	$f\phi$	$f\phi$= FREF/R	10	-	12.8	MHz
VCO Center Frequency Range	f_{CEN}		2.3	2.5	2.7	GHz
OUT1 Integrated Jitter[2,3]	JITT1	155.52 MHz (12 kHz – 20 MHz)	-	0.56	0.8	ps (rms)
OUT1 Integrated Jitter[2,3]	JITT1	125 MHz (637 kHz – 20 MHz)	-	0.15	0.8	ps (rms)
OUT1 Integrated Jitter[2,3]	JITT1	125 MHz (1.875 MHz – 20 MHz)	-	0.11	0.8	ps (rms)
OUT1 Integrated Jitter[2,3]	JITT1	156.25 MHz (4 MHz – 80 MHz)	-	0.29	0.8	ps (rms)
OUT2 Integrated Jitter[2,3,4]	JITT2	25 MHz (12 kHz to 5 MHz)	-	0.8	1.0	ps (rms)
Loop Bandwidth	BW	Closed Loop	-	160	-	kHz
Harmonic Suppression	H2	Second Harmonic	TBA	-20	-	dBc
Output Reference Spurs		Offset = 12.8MHz	-	-67	-	dBc
Settling Time	T_{SET}	Across entire tuning range to 1 ppm precision	-	250	500	ms
Narrowband Lock Range	T_{RI}	Across entire tuning range	500	-	-	ppm
Tuning Step Size	f_{STEP}		-	-	1	ppb
Lock Time From Reset[5]	T_{LOCKR}		-	-	20	ms
Lock Time From Calibration[5]	T_{LOCKC}		-	-	10	ms

Notes:

1) Value of $f\phi$ is dependent on the input divider
2) Measured using Rakon CFPO-DO reference clock (12.8 MHz)
3) Measured using bandpass filter range and carrier frequency specified in “Test Condition” column
4) Measured using VDDD2 = 2.5V
5) As indicated by LD pin state

Table 13 : I²C Timing Specification

Parameter[1]	Symbol	Conditions	Min	Typ	Max	Unit
SCL Clock Frequency	f_{SCL}		0	-	400	kHz
SCL low period	t_{LOW}		1.3	-	-	us
SCL high period	t_{HIGH}		0.6	-	-	us
Data setup time	$t_{SU:DAT}$		100	-	-	ns
Data hold time	$t_{HD:DAT}$		0	-	-	ns
Repeated start setup time	$t_{SU:STA}$		0.6	-	-	us
Start condition hold time	$t_{SU:STA}$		0.6	-	-	us
Stop condition hold time	$t_{SU:STO}$		0.6	-	-	us
Bus free time between stop and start	t_{BUF}		1.3	-	-	us
Input glitch suppression	t_{SP}			-	50	ns

Notes:
1) Timing specifications refer to voltage levels (V_{IL}, V_{IH}, V_{OL}) defined in DC Characteristics

The interface complies with slave F/S mode as described by NXP: "I²C-bus specification, Rev. 03 – 19 June 2007".

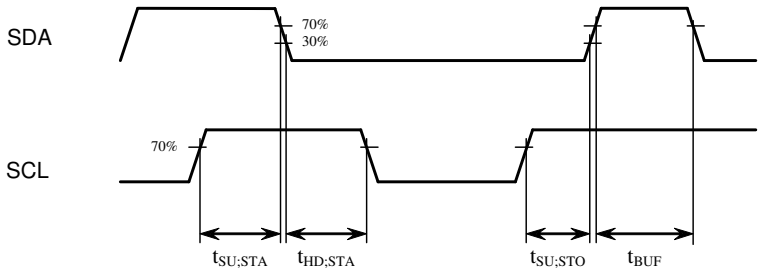

Figure 6 : I²C Start and Stop Timing

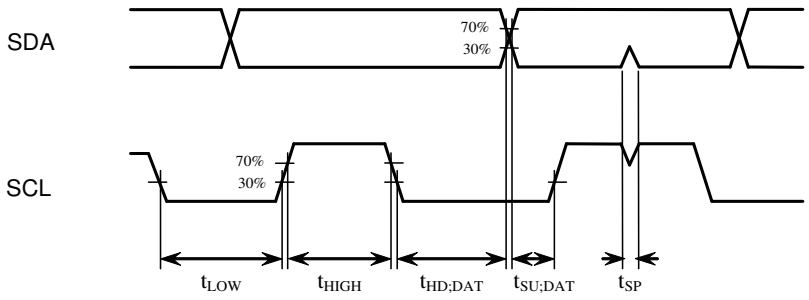

Figure 7 : I²C Data Timing