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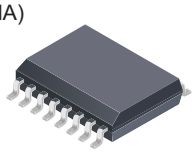
Single Phase, Isolated, Power Monitoring IC with Voltage Zero Crossing and Overcurrent Detection

FEATURES AND BENEFITS

- Accurate power monitoring of AC/DC applications
- Reinforced isolation up to 517 V_{RMS} in a single package eliminates the need for dual isolated supplies (certification pending)
- Active, reactive, and apparent power measurements, and power factor
- RMS and instantaneous voltage and current measurements
- 0.85 mΩ primary conductor resistance for low power loss and high inrush current withstand capability
- Dedicated voltage zero crossing pin
- Overcurrent fault output pin
- Hall-effect-based current measurement with common-mode stray field rejection
- User-programmable V_{RMS} under/overvoltage pin
- 1 kHz bandwidth
- Current-sensing range from 0 to 90 A
- I^2C or SPI communication
- User-programmable through EEPROM registers
- 16-bit voltage and current ADCs

PACKAGE

16-pin SOICW (suffix MA)



Not to scale

DESCRIPTION

The ACS71020 power monitoring IC greatly simplifies the addition of power monitoring to any AC/DC powered device. By making use of Allegro's Hall-effect-based, galvanically isolated integrated current sensor technology, reinforced isolation can be achieved. The sensor can be powered from the same supply as the MCU, eliminating the need for multiple power supplies and digital isolation ICs.

The isolated current measurement is done by detecting the magnetic field from the integrated conductor, eliminating the need for external sense resistors, current transformers, or Rogowski coils. Two Hall plates are used for this measurement to differentially sense the field, thus eliminating errors due to stray magnetic fields. Multiple parameters like bandwidth, averaging time, and fault levels are user-programmable.

The sensor features all key power measurements, which can be read out through I^2C or SPI, as well as dedicated pins for voltage zero crossing (suitable for light-dimming applications) and fast overcurrent fault (for short-circuit detection). As the sensor is isolated, these pins can be easily accessed by the MCU without additional isolation to each signal. These two pins can also be configured to flag a V_{RMS} under/overvoltage.

The ACS71020 is provided in a small, low-profile, surface-mount SOIC16 wide-body package. The ACS71020 is lead (Pb) free, and is fully calibrated prior to shipment from the factory. Further customer calibration in application can improve accuracy.

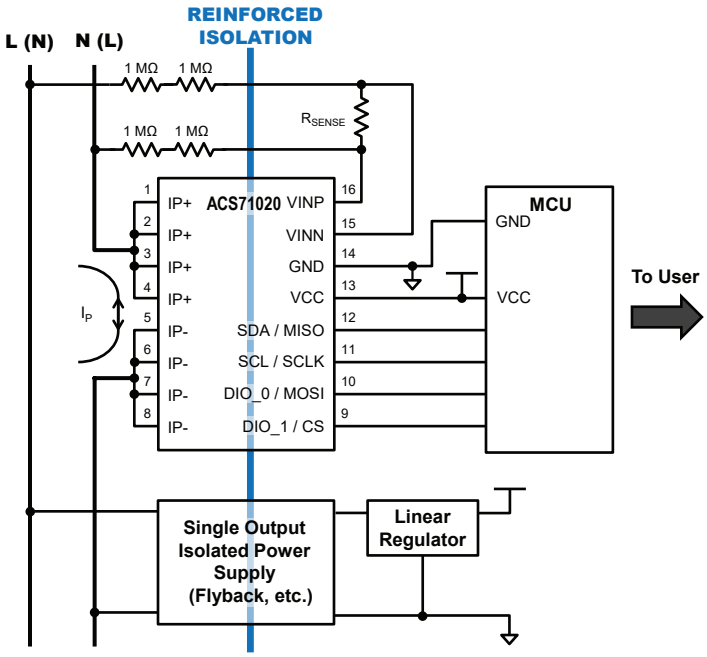
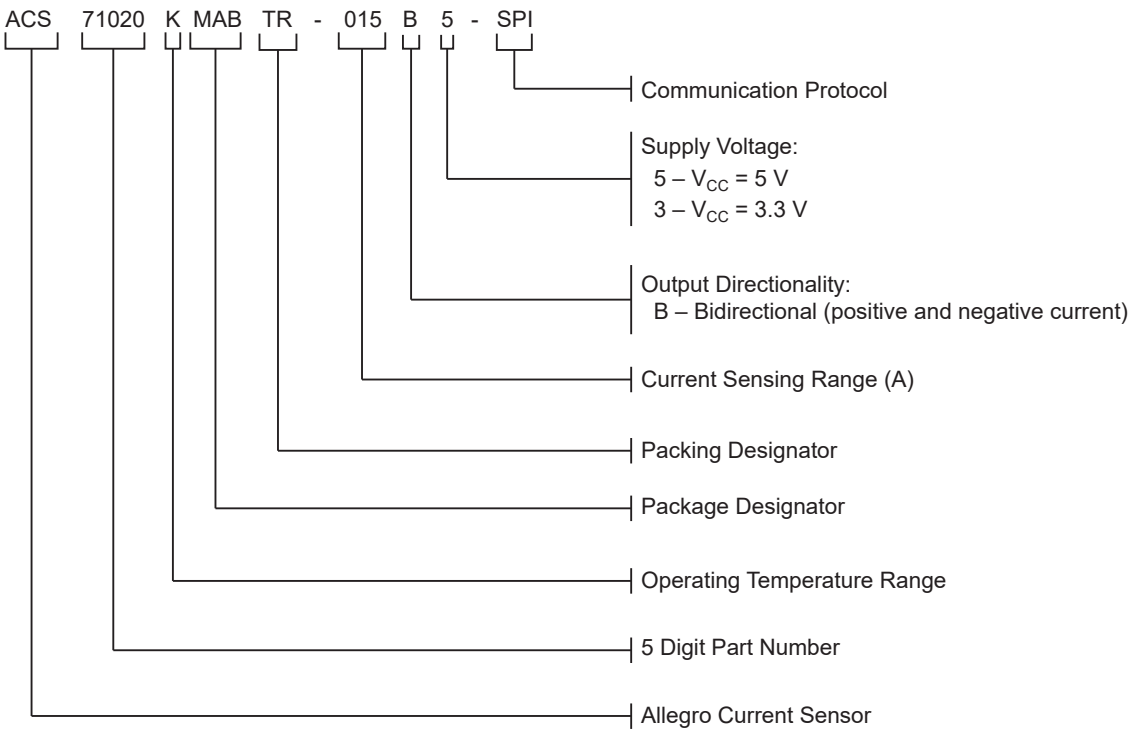


Figure 1: Typical Application

SELECTION GUIDE

Part Number	$V_{CC(NOM)}$ (V)	I_{PR} (A)	Communication Protocol	T_A (°C)	Packing [1]
ACS71020KMABTR-015B5-SPI	5	±15	SPI	–40 to 125	Tape and reel, 1000 pieces per reel, 3000 pieces per box
ACS71020KMABTR-030B3-SPI	3.3	±30			
ACS71020KMABTR-030B3-I2C	3.3	±30	I^2C		
ACS71020KMABTR-090B3-I2C	3.3	±90			

[1] Contact Allegro for additional packing options.



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		6.5	V
Reverse Supply Voltage	V_{RCC}		–0.5	V
Input Voltage	V_{INP}, V_{INN}		V_{CC} + 0.5	V
Reverse Input Voltage	V_{RNP}, V_{RNN}		–0.5	V
Digital I/O Voltage	V_{DIO}	SPI, I^2C, and general purpose I/O	6	V
Reverse Digital I/O Voltage	V_{RDIO}		–0.5	V
Operating Ambient Temperature	T_A	Range K	–40 to 125	°C
Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Dielectric Strength Test Voltage	V_{ISO}	Agency type-tested for 60 seconds per UL 60950-1 (edition 2). Production tested at 3000 V_{RMS} for 1 second, in accordance with UL 60950-1 (edition 2). (certification pending)	4800	V_{RMS}
Working Voltage for Basic Isolation	V_{WVBI}	Maximum approved working voltage for basic (single) isolation according to UL 60950-1 (edition 2). (certification pending)	1480	V_{PK}
			1047	V_{RMS} or V_{DC}
Working Voltage for Reinforced Isolation	V_{WVRI}	Maximum approved working voltage for reinforced isolation according to UL 60950-1 (edition 2). (certification pending)	730	V_{PK}
			517	V_{RMS} or V_{DC}
Clearance	D_{cl}	Minimum distance through air from IP leads to signal leads.	7.5	mm
Creepage	D_{cr}	Minimum distance along package body from IP leads to signal leads	7.5	mm

THERMAL CHARACTERISTICS

See https://www.allegromicro.com/en/Design-Center/Technical-Documents/Hall-Effect-Sensor-IC-Publications/DC-and-Transient-Current-Capability-Fuse-Characteristics.aspx.

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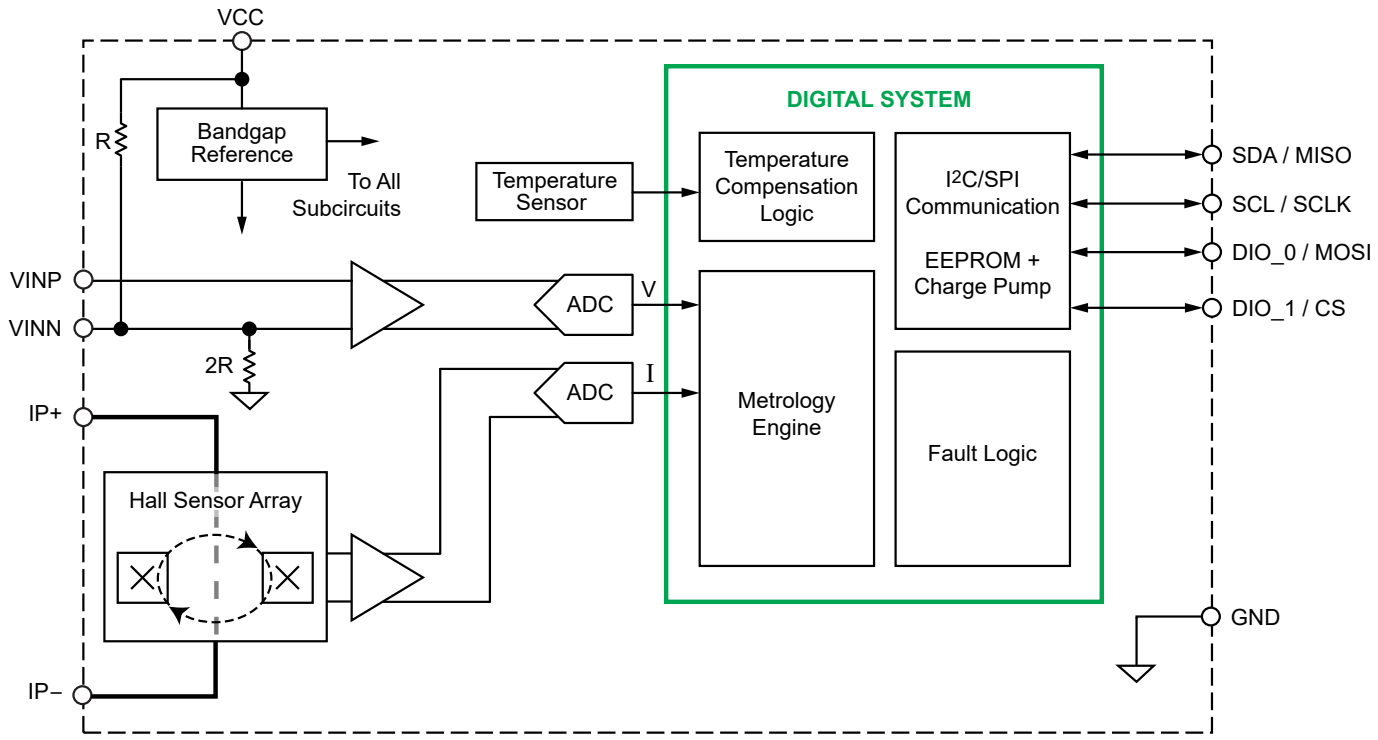
FUNCTIONAL BLOCK DIAGRAM



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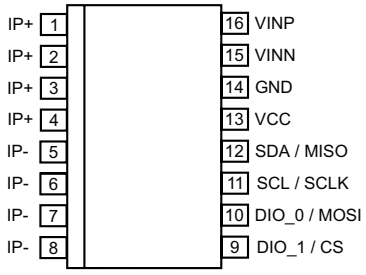
PINOUT DIAGRAM AND TERMINAL LIST



Pinout Diagram

Terminal List Table

Number	Name	Description	
		I2C	SPI
1, 2, 3, 4	IP+	Terminals for current being sensed; fused internally	
5, 6, 7, 8	IP-	Terminals for current being sensed; fused internally	
9	DIO_1 / CS	Digital I/O 1	Chip Select (CS)
10	DIO_0 / MOSI	Digital I/O 0	MOSI
11	SCL / SCLK	SCL	SCLK
12	SDA / MISO	SDA	MISO
13	VCC	Device power supply terminal	
14	GND	Device Power and Signal ground terminal	
15	VINN	Negative Input Voltage	
16	VINP	Positive Input Voltage	

DIGITAL I/O

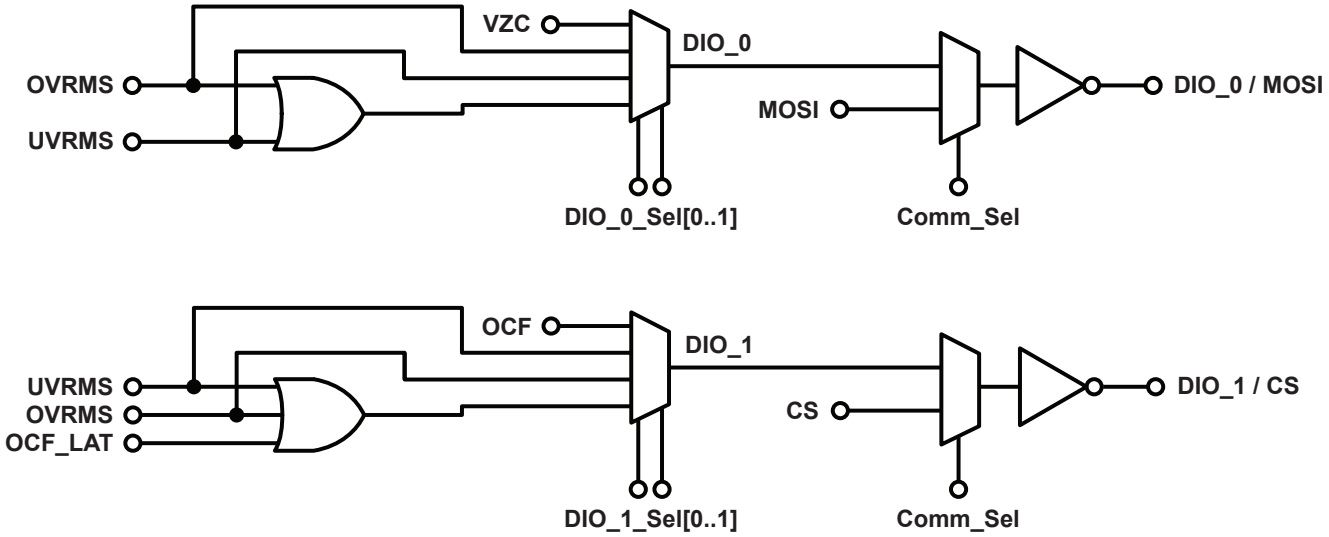
The Digital I/O can be programmed to represent the following functions (Digital Output pins are low true):

DIO_0:

0. VZC: Voltage zero crossing
1. OVRMS: The VRMS overvoltage flag
2. UVRMS: The VRMS undervoltage flag
3. The OR of OVRMS and UVRMS (if either flag is triggered, the DIO_0 pin will be asserted)

DIO_1:

0. OCF: Overcurrent fault
1. UVRMS: The VRMS undervoltage flag
2. OVRMS: The VRMS overvoltage flag
3. The OR of OVRMS, UVRMS, and OCF_LAT [Latched Overcurrent fault] (if any of the three flags are triggered, the DIO_1 pin will be asserted)



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COMMON ELECTRICAL CHARACTERISTICS [1]: Valid through the full range of T_A and V_{CC} = V_{CC}(nom), unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		$V_{CC(nom)}$ × 0.9	$V_{CC(nom)}$	$V_{CC(nom)}$ × 1.1	V
Supply Current	I_{CC}	V_{CC}(min) ≤ V_{CC} ≤ V_{CC}(max), no load on output pins	–	12	14	mA
VOLTAGE BUFFER						
Differential Input Range	ΔV_{IN}	$V_{INP} – V_{INN}$	–275	–	275	mV
Common Mode Input Voltage	$V_{IN(CM)}$		$^2/_3 \times V_{CC}$ – 0.275	–	$^2/_3 \times V_{CC}$ + 0.275	V
VOLTAGE ADC						
Sample Frequency	f_S		–	32	–	kHz
Number of Bits	$N_{ADC(V)}$		–	16	–	bits
Voltage ADC Power Supply Rejection	V_PSRR	Ratio of change on V_{CC} to change in ADC internal reference at DC	60	70	–	dB
VOLTAGE SIGNAL CHAIN						
Noise	V_N		–	10	–	LSB
Internal Bandwidth	BW		–	1	–	kHz
Linearity Error	E_{LIN}		–	±0.2	–	%
CURRENT CHANNEL ADC						
Sample Frequency	f_S		–	32	–	kHz
Number of Bits	$N_{ADC(I)}$		–	16	–	bits
Current Channel ADC Power Supply Rejection	I_PSRR	Ratio of change on V_{CC} to change in ADC internal reference at DC	60	70	–	dB
CURRENT CHANNEL						
Internal Bandwidth	BW		–	1	–	kHz
Primary Conductor Resistance	R_{IP}	T_A = 25°C	–	0.85	–	mΩ
Noise	V_N		–	100	–	LSB
Linearity Error	E_{LIN}		–	±1.5	–	%
OVERCURRENT FAULT CHARACTERISTICS						
Fault Response Time	t_{RF}	Time from I_P rising above I_{FAULT} until V_{FAULT} < $V_{FAULT(max)}$ for a current step from 0 to 1.2 × I_{FAULT}; 10 kΩ and 100 pF from DIO_1 to ground; fltdly set to 0	–	5	–	µs
Internal Bandwidth	BW		–	200	–	kHz
Fault Hysteresis [2]	I_{HYST}		–	0.05 × I_{PR}	–	A
Fault Range	I_{FAULT}	Set using FAULT field in EEPROM	0.5 × I_{PR}	–	1.75 × I_{PR}	A
VOLTAGE ZERO CROSSING						
Voltage Zero Crossing Delay	t_d		_	700		µs

[1] Device may be operated at higher primary current levels, I_P, ambient, T_A, and internal leadframe temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.
[2] After I_P goes above I_{FAULT}, tripping the internal fault comparator, I_P must go below $I_{FAULT} – I_{HYST}$, before the internal fault comparator will reset.

Continued on next page...

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xKMATR-I2C OPERATING CHARACTERISTICS: Valid through the full range of T_A, V_{CC} = V_{CC}(nom), R_{EXT} = 10 kΩ, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
I²C INTERFACE CHARACTERISTICS [1]						
Bus Free Time Between Stop and Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	t_{hdSTA}		0.6	–	–	µs
Setup Time for Repeated Start Condition	t_{suSTA}		0.6	–	–	µs
SCL Low Time	t_{LOW}		1.3	–	–	µs
SCL High Time	t_{HIGH}		0.6	–	–	µs
Data Setup Time	t_{suDAT}		100	–	–	µs
Data Hold Time	t_{hdDAT}		0	–	900	µs
Setup Time for Stop Condition	t_{suSTO}		0.6	–	–	µs
Logic Input Low Level (SDA, SCL pins)	V_{IL}		–	–	30	%V_{CC}
Logic Input High Level (SDA, SCL pins)	V_{IH}		70	_	–	%V_{CC}
Logic Input Current	I_{IN}	Input voltage on SDA or SCL = 0 V to V_{CC}	–1	_	1	µA
Output Low Voltage (SDA)	V_{OL}	SDA sinking = 1.5 mA	–	_	0.36	V
Clock Frequency (SCL pin)	f_{CLK}		–	_	400	kHz
Output Fall Time (SDA pin)	t_f	R_{EXT} = 2.4 kΩ, C_B = 100 pF	–	_	250	ns
I²C Pull-Up Resistance	R_{EXT}		2.4	10	–	kΩ
Total Capacitive Load for Each of SDA and SCL Buses	C_B		–	–	20	pF

[1] These values are ratiometric to the supply voltage, I²C Interface Characteristics are ensured by design and not factory tested.

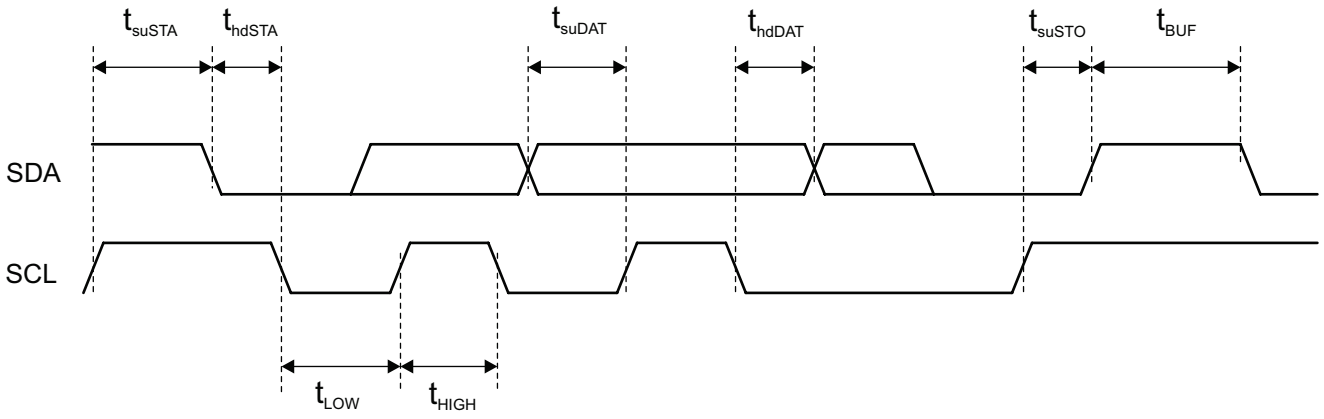

Figure 2: I²C Interface Timing

xKMATR-SPI OPERATING CHARACTERISTICS: Valid through the full range of T_A, V_{CC} = V_{CC}(nom), unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SPI INTERFACE CHARACTERISTICS						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, CS pins, V_{CC} (nom) = 3.3 V	2.8	–	3.63	V
		MOSI, SCLK, CS pins, V_{CC} (nom) = 5 V	4	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, CS pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	MISO pin, C_L = 20 pF, T_A = 25°C, V_{CC} (nom) = 3.3 V	2.8	3.3	3.8	V
		MISO pin, C_L = 20 pF, T_A = 25°C, V_{CC} (nom) = 5 V	4	5	5.5	V
SPI Output Low Voltage	V_{OL}	MISO pin, C_L = 20 pF, T_A = 25°C	–	0.3	0.5	V
SPI Clock Frequency	f_{SCLK}	MISO pin, C_L = 20 pF	0.1	–	10	MHz
SPI Frame Rate	t_{SPI}		5.8	–	588	kHz
Chip Select to First SCLK Edge	t_{CS}	Time from CS going low to SCLK falling edge	50	–	–	ns
Data Output Valid Time	t_{DAV}	Data output valid after SCLK falling edge	–	40	–	ns
MOSI Setup Time	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time	t_{CHD}	Hold SCLK high time before CS rising edge	5	–	–	ns
Load Capacitance	C_L	Loading on digital output (MISO) pin	–	–	20	pF

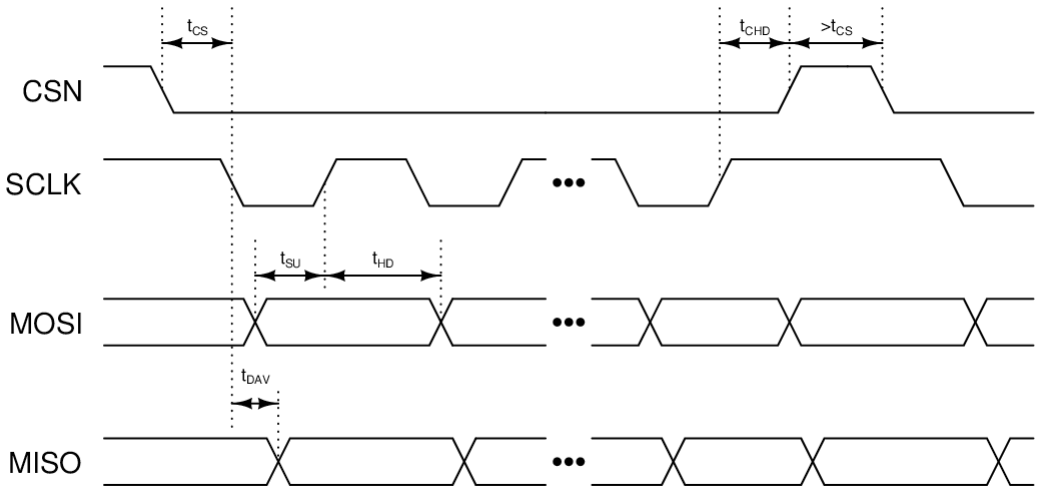

Figure 3: SPI Timing

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ACS71020KMA-015B5 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
GENERAL CHARACTERISTICS						
Nominal Supply Voltage	V_{CC} (nom)		–	5	–	V
NOMINAL PERFORMANCE – CURRENT CHANNEL						
Current Sensing Range	I_{PR}		–15	–	15	A
Sensitivity	$Sens_{(I)}$	I_{PR} (min) < I_P < I_{PR} (max)	–	2184	–	LSB/A
ACCURACY PERFORMANCE – CURRENT CHANNEL						
Total Output Error	$E_{TOT(I)}$	Measured at I_P = I_{PR} (max), T_A = 25°C to 125°C	–	±2	–	%
		Measured at I_P = I_{PR} (max), T_A = –40°C to 25°C	–	±3	–	%
TOTAL OUTPUT ERROR COMPONENTS – CURRENT CHANNEL						
Sensitivity Error	$E_{SENS(I)}$	Measured at I_P = I_{PR} (max), T_A = 25°C to 125°C	–	±1	–	%
		Measured at I_P = I_{PR} (max), T_A = –40°C to 25°C	–	±1.5	–	%
Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C	–	±300	–	LSB
		I_P = 0 A, T_A = –40°C to 25°C	–	±500	–	LSB
NOMINAL PERFORMANCE – VOLTAGE CHANNEL						
Sensitivity	$Sens_{(V)}$	V_{PR} (min) < V_P < V_{PR} (max)	–	238	–	LSB/mV
ACCURACY PERFORMANCE – VOLTAGE CHANNEL						
Total Output Error	$E_{TOT(V)}$	Measured at V_P = V_{PR} (max), T_A = 25°C to 125°C	–	±1.2	–	%
		Measured at V_P = V_{PR} (max), T_A = –40°C to 25°C	–	±1.3	–	%
TOTAL OUTPUT ERROR COMPONENTS – VOLTAGE CHANNEL						
Sensitivity Error	$E_{SENS(V)}$	Measured at V_P = V_{PR} (max), T_A = 25°C to 125°C	–	±1	–	%
		Measured at V_P = V_{PR} (max), T_A = –40°C to 25°C	–	±1	–	%
Offset Error	$E_{O(V)}$	V_P = 0 mV, T_A = 25°C to 125°C	–	±100	–	LSB
		V_P = 0 mV, T_A = –40°C to 25°C	–	±150	–	LSB
ACCURACY PERFORMANCE – ACTIVE POWER						
Total Output Error	$E_{TOT(P)}$	Measured at V_P = V_{PR} (max), T_A = 25°C to 125°C	–	±2.3	–	%
		Measured at V_P = V_{PR} (max), T_A = –40°C to 25°C	–	±3.3	–	%

[1] Typical values are based on mean ±3 sigma.

ACS71020KMA-030B3 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
GENERAL CHARACTERISTICS						
Nominal Supply Voltage	V_{CC} (nom)		–	3.3	–	V
NOMINAL PERFORMANCE – CURRENT CHANNEL						
Current Sensing Range	I_{PR}		–30	–	30	A
Sensitivity	$Sens_{(I)}$	I_{PR} (min) < I_P < I_{PR} (max)	–	1092	–	LSB/A
ACCURACY PERFORMANCE – CURRENT CHANNEL						
Total Output Error	$E_{TOT(I)}$	Measured at I_P = I_{PR} (max), T_A = 25°C to 125°C	–	±2	–	%
		Measured at I_P = I_{PR} (max), T_A = –40°C to 25°C	–	±3	–	%
TOTAL OUTPUT ERROR COMPONENTS – CURRENT CHANNEL						
Sensitivity Error	$E_{SENS(I)}$	Measured at I_P = I_{PR} (max), T_A = 25°C to 125°C	–	±1	–	%
		Measured at I_P = I_{PR} (max), T_A = –40°C to 25°C	–	±1.5	–	%
Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C	–	±500	–	LSB
		I_P = 0 A, T_A = –40°C to 25°C	–	±700	–	LSB
NOMINAL PERFORMANCE – VOLTAGE CHANNEL						
Sensitivity	$Sens_{(V)}$	V_{PR} (min) < V_P < V_{PR} (max)	–	238	–	LSB/mV
ACCURACY PERFORMANCE – VOLTAGE CHANNEL						
Total Output Error	$E_{TOT(V)}$	Measured at V_P = V_{PR} (max), T_A = 25°C to 125°C	–	±1.2	–	%
		Measured at V_P = V_{PR} (max), T_A = –40°C to 25°C	–	±1.3	–	%
TOTAL OUTPUT ERROR COMPONENTS – VOLTAGE CHANNEL						
Sensitivity Error	$E_{SENS(V)}$	Measured at V_P = V_{PR} (max), T_A = 25°C to 125°C	–	±1	–	%
		Measured at V_P = V_{PR} (max), T_A = –40°C to 25°C	–	±1	–	%
Offset Error	$E_{O(V)}$	V_P = 0 mV, T_A = 25°C to 125°C	–	±60	–	LSB
		V_P = 0 mV, T_A = –40°C to 25°C	–	±80	–	LSB
ACCURACY PERFORMANCE – ACTIVE POWER						
Total Output Error	$E_{TOT(P)}$	Measured at V_P = V_{PR} (max), T_A = 25°C to 125°C	–	±2.3	–	%
		Measured at V_P = V_{PR} (max), T_A = –40°C to 25°C	–	±3.3	–	%

[1] Typical values are based on mean ±3 sigma.

ACS71020KMA-090B3 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
GENERAL CHARACTERISTICS						
Nominal Supply Voltage	V_{CC} (nom)		–	3.3	–	V
NOMINAL PERFORMANCE – CURRENT CHANNEL						
Current Sensing Range	I_{PR}		–90	–	90	A
Sensitivity	$Sens_{(I)}$	I_{PR} (min) < I_P < I_{PR} (max)	–	364	–	LSB/A
ACCURACY PERFORMANCE – CURRENT CHANNEL						
Total Output Error	$E_{TOT(I)}$	Measured at I_P = I_{PR} (max), T_A = 25°C to 125°C	–	±2	–	%
		Measured at I_P = I_{PR} (max), T_A = –40°C to 25°C	–	±3	–	%
TOTAL OUTPUT ERROR COMPONENTS – CURRENT CHANNEL						
Sensitivity Error	$E_{SENS(I)}$	Measured at I_P = I_{PR} (max), T_A = 25°C to 125°C	–	±1	–	%
		Measured at I_P = I_{PR} (max), T_A = –40°C to 25°C	–	±1.5	–	%
Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C	–	±300	–	LSB
		I_P = 0 A, T_A = –40°C to 25°C	–	±500	–	LSB
NOMINAL PERFORMANCE – VOLTAGE CHANNEL						
Sensitivity	$Sens_{(V)}$	V_{PR} (min) < V_P < V_{PR} (max)	–	238	–	LSB/mV
ACCURACY PERFORMANCE – VOLTAGE CHANNEL						
Total Output Error	$E_{TOT(V)}$	Measured at V_P = V_{PR} (max), T_A = 25°C to 125°C	–	±1.2	–	%
		Measured at V_P = V_{PR} (max), T_A = –40°C to 25°C	–	±1.3	–	%
TOTAL OUTPUT ERROR COMPONENTS – VOLTAGE CHANNEL						
Sensitivity Error	$E_{SENS(V)}$	Measured at V_P = V_{PR} (max), T_A = 25°C to 125°C	–	±1	–	%
		Measured at V_P = V_{PR} (max), T_A = –40°C to 25°C	–	±1	–	%
Offset Error	$E_{O(V)}$	V_P = 0 mV, T_A = 25°C to 125°C	–	±100	–	LSB
		V_P = 0 mV, T_A = –40°C to 25°C	–	±150	–	LSB
ACCURACY PERFORMANCE – ACTIVE POWER						
Total Output Error	$E_{TOT(P)}$	Measured at V_P = V_{PR} (max), T_A = 25°C to 125°C	–	±2.3	–	%
		Measured at V_P = V_{PR} (max), T_A = –40°C to 25°C	–	±3.3	–	%

[1] Typical values are based on mean ±3 sigma.

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DATA ACQUISITION

ADCs

Both the Current and Voltage channels are sampled at a high frequency and then digitally filtered and decimated to avoid large anti-aliasing filters. The final sample rate will be near 32 kHz for an 8 MHz clock. The digital low-pass filters are EEPROM programmable and have a cutoff from 1 to 8 kHz. The digital word from the ADC is 16 bits for both the current and the voltage.

Raw Signal Sensitivity and Offset Trim

The gain and offset for both current and voltage channels use a shared temperature compensation engine which is trimmed in production. The fine sensitivity and offset are also trimmed in production at the factory; however, the user has access to the fine sensitivity field for the current channel should they want to trim the gain in application.

Phase Compensation

Phase delay may be introduced on either the voltage or current channels. The range is EEPROM selectable, either 5° of delay (step size of 0.67°) or 40° of delay (step size of 5.36°).

Zero Crossing

The zero crossings are only detected on the voltage signal. Both the high-to-low and low-to-high transitions will be detected with time-based hysteresis that removes the possibility of noise causing multiple zero crossings to be reported at each true zero crossing.

The zero crossing output can be a square wave that transitions at each zero crossing or a pulse with a fixed width at each zero crossing. When in pulse mode, the width of the pulse is t_P (see delaycnt_sel; nominal setting is 32 µs). There will be a fixed delay, t_D, from the time that a true zero crossing has occurred to the time that it is reported. This delay helps to keep the zero crossing detection more precise.

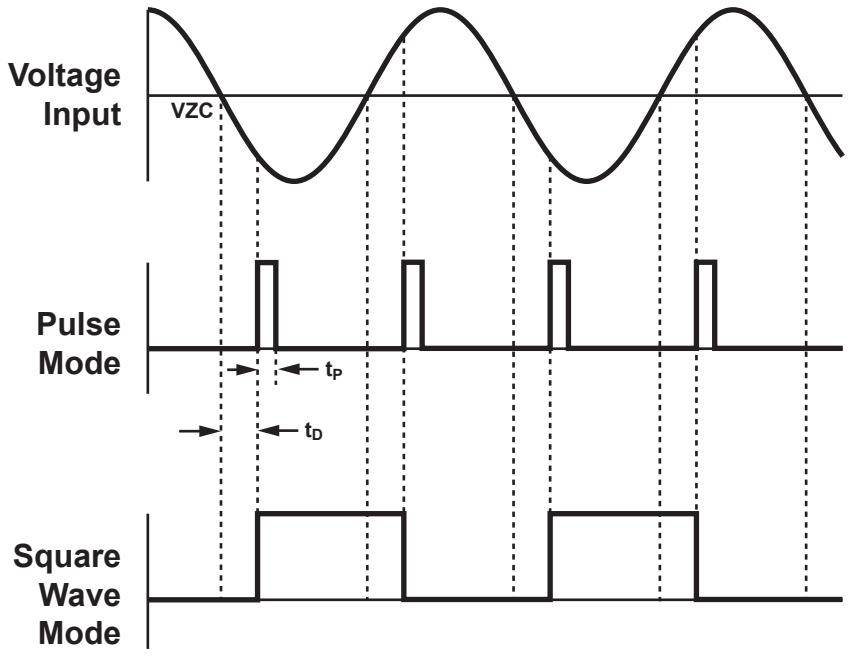

Figure 4: Zero Crossing

POWER CALCULATIONS

I_{RMS} / V_{RMS}

Cycle by cycle calculation of the root mean square of both the current and voltage channels:

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{n=N-1} I_n^2}{N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{n=N-1} V_n^2}{N}}$$

where I_n (Icodes) and V_n (Vcodes) are the instantaneous measurements of current and voltage, respectively.

Active Power

The real component of power being measured; calculated cycle by cycle:

$$P_{ACTIVE} = \frac{\sum_{n=0}^{n=N-1} P_n}{N} \qquad P_n = I_n \times V_n$$

Apparent Power

The magnitude of the complex power being measured; calculated at the end of each cycle:

$$|S| = I_{RMS} \times V_{RMS}$$

Reactive Power

Imaginary component of power being measured; calculated at the end of each cycle:

$$Q = \sqrt{S^2 - P_{ACTIVE}{}^2}$$

Power Factor

The magnitude of the ratio of real power to apparent power; calculated at the end of each cycle:

$$|PF| = \frac{P_{ACTIVE}}{|S|}$$

Lead/Lag

The voltage leading or lagging the current will be communicated as a single bit. This bit also represents the sign of the Apparent Power.

Overcurrent Fault

The overcurrent fault threshold may be set from 50% to 175% of I_P. The user sets the trip point with an 8-bit word. The user also has the ability to set the trip level digital delay. This allows for up to a 32 µs delay on the Fault.

Averaging Over Time

The following values can be averaged over a programmable number of updates:

- IRMS or VRMS
- PACTIVE

The number of averages is controlled by two different registers. There is an accumulator that averages the above values. A 7-bit number, rms_avg_1, is used to determine the number of averages. There is an additional accumulator that will be used to average the output of the first accumulator. There is a 10-bit number, rms_avg_2, that will be used to determine the number of averages for this accumulator. The combination of the two accumulator allows the user to select how long to average for as well as how often the values are updated. The exact time this averages over depends on n (the number of samples per cycle). Averages could be read in Reg 0x26 to 0x29.

Over/Undervoltage Detection

There are two flags that can be used to detect undervoltage and overvoltage. These flags have a programmable voltage trip level. Refer to the Digital I/O section for all possible configurations.

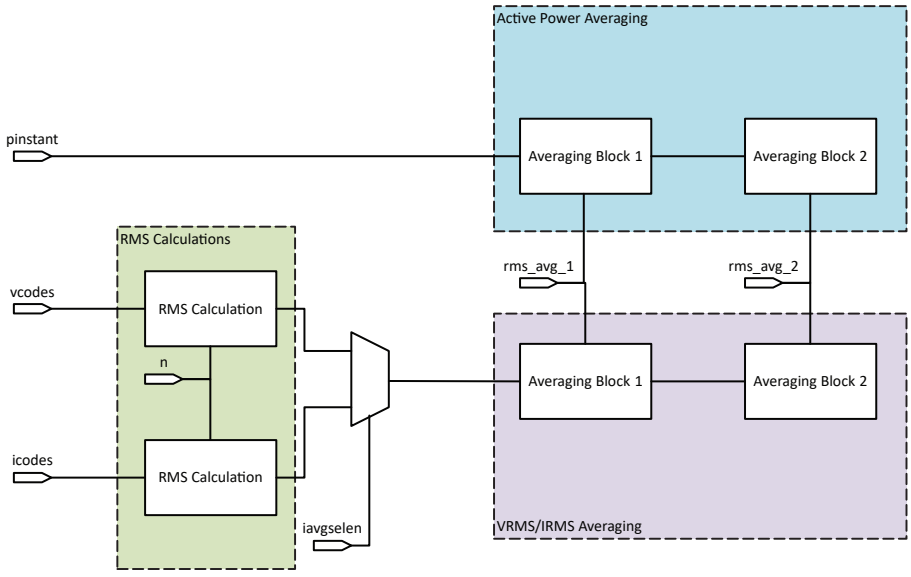

Figure 5: ACS71020 Trim Diagram

DIGITAL COMMUNICATION

Communication Interfaces

The ACS71020 supports communication over 1 MHz I²C and 10 MHz SPI. However, the communication protocol is fixed during factory programming. Refer to the Selection Guide for more information.

SPI

The SPI frame consists of:

- The Master writes on the MOSI line the 7-bit address of the register to be read from or written to.
- The next bit on the MOSI line is the RW indicator. A high state indicates a Read and a low state indicates a Write.
- On the next 32 bits, the MISO line contains the response to the previous command.
- On the MOSI line, if the current command is a write, the 32 bits correspond to the Write data, and in case of a write the data is ignored.

Registers and EEPROM

WRITE ACCESS

The ACS71020 supports factory and customer EEPROM space as well as volatile registers. The customer access code must be sent prior to writing these customer EEPROM spaces. In addition, the device includes a set of free space EEPROM registers that are accessible with or without writing the access code.

READ ACCESS

All EEPROM and volatile registers may be read at any time regardless of the access code.

EEPROM

All configuration EEPROM will be shadowed to volatile memory, and the shadow registers are loaded from EEPROM on power-up. The shadow registers can be written to in order to change the device behavior without having to perform an EEPROM write. Any changes made it shadow memory are volatile and do not persist through a reset event.

WRITING

The Timing Diagram for an EEPROM write is shown in Figure 6 and Figure 7.

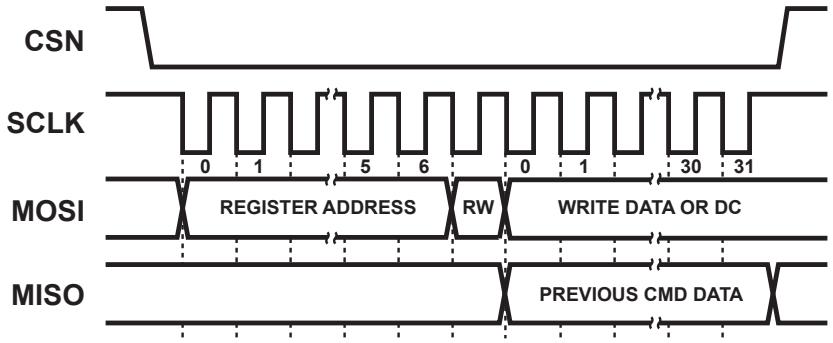

Figure 6: EEPROM Write – SPI Mode

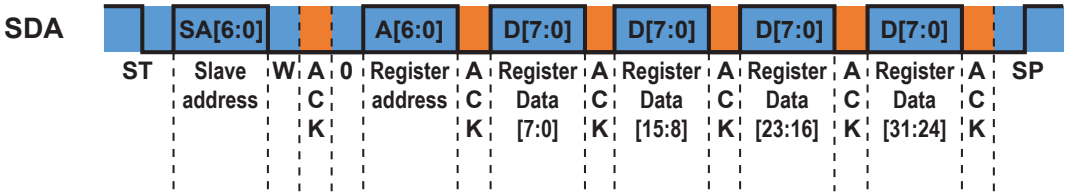

Figure 7: EEPROM Write – I²C Mode
Blue represents data sent by the master and orange is the data sent by the slave.

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READING

The timing diagram for an EEPROM read is shown in Figure 8 and Figure 9.

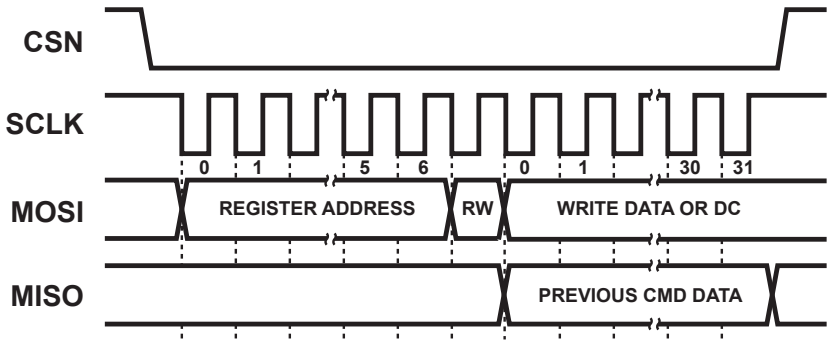


Figure 8: EEPROM Read – SPI Mode
For SPI, the read data will be sent out during the above command.

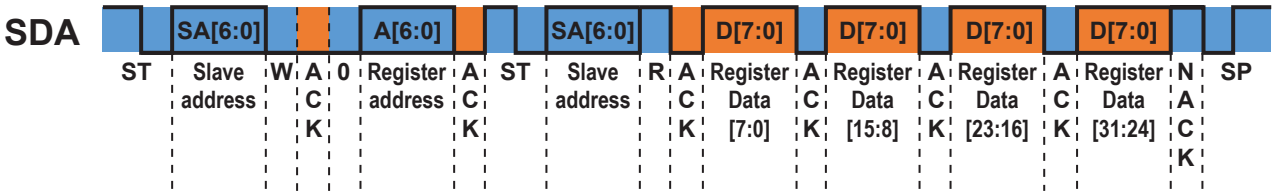


Figure 9: EEPROM Read – I²C Mode
Blue represents data sent by the master and orange is the data sent by the slave.

EEPROM Error Checking and Correction (ECC)

Hamming code methodology is implemented for EEPROM checking and correction (ECC). ECC is enabled after power-up.

The ACS71020 analyzes message data sent by the controller and the ECC bits are added. The first 6 bits sent from the device to the controller are dedicated to ECC. The device always returns 32 bits.

EEPROM ECC Errors

Bits	Name	Description
31:28	–	No meaning
27:26	ECC	00 = No Error 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
25:0	D[25:0]	EEPROM data

MEMORY MAP

EEPROM/Shadow Memory

	Address	Bits																														
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EEPROM	0x0B	ECC										iavgselen	crs_sns			sns_fine									qvo_fine								
	0x0C	ECC						n													rms_avg_2										rms_avg_1		
	0x0D	ECC						squarewave_en	halfcycle_en	fltdly			fault									chan_del_sel				ichan_del_en	pacc_trim					
	0x0E	ECC											delaycnt_sel	undervreg					overvreg							bypass_n_en	vadc_rate_set	vevent_cycs					
	0x0F	ECC												dio_1_sel		dio_0_sel								i2c_dis_slv_addr		i2c_slv_addr							
Shadow	0x1B											iavgselen	crs_sns			sns_fine									qvo_fine								
	0x1C							n													rms_avg_2										rms_avg_1		
	0x1D							squarewave_en	halfcycle_en	fltdly			fault									unused	chan_del_sel		unused	ichan_del_en	pacc_trim					
	0x1E												delaycnt_sel	undervreg					overvreg							bypass_n_en	vadc_rate_set	vevent_cycs					
	0x1F													dio_1_sel		dio_0_sel								i2c_dis_slv_addr		i2c_slv_addr							

Device Trim Flow

The trim process for voltage, current, and power channels are depicted in Figure 10 through Figure 12. Refer to the "Register Details" Section for more information regarding trim fields.

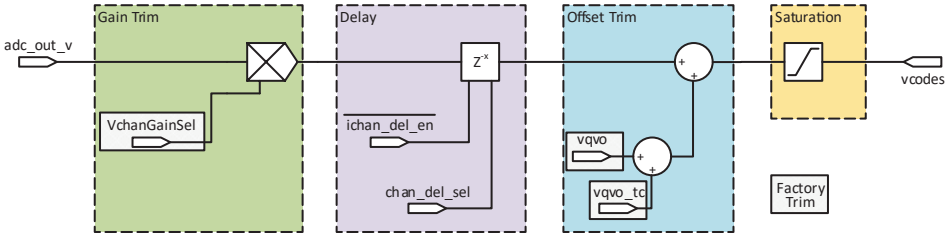


Figure 10: Voltage Channel Trim Flow

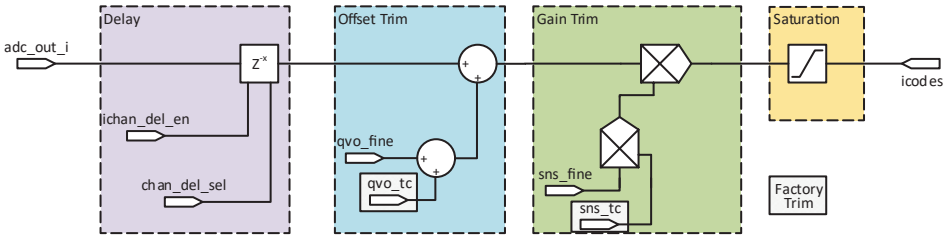


Figure 11: Current Channel Trim Flow

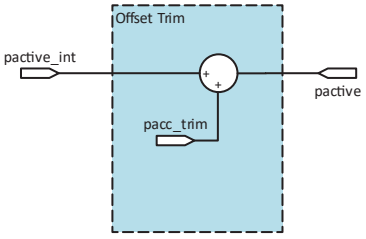


Figure 12: Power Channel Trim Flow

Register Details – EEPROM

Register 0x0B/0x1B

Bits	Name	Description
8:0	qvo_fine	Offset fine trimming on current channel
17:9	sns_fine	Fine gain trimming on the current channel
20:18	crs_sns	Coarse gain setting
21	iavgselen	Current Averaging selection
25:22	unused	Unused
31:26	ecc	Error Code Correction

qvo_fine

Offset adjustment for the current channel. This is a signed 9-bit number and ranges from –256 to 255. With a step size of 64 LSB this equates to an offset trim range of –16384 to 16320 LSB added to the icodes value. The trim is implemented as shown in Figure 11. The offset trim on the current channel should be done before the gain trim. Settings are further described in Table 1.

Table 1: qvo_fine

Range	Value	Units
–256 to 255	–16,384 to 16,320	LSB

sns_fine

Gain adjustment for the current channel. This is a signed 9-bit number so it can range from –256 to 255. This gain adjustment is implemented as a percentage multiplier centered around 1 (i.e. writing a 0 to this field multiplies the gain by 1, leaving the gain unaffected). The range then equates to 0.5 to 1.5 (nominal sensitivity ±50%). The offset trim on the current channel should be done before the gain trim. Settings are further described in Table 2.

Table 2: sns_fine

Range	Value	Units
–256 to 255	0.5 to 1.5	–

crs_sns

Coarse gain adjustment for the current channel. This gain is implemented in the analog domain before the ADC. This is a 3-bit number that allows for 8 gain selections. Changing these settings will likely change the device performance over temperature so the temperature accuracy is only guaranteed in the crs_sns setting that was set in factory. The gain settings map to 1×, 2×, 3×, 3.5×, 4×, 4.5×, 5.5×, and 8×. Settings are further described in Table 3.

Table 3: crs_sns

Range	Value	Units
0	1×	–
1	2×	–
2	3×	–
3	3.5×	–
4	4×	–
5	4.5×	–
6	5.5×	–
7	8×	–

iavgselen

Current Averaging selection. 0 will select vrms for averaging. 1 will select irms for averaging. See Figure 5.

Register 0x0C/0x1C

Bits	Name	Description
6:0	rms_avg_1	Average of the rms voltage or current – stage 1
16:7	rms_avg_2	Average of the rms voltage or current – stage 2
25:17	n	Number of samples per half period.
31:26	ecc	Error Code Correction

rms_avg_1

Number of averages for the first averaging stage (vrmsavgonesec or irmsavgonesec). The value written into this field directly maps to the number of averages ranging from 0 to 127. The channel to be averaged is selected by iavgselen.

Table 4: rms_avg_1

Range	Value	Units
0 to 127	0 to 127	number of averages

rms_avg_2

Number of averages for the second averaging stage (vrmsavgonemin or irmsavgonemin). This stage averages the outputs of the first averaging stage. The value written into this field directly maps to the number of averages ranging from 0 to 1023. The channel to be averaged is selected by iavgselen.

Table 5: rms_avg_2

Range	Value	Units
0 to 1023	0 to 1023	number of averages

n

This is the number of samples to be used in all rms calculations if the bypass_n_en is set. If bypass_n_en is 0 (Reg 0x0E), then this field is unused. The value written into this field directly maps to the number of samples ranging from 0 to 511.

Table 6: n

Range	Value	Units
0 to 511	0 to 511	number of samples

Register 0x0D/0x1D

Bits	Name	Description
6:0	pacc_trim	Trims the active power
7	ichan_del_en	Selects which channel gets delayed
8	unused	unused
11:9	chan_del_sel	Selects the amount of delay for the channel being delayed
12	unused	unused
20:13	fault	Fault level setting
23:21	fltdly	Fault delay count bits
24	halfcycle_en	Outputs pulses at every zero crossing when enabled, and every rising edge when disabled
25	squarewave_en	Selects pulse or square wave output for the zero crossing reporting
31:26	ecc	Error Code Correction

pacc_trim

Offset trim in the active power calculation. Implemented as shown in Figure 12. This is a 7-bit signed number. This then equates to a trim of –384 to 378 LSB to be added to the pactive value.

Table 7: pacc_trim

Range	Value	Units
–64 to 63	–384 to 378	LSB

ichan_del_en

Enables delay for either the voltage or current channel. Setting to 1 enables delay for the current channel. This behavior is depicted in Figure 10 and Figure 11.

Table 8: ichan_del_en

Range	Value	Units
0	0 – voltage channel	LSB
1	1 – current channel	LSB

chan_del_sel

Selection of delays applied to the channel based on ichan_del_en section. The step size of this field is determined by the value of vadc_rate_sel.

Table 9: chan_del_sel

vadc_rate_sel	Range	Value[x]	Units
0	0 to 7	0 to 219	µs
1	0 to 7	0 to 875	µs

fault

Overcurrent fault threshold. This field is an 8-bit number ranging from 0 to 255. This equates to a fault range of 0.5 to 1.75 $\%I_P$. The factory setting of this field is 0.

Table 10: fault

Range	Value	Units
0 to 255	0.5 to 1.75	$\%I_P$

fltdly

Fault delay setting of the amount of delay applied before flagging a fault condition.

Table 11: fltdly

Range	Value	Units
0	0	µs
1	0	µs
2	4.75	µs
3	9.25	µs
4	13.75	µs
5	18.5	µs
6	23.25	µs
7	27.75	µs

halfcycle_en

Setting for the voltage zero-crossing detection. When set to 0, the voltage zero-crossing will be indicated on every rising edge. When set to 1, the voltage zero-crossing will be indicated on both rising and falling edges.

squarewave_en

Setting for the voltage zero-crossing detection. When set to 0, if the voltage zero-crossing is being output on a DIO pin, then the event will be indicated by a pulse on the DIO pin. When set to 1, if the voltage zero-crossing is being output on a DIO pin, then the event will be indicated by a level change on the DIO pin.

Register 0x0E/0x1E

Bits	Name	Description
5:0	vevent_cycs	Sets the number of qualifying cycles needed to flag overvoltage or undervoltage
6	vadc_rate_set	Sample Frequency Selection
7	bypass_n_en	When enabled, the dynamic calibration of n is ignored and instead uses the programmed n value for computations
13:8	overvreg	Level to flag overvoltage
19:14	undervreg	Level to flag undervoltage
20	delaycnt_sel	Selects zero cross output pulse width
25:21	unused	Unused
31:26	ecc	Error Code Correction

vevent_cycs

Setting to determine the number of cycles required to set the OVRMS flag or the UVRMS flag. This is a 6-bit number ranging from 0 to 63. The value in this field directly maps to the number of cycles.

Table 12: vevent_cycs

Range	Value	Units
0 to 63	1 to 64	cycles

vadc_rate_set

Rate selection for the ADC update. Setting this field to a 0 selects a 32 kHz update. Setting this field to a 1 selects an 8 kHz update. The setting of this field to 1 will reduce the number of samples used in each rms calculation, but it will allow for a larger phase delay correction between channels (see chan_del_sel).

Table 13: vadc_rate_set

Range	Value	Units
0	32	kHz
1	8	kHz

bypass_n_en

When enabled, the dynamic calibration of n is ignored and instead uses the programmed n value for computations.

overvreg

Setting for the trip level of the overvoltage rms flag (ovrms). This is a 6-bit number ranging from 0 to 63. This trip level spans the entire range of the vrms register. The flag is set if the rms value is above this threshold for the number of cycles selected in vevent_cycs.

Table 14: overvreg

Range	Value	Units
0 to 63	0 to 32,768	LSB

undervreg

Setting for the trip level of the undervoltage rms flag (uvrms). This is a 6-bit number ranging from 0 to 63. This trip level spans one entire range of the vrms register. The flag is set if the rms value is below this threshold for the number of cycles selected in vevent_cycs.

Table 15: undervreg

Range	Value	Units
0 to 63	0 to 32,768	LSB

delaycnt_sel

Selection bit for the width of pulse for a voltage zero-crossing event. When set to 0, the pulse is 32 µs. When set to 1, the pulse is 256 µs. When the squarewave_en bit is set, this field is ignored.

Table 16: delaycnt_sel

Range	Value	Units
0	32	µs
1	256	µs

Register 0x0F/0x1F

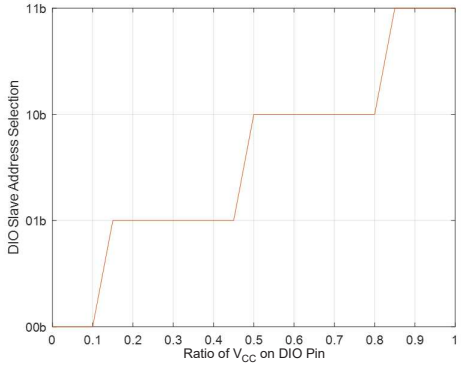
Bits	Name	Description
1:0	unused	Unused
8:2	i2c_slv_addr	I²C slave address selection
9	i2c_dis_slv_addr	Disable I²C slave address selection circuit
15:10	unused	Unused
17:16	dio_0_sel	Digital output 0 multiplexor selection bits
19:18	dio_1_sel	Digital output 1 multiplexor selection bits
25:20	unused	Unused
31:26	ecc	Error Code Correction

i2c_slv_addr

Settings for the I²C slave address. The voltage on the DIO pins will be measured at power up and this will be used to select the slave address that the device will respond to. This can be kept down with a resistor divider off of V_{CC}. Each DIO pin has 4 different regions that affect the slave address chosen as shown in the figure below.

Table 17: i2c_slv_addr

DIO_1		DIO_0		A6	A5	A4	A3	A2	A1	A0	Slave Address (decimal)
0	0	0	0	1	1	0	0	0	0	0	96
0	0	0	1	1	1	0	0	0	0	1	97
0	0	1	0	1	1	0	0	0	1	0	98
0	0	1	1	1	1	0	0	0	1	1	99
0	1	0	0	1	1	0	0	1	0	0	100
0	1	0	1	1	1	0	0	1	0	1	101
0	1	1	0	1	1	0	0	1	1	0	102
0	1	1	1	1	1	0	0	1	1	1	103
1	0	0	0	1	1	0	1	0	0	0	104
1	0	0	1	1	1	0	1	0	0	1	105
1	0	1	0	1	1	0	1	0	1	0	106
1	0	1	1	1	1	0	1	0	1	1	107
1	1	0	0	1	1	0	1	1	0	0	108
1	1	0	1	1	1	0	1	1	0	1	109
1	1	1	0	1	1	0	1	1	1	0	110
1	1	1	1	EE	EE	EE	EE	EE	EE	EE	EEPROM value



i2c_dis_slv_addr

This bit is used to disable the analog portion of the I²C slave address that is done on power on. When this bit is set, the i2c_slv_addr will directly set the slave address.

dio_0_sel

Selection bits for which flags are output on the DIO0 pin. Only used when the device is in I²C programming mode.

Table 18: dio_0_sel

Value	Selection
0	VZC: Voltage zero crossing
1	OVRMS: The VRMS overvoltage flag
2	UVRMS: The VRMS undervoltage flag
3	The OR of OVRMS and UVRMS (if either flag is triggered, the DIO_0 pin will be asserted)

dio_1_sel

Selection bits for which flags are output on the DIO1 pin. Only used when the device is in I²C programming mode.

Table 19: dio_1_sel

Value	Selection
0	OCF: Overcurrent fault
1	UVRMS: The VRMS undervoltage flag
2	OVRMS: The VRMS overvoltage flag
3	The OR of OVRMS, UVRMS, and OCF (if any of the three flags are triggered, the DIO_0 pin will be asserted).

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