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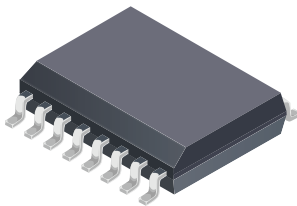
## 120 kHz Bandwidth, High-Voltage Isolation Current Sensor with Integrated Overcurrent Detection

### Features and Benefits

- Industry-leading noise performance with greatly improved bandwidth through proprietary amplifier and filter design techniques
- Small footprint package suitable for space-constrained applications
- 1 mΩ primary conductor resistance for low power loss
- High isolation voltage, suitable for line-powered applications
- User-adjustable Overcurrent Fault level
- Overcurrent Fault signal typically responds to an overcurrent condition in  $< 2 \mu\text{s}$
- Integrated shield virtually eliminates capacitive coupling from current conductor to die due to high  $dV/dt$  voltage transients
- Filter pin capacitor improves resolution in low bandwidth applications
- 3 to 5.5 V single supply operation
- Factory-trimmed sensitivity and quiescent output voltage
- Chopper stabilization results in extremely stable quiescent output voltage
- Ratiometric output from supply voltage



### Package: 16-Pin SOIC Hall-Effect IC Package (suffix LA)



Not to scale

### Description

The Allegro™ ACS710 current sensor provides economical and precise means for current sensing applications in industrial, commercial, and communications systems. The device is offered in a small footprint surface-mount package that allows easy implementation in customer applications.

The ACS710 consists of a precision linear Hall sensor integrated circuit with a copper conduction path located near the surface of the silicon die. Applied current flows through the copper conduction path, and the analog output voltage from the Hall sensor linearly tracks the magnetic field generated by the applied current. The accuracy of the ACS710 is maximized with this patented packaging configuration because the Hall element is situated in extremely close proximity to the current to be measured.

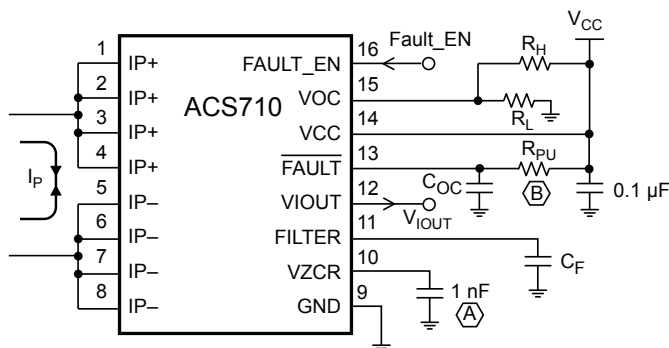
High-level immunity to current conductor  $dV/dt$  and stray electric fields, offered by Allegro proprietary integrated shield technology, results in low ripple on the output and low offset drift in high-side, high-voltage applications.

The voltage on the Overcurrent Input (VOC pin) allows customers to define an overcurrent fault threshold for the device. When the current flowing through the copper conduction path (between the IP+ and IP- pins) exceeds this threshold, the open drain Overcurrent Fault pin will transition to a logic low state. Factory programming of the linear Hall sensor inside of the ACS710 results in exceptional accuracy in both analog and digital output signals.

The internal resistance of the copper path used for current sensing is typically 1 mΩ, for low power loss. Also, the current conduction path is electrically isolated from the low-voltage

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### Typical Application Circuit



$R_H, R_L$	Sets resistor divider reference for $V_{OC}$
$C_F$	Noise and bandwidth limiting filter capacitor
$C_{OC}$	Fault delay setting capacitor, 22 nF maximum
(A)	Use of capacitor required
(B)	Use of resistor optional, 330 kΩ recommended. If used, resistor must be connected between $\overline{FAULT}$ pin and $V_{CC}$ .



### Description (continued)

sensor inputs and outputs. This allows the ACS710 family of sensors to be used in applications requiring electrical isolation, without the use of opto-isolators or other costly isolation techniques.

The ACS710 is provided in a small, surface-mount SOIC16 package. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature

Pb-based solder balls, currently exempt from RoHS. The device is fully calibrated prior to shipment from the factory.

Applications include:

- Motor control and protection
- Load management and overcurrent detection
- Power conversion and battery monitoring / UPS systems

### Selection Guide

Part Number	$I_P$ (A)	Sens (typ) at $V_{CC} = 5\text{ V}$ (mV/A)	Latched Fault	$T_A$ (°C)	Packing <sup>1</sup>
ACS710KLATR-6BB-T <sup>2,3</sup>	±6	151	Yes	-40 to 125	Tape and Reel, 1000 pieces per reel
ACS710KLATR-10BB-T <sup>2</sup>	±10	85			
ACS710KLATR-12CB-T <sup>2</sup>	±12.5	56			
ACS710KLATR-25CB-T <sup>2</sup>	±25	28			
ACS710KLATR-6BB-NL-T <sup>2,3</sup>	±6	151	No	-40 to 125	Tape and Reel, 1000 pieces per reel
ACS710KLATR-10BB-NL-T <sup>2</sup>	±10	85			
ACS710KLATR-12CB-NL-T <sup>2</sup>	±12.5	56			
ACS710KLATR-25CB-NL-T <sup>2</sup>	±25	28			

<sup>1</sup> Contact Allegro for packing options.

<sup>2</sup> Variant not intended for automotive applications.

<sup>3</sup> The formerly offered  $V_{CC} = 3.3\text{ V}$  version of the  $I_P = \pm 6\text{ A}$  variant (formerly the ACS710KLATR-6BB-T) is now offered as the ACS716KLATR-6BB-T. For additional information, please refer to the ACS716 datasheet.

### Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	$V_{CC}$		8	V
Filter Pin	$V_{FILTER}$		8	V
Analog Output Pin	$V_{IOUT}$		32	V
Overcurrent Input Pin	$V_{OC}$		8	V
Overcurrent $\overline{FAULT}$ Pin	$V_{\overline{FAULT}}$		8	V
Fault Enable (FAULT_EN) Pin	$V_{FAULTEN}$		8	V
Voltage Reference Output Pin	$V_{ZCR}$		8	V
DC Reverse Voltage: VCC, FILTER, VIOUT, VOC, $\overline{FAULT}$ , FAULT_EN, and VZCR Pins	$V_{Rdcx}$		-0.5	V
Excess to Supply Voltage: FILTER, VIOUT, VOC, $\overline{FAULT}$ , FAULT_EN, and VZCR Pins	$V_{EX}$	Voltage by which pin voltage can exceed the VCC pin voltage	0.3	V
Output Current Source	$I_{IOUT(SOURCE)}$		3	mA
Output Current Sink	$I_{IOUT(SINK)}$		1	mA
Operating Ambient Temperature	$T_A$	Range K	-40 to 125	°C
Junction Temperature	$T_J(max)$		165	°C
Storage Temperature	$T_{stg}$		-65 to 170	°C

### Isolation Characteristics

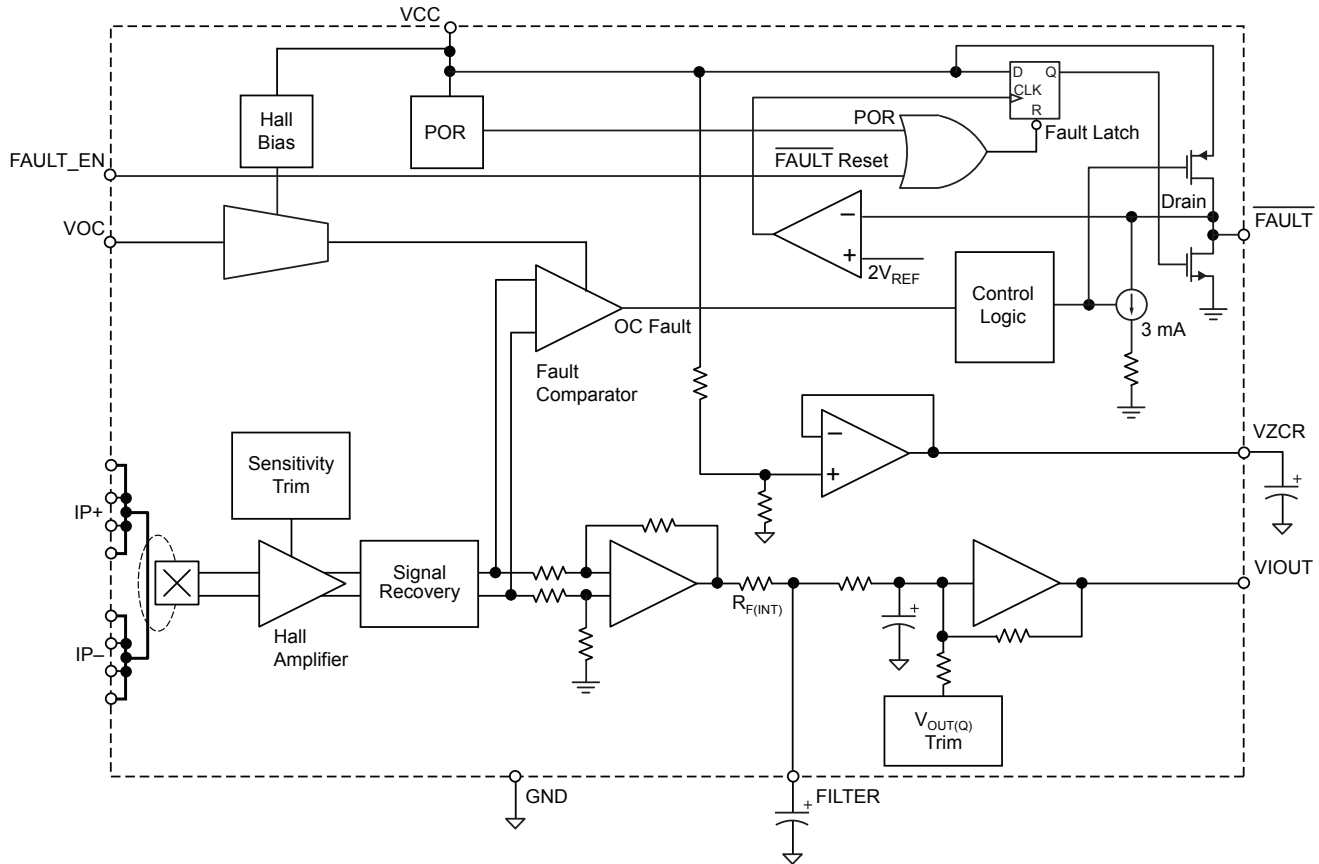
Characteristic	Symbol	Notes	Rating	Unit
Dielectric Strength Test Voltage*	$V_{ISO}$	Agency type-tested for 60 seconds per IEC/UL 60950-1 (2nd Edition).	3600	$V_{RMS}$
		Agency type-tested for 60 seconds per UL 1577.	3000	$V_{RMS}$
Working Voltage for Basic Isolation	$V_{WVBI}$	Maximum approved working voltage for basic (single) isolation according to IEC/UL 60950-1 (2nd Edition).	870	$V_{PK}$ or VDC
			616	$V_{RMS}$
Clearance	$D_{CL}$	Minimum distance through air from IP leads to signal leads.	7.5	mm
Creepage	$D_{CR}$	Minimum distance along package body from IP leads to signal leads.	7.5	mm

\*Production tested for 1 second at 3600  $V_{RMS}$  in accordance with both UL 1577 and IEC/UL 60950-1 (edition 2).

### Thermal Characteristics

Characteristic	Symbol	Test Conditions	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	When mounted on Allegro demo board with 1332 mm <sup>2</sup> (654 mm <sup>2</sup> on component side and 678 mm <sup>2</sup> on opposite side) of 2 oz. copper connected to the primary leadframe and with thermal vias connecting the copper layers. Performance is based on current flowing through the primary leadframe and includes the power consumed by the PCB.	17	°C/W

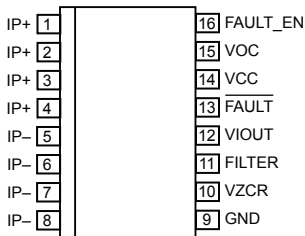
### Functional Block Diagram Latching Version



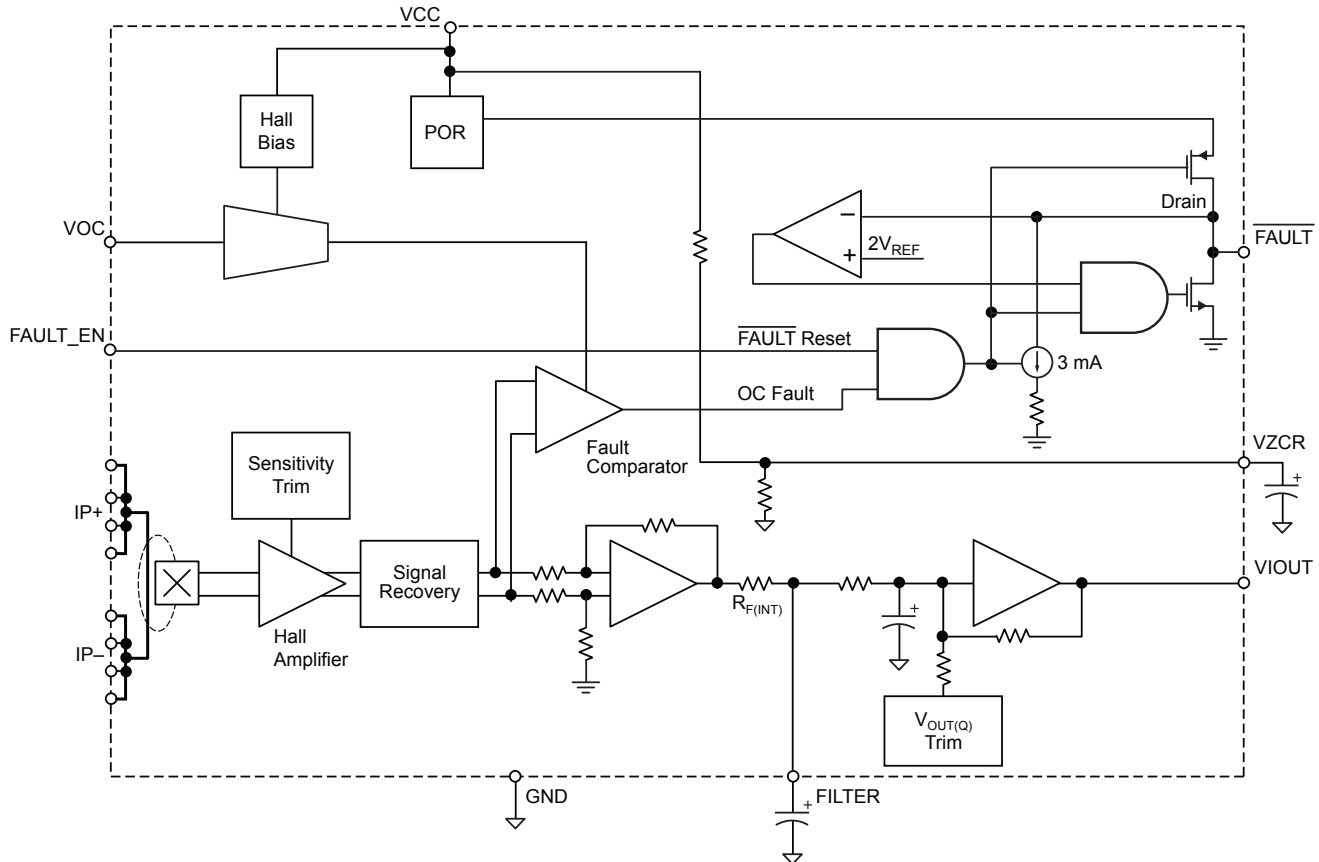
### Terminal List Table, Latching Version

Number	Name	Description
1,2,3,4	IP+	Sensed current copper conduction path pins. Terminals for current being sensed; fused internally, loop to IP- pins; unidirectional or bidirectional current flow.
5,6,7,8	IP-	Sensed current copper conduction path pins. Terminals for current being sensed; fused internally, loop to IP+ pins; unidirectional or bidirectional current flow.
9	GND	Device ground connection.
10	VZCR	Voltage Reference Output pin. Zero current (0 A) reference; output voltage on this pin scales with $V_{CC}$ . (Not a highly accurate reference.)
11	FILTER	Filter pin. Terminal for an external capacitor connected from this pin to GND to set the device bandwidth.
12	VIOUT	Analog Output pin. Output voltage on this pin is proportional to current flowing through the loop between the IP+ pins and IP- pins.
13	$\overline{\text{FAULT}}$	Overcurrent Fault pin. When current flowing between IP+ pins and IP- pins exceeds the overcurrent fault threshold, this pin transitions to a logic low state.
14	VCC	Supply voltage.
15	VOC	Overcurrent Input pin. Analog input voltage on this pin sets the overcurrent fault threshold.
16	FAULT_EN	Enables overcurrent faulting when high. Resets $\overline{\text{FAULT}}$ when low.

### Pin-Out Diagram



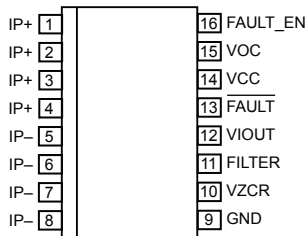
### Functional Block Diagram Non-Latching Version



**Terminal List Table, Non-Latching Version**

Number	Name	Description
1,2,3,4	IP+	Sensed current copper conduction path pins. Terminals for current being sensed; fused internally, loop to IP- pins; unidirectional or bidirectional current flow.
5,6,7,8	IP-	Sensed current copper conduction path pins. Terminals for current being sensed; fused internally, loop to IP+ pins; unidirectional or bidirectional current flow.
9	GND	Device ground connection.
10	VZCR	Voltage Reference Output pin. Zero current (0 A) reference; output voltage on this pin scales with V <sub>CC</sub> . (Not a highly accurate reference.)
11	FILTER	Filter pin. Terminal for an external capacitor connected from this pin to GND to set the device bandwidth.
12	VIOOUT	Analog Output pin. Output voltage on this pin is proportional to current flowing through the loop between the IP+ pins and IP- pins.
13	$\overline{\text{FAULT}}$	Overcurrent Fault pin. When current flowing between IP+ pins and IP- pins exceeds the overcurrent fault threshold, this pin transitions to a logic low state.
14	VCC	Supply voltage.
15	VOC	Overcurrent Input pin. Analog input voltage on this pin sets the overcurrent fault threshold.
16	FAULT_EN	Enables overcurrent faulting when high.

### Pin-Out Diagram



**COMMON OPERATING CHARACTERISTICS:** Valid at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
<b>ELECTRICAL CHARACTERISTICS</b>						
Supply Voltage <sup>1</sup>	$V_{CC}$		3	–	5.5	V
Nominal Supply Voltage	$V_{CCN}$		–	5	–	V
Supply Current	$I_{CC}$	V <sub>IOUT</sub> open, $\overline{\text{FAULT}}$ pin high	–	11	14.5	mA
Output Capacitance Load	$C_{LOAD}$	V <sub>IOUT</sub> pin to GND	–	–	10	nF
Output Resistive Load	$R_{LOAD}$	V <sub>IOUT</sub> pin to GND	10	–	–	k $\Omega$
Magnetic Coupling from Device Conductor to Hall Element	$MC_{HALL}$	Current flowing from IP+ to IP– pins	–	9.5	–	G/A
Internal Filter Resistance <sup>2</sup>	$R_{F(INT)}$		–	1.7	–	k $\Omega$
Primary Conductor Resistance	$R_{PRIMARY}$	$T_A = 25^\circ\text{C}$	–	1	–	m $\Omega$
<b>ANALOG OUTPUT SIGNAL CHARACTERISTICS</b>						
Full Range Linearity <sup>3</sup>	$E_{LIN}$	$I_P = \pm I_{P0A}$	–0.75	$\pm 0.25$	0.75	%
Symmetry <sup>4</sup>	$E_{SYM}$	$I_P = \pm I_{P0A}$	99.1	100	100.9	%
Bidirectional Quiescent Output	$V_{OUT(QBI)}$	$I_P = 0\text{ A}$ , $T_A = 25^\circ\text{C}$	–	$V_{CC} \times 0.5$	–	V
<b>TIMING PERFORMANCE CHARACTERISTICS</b>						
V <sub>IOUT</sub> Signal Rise Time	$t_r$	$T_A = 25^\circ\text{C}$ , Swing $I_P$ from 0 A to $I_{P0A}$ , no capacitor on FILTER pin, 100 pF from V <sub>IOUT</sub> to GND	–	3	–	$\mu\text{s}$
V <sub>IOUT</sub> Signal Propagation Time	$t_{PROP}$	$T_A = 25^\circ\text{C}$ , no capacitor on FILTER pin, 100 pF from V <sub>IOUT</sub> to GND	–	1	–	$\mu\text{s}$
V <sub>IOUT</sub> Signal Response Time	$t_{RESPONSE}$	$T_A = 25^\circ\text{C}$ , Swing $I_P$ from 0 A to $I_{P0A}$ , no capacitor on FILTER pin, 100 pF from V <sub>IOUT</sub> to GND	–	4	–	$\mu\text{s}$
V <sub>IOUT</sub> Large Signal Bandwidth	$f_{3dB}$	–3 dB, Apply $I_P$ such that $V_{IOUT} = 1\text{ V}_{pk-pk}$ , no capacitor on FILTER pin, 100 pF from V <sub>IOUT</sub> to GND	–	120	–	kHz
Power-On Time	$t_{PO}$	Output reaches 90% of steady-state level, no capacitor on FILTER pin, $T_A = 25^\circ\text{C}$	–	35	–	$\mu\text{s}$
<b>OVERCURRENT CHARACTERISTICS</b>						
Setting Voltage for Overcurrent Switchpoint <sup>5</sup>	$V_{OC}$		$V_{CC} \times 0.25$	–	$V_{CC} \times 0.4$	V
Signal Noise at Overcurrent Comparator Input	$I_{NCOMP}$		–	$\pm 1$	–	A
Overcurrent Fault Switchpoint Error <sup>6,7</sup>	$E_{OC}$	Switchpoint in $V_{OC}$ safe operating area; assumes $I_{NCOMP} = 0\text{ A}$	–	$\pm 5$	–	%
Overcurrent $\overline{\text{FAULT}}$ Pin Output Voltage	$V_{\overline{\text{FAULT}}}$	1 mA sink current at $\overline{\text{FAULT}}$ pin	–	–	0.4	V
Fault Enable (FAULT_EN Pin) Input Low Voltage Threshold	$V_{IL}$		–	–	$0.1 \times V_{CC}$	V
Fault Enable (FAULT_EN Pin) Input High Voltage Threshold	$V_{IH}$		$0.8 \times V_{CC}$	–	–	V
Fault Enable (FAULT_EN Pin) Input Resistance	$R_{FEI}$		–	1	–	M $\Omega$

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**COMMON OPERATING CHARACTERISTICS (continued):** Valid at  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{CC} = 5\text{ V}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
<b>OVERCURRENT CHARACTERISTICS (continued)</b>						
Fault Enable (FAULT_EN Pin) Delay <sup>8</sup>	$t_{FED}$	Set FAULT_EN to low, $V_{OC} = 0.25 \times V_{CC}$ , $C_{OC} = 0\text{ F}$ ; then run a DC $I_P$ exceeding the corresponding overcurrent threshold; then reset FAULT_EN from low to high and measure the delay from the rising edge of FAULT_EN to the falling edge of FAULT	–	15	–	$\mu\text{s}$
Fault Enable (FAULT_EN Pin) Delay (Non-Latching versions) <sup>9</sup>	$t_{FED(NL)}$	Set FAULT_EN to low, $V_{OC} = 0.25 \times V_{CC}$ , $C_{OC} = 0\text{ F}$ ; then run a DC $I_P$ exceeding the corresponding overcurrent threshold; then reset FAULT_EN from low to high and measure the delay from the rising edge of FAULT_EN to the falling edge of FAULT	–	150	–	ns
Overcurrent Fault Response Time	$t_{OC}$	FAULT_EN set to high for a minimum of 20 $\mu\text{s}$ before the overcurrent event; switchpoint set at $V_{OC} = 0.25 \times V_{CC}$ ; delay from $I_P$ exceeding overcurrent fault threshold to $V_{FAULT} < 0.4\text{ V}$ , without external $C_{OC}$ capacitor	–	1.9	–	$\mu\text{s}$
Undercurrent Fault Response Time (Non-Latching versions)	$t_{UC}$	FAULT_EN set to high for a minimum of 20 $\mu\text{s}$ before the undercurrent event; switchpoint set at $V_{OC} = 0.25 \times V_{CC}$ ; delay from $I_P$ falling below the overcurrent fault threshold to $V_{FAULT} > 0.8 \times V_{CC}$ , without external $C_{OC}$ capacitor, $R_{PU} = 330\text{ k}\Omega$	–	3	–	$\mu\text{s}$
Overcurrent Fault Reset Delay	$t_{OCR}$	Time from $V_{FAULTEN} < V_{IL}$ to $V_{FAULT} > 0.8 \times V_{CC}$ , $R_{PU} = 330\text{ k}\Omega$	–	500	–	ns
Overcurrent Fault Reset Hold Time	$t_{OCH}$	Time from $V_{FAULTEN} < V_{IL}$ to rising edge of $V_{FAULT}$	–	250	–	ns
Overcurrent Input Pin Resistance	$R_{OC}$	$T_A = 25^{\circ}\text{C}$ , VOC pin to GND	2	–	–	M $\Omega$
<b>VOLTAGE REFERENCE CHARACTERISTICS</b>						
Voltage Reference Output	$V_{ZCR}$	$T_A = 25^{\circ}\text{C}$ (Not a highly accurate reference)	$0.48 \times V_{CC}$	$0.5 \times V_{CC}$	$0.51 \times V_{CC}$	V
Voltage Reference Output Load Current	$I_{ZCR}$	Source current	3	–	–	mA
		Sink current	50	–	–	$\mu\text{A}$
Voltage Reference Output Drift	$\Delta V_{ZCR}$		–	$\pm 10$	–	mV

<sup>1</sup> Devices are programmed for maximum accuracy at  $V_{CC} = 5\text{ V}$ . The device contains ratiometry circuits that accurately alter the 0 A Output Voltage and Sensitivity level of the device in proportion to the applied  $V_{CC}$  level. However, as a result of minor nonlinearities in the ratiometry circuit, additional output error will result when  $V_{CC}$  varies from the  $V_{CC}$  level at which the device was programmed. Customers that plan to operate the device at a  $V_{CC}$  level other than the  $V_{CC}$  level at which the device was programmed should contact their local Allegro sales representative regarding expected device accuracy levels under these bias conditions.

<sup>2</sup>  $R_{F(INT)}$  forms an RC circuit via the FILTER pin.

<sup>3</sup> This parameter can drift by as much as 0.8% over the lifetime of this product.

<sup>4</sup> This parameter can drift by as much as 1% over the lifetime of this product.

<sup>5</sup> See page 8 on how to set overcurrent fault switchpoint.

<sup>6</sup> Switchpoint can be lower at the expense of switchpoint accuracy.

<sup>7</sup> This error specification does not include the effect of noise. See the  $I_{NCOMP}$  specification in order to factor in the additional influence of noise on the fault switchpoint.

<sup>8</sup> Fault Enable Delay is designed to avoid false tripping of an Overcurrent (OC) fault at power-up. A 15  $\mu\text{s}$  (typical) delay will always be needed, every time FAULT\_EN is raised from low to high, before the device is ready for responding to any overcurrent event.

<sup>9</sup> During power-up, this delay is 15  $\mu\text{s}$  in order to avoid false tripping of an Overcurrent (OC) fault.



**PERFORMANCE CHARACTERISTICS: T<sub>A</sub> Range K, valid at T<sub>A</sub> = -40°C to 125°C, V<sub>CC</sub> = 5 V, unless otherwise specified**

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
<b>X6BB CHARACTERISTICS</b>						
Optimized Accuracy Range <sup>1</sup>	I <sub>POA</sub>		-7.5	-	7.5	A
Linear Sensing Range	I <sub>R</sub>		-14	-	14	A
Noise <sup>2</sup>	V <sub>NOISE(rms)</sub>	T <sub>A</sub> = 25°C, Sens = 100 mV/A, C <sub>f</sub> = 0, C <sub>LOAD</sub> = 4.7 nF, R <sub>LOAD</sub> open	-	4.05	-	mV
Sensitivity <sup>3</sup>	Sens	I <sub>P</sub> = 6.5 A, T <sub>A</sub> = 25°C	-	151	-	mV/A
		I <sub>P</sub> = 6.5 A, T <sub>A</sub> = 25°C to 125°C	-	151	-	mV/A
		I <sub>P</sub> = 6.5 A, T <sub>A</sub> = -40°C to 25°C	-	152	-	mV/A
Electrical Offset Voltage Variation Relative to V <sub>OUT(QBI)</sub> <sup>4</sup>	V <sub>OE</sub>	I <sub>P</sub> = 0 A, T <sub>A</sub> = 25°C	-	±10	-	mV
		I <sub>P</sub> = 0 A, T <sub>A</sub> = 25°C to 125°C	-	±11	-	mV
		I <sub>P</sub> = 0 A, T <sub>A</sub> = -40°C to 25°C	-	±40	-	mV
Total Output Error <sup>5</sup>	E <sub>TOT</sub>	Over full scale of I <sub>POA</sub> , I <sub>P</sub> applied for 5 ms, T <sub>A</sub> = 25°C to 125°C	-	±1.6	-	%
		Over full scale of I <sub>POA</sub> , I <sub>P</sub> applied for 5 ms, T <sub>A</sub> = -40°C to 25°C	-	±5.6	-	%
<b>X10BB CHARACTERISTICS</b>						
Optimized Accuracy Range <sup>1</sup>	I <sub>POA</sub>		-10	-	10	A
Linear Sensing Range	I <sub>R</sub>		-24	-	24	A
Noise <sup>2</sup>	V <sub>NOISE(rms)</sub>	T <sub>A</sub> = 25°C, Sens = 85 mV/A, C <sub>f</sub> = 0, C <sub>LOAD</sub> = 4.7 nF, R <sub>LOAD</sub> open	-	2.3	-	mV
Sensitivity <sup>3</sup>	Sens	I <sub>P</sub> = 10 A, T <sub>A</sub> = 25°C	-	85	-	mV/A
		I <sub>P</sub> = 10 A, T <sub>A</sub> = 25°C to 125°C	-	85	-	mV/A
		I <sub>P</sub> = 10 A, T <sub>A</sub> = -40°C to 25°C	-	85	-	mV/A
Electrical Offset Voltage Variation Relative to V <sub>OUT(QBI)</sub> <sup>4</sup>	V <sub>OE</sub>	I <sub>P</sub> = 0 A, T <sub>A</sub> = 25°C	-	±5	-	mV
		I <sub>P</sub> = 0 A, T <sub>A</sub> = 25°C to 125°C	-	±12	-	mV
		I <sub>P</sub> = 0 A, T <sub>A</sub> = -40°C to 25°C	-	±22	-	mV
Total Output Error <sup>5</sup>	E <sub>TOT</sub>	Over full scale of I <sub>POA</sub> , I <sub>P</sub> applied for 5 ms, T <sub>A</sub> = 25°C to 125°C	-	±1.8	-	%
		Over full scale of I <sub>POA</sub> , I <sub>P</sub> applied for 5 ms, T <sub>A</sub> = -40°C to 25°C	-	±5	-	%
<b>X12CB CHARACTERISTICS</b>						
Optimized Accuracy Range <sup>1</sup>	I <sub>POA</sub>		-12.5	-	12.5	A
Linear Sensing Range	I <sub>R</sub>		-37.5	-	37.5	A
Noise <sup>2</sup>	V <sub>NOISE(rms)</sub>	T <sub>A</sub> = 25°C, Sens = 56 mV/A, C <sub>f</sub> = 0, C <sub>LOAD</sub> = 4.7 nF, R <sub>LOAD</sub> open	-	1.50	-	mV
Sensitivity <sup>3</sup>	Sens	I <sub>P</sub> = 12.5 A, T <sub>A</sub> = 25°C	-	56	-	mV/A
		I <sub>P</sub> = 12.5 A, T <sub>A</sub> = 25°C to 125°C	-	56	-	mV/A
		I <sub>P</sub> = 12.5 A, T <sub>A</sub> = -40°C to 25°C	-	57	-	mV/A
Electrical Offset Voltage Variation Relative to V <sub>OUT(QBI)</sub> <sup>4</sup>	V <sub>OE</sub>	I <sub>P</sub> = 0 A, T <sub>A</sub> = 25°C	-	±4	-	mV
		I <sub>P</sub> = 0 A, T <sub>A</sub> = 25°C to 125°C	-	±14	-	mV
		I <sub>P</sub> = 0 A, T <sub>A</sub> = -40°C to 25°C	-	±23	-	mV
Total Output Error <sup>5</sup>	E <sub>TOT</sub>	Over full scale of I <sub>POA</sub> , I <sub>P</sub> applied for 5 ms, T <sub>A</sub> = 25°C to 125°C	-	±2.2	-	%
		Over full scale of I <sub>POA</sub> , I <sub>P</sub> applied for 5 ms, T <sub>A</sub> = -40°C to 25°C	-	±3.9	-	%

Continued on the next page...

**PERFORMANCE CHARACTERISTICS (continued):  $T_A$  Range K, valid at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ , unless otherwise specified**

<b>X25CB CHARACTERISTICS</b>						
Optimized Accuracy Range <sup>1</sup>	$I_{POA}$		-25	-	25	A
Linear Sensing Range	$I_R$		-75	-	75	A
Noise <sup>2</sup>	$V_{NOISE(rms)}$	$T_A = 25^\circ\text{C}$ , Sens = 28 mV/A, $C_f = 0$ , $C_{LOAD} = 4.7\text{ nF}$ , $R_{LOAD}$ open	-	1	-	mV
Sensitivity <sup>3</sup>	Sens	$I_P = 25\text{ A}$ , $T_A = 25^\circ\text{C}$	-	28	-	mV/A
		$I_P = 25\text{ A}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	-	27.9	-	mV/A
		$I_P = 25\text{ A}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	-	28.5	-	mV/A
Electrical Offset Voltage Variation Relative to $V_{OUT(QBI)}$ <sup>4</sup>	$V_{OE}$	$I_P = 0\text{ A}$ , $T_A = 25^\circ\text{C}$	-	$\pm 3$	-	mV
		$I_P = 0\text{ A}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	-	$\pm 12$	-	mV
		$I_P = 0\text{ A}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	-	$\pm 18$	-	mV
Total Output Error <sup>5</sup>	$E_{TOT}$	Over full scale of $I_{POA}$ , $I_P$ applied for 5 ms, $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	-	$\pm 2.9$	-	%
		Over full scale of $I_{POA}$ , $I_P$ applied for 5 ms, $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	-	$\pm 5.2$	-	%

<sup>1</sup> Although the device is accurate over the entire linear range, the device is programmed for maximum accuracy over the range defined by  $I_{POA}$ . The reason for this is that in many applications, such as motor control, the start-up current of the motor is approximately three times higher than the running current.

<sup>2</sup>  $V_{pk-pk}$  noise (6 sigma noise) is equal to  $6 \times V_{NOISE(rms)}$ . Lower noise levels than this can be achieved by using  $C_f$  for applications requiring narrower bandwidth. See Characteristic Performance page for graphs of noise versus  $C_f$  and bandwidth versus  $C_f$ .

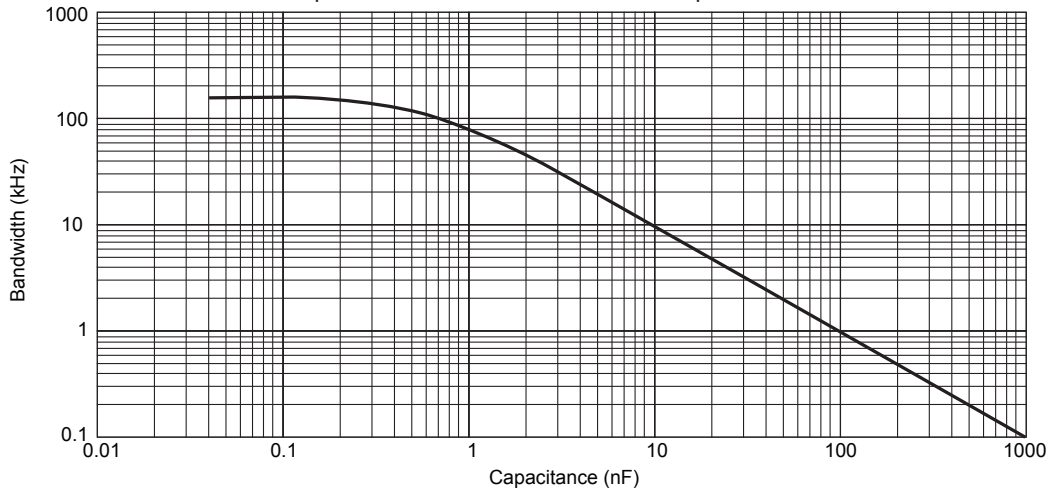
<sup>3</sup> This parameter can drift by as much as 2.4% over the lifetime of this product.

<sup>4</sup> This parameter can drift by as much as 13 mV over the lifetime of this product.

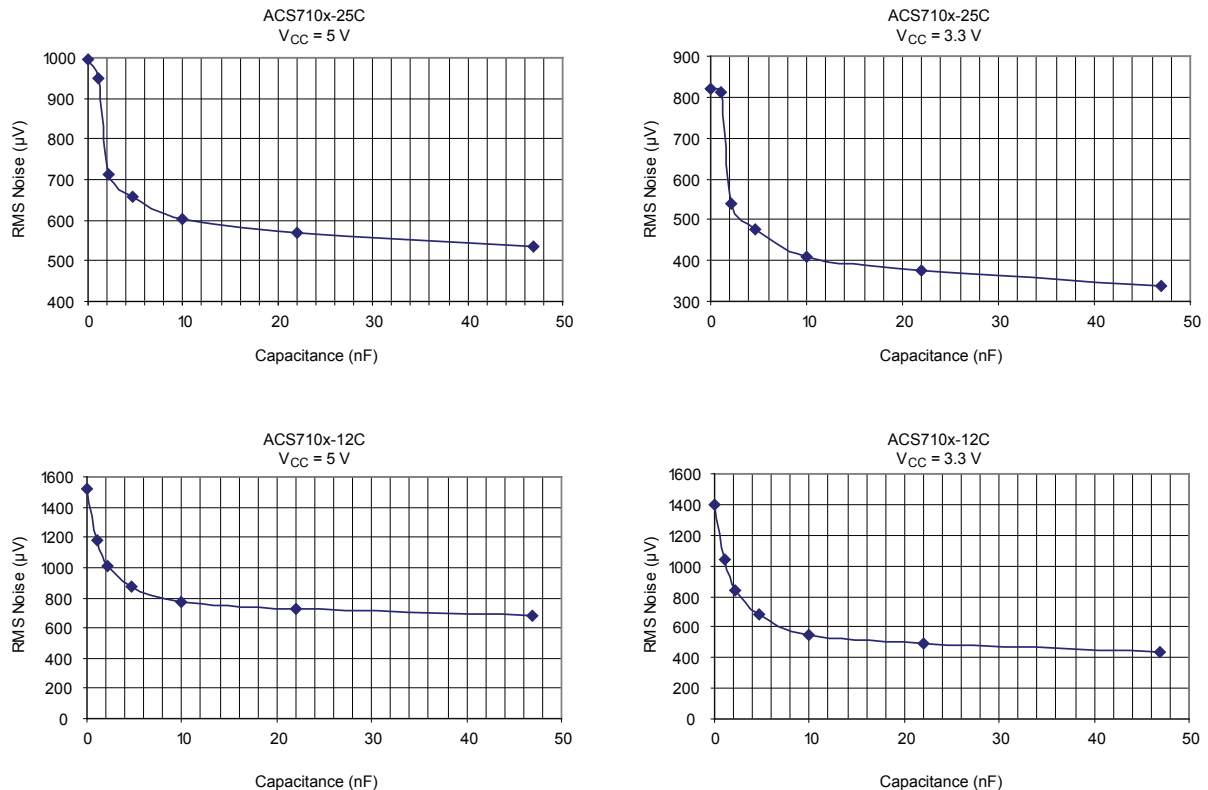
<sup>5</sup> This parameter can drift by as much as 2.5% over the lifetime of this product.

### Characteristic Performance

ACS710 Bandwidth versus External Capacitor Value,  $C_F$   
Capacitor connected between FILTER pin and GND



ACS710 Noise versus External Capacitor Value,  $C_F$   
Capacitor connected between FILTER pin and GND

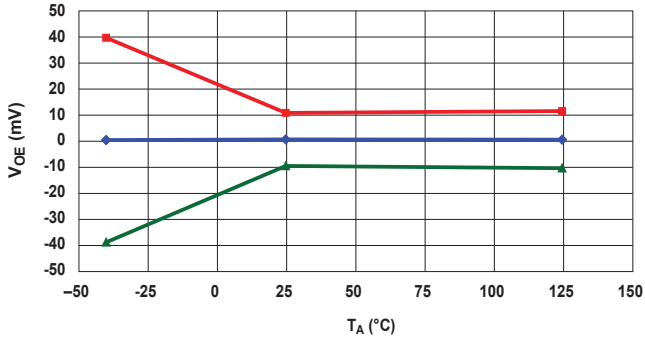


### Characteristic Performance Data

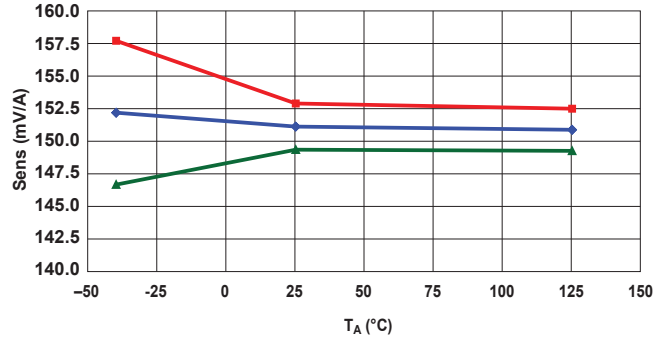
Data taken using the ACS710-6BB

### Accuracy Data

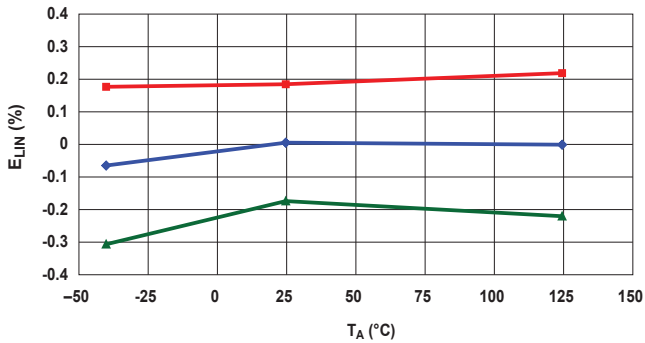
Electrical Offset Voltage versus Ambient Temperature



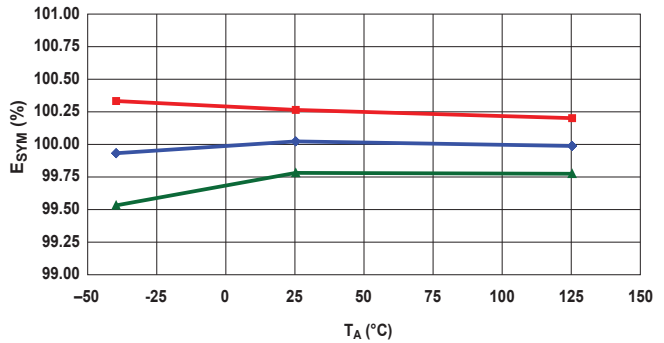
Sensitivity versus Ambient Temperature



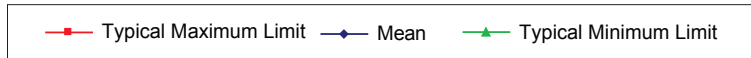
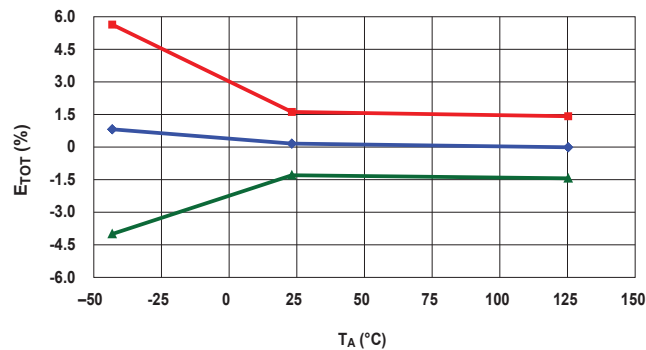
Nonlinearity versus Ambient Temperature



Symmetry versus Ambient Temperature



Total Output Error versus Ambient Temperature



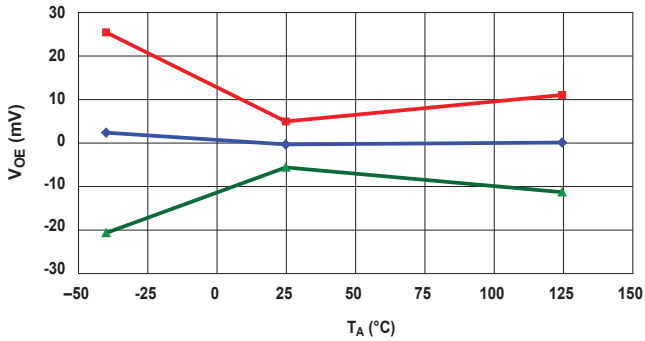


## Characteristic Performance Data

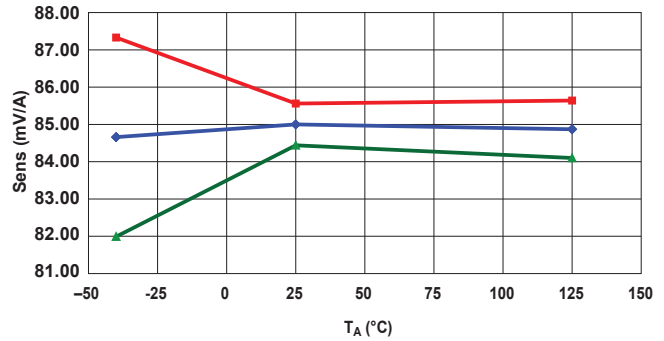
Data taken using the ACS710-10BB

### Accuracy Data

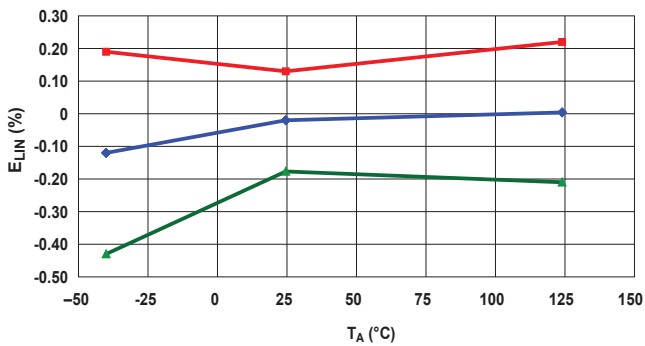
Electrical Offset Voltage versus Ambient Temperature



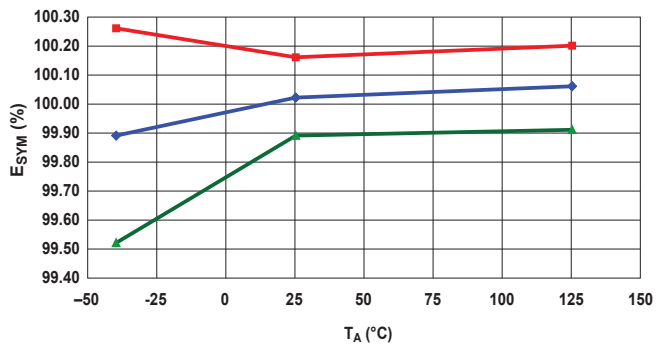
Sensitivity versus Ambient Temperature



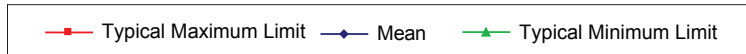
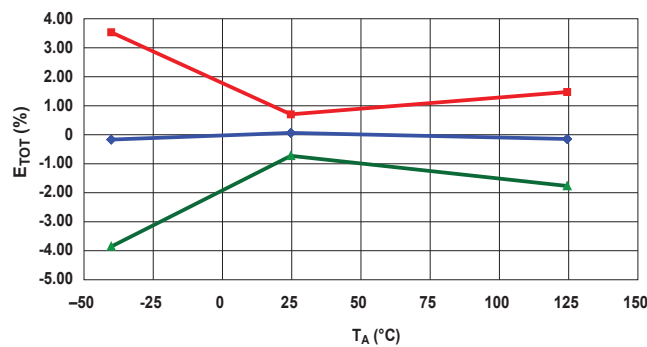
Nonlinearity versus Ambient Temperature



Symmetry versus Ambient Temperature



Total Output Error versus Ambient Temperature

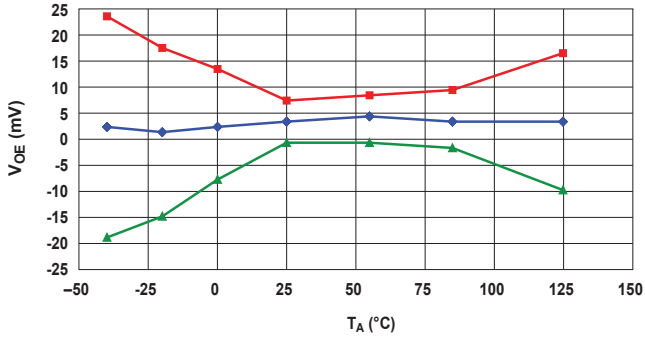


## Characteristic Performance Data

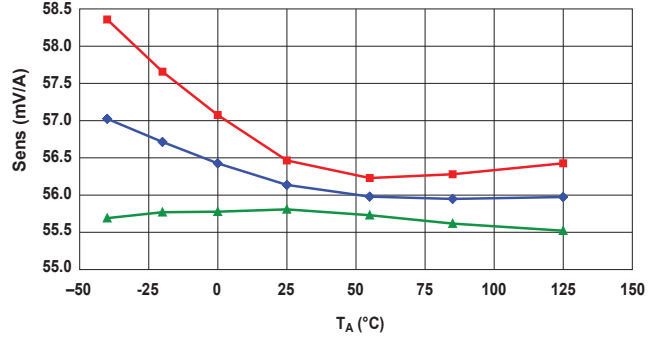
Data taken using the ACS710-12CB

### Accuracy Data

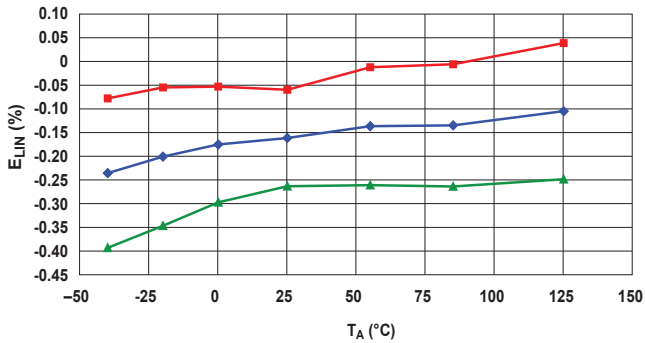
Electrical Offset Voltage versus Ambient Temperature



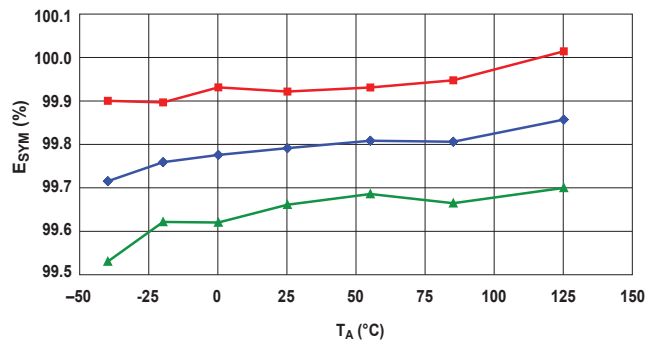
Sensitivity versus Ambient Temperature



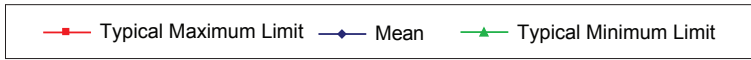
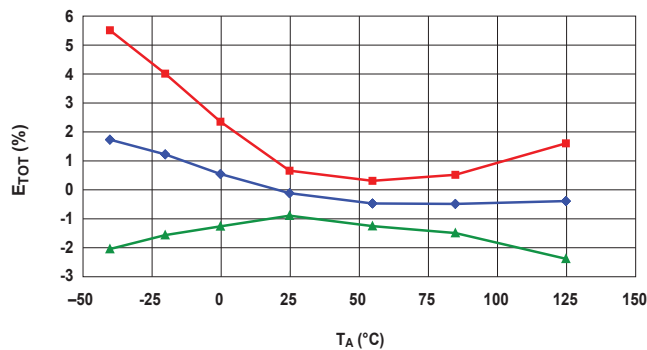
Nonlinearity versus Ambient Temperature



Symmetry versus Ambient Temperature



Total Output Error versus Ambient Temperature

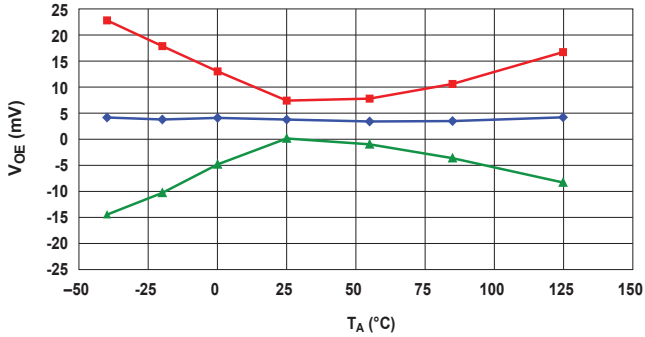


## Characteristic Performance Data

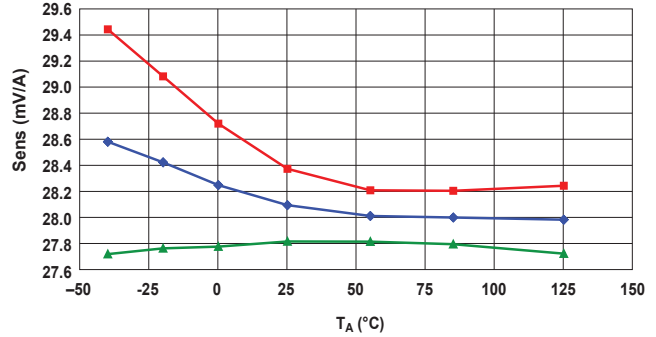
Data taken using the ACS710-25CB

### Accuracy Data

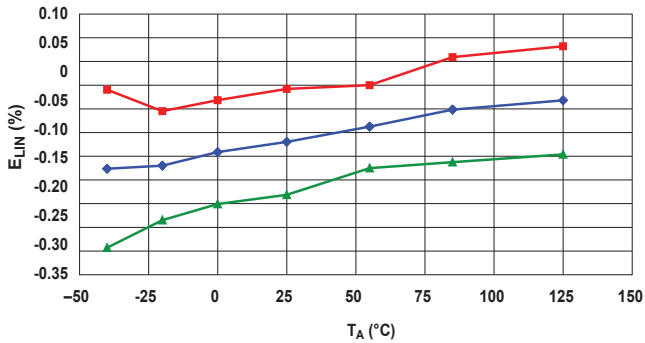
Electrical Offset Voltage versus Ambient Temperature



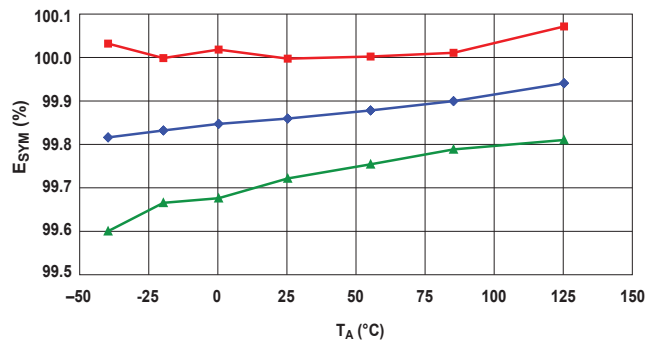
Sensitivity versus Ambient Temperature



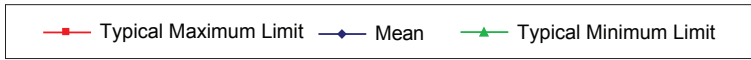
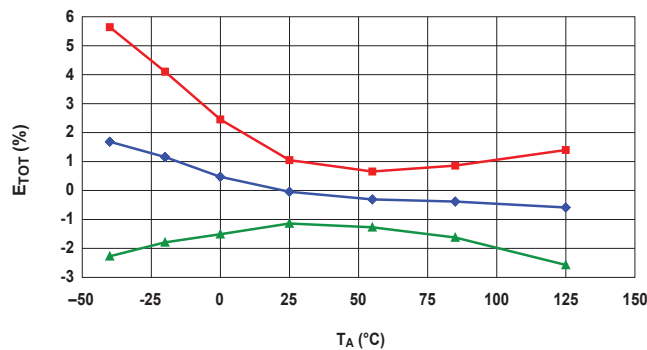
Nonlinearity versus Ambient Temperature



Symmetry versus Ambient Temperature



Total Output Error versus Ambient Temperature



### Setting Overcurrent Fault Switchpoint

#### Setting 12CB and 25CB Versions

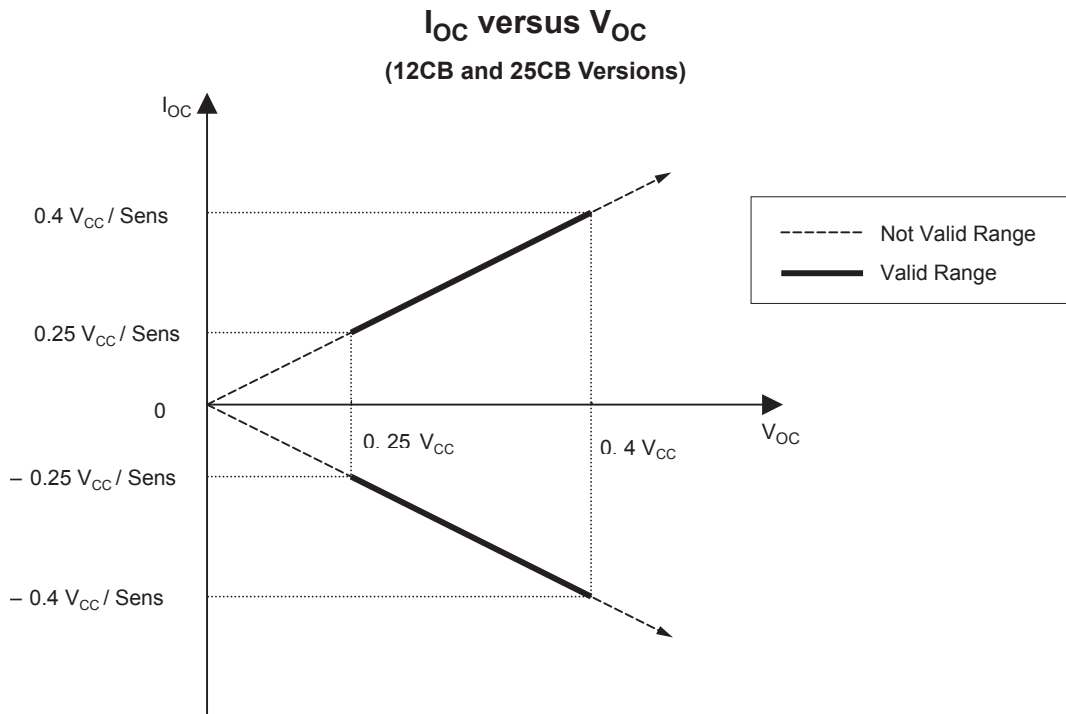
The  $V_{OC}$  needed for setting the overcurrent fault switchpoint can be calculated as follows:

$$V_{OC} = \text{Sens} \times |I_{OC}| ,$$

where  $V_{OC}$  is in mV, Sens in mV/A, and  $I_{OC}$  (overcurrent fault switchpoint) in A.

$|I_{OC}|$  is the overcurrent fault switchpoint for a bidirectional (AC) current, which means a bidirectional sensor will have two symmetrical overcurrent fault switchpoints,  $+I_{OC}$  and  $-I_{OC}$ .

See the following graph for  $I_{OC}$  and  $V_{OC}$  ranges.



Example: For ACS710KLATR-25CB-T, if required overcurrent fault switchpoint is 50 A, and  $V_{CC} = 5$  V, then the required  $V_{OC}$  can be calculated as follows:

$$V_{OC} = \text{Sens} \times I_{OC} = 28 \times 50 = 1400 \text{ (mV)}$$



### Setting 6BB and 10BB Versions

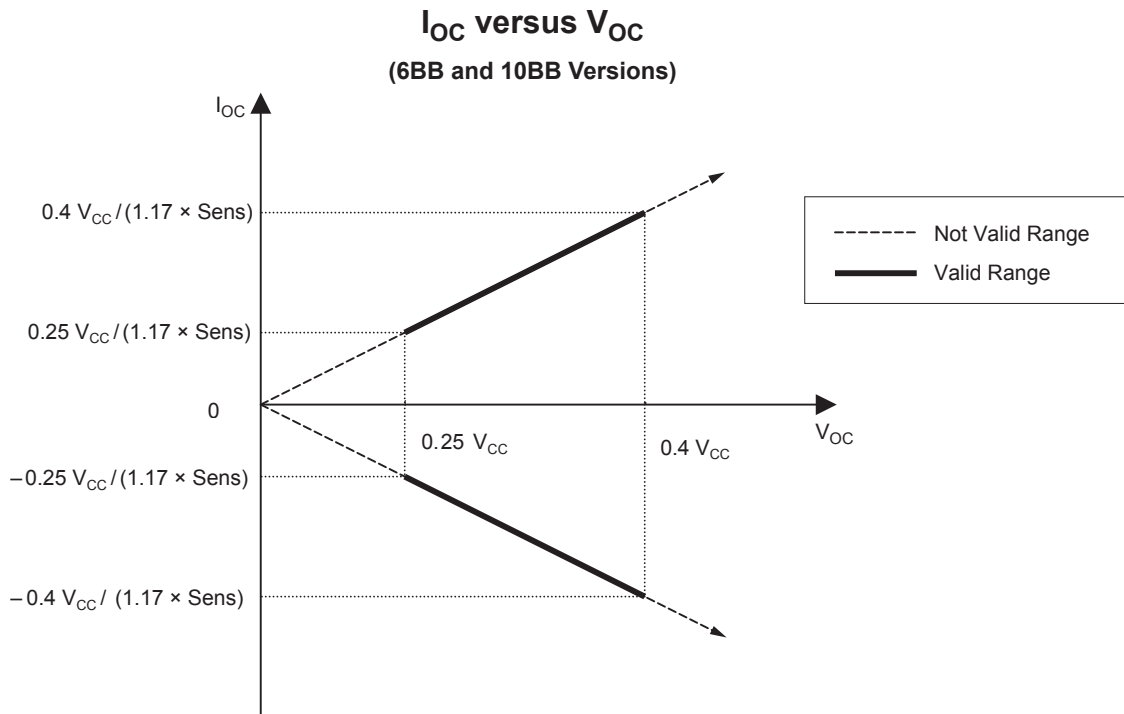
The  $V_{OC}$  needed for setting the overcurrent fault switchpoint can be calculated as follows:

$$V_{OC} = 1.17 \times \text{Sens} \times |I_{OC}| ,$$

where  $V_{OC}$  is in mV, Sens in mV/A, and  $I_{OC}$  (overcurrent fault switchpoint) in A.

$|I_{OC}|$  is the overcurrent fault switchpoint for a bidirectional (AC) current, which means a bidirectional sensor will have two symmetrical overcurrent fault switchpoints,  $+I_{OC}$  and  $-I_{OC}$ .

See the following graph for  $I_{OC}$  and  $V_{OC}$  ranges.



Example: For ACS710KLATR-6BB-T, if required overcurrent fault switchpoint is 10 A, and  $V_{CC} = 5$  V, then the required  $V_{OC}$  can be calculated as follows:

$$V_{OC} = 1.17 \times \text{Sens} \times I_{OC} = 1.17 \times 151 \times 10 = 1767 \text{ (mV)}$$

### Functional Description (Latching Versions)

#### Overcurrent Fault Operation

The primary concern with high-speed fault detection is that noise may cause false tripping. Various applications have or need to be able to ignore certain faults that are due to switching noise or other parasitic phenomena, which are application dependant. The problem with simply trying to filter out this noise in the main signal path is that in high-speed applications, with asymmetric noise, the act of filtering introduces an error into the measurement. To get around this issue, and allow the user to prevent the fault signal from being latched by noise, a circuit was designed to slew the  $\overline{\text{FAULT}}$  pin voltage based on the value of the capacitor from that pin to ground. Once the voltage on the pin falls below 2 V, as established by an internal reference, the fault output is latched and pulled to ground quickly with an internal N-channel MOSFET.

#### Fault Walkthrough

The following walkthrough references various sections and attributes in the figure below. This figure shows different fault set/reset scenarios and how they relate to the voltages on the  $\overline{\text{FAULT}}$  pin,  $\text{FAULT\_EN}$  pin, and the internal Overcurrent (OC) Fault node, which is invisible to the customer.

1. Because the device is enabled ( $\text{FAULT\_EN}$  is high for a minimum period of time, the Fault Enable Delay,  $t_{\text{FED}}$ , 15  $\mu\text{s}$  typical) and there is an OC fault condition, the device  $\overline{\text{FAULT}}$  pin starts discharging.
2. When the  $\overline{\text{FAULT}}$  pin voltage reaches approximately 2 V, the fault is latched, and an internal NMOS device pulls the  $\overline{\text{FAULT}}$  pin voltage to approximately 0 V. The rate at which the  $\overline{\text{FAULT}}$  pin slews downward (see [4] in the figure) is dependent on the external capacitor,  $C_{\text{OC}}$ , on the  $\overline{\text{FAULT}}$  pin.
3. When the  $\text{FAULT\_EN}$  pin is brought low, the  $\overline{\text{FAULT}}$  pin starts resetting if no OC fault condition exists, and if  $\text{FAULT\_EN}$  is low for a time period greater than  $t_{\text{OCH}}$ . The

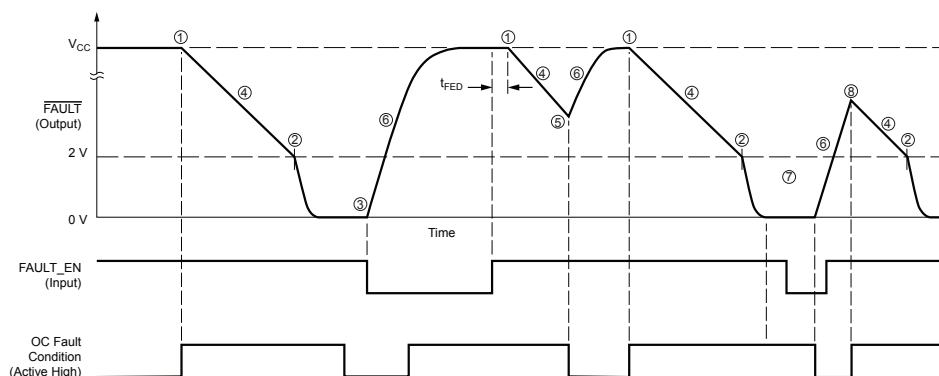
internal NMOS pull-down turns off and an internal PMOS pull-up turns on (see [7] if the OC fault condition still exists).

4. The slope, and thus the delay to latch the fault is controlled by the capacitor,  $C_{\text{OC}}$ , placed on the  $\overline{\text{FAULT}}$  pin to ground. During this portion of the fault (when the  $\overline{\text{FAULT}}$  pin is between  $V_{\text{CC}}$  and 2 V), there is a 3 mA constant current sink, which discharges  $C_{\text{OC}}$ . The length of the fault delay,  $t$ , is equal to:

$$t = \frac{C_{\text{OC}} \times (V_{\text{CC}} - 2 \text{ V})}{3 \text{ mA}} \quad (1)$$

where  $V_{\text{CC}}$  is the device power supply voltage in volts,  $t$  is in seconds and  $C_{\text{OC}}$  is in Farads. This formula is valid for  $R_{\text{PU}}$  equal to or greater than 330 k $\Omega$ . For lower-value resistors, the current flowing through the  $R_{\text{PU}}$  resistor during a fault event,  $I_{\text{PU}}$ , will be larger. Therefore, the current discharging the capacitor would be  $3 \text{ mA} - I_{\text{PU}}$  and equation 1 may not be valid.

5. The  $\overline{\text{FAULT}}$  pin did not reach the 2 V latch point before the OC fault condition cleared. Because of this, the fixed 3 mA current sink turns off, and the internal PMOS pull-up turns on to recharge  $C_{\text{OC}}$  through the  $\overline{\text{FAULT}}$  pin.
6. This curve shows  $V_{\text{CC}}$  charging external capacitor  $C_{\text{OC}}$  through the internal PMOS pull-up. The slope is determined by  $C_{\text{OC}}$ .
7. When the  $\text{FAULT\_EN}$  pin is brought low, if the fault condition still exists, the latched  $\overline{\text{FAULT}}$  pin will be pulled low by the internal 3mA current source. When fault condition is removed then the Fault pin charges as shown in step 6.
8. At this point there is a fault condition, and the part is enabled before the  $\overline{\text{FAULT}}$  pin can charge to  $V_{\text{CC}}$ . This shortens the user-set delay, so the fault is latched earlier. The new delay time can be calculated by equation 1, after substituting the voltage seen on the  $\overline{\text{FAULT}}$  pin for  $V_{\text{CC}}$ .



### Functional Description (Non-Latching Versions)

#### Overcurrent Fault Operation

The primary concern with high-speed fault detection is that noise may cause false tripping. Various applications have or need to be able to ignore certain faults that are due to switching noise or other parasitic phenomena, which are application dependant. The problem with simply trying to filter out this noise in the main signal path is that in high-speed applications, with asymmetric noise, the act of filtering introduces an error into the measurement.

To get around this issue, and allow the user to prevent the fault signal from going low due to noise, a circuit was designed to slew the  $\overline{\text{FAULT}}$  pin voltage based on the value of the capacitor from that pin to ground. Once the voltage on the pin falls below 2 V, as established by an internal reference, the fault output is pulled to ground quickly with an internal N-channel MOSFET.

#### Fault Walkthrough

The following walkthrough references various sections and attributes in the figure below. This figure shows different fault set/reset scenarios and how they relate to the voltages on the  $\overline{\text{FAULT}}$  pin,  $\text{FAULT\_EN}$  pin, and the internal Overcurrent (OC) Fault node, which is invisible to the customer.

1. Because the device is enabled ( $\text{FAULT\_EN}$  is high for a minimum period of time, the Fault Enable Delay,  $t_{\text{FED}}$ , and there is an OC fault condition, the device  $\overline{\text{FAULT}}$  pin starts discharging.
2. When the  $\overline{\text{FAULT}}$  pin voltage reaches approximately 2 V, an internal NMOS device pulls the  $\overline{\text{FAULT}}$  pin voltage to approximately 0 V. The rate at which the  $\overline{\text{FAULT}}$  pin slews downward (see [4] in the figure) is dependent on the external capacitor,  $C_{\text{OC}}$ , on the  $\overline{\text{FAULT}}$  pin.
3. When the  $\text{FAULT\_EN}$  pin is brought low, the  $\overline{\text{FAULT}}$  pin starts resetting if  $\text{FAULT\_EN}$  is low for a time period greater

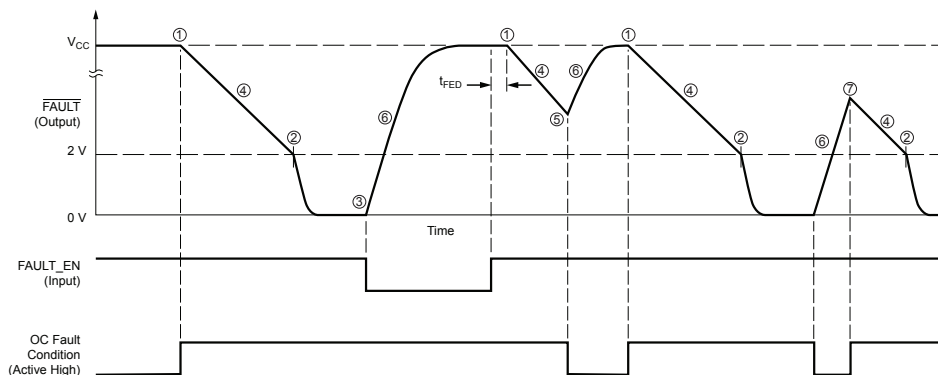
than  $t_{\text{OCH}}$ . The internal NMOS pull-down turns off and an internal PMOS pull-up turns on.

4. The slope, and thus the delay to pull the fault low is controlled by the capacitor,  $C_{\text{OC}}$ , placed on the  $\overline{\text{FAULT}}$  pin to ground. During this portion of the fault (when the  $\overline{\text{FAULT}}$  pin is between  $V_{\text{CC}}$  and 2 V), there is a 3 mA constant current sink, which discharges  $C_{\text{OC}}$ . The length of the fault delay,  $t$ , is equal to:

$$t = \frac{C_{\text{OC}} \times (V_{\text{CC}} - 2 \text{ V})}{3 \text{ mA}} \quad (2)$$

where  $V_{\text{CC}}$  is the device power supply voltage in volts,  $t$  is in seconds and  $C_{\text{OC}}$  is in Farads. This formula is valid for  $R_{\text{PU}}$  equal to or greater than 330 k $\Omega$ . For lower-value resistors, the current flowing through the  $R_{\text{PU}}$  resistor during a fault event,  $I_{\text{PU}}$ , will be larger. Therefore, the current discharging the capacitor would be  $3 \text{ mA} - I_{\text{PU}}$  and equation 1 may not be valid.

5. The  $\overline{\text{FAULT}}$  pin did not reach the 2 V latch point before the OC fault condition cleared. Because of this, the fixed 3 mA current sink turns off, and the internal PMOS pull-up turns on to recharge  $C_{\text{OC}}$  through the  $\overline{\text{FAULT}}$  pin.
6. This curve shows  $V_{\text{CC}}$  charging external capacitor  $C_{\text{OC}}$  through the internal PMOS pull-up. The slope is determined by  $C_{\text{OC}}$ .
7. At this point there is a fault condition, and the part is enabled before the  $\overline{\text{FAULT}}$  pin can charge to  $V_{\text{CC}}$ . This shortens the user-set delay, so the fault gets pulled low earlier. The new delay time can be calculated by equation 1, after substituting the voltage seen on the  $\overline{\text{FAULT}}$  pin for  $V_{\text{CC}}$ .

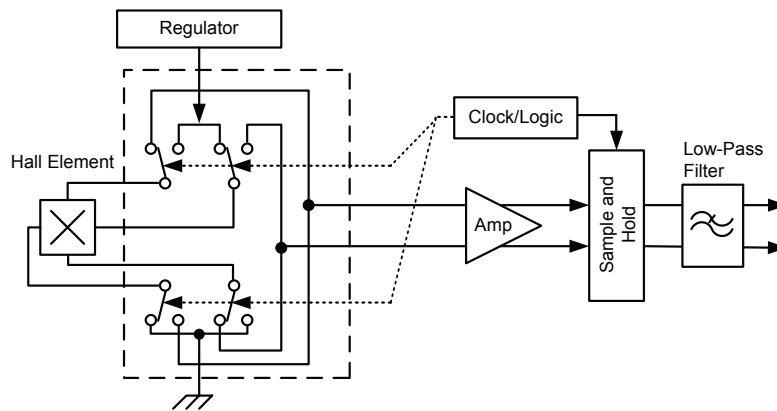


### Chopper Stabilization Technique

Chopper stabilization is an innovative circuit technique that is used to minimize the offset voltage of a Hall element and an associated on-chip amplifier. Allegro patented a chopper stabilization technique that nearly eliminates Hall IC output drift induced by temperature or package stress effects. This offset reduction technique is based on a signal modulation-demodulation process. Modulation is used to separate the undesired DC offset signal from the magnetically induced signal in the frequency domain. Then, using a low-pass filter, the modulated DC offset is suppressed while the magnetically induced signal passes through the filter. As a result of this chopper stabilization approach, the

output voltage from the Hall IC is desensitized to the effects of temperature and mechanical stress. This technique produces devices that have an extremely stable electrical offset voltage, are immune to thermal stress, and have precise recoverability after temperature cycling.

This technique is made possible through the use of a BiCMOS process that allows the use of low-offset and low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Concept of Chopper Stabilization Technique



### Definitions of Accuracy Characteristics

**Sensitivity (Sens).** The change in sensor output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

**Noise ( $V_{NOISE}$ ).** The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall-effect linear IC. The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

**Linearity ( $E_{LIN}$ ).** The degree to which the voltage output from the sensor varies in direct proportion to the primary current through its full-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100 \left\{ 1 - \left[ \frac{V_{IOUT\_full\text{-}scale\text{ amperes}} - V_{IOUT(Q)}}{2 (V_{IOUT\_1/2\text{ full-scale amperes}} - V_{IOUT(Q)})} \right] \right\}$$

where  $V_{IOUT\_full\text{-}scale\text{ amperes}}$  = the output voltage (V) when the sensed current approximates full-scale  $\pm I_p$ .

**Symmetry ( $E_{SYM}$ ).** The degree to which the absolute voltage output from the sensor varies in proportion to either a positive or negative full-scale primary current. The following formula is used to derive symmetry:

$$100 \left( \frac{V_{IOUT\_+full\text{-}scale\text{ amperes}} - V_{IOUT(Q)}}{V_{IOUT(Q)} - V_{IOUT\_full\text{-}scale\text{ amperes}}} \right)$$

**Quiescent output voltage ( $V_{IOUT(Q)}$ ).** The output of the sensor when the primary current is zero. For a unipolar supply voltage, it nominally remains at  $0.5 \times V_{CC}$ . For example, in the case of a bidirectional output device,  $V_{CC} = 5\text{ V}$  translates into  $V_{IOUT(Q)} = 2.5\text{ V}$ . Variation in  $V_{IOUT(Q)}$  can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

**Electrical offset voltage ( $V_{OE}$ ).** The deviation of the device output from its ideal quiescent voltage due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

**Accuracy ( $E_{TOT}$ ).** The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total output error. The accuracy is illustrated graphically in the output voltage versus current chart at right. Note that error is directly measured during final test at Allegro.

Accuracy is divided into four areas:

- **0 A at 25°C.** Accuracy of sensing zero current flow at 25°C, without the effects of temperature.
- **0 A over  $\Delta$  temperature.** Accuracy of sensing zero current flow including temperature effects.
- **Full-scale current at 25°C.** Accuracy of sensing the full-scale current at 25°C, without the effects of temperature.
- **Full-scale current over  $\Delta$  temperature.** Accuracy of sensing full-scale current flow including temperature effects.

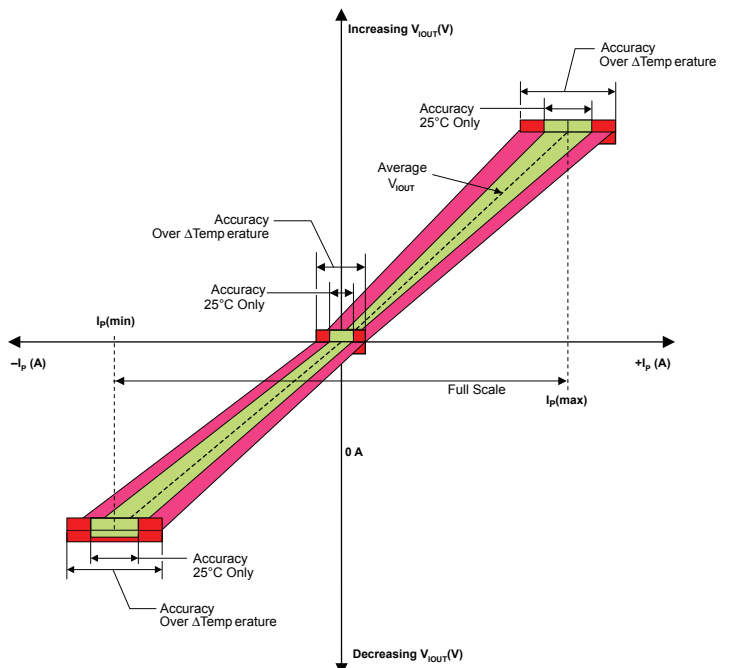
**Ratiometry.** The ratiometric feature means that its 0 A output,  $V_{IOUT(Q)}$ , (nominally equal to  $V_{CC}/2$ ) and sensitivity, Sens, are proportional to its supply voltage,  $V_{CC}$ . The following formula is used to derive the ratiometric change in 0 A output voltage,  $\Delta V_{IOUT(Q)RAT}$  (%).

$$100 \left( \frac{V_{IOUT(Q)VCC} / V_{IOUT(Q)5V}}{V_{CC} / 5\text{ V}} \right)$$

The ratiometric change in sensitivity,  $\Delta Sens_{RAT}$  (%), is defined as:

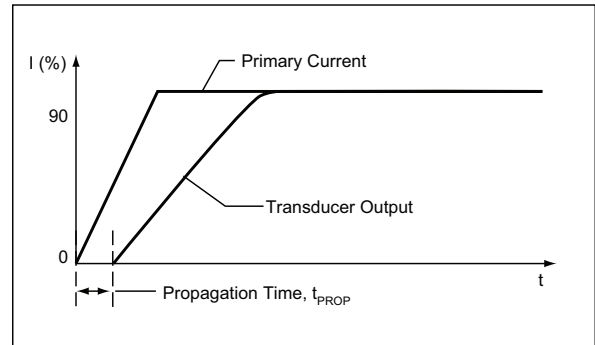
$$100 \left( \frac{Sens_{VCC} / Sens_{5V}}{V_{CC} / 5\text{ V}} \right)$$

**Output Voltage versus Sensed Current**  
Accuracy at 0 A and at Full-Scale Current

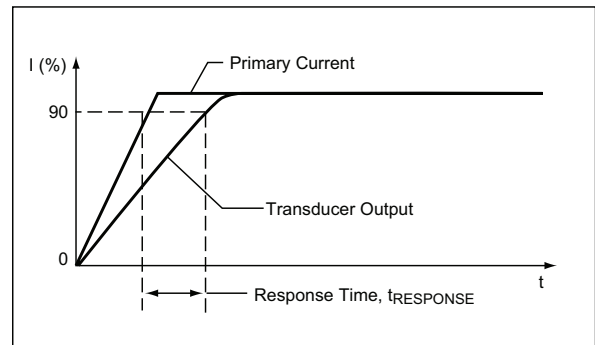


### Definitions of Dynamic Response Characteristics

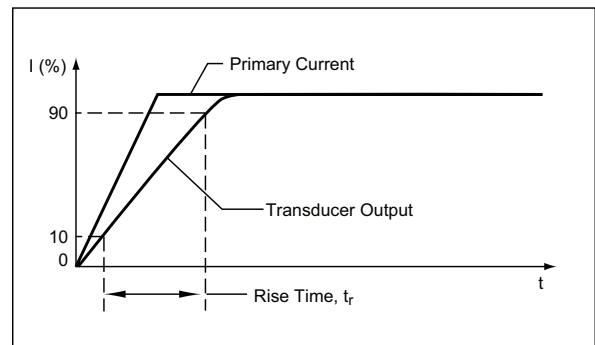
**Propagation delay ( $t_{PROP}$ ).** The time required for the sensor output to reflect a change in the primary current signal. Propagation delay is attributed to inductive loading within the linear IC package, as well as in the inductive loop formed by the primary conductor geometry. Propagation delay can be considered as a fixed-time offset and may be compensated.



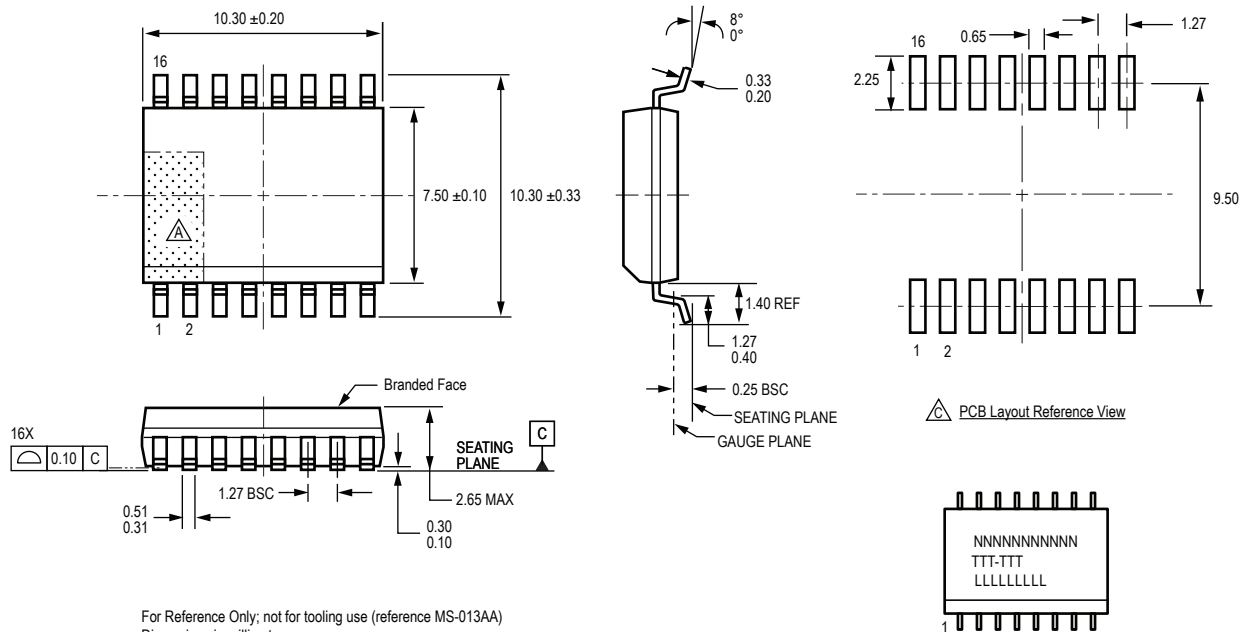
**Response time ( $t_{RESPONSE}$ ).** The time interval between a) when the primary current signal reaches 90% of its final value, and b) when the sensor reaches 90% of its output corresponding to the applied current.



**Rise time ( $t_r$ ).** The time interval between a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value. The rise time to a step response is used to derive the bandwidth of the current sensor, in which  $f(-3 \text{ dB}) = 0.35/t_r$ . Both  $t_r$  and  $t_{RESPONSE}$  are detrimentally affected by eddy current losses observed in the conductive IC ground plane.



### Package LA, 16-Pin SOICW



For Reference Only; not for tooling use (reference MS-013AA)  
 Dimensions in millimeters  
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
 Exact case and lead configuration at supplier discretion within limits shown

- Terminal #1 mark area
- Branding scale and appearance at supplier discretion
- Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Standard Branding Reference View

N = Device part number  
 T = Temperature range, package - amperage  
 L = Lot number

**Revision History**

<b>Revision</b>	<b>Revision Date</b>	<b>Description of Revision</b>
9	June 17, 2013	Add 10BB variant
10	August 19, 2015	Added certificate number under UL stamp on page 1; updated Isolation Characteristics table.

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