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ACS8510 Rev2.1 SETS

Synchronous **E**quipment **T**iming **S**ource
for SONET or SDH Network Elements

ADVANCED COMMUNICATIONS **FINAL**

Description

The ACS8510 is a highly integrated, single-chip solution for the Synchronous Equipment Timing Source (SETS) function in a SONET or SDH Network Element. The device generates SONET or SDH Equipment Clocks (SEC) and frame synchronization clocks. The ACS8510 is fully compliant with the required specifications and standards.

The device supports Free-run, Locked and Holdover modes. It also supports all three types of reference clock source: recovered line clock, PDH network, and node synchronization. The ACS8510 generates independent SEC and BITS clocks, an 8 kHz Frame Synchronization clock and a 2 kHz Multi-Frame Synchronization clock.

Two ACS8510 devices can be used together in a Master/Slave configuration mode allowing system protection against a single ACS8510 failure.

A microprocessor port is incorporated, providing access to the configuration and status registers for device setup and monitoring. The ACS8510 supports IEEE 1149.1 JTAG boundary scan.

Rev2.1 adds choice of edge alignment for 8kHz input, as well as a low jitter n x E1/DS1 output mode. Other minor changes are made, with all described in Appendix A.

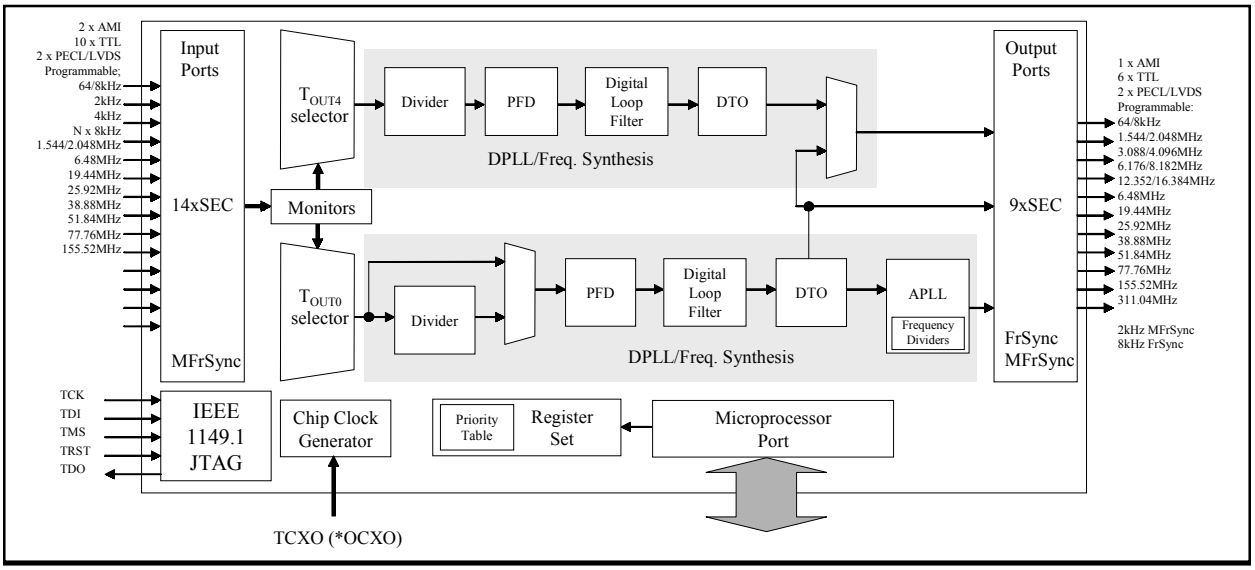
Features

- Suitable for Stratum 3E*, 3, 4E and 4 SONET or SDH Equipment Clock (SEC) applications
- Meets AT&T, ITU-T, ETSI and Telcordia specifications
- Accepts 14 individual input reference clocks
- Generates 11 output clocks
- Supports Free-run, Locked and Holdover modes of operation
- Robust input clock source quality monitoring on all inputs
- Automatic ‘hit-less’ source switchover on loss of input
- Phase build out for output clock phase continuity during input switchover and mode transitions
- Microprocessor interface - Intel, Motorola, Serial, Multiplexed, EPROM
- Programmable wander and jitter tracking attenuation 0.1 Hz to 20 Hz
- Support for Master/Slave device configuration alignment and hot/standby redundancy
- IEEE 1149.1 JTAG Boundary Scan
- Single +3.3 V operation, +5 V I/O compatible
- Operating temperature (ambient) -40°C to +85°C
- Available in 100 pin LQFP package

* Meets Holdover requirements, lowest bandwidth 0.1 Hz.

Block Diagram

Figure 1. Simple Block Diagram



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Pin Diagram

Figure 2. ACS8510 Pin Diagram

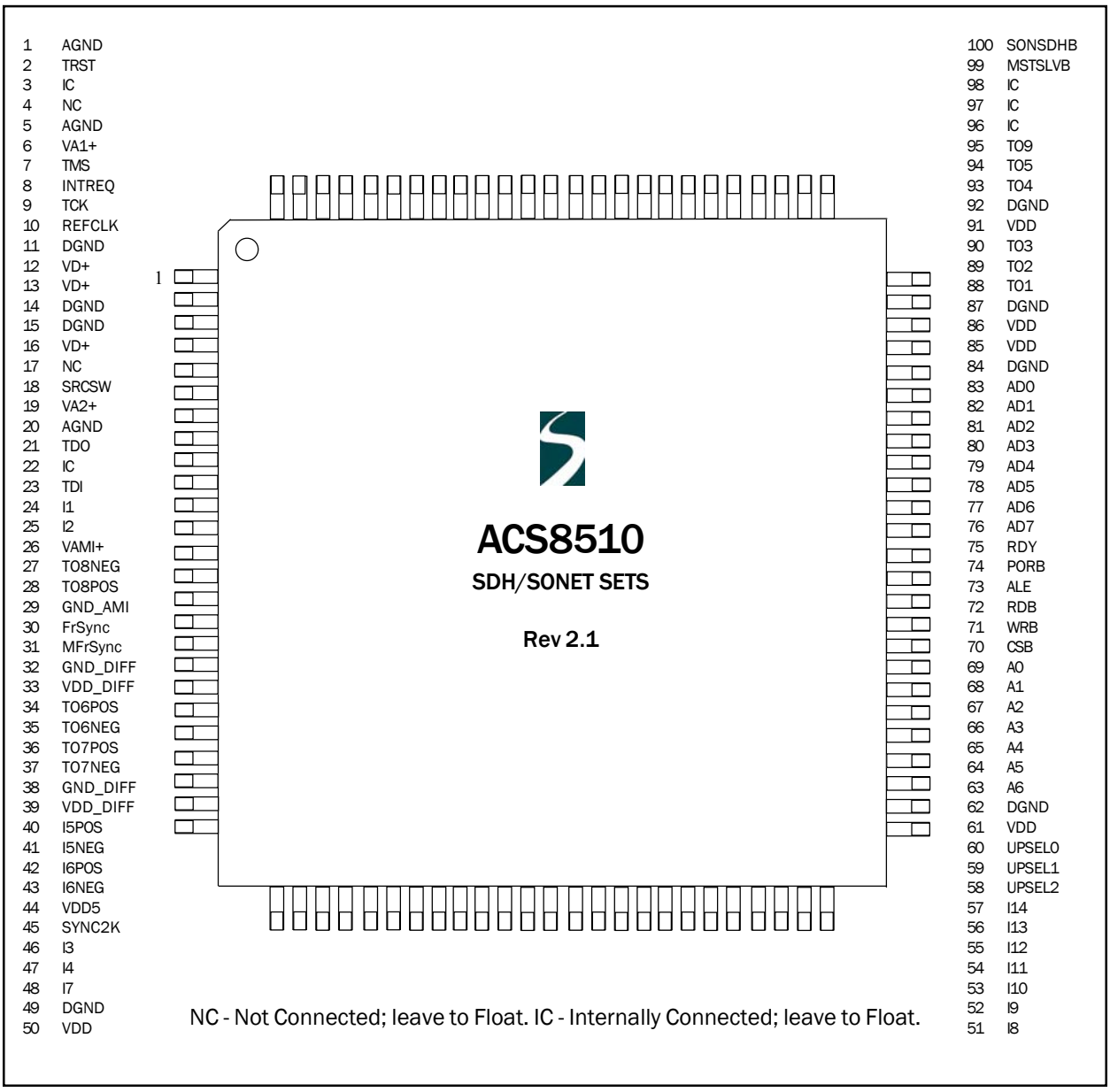


Table 1. Power Pins

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
12, 13, 16	VD+	P	-	**Supply voltage:** Digital supply to gates in analog section, +3.3 Volts. +/- 10%
26	VAMI+	P	-	**Supply voltage :** Digital supply to AMI output, +3.3 Volts. +/- 10%
33, 39	VDD_DIFF	P	-	**Supply voltage :** Digital supply for differential ports, +3.3 Volts. +/- 10%
44	VDD5	P	-	**VDD5**: Digital supply for +5 Volts tolerance to input pins. Connect to +5 Volts (+/- 10%) for clamping to +5 Volts. Connect to VDD for clamping to +3.3 Volts. Leave floating for no clamping, input pins tolerant up to +5.5 Volts.
50, 61, 85, 86, 91	VDD	P	-	**Supply voltage :** Digital supply to logic, +3.3 Volts. +/- 10%
6	VA1+	P	-	**Supply voltage:** Analog supply to clock multipying PLL, +3.3 Volts. +/- 10%
19	VA2+	P	-	**Supply voltage** : Analog supply to output PLL, +3.3 Volts. +/- 10%
11, 14, 15, 49, 62, 84, 87, 92	DGND	P	-	**Supply Ground**: Digital ground for logic
29	GND_AMI	P	-	**Supply Ground**: Digital ground for AMI output
32, 38	GND_DIFF	P	-	**Supply Ground**: Digital ground for differential ports
1, 5, 20	AGND	P	-	**Supply Ground**: Analog ground

Table 2. No Connections

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
4, 17	NC	-	-	**Not Connected**: Leave to Float
3, 22, 96, 97,98	IC	-	-	**Internally Connected**: Leave to Float

Note: I = input, O = output, P = power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor

Table 3. Other Pins

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
2	TRST	I	TTL_D	**JTAG Control Reset Input**: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 for normal device operation (JTAG logic transparent). If not used connect to GND or leave floating.
7	TMS	I	TTL^U	**JTAG Test Mode Select**: Boundary Scan enable. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
8	INTREQ	O	TTL CMOS	**Interrupt Request**: Active high software Interrupt output
9	TCK	I	TTL_D	**JTAG Clock**: Boundary Scan clock input. If not used connect to GND or leave floating. This pin may require a capacitor placed between the pin and the nearest GND, to reduce noise pickup. A value of 10 pF should be adequate, but the value is dependent on PCB layout.
10	REFCLK	I	TTL	**Reference Clock**: 12.8 MHz (refer to section headed Local Oscillator Clock)
18	SRCSW	I	TTL_D	**Source Switching**: Force Fast Source Switching
21	TDO	O	TTL CMOS	**JTAG Output**: Serial test data output. Updated on falling edge of TCK. If not used leave floating.
23	TDI	I	TTL^U	**JTAG Input**: Serial test data Input. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
24	I1	I	AMI	**Input reference 1**: composite clock 64 kHz + 8 kHz
25	I2	I	AMI	**Input reference 2**: composite clock 64 kHz + 8 kHz
27	TO8NEG	O	AMI	**Output reference 8**: composite clock, 64 kHz + 8 kHz negative pulse
28	TO8POS	O	AMI	**Output reference 8**: composite clock, 64 kHz + 8 kHz positive pulse
30	FrSync	O	TTL CMOS	**Output reference 10**: 8 kHz Frame Sync clock output (square wave)
31	MFrSync	O	TTL CMOS	**Output reference 11**: 2 kHz Multi-Frame Sync clock output (square wave)
34 35	TO6POS TO6NEG	O	LVDS PECL	**Output reference 6**: default 38.88 MHz. Also Dig1 (1.544 MHz/2.048 MHz and 2, 4, 8 x), 19.44 MHz, 155.52 MHz, 311.04 MHz. Default type LVDS.
36 37	TO7POS TO7NEG	O	PECL LVDS	**Output reference 7**: default 19.44 MHz. Also 51.84 MHz, 77.76 MHz, 155.52 MHz. Default type PECL.
40 41	I5POS I5NEG	I	LVDS PECL	**Input reference 5**: default 19.44 MHz, default type LVDS
42 43	I6POS I6NEG	I	PECL LVDS	**Input reference 6**: default 19.44 MHz, default type PECL

Table 3. Other Pins (continued)

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
45	SYNC2K	I	TTL_D	**Synchronise 2 kHz**: Connect to 2 kHz Multi-Frame Sync output of partner ACS8510 in redundancy system
46	I3	I	TTL_D	**Input reference 3**: programmable, default 8 kHz
47	I4	I	TTL_D	**Input reference 4**: programmable, default 8 kHz
48	I7	I	TTL_D	**Input reference 7**: programmable, default 19.44 MHz
51	I8	I	TTL_D	**Input reference 8**: programmable, default 19.44 MHz
52	I9	I	TTL_D	**Input reference 9**: programmable, default 19.44 MHz
53	I10	I	TTL_D	**Input reference 10**: programmable, default 19.44 MHz.
54	I11	I	TTL_D	**Input reference 11:** programmable, default (master mode)1.544/2.048 MHz, default (slave mode) 6.48 MHz
55	I12	I	TTL_D	**Input reference 12**: programmable, default 1.544/2.048 MHz.
56	I13	I	TTL_D	**Input reference 13**: programmable, default 1.544/2.048 MHz.
57	I14	I	TTL_D	**Input reference 14**: programmable, default 1.544/2.048 MHz.
58 - 60	UPSEL(2:0)	I	TTL_D	**Microprocessor select**: Configures the interface for a particular microprocessor type.
63 - 69	A(6:0)	I	TTL_D	**Microprocessor Interface Address**: Address bus for the microprocessor interface registers. A(0) is SDI in Serial mode.
70	CSB	I	TTL^U	**Chip Select (Active Low)**: This pin is asserted Low by the microprocessor to enable the microprocessor interface.
71	WRB	I	TTL^U	**Write (Active Low)**: This pin is asserted Low by the microprocessor to initiate a write cycle. In Motorola mode, WRB = 1 for Read.
72	RDB	I	TTL^U	**Read (Active Low)**: This pin is asserted Low by the microprocessor to initiate a read cycle.
73	ALE	I	TTL_D	**Address Latch Enable**: This pin becomes the address latch enable from the microprocessor. When this pin transitions from Low to High, the address bus inputs are latched into the internal registers. ALE = SCLK in Serial mode.
74	PORB	I	TTL^U	**Power On Reset**: Master reset. If PORB is forced Low, all internal states are reset back to default values.
75	RDY	O	TTL CMOS	**Ready/Data acknowledge**: This pin is asserted High to indicate the device has completed a read or write operation.
76 - 83	AD(7:0)	IO	TTL_D	**Address/Data**: Multiplexed data/address bus depending on the microprocessor mode selection. AD(0) is SDO in Serial mode.

Table 3. Other Pins (continued)

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
88	TO1	O	TTL CMOS	**Output reference 1**: default 6.48 MHz. Also Dig1 (1.544 MHz/2.048 MHz and 2, 4, 8 x), 19.44 MHz, 25.92 MHz
89	TO2	O	TTL CMOS	**Output reference 2**: default 38.88 MHz. Also Dig2 (1.544 MHz/2.048 MHz and 2, 4, 8 x), 25.92 MHz, 51.84 MHz
90	TO3	O	TTL CMOS	**Output reference 3**: 19.44 MHz - fixed.
93	TO4	O	TTL CMOS	**Output reference 4**: 38.88 MHz - fixed.
94	TO5	O	TTL CMOS	**Output reference 5**: 77.76 MHz - fixed.
95	TO9	O	TTL CMOS	**Output reference 9**: 1.544/2.048 MHz. (T4 BITS)
99	MSTSLVB	I	TTL^U	**MASTERSLAVEB**: Master slave select: sets the initial power up state (or state after a PORB) of the Master/Slave selection register, addr 34, bit 1. The register state can be changed after power up by software.
100	SONSDHB	I	TTL_D	**SONETSDHB**: SONET or SDH frequency select: sets the initial power up state (or state after a PORB) of the SONET/SDH frequency selection registers, addr 34h, bit 2 and addr 38, bits 5 and 6. The register states can be changed after power up by software.

Functional Description

The ACS8510 is a highly integrated, single-chip solution for the SETS function in a SONET/SDH Network Element, for the generation of SEC and frame synchronization pulses. In Free-run mode, the ACS8510 generates a stable, low-noise clock signal from an internal oscillator. In Locked mode, the ACS8510 selects the most appropriate input reference source and generates a stable, low-noise clock signal locked to the selected reference. In Holdover mode, the ACS8510 generates a stable, low-noise clock signal from the internal oscillator, adjusted to match the last known good frequency of the last selected reference source. In all modes, the frequency accuracy, jitter and drift performance of the clock meet the requirements of ITU G.812, G.813, G.823, and GR-1244-CORE.

The ACS8510 supports all three types of reference clock source: recovered line clock (T_{IN1}), PDH network synchronization timing (T_{IN2}) and node synchronization (T_{IN3}). The ACS8510 generates independent T_{OUT0} and T_{OUT4} clocks, an 8 kHz Frame Synchronization clock and a 2 kHz Multi-Frame Synchronization clock.

The ACS8510 has a high tolerance to input jitter and wander. The jitter/wander transfer is programmable (0.1 Hz up to 20 Hz cut-off points).

The ACS8510 supports protection. Two ACS8510 devices can be configured to provide protection against a single ACS8510 failure. The protection maintains alignment of the two ACS8510 devices (Master and Slave) and ensures that both ACS8510 devices maintain the same priority table, choose the same

reference input and generate the T_{OUT0} clock, the 8 kHz Frame Synchronization clock and the 2 kHz Multi-Frame Synchronization clock with the same phase. The ACS8510 includes a microprocessor port, providing access to the configuration and status registers for device setup and monitoring.

Local Oscillator Clock

The Master system clock on the ACS8510 should be provided by an external clock oscillator of frequency 12.80 MHz. The clock specification is important for meeting the ITU/ETSI and Telcordia performance requirements for Holdover mode. ITU and ETSI specifications permit a combined drift characteristic, at constant temperature, of all non-temperature-related parameters, of up to 10 ppb per day. The same specifications allow a drift of 1 ppm over a temperature range of 0 to +70 °C. Telcordia specifications are somewhat tighter, requiring a non-temperature-related drift of less than 40 ppb per day and a drift of 280 ppb over the temperature range 0 to +50 °C.

ITU and ETSI Specification

Tolerance:	+/- 4.6 ppm over 20 year life time.
Drift*:	+/- 0.05 ppm/15 seconds @ constant temp.
	+/- 0.01 ppm/day @ constant temp.
	+/- 1 ppm over temp. range 0 to +70 °C

*Frequency drift over supply range of +2.7V to +3.3V.

Telcordia GR-1244 CORE Specification

Tolerance:	+/- 4.6 ppm over 20 year life time.
Drift*:	+/- 0.05 ppm/15 seconds @ constant temp.
	+/- 0.04 ppm/day @ constant temp.
	+/- 0.28 ppm over temp. range 0 to +50 °C

*Frequency drift over supply range of +2.7V to +3.3V.

Please contact Semtech for information on crystal oscillator suppliers.

Crystal Frequency Calibration

The absolute crystal frequency accuracy is less important than the stability since any frequency offset can be compensated by adjustment of register values in the IC. This allows for calibration and compensation of any crystal frequency variation away from its nominal value. +/- 50 ppm adjustment would be sufficient to cope with most crystals, in fact the range is an order of magnitude larger due to the use of two 8 bit register locations. The setting of the *conf_nominal_frequency* register allows for this adjustment. An increase in the register value increases the output frequencies by 0.02 ppm for each LSB step. The default value (in decimal) is 39321. The minimum being 0 and the maximum 65535, gives a -700 ppm to +500 ppm adjustment range of the output frequencies.

For example, if the crystal was oscillating at 12.8 MHz + 5 ppm, then the calibration value in the register to give a -5 ppm adjustment in output frequencies to compensate for the crystal inaccuracy, would be :

39321 - (5 / 0.02) = 39071 (decimal)

Input Interfaces

The ACS8510 supports up to fourteen input reference clock sources from input types T_{IN1}, T_{IN2} and T_{IN3} using TTL, CMOS, PECL, LVDS and AMI buffer I/O technologies. These interface technologies support +3.3 V and +5 V operation.

Over-Voltage Protection

The ACS8510 may require Over-Voltage Protection on input reference clock ports according to ITU Recommendation K.41. Semtech protection devices are recommended for this purpose (see separate Semtech data book).

Input Reference Clock Ports

Table 4 gives details of the input reference ports, showing the input technologies and the range of frequencies supported on each port; the default spot frequencies and default priorities assigned to each port on power-up or by reset are also shown. Note that SDH and SONET networks use different default frequencies; the network type is pin-selectable (using the SONSDHB pin). Specific frequencies and priorities are set by configuration.

Although each input port is shown as belonging to one of the types, T_{IN1}, T_{IN2} or T_{IN3}, they are fully interchangeable as long as the selected speed is within the maximum operating speed of the input port technology.

SDH and SONET networks use different default frequencies; the network type is selectable using the *config_mode* register 34 Hex, bit 2. For SONET, *config_mode* register 34 Hex, bit 2 = 1, for SDH *config_mode* register 34 Hex, bit 2 = 0. On power-up or by reset, the default will be set by the state of the SONSDHB pin (pin 100). Specific frequencies and priorities are set by configuration.

TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies supported are:

- 2 kHz
- 4 kHz
- 8 kHz (and N x 8 kHz)
- 1.544 MHz (SONET)/2.048 MHz (SDH)
- 6.48 MHz,
- 19.44 MHz,
- 25.92 MHz,
- 38.88 MHz,
- 51.84 MHz,
- 77.76 MHz.

The frequency selection is programmed via the *cnfg_ref_source_frequency* register. The internal DPLL will normally lock to the selected input at the frequency of the input, eg. 19.44 MHz will lock the DPLL phase comparisons at 19.44 MHz. It is, however, possible to utilise an internal pre-divider to the DPLL to divide the input frequency before it is used for phase comparisons in the DPLL. This pre-divider can be used in one of 2 ways:

1. Any of the supported spot frequencies can be divided to 8 kHz by setting the 'lock8K' bit (bit 6) in the appropriate *cnfg_ref_source_frequency* register location. For good jitter tolerance for all frequencies and for operation at 19.44 MHz and above, use lock8K. It is possible to choose which edge of the 8kHz input to lock to, by setting the appropriate bit of the *cnfg_control1* register.

2. Any multiple of 8 kHz between 1544 kHz to 100 MHz can be supported by using the 'DivN' feature (bit 7 of the *cnfg_ref_source_frequency* register). Any reference input can be set to use DivN independently of the frequencies and configurations of the other inputs.

Any reference input with the DivN bit set in the *cnfg_ref_source_frequency* register will employ the internal pre-divider prior to the DPLL locking. The *cnfg_freq_divn* register contains the divider ratio N where the reference input will get divided by (N+1) where $0<N<2^{14}-1$. The *cnfg_ref_source_frequency* register must be set to the closest supported spot frequency to the input frequency, but must be lower than the input frequency. When using the DivN feature the post-divider frequency must be 8 kHz, which is indicated by setting the 'lock8k' bit high (bit 6 in *cnfg_ref_source_frequency* register). Any input set to DivN must have the frequency monitors disabled (If the frequency monitors are disabled, they are disabled for all inputs regardless of the input configurations, in this case only activity monitoring will take place). Whilst any number of inputs can be set to use the DivN feature, only one N can be programmed, hence all inputs using the DivN feature must require the same division to get to 8 kHz.

Table 4. Input Reference Source Selection and Priority Table

Port Number	Channel Number	Port Type	Input Port Technology	Frequencies Supported	Default Priority
I_1	0001	T_{IN3}	AMI	64/8kHz (composite clock, 64kHz + 8kHz) Default (SONET): 64/8kHz Default (SDH): 64/8kHz	2
I_2	0010	T_{IN3}	AMI	64/8kHz (composite clock, 64kHz + 8kHz) Default (SONET): 64/8kHz Default (SDH): 64/8kHz	3
I_3	0011	T_{IN3}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 8kHz Default (SDH): 8kHz	4
I_4	0100	T_{IN3}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 8kHz Default (SDH): 8kHz	5
I_5	0101	T_{IN1}	LVDS/PECL LVDS default	Up to 155.52MHz (see Note 2) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	6
I_6	0110	T_{IN1}	PECL/LVDS PECL default	Up to 155.52MHz (see Note 2) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	7
I_7	0111	T_{IN1}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	8
I_8	1000	T_{IN1}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	9
I_9	1001	T_{IN1}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	10
I_10	1010	T_{IN1}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	11
I_11	1011	T_{IN2}	TTL/CMOS	Up to 100MHz (see Note 1) Default (Master) (SONET): 1.544MHz Default (Master) (SDH): 2.048MHz Default (Slave) 6.48MHz	12/1 (Note 3)
I_12	1100	T_{IN2}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 1.544MHz Default (SDH): 2.048MHz	13
I_13	1101	T_{IN2}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 1.544MHz Default (SDH): 2.048MHz	14
I_14	1110	T_{IN2}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 1.544MHz Default (SDH): 2.048MHz	15

Notes for Table 4.

Note 1: TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies are: 2 kHz, 4 kHz, 8 kHz (and N x 8 kHz), 1.544 MHz (SONET)/2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz. SONET or SDH is selected using the SONSDHB pin. When the SONSDHB pin is High SONET is selected, when the SONSDHB pin is Low SDH is selected.

Note 2: PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz and 311.04 MHz.

Note 3: Input port <I_11> is set at 12 on the Master SETS IC and 1 on the Slave SETS IC, as default on power up (or PORB). The default setup of Master or Slave <I_11> priority is determined by the MSTSLVB pin.

DivN examples

To lock to 2.000 MHz.

(1) The *cnfg_ref_source_frequency* register is set to 11XX0001 (binary) to set the DivN, lock8k bits, and the frequency to E1/DS1. (XX = 'leaky bucket' ID for this input).

(2) The *cnfg_mode* register (34Hex) bit 2 needs to be set to 1 to select SONET frequencies (DS1).

(3) The frequency monitors are disabled in *cnfg_monitors* register (48Hex) by writing 00 to bits 0 and 1.

(4) The DivN register is set to F9 Hex (249 decimal).

To lock to 10.000 MHz.

(1) The *cnfg_ref_source_frequency* register is set to 11XX0010 (binary) to set the DivN, lock8k bits, and the frequency to 6.48 MHz. (XX = 'leaky bucket' ID for this input).

(2) The frequency monitors are disabled in *cnfg_monitors* register (48Hex) by writing 00 to bits 0 and 1.

(3) The DivN register is set to 4E1 Hex (1249 decimal).

PECL and LVDS ports support the spot clock frequencies listed plus 155.52 MHz and 311.04 MHz. The choice of PECL or LVDS compatibility is programmed via the *cnfg_differential_inputs* register. Unused PECL/LVDS differential inputs should be fixed with one input high (VDD) and the other input low (GND), or set in LVDS mode and left floating, in which case one input is internally pulled high and the other low.

An AMI port supports a composite clock, consisting of a 64 kHz AMI clock with 8 kHz boundaries marked by deliberate violations of the AMI coding rules, as specified in ITU recommendation G.703. Departures from the nominal pattern are detected within the ACS8510, and may cause reference-switching if too frequent. See section DC Characteristics: AMI Input/Output Port, for more details. If the AMI port is unused, the pins (I1 and I2) should be tied to GND and the VAMI+ supply pin (pin 26) disconnected.

Input Wander and Jitter Tolerance

The ACS8510 is compliant to the requirements of all relevant standards, principally ITU Recommendation G.825, ANSI DS1.101-1994 and ETS 300 462-5 (1997).

All reference clock inputs have a tight frequency tolerance but a generous jitter tolerance. Pull-in, hold-in and pull-out ranges are specified for each input port in Table 5. Minimum jitter

tolerance masks are specified in Figures 3 and 4, and Tables 6 and 7, respectively. The ACS8510 will tolerate wander and jitter components greater than those shown in Figure 3 and Figure 4, up to a limit determined by a combination of the apparent long-term frequency offset caused by wander and the eye-closure caused by jitter (the input source will be rejected if the offset pushes the frequency outside the hold-in range for long enough to be detected, whilst the signal will also be rejected if the eye closes sufficiently to affect the signal purity). The '8klocking' mode should be engaged for high jitter tolerance according to these masks. All reference clock ports are monitored for quality, including frequency offset and general activity. Single short-term interruptions in selected reference clocks may not cause rearrangements, whilst longer interruptions, or multiple, short-term interruptions, will cause rearrangements, as will frequency offsets which are sufficiently large or sufficiently long to cause loss-of-lock in the phase-locked loop. The failed reference source will be removed from the priority table and declared as unserviceable, until its perceived quality has been restored to an acceptable level.

The registers *sts_curr_inc_offset* (address 0C, 0D, 07) report the frequency of the DPLL with respect to the external TCXO frequency. This is a 19 bit signed number with one LSB representing 0.0003 ppm (range of +/- 80 ppm). Reading this regularly can show how the currently locked source is varying in value e.g. due to wander on its input.

The ACS8510 performs automatic frequency monitoring with an acceptable input frequency offset range of +/- 16.6 ppm. The ACS8510 DPLL has a programmable frequency limit of +/- 80 ppm. If the range is programmed to be > 16.6 ppm, the frequency monitors should be disabled so the input reference source is not automatically rejected as out of frequency range.

Table 5. Input Reference Source Jitter Tolerance

Jitter Tolerance	Frequency Monitor Acceptance Range	Frequency Acceptance Range (Pull-in)	Frequency Acceptance Range (Hold-in)	Frequency Acceptance Range (Pull-out)
G.703	+/- 16.6 ppm	+/- 4.6 ppm (see Note 1)	+/- 4.6 ppm (see Note 1)	+/- 4.6 ppm (see Note 1)
G.783				
G.823		+/- 9.2 ppm (see Note 2)	+/- 9.2 ppm (see Note 2)	+/- 9.2 ppm (see Note 2)
GR-1244-CORE				

Notes for Table 5.

Note 1. The frequency acceptance and generation range will be +/-4.6 ppm around the required frequency when the external crystal frequency accuracy is within a tolerance of +/- 4.6 ppm.

Note 2. The fundamental acceptance range and generation range is +/- 9.2 ppm with an exact external crystal frequency of 12.8 MHz. This is the default DPLL range, the range is also programmable from 0 to 80 ppm in 0.08 ppm steps.

Figure 3. Minimum Input Jitter Tolerance (OC-3/STM-1)
(for inputs supporting G.783 compliant sources)

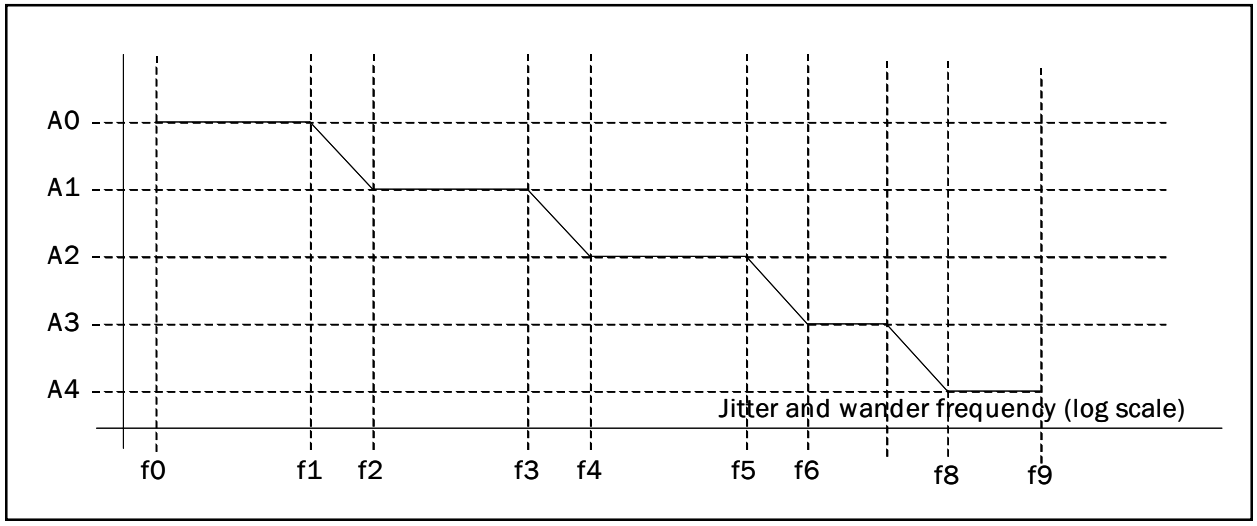


Table 6. Amplitude and Frequency Values for Jitter Tolerance

STM level	Peak to peak amplitude (unit Interval)					Frequency (Hz)									
	A0	A1	A2	A3	A4	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9
STM-1	2800	311	39	1.5	0.15	12u	178u	1.6m	15.6m	0.125	19.3	500	6.5k	65k	1.3m

Output Clock Ports

The device supports a set of main output clocks, T_{OUT0} and T_{OUT4}, and a pair of secondary output clocks, 'Frame-Sync' and 'Multi-Frame-Sync'. The two main output clocks, T_{OUT0} and T_{OUT4}, are independent of each other and are individually selectable. The two secondary output clocks, 'Frame-Sync' and 'Multi-Frame-Sync', are derived from T_{OUT0}. The frequencies of the output clocks are selectable from a range of pre-defined spot frequencies and a variety of output technologies are supported, as defined in Table 8.

Low-speed Output Clock (T_{OUT4})

The T_{OUT4} clock is supplied on two output ports, T_{O8} and T_{O9}. The former port will provide an AMI signal carrying a composite clock of 64 kHz and 8 kHz, according to ITU Recommendation G.703. The latter port will provide a TTL/CMOS signal at either 1.544 MHz or 2.048 MHz, depending on the setting of the SONSDHB pin.

High-speed Output Clock (Part of T_{OUT0})

The T_{OUT0} port has multiple outputs. Outputs T_{O1} and T_{O2} are TTL/CMOS output with a choice of 11 different frequencies up to 51.84 MHz. Outputs T_{O3} to T_{O5} are all TTL/CMOS outputs with fixed frequencies of 19.44 MHz, 38.88 MHz and 77.76 MHz respectively. Output T_{O6} is differential and can support clocks up to 155.52 MHz. Output T_{O7} is also differential and can support clocks up to 155.52 MHz. Each output is individually configured to operate at the frequencies shown in Table 8 (configuration must be consistent between ACS8510 devices for protection-switching to be effective - output clocks will be phase-aligned

Figure 4. Minimum Input Jitter Tolerance (DS1/E1)
(for inputs supporting G.783 compliant sources)

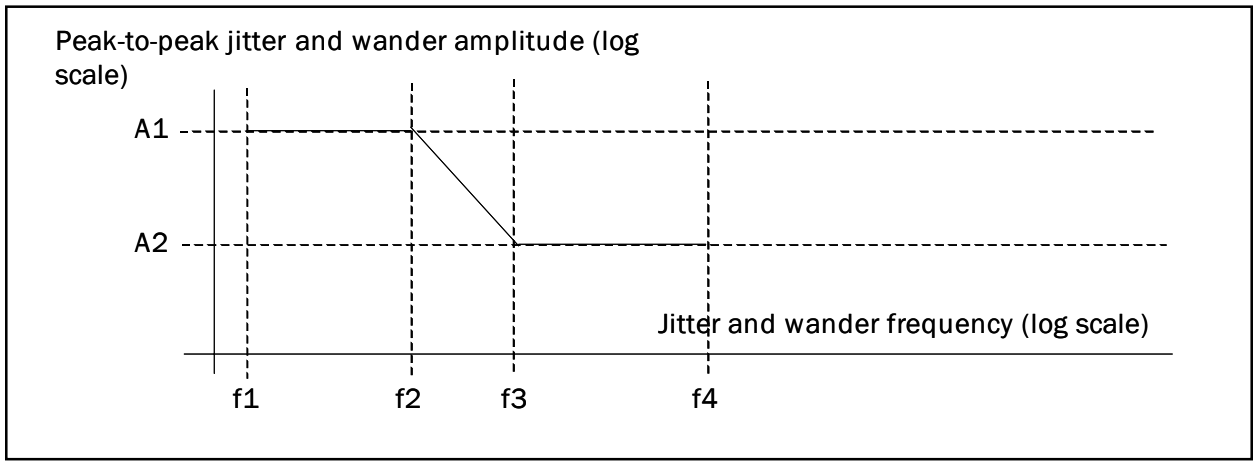


Table 7. Amplitude and Frequency Values for Jitter Tolerance

Type	Spec.	Amplitude (UI pk-pk)		Frequency (Hz)			
		A1	A2	F1	F2	F3	F4
DS1	GR-1244-CORE	5	0.1	10	500	8k	40k
E1	ITU G.823	1.5	0.2	20	2.4k	18k	100k

between devices). Using the *cnfg_differential_outputs* register, outputs T_{O6} and T_{O7} can be made to be LVDS or PECL compatible.

Frame Sync and Multi-Frame Sync Clocks (Part of T_{OUT0})

Frame Sync (8 kHz) and Multi-Frame Sync (2 kHz) clocks are provided on outputs T_{O10} (FrSync) and T_{O11} (MFrSync). The FrSync and MFrSync clocks have a 50:50 mark space ratio. These are driven from the T_{OUT0} clock. They are synchronized with their counterparts in a second ACS8510 device (if used), using the technique described later.

Low Jitter Multiple E1/DS1 Outputs

This feature added to Rev2.1 is activated using the *cnfg_control1* register. This sends a frequency of twice the Dig2 rate (see reg addr 39h, bits 7:6) to the APLL instead of the normal 77.76MHz. For this feature to be used, the Dig2 rate must only be set to 12352kHz/16384kHz using the *cnfg_T0_output_frequencies* register. The normal OC3 rate outputs are then replaced with E1/DS1 multiple rates. The E1(SONET)/DS1(SDH) selection is made in the same way as for Dig2 using the *cnfg_T0_output_enable* register. Table 9 shows the relationship between primary output frequencies and the corresponding output in E1/DS1 mode, and which output they are available from.

Output Wander and Jitter

Wander and jitter present on the output clocks are dependent on:

1. The magnitude of wander and jitter on the selected input reference clock (in Locked mode)

2. The internal wander and jitter transfer characteristic (in Locked mode)

3. The jitter on the local oscillator clock

4. The wander on the local oscillator clock (in Holdover mode)

Wander and jitter are treated in different ways to reflect their differing impacts on network design. Jitter is always strongly attenuated, whilst wander attenuation can be varied to suit the application and operating state. Wander and jitter attenuation is performed using a digital phase locked loop (DPLL) with a programmable bandwidth. This gives a transfer characteristic of a low pass filter, with a programmable pole. It is sometimes necessary to change the filter dynamics to suit particular circumstances - one example being when locking to a new source,

Table 8. Output Reference Source Selection Table

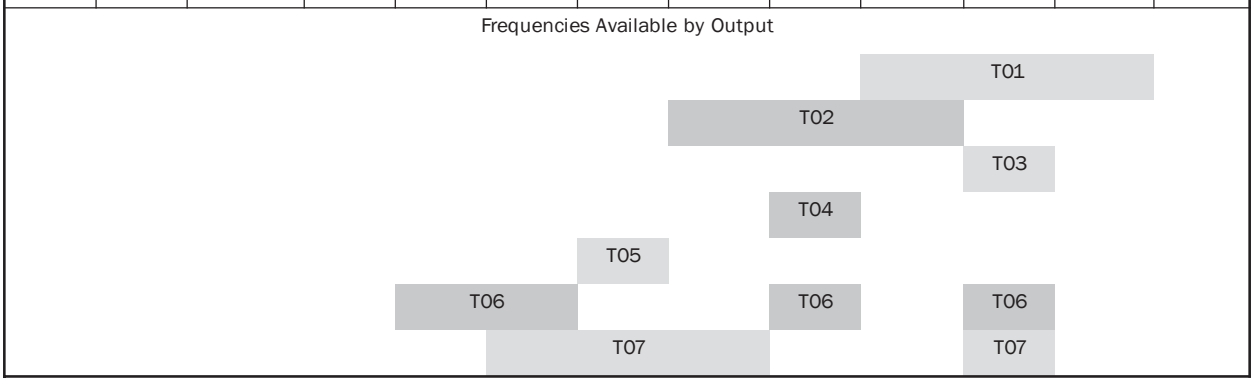
Port Name	Output Port Technology	Frequencies Supported
T_{01}	TTL/CMOS	1.544 MHz/2.048 MHz, 3.088 MHz/4.096 MHz, 6.176 MHz/8.192 MHz, 6.48 MHz (default), 12.352 MHz/16.384 MHz, 19.44 MHz, 25.92 MHz
T_{02}	TTL/CMOS	1.544 MHz/2.048 MHz, 3.088 MHz/4.096 MHz, 6.176 MHz/8.192 MHz, 12.352 MHz/16.384 MHz, 25.92 MHz, 38.88 MHz (default), 51.84 MHz
T_{03}	TTL/CMOS	19.44 MHz - fixed
T_{04}	TTL/CMOS	38.88 MHz - fixed
T_{05}	TTL/CMOS	77.76 MHz - fixed
T_{06}	LVDS/PECL (LVDS default)	1.544 MHz/2.048 MHz, 3.088 MHz/4.096 MHz, 6.176 MHz/8.192 MHz, 12.352 MHz/16.384 MHz, 19.44 MHz, 38.88 MHz (default), 155.52 MHz, 311.04 MHz
T_{07}	PECL/LVDS (PECL default)	19.44 MHz (default), 51.84 MHz, 77.76 MHz, 155.52 MHz
T_{08}	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz)
T_{09}	TTL/CMOS	1.544 MHz/2.048 MHz
T_{010}	TTL/CMOS	FrSync, 8 kHz - with a 50:50 MSR
T_{011}	TTL/CMOS	MFrSync, 2 kHz - with a 50:50 MSR

Note for Table 8.

Where 1.544 MHz/2.048 MHz is shown, 1.544 MHz is SONET, and 2.048 MHz is SDH. Pin SONSDHB controls the default frequency output. Where the SONSDHB pin is High SONET is default, and when SONSDHB pin is Low SDH is default.

Table 9. Multiple E1/DS1 Ouputs in relation to Standard Outputs

Mode	Freq to APLL	APLL Multiplier	APLL Freq	clk_ filt	clk_ filt/2	clk_ filt/4	clk_ filt/6	clk_ filt/8	clk_ filt/12	clk_ filt/16	clk_ filt/48	DPLL Freq
Default	77.76	4	311.04	311.04	155.52	77.76	51.84	38.88	25.92	19.44	6.48	77.76
n value						**16**		**8**		**4**		
n x E1	32.768	4	131.072	131.072	65.536	**32.768**	21.84533	**16.384**	10.92267	**8.192**	2.730667	77.76
n x T1	24.704	4	98.816	98.816	49.408	**24.704**	16.46933	**12.352**	8.234667	**6.176**	2.058667	77.76



the filter can be opened up to reduce locking time and can then be gradually tightened again to remove wander. Since wander represents a relatively long-term deviation from the nominal operating frequency, it affects the rate of supply of data to the network element. Strong wander attenuation limits the rate of consumption of data to within a smaller range, so a larger buffer store is required to prevent data loss. But, since any buffer store potentially increases latency, wander may often only need to be removed at specific points within a network where buffer stores are acceptable, such as at digital cross connects. Otherwise, wander is sometimes not required to be attenuated and can be passed through transparently. The ACS8510 has programmable wander transfer characteristics in a range from 0.1 Hz to 20 Hz. The wander and jitter transfer characteristic is shown in Figure 5.

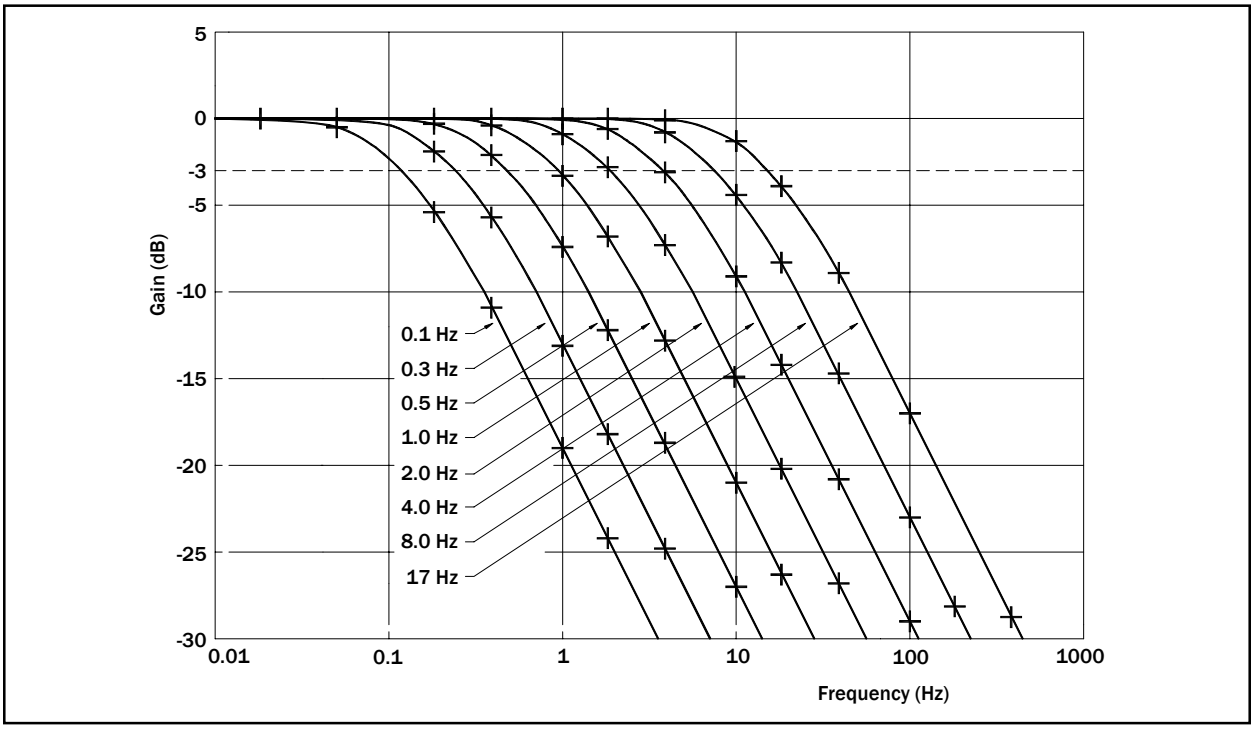
Wander on the local oscillator clock will not have significant effect on the output clock whilst in Locked mode, so long as the DPLL bandwidth is set high enough so that the DPLL can compensate quickly enough for any frequency changes in the crystal. In Free-run or Holdover mode wander on the crystal is more significant. Variation in crystal temperature or supply voltage both cause drifts in operating frequency, as does ageing. These effects must be limited by careful selection of a suitable component for the local oscillator, as specified in the section 'Local Oscillator Clock'.

Phase Variation

There will be a phase shift across the ACS8510 between the selected input reference source and the output clock. This phase shift may vary over time but will be constrained to lie within specified limits. The phase shift is characterised using two parameters, MTIE (Maximum Time Interval Error), and TDEV (Time Deviation), which, although being specified in all relevent specifications, differ in acceptable limits in each one. Typical measurements for the ACS8510 are shown in Figures 6 and 7, for Locked mode operation. Figure 8 shows a typical measurement of Phase Error accumulation in Holdover mode operation.

The required performance for phase variation during Holdover is specified in several ways depending upon the particular circumstances pertaining:

Figure 5. Wander and Jitter Measured Transfer Characteristics



1. ETSI 300 462-5, Section 9.1, requires that the short-term phase error during switchover (i.e., Locked to Holdover to Locked) be limited to an accumulation rate no greater than 0.05 ppm during a 15 second interval.

2. ETSI 300 462-5, Section 9.2, requires that the long-term phase error in the Holdover mode should not exceed

$$\{(a1+a2)S+0.5bS^2+c\}$$

where

a1 = 50 ns/s (allowance for initial frequency offset)

a2 = 2000 ns/s (allowance for temperature variation)

b = 1.16×10^{-4} ns/s^2 (allowance for ageing)

c = 120 ns (allowance for entry into Holdover mode).

3. ANSI Tin1.101-1994, Section 8.2.2, requires that the phase variation be limited so that no more than 255 slips (of 125 µs each) occur during the first day of Holdover. This requires a frequency accuracy better than:

((24x60x60)+(255x125µs))/(24x60x60) = 0.37 ppm

Temperature variation is not restricted, except to within the normal bounds of 0 to 50 °C.

4. Telcordia GR.1244.CORE, Section 5.2., Table 4, shows that an initial frequency offset of 50 ppb is permitted on entering Holdover, whilst a drift over temperature of 280 ppb is allowed; an allowance of 40 ppb is permitted for all other effects.

5. ITU G.822, Section 2.6, requires that the slip rate during category(b) operation (interpreted as being applicable to Holdover mode operation) be limited to less than 30 slips (of 125 µs each) per hour

((((60 x 60)/30)+125µs)/(60x60)) = 1.042 ppm

Figure 6. Maximum Time Interval Error of T_{OUT0} output port

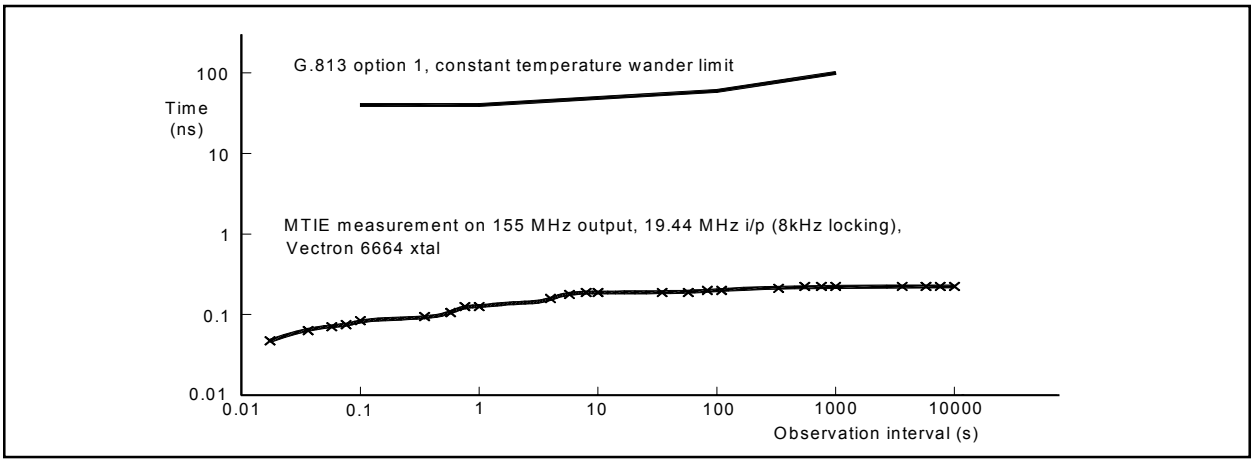


Figure 7. Time Deviation of T_{OUT0} output port

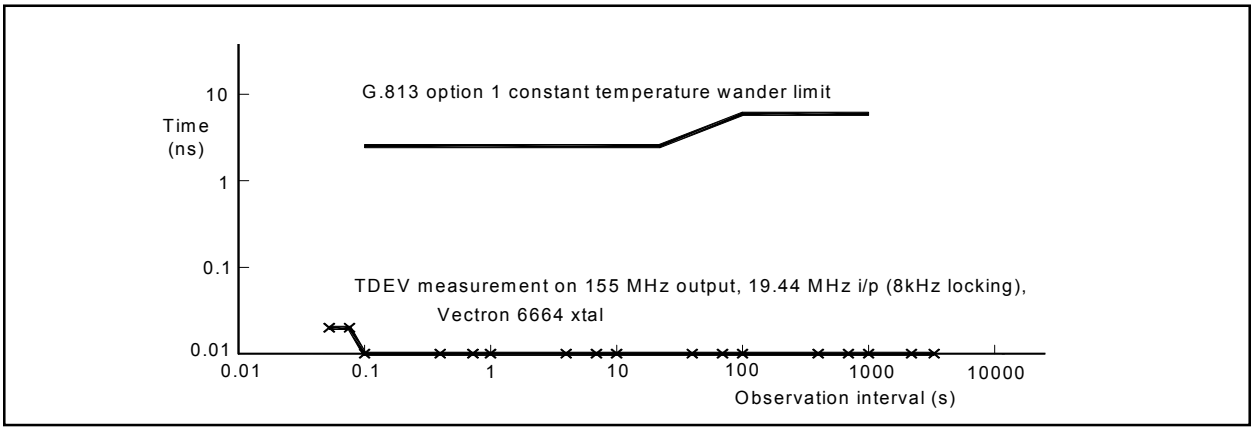
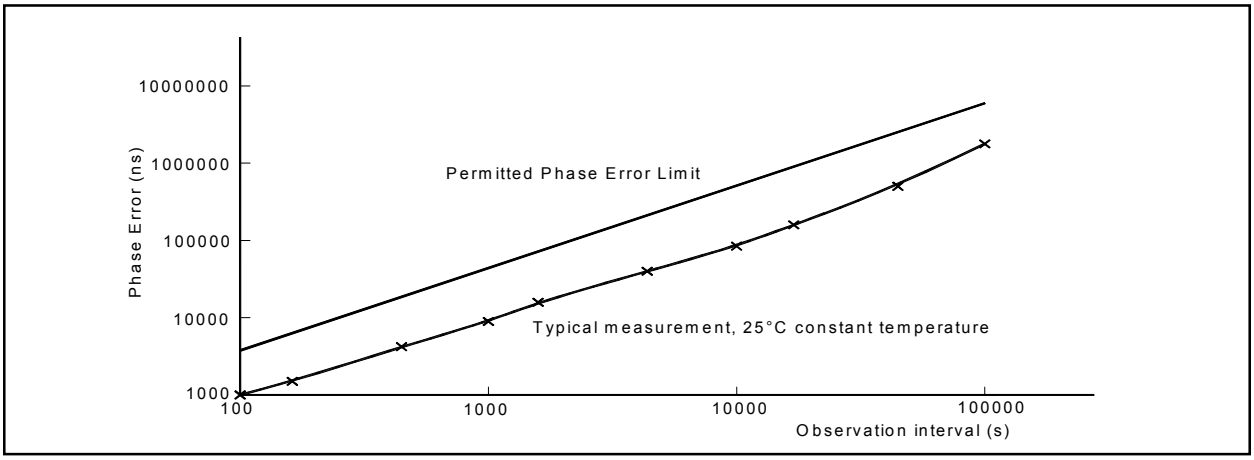


Figure 8. Phase error accumulation of T_{OUT0} output port in Holdover mode



Phase Build Out

Phase Build Out (PBO) is the function to minimise phase transients on the output SEC clock during input reference switching. If the currently selected input reference clock source is lost (due to a short interruption, out of frequency detection, or complete loss of reference), the second, next highest priority reference source will be selected. During this transition, the Lost_Phase mode is entered.

The typical phase disturbance on clock reference source switching will be less than 12 ns on the ACS8510. For clock reference switching caused by the main input failing or being disconnected, then the phase disturbance on the output will still be less than the 120 ns allowed for in the G.813 spec. The actual value is dependent on the frequency being locked to.

ITU-T G.813 states that the max allowable short term phase transient response, resulting from a switch from one clock source to another, with Holdover mode entered in between, should be a maximum of 1 µs over a 15 second interval. The maximum phase transient or jump should be less than 120 ns at a rate of change of less than 7.5 ppm and the Holdover performance should be better than 0.05 ppm.

On the ACS8510, PBO can be enabled, disabled or frozen using the µP interface. By default, it is enabled. When PBO is enabled, it can also be frozen, which will disable the PBO operation on the next input reference switch, but will remain with the current offset. If PBO is disabled while the device is in the Locked mode, there will be a phase jump on the output SEC clocks as the DPLL locks back to 0 degree phase error.

Microprocessor Interface

The ACS8510 incorporates a microprocessor interface, which can be configured for the following modes via the bus interface mode control pins UPSEL(2:0) as defined in Table 10.

Table 10. Microprocessor Interface Mode Selection

UPSEL(2:0)	Mode	Description
111 (7)	OFF	Interface disabled
110 (6)	OFF	Interface disabled
101 (5)	SERIAL	Serial uP bus interface
100 (4)	MOTOROLA	Motorola interface
011 (3)	INTEL	Intel compatible bus interface
010 (2)	MULTIPLEXED	Multiplexed bus interface
001 (1)	EPROM	EPROM read mode
000 (0)	OFF	Interface disabled

Motorola Mode

Parallel data + address: this mode is suitable for use with Motorola's 68x0 type bus.

Intel Mode

Parallel data + address: this mode is suitable for use with Intel's 80x86 type bus.

Multiplexed Mode

Data/address: this mode is suitable for use with microprocessors which share bus signals between address and data (e.g., Intel's 80x86 family).

Serial Mode

This mode is suitable for use with micro-processor which use a serial interface.

EPROM Mode

This mode is suitable for simple standalone applications where it is required to change the default loading of the register values to suit different applications.

This can be done by loading values from an external ROM. The data is read from the ROM automatically after power up when the UPSEL(2:0) pins are set to '001'. Each register value is stored sequentially, with ROM address 0 corresponding to register address 0 and so on.

The value in the 'chip_id' location (address 00 & 01) is checked to see if it matches the ID number of the ACS8510 V2 (value 213E). Upon a successful number match, the remaining data

from the ROM is used to set the internal register values. Only 64 locations in the ROM are required.

Register Set

All registers are 8-bits wide, organised with the most-significant bit positioned in the left-most bit, with bit significance decreasing towards the right most bit. Some registers carry several individual data fields of various sizes, from single-bit values (e.g. flags) upwards. Several data fields are spread across multiple registers; their organisation is shown in the register map, Table 11.

Configuration Registers

Each configuration register reverts to a default value on power-up or following a reset. Most default values are fixed, but some will be pin-settable. All configuration registers can be read out over the microprocessor port.

Status Registers

The Status Registers contain readable registers. They may all be read from outside the chip but are not writeable from outside the chip (except for a clearing operation). All status registers are read via shadow registers to avoid data hits due to dynamic operation. Each individual status register has a unique location.

Register Access

Most registers are of one of two types, configuration registers or status registers, the exceptions being the *chip_ID* and *chip_revision* registers. Configuration registers may be written to or read from at any time (the complete 8-bit register must be written, even if only one bit is being modified). All status registers may be read at any time and, in some status registers (such as the *sts_interrupts* register), any individual data field may be cleared by writing a '1' into each bit of the field (writing a '0' value into a bit will not affect the value of the bit). A description of each register is given in the Register Map, and Register Map Description.

Interrupt Enable and Clear

Interrupt requests are flagged on pin INTREQ (active High). Bits in the interrupt status register are set (high) by the following conditions:

1. Any reference source becoming valid or going invalid

2. A change in the operating state (eg. Locked, Holdover etc.)

3. A brief loss of the currently selected reference source

4. An AMI input error

All interrupt sources are maskable via the mask register, each one being enabled by writing a '1' to the appropriate bit. Any unmasked bit set in the interrupt status register will cause the interrupt request pin to be asserted (high). All interrupts are cleared by writing a '1' to the bit(s) to be cleared in the status register. When all pending unmasked interrupts are cleared the interrupt pin will go inactive (low).

The loss of the currently selected reference source will eventually cause the input to be considered invalid, triggering an interrupt. The time taken to raise this interrupt is dependant on the leaky bucket configuration of the activity monitors. The fastest leaky bucket setting will still take up to 128 ms to trigger the interrupt. The interrupt caused by the brief loss of the currently selected reference source is provided to facilitate very fast source failure detection if desired. It is triggered after missing just a couple of cycles of the reference source. Some applications require the facility to switch downstream devices based on the status of the reference sources. In order to provide extra flexibility, it is possible to flag the 'main reference failed' interrupt (addr 06, bit 6) on the pin TDO. This is simply a copy of the status bit in the interrupt register and is independent of the mask register settings. The bit is reset by writing to the interrupt status register in the normal way. This feature can be enabled and disabled by writing to bit 6 of register 48Hex.

Register Map

Shaded areas in the map are 'don't care' and writing either 0 or 1 will not affect any function of the device.

Bits labelled 'Set to 0' or 'Set to 1' must be set as stated during initialisation of the device, either following power up, or after a power on reset (POR). Failure to correctly set these bits may result in the device operating in an unexpected way.

Some registers do not appear in this list. These are either not used, or have test functionality. Do not write to any undefined registers as this may cause the device to operate in a test mode. If an undefined register has been inadvertently addressed, the device should be reset to ensure the undefined registers are at default values.

Table 11. Register Map

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
00	chip_id (read only)	Device part number (7:0)							
01		Device part number (15:8)							
02	chip_revision (read only)	Chip revision number (7:0)							
03	cnfg_control1 (read/write)			Multiple E1/T1 O/P	Analog div sync	Set to '0'	8k Edge Polarity	Set to '0'	Set to '0'
04	cnfg_control2 (read/write)			Phase loss flag limit			Set to '0'	Set to '1'	Set to '0'
05	sts_interrupts (read/write)	<I_8> valid change	<I_7> valid change	<I_6> valid change	<I_5> valid change	<I_4> valid change	<I_3> valid change	<I_2> valid change	<I_1> valid change
06		Operating mode	Main ref. failed	<I_14> valid change	<I_13> valid change	<I_12> valid change	<I_11> valid change	<I_10> valid change	<I_9> valid change
08	sts_T4_inputs (read/write)				T4 ref failed	Ami2 Violation	Ami2 L.O.S.	Ami1 Violation	Ami1 L.O.S.
09	sts_operating_mode (read only)						Operating mode (2:0)		
0A	sts_priority_table (read only)	Highest priority valid source				Currently selected reference source			
0B		3rd highest priority valid source				2nd highest priority valid source			
0C	sts_curr_inc_offset (read only)	Current increment offset (7:0)							
0D		Current increment offset (15:8)							
07							Current increment offset (18:16)		
0E	sts_sources_valid (read only)	<I_8>	<I_7>	<I_6>	<I_5>	<I_4>	<I_3>	<I_2>	<I_1>
0F				<I_14>	<I_13>	<I_12>	<I_11>	<I_10>	<I_9>

Table 11. Register Map (continued).

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
10	sts_reference_sources (read/write)	status <I_2>				status <I_1>			
11		status <I_4>				status <I_3>			
12		status <I_6>				status <I_5>			
13		status <I_8>				status <I_7>			
14		status <I_10>				status <I_9>			
15		status <I_12>				status <I_11>			
16		status <I_14>				status <I_13>			
18	cnfg_ref_selection_priority (read/write)	programmed_priority <I_2>				programmed_priority <I_1>			
19		programmed_priority <I_4>				programmed_priority <I_3>			
1A		programmed_priority <I_6>				programmed_priority <I_5>			
1B		programmed_priority <I_8>				programmed_priority <I_7>			
1C		programmed_priority <I_10>				programmed_priority <I_9>			
1D		programmed_priority <I_12>				programmed_priority <I_11>			
1E		programmed_priority <I_14>				programmed_priority <I_13>			
20	cnfg_ref_source_frequency (read/write)	divn	lock8k	bucket_id <I_1>(1:0)		reference_source_frequency <I_1>(3:0)			
21		divn	lock8k	bucket_id <I_2>(1:0)		reference_source_frequency <I_2>(3:0)			
22		divn	lock8k	bucket_id <I_3>(1:0)		reference_source_frequency <I_3>(3:0)			
23		divn	lock8k	bucket_id <I_4>(1:0)		reference_source_frequency <I_4>(3:0)			
24		divn	lock8k	bucket_id <I_5>(1:0)		reference_source_frequency <I_5>(3:0)			
25		divn	lock8k	bucket_id <I_6>(1:0)		reference_source_frequency <I_6>(3:0)			
26		divn	lock8k	bucket_id <I_7>(1:0)		reference_source_frequency <I_7>(3:0)			
27		divn	lock8k	bucket_id <I_8>(1:0)		reference_source_frequency <I_8>(3:0)			
28		divn	lock8k	bucket_id <I_9>(1:0)		reference_source_frequency <I_9>(3:0)			
29		divn	lock8k	bucket_id <I_10>(1:0)		reference_source_frequency <I_10>(3:0)			
2A		divn	lock8k	bucket_id <I_11>(1:0)		reference_source_frequency <I_11>(3:0)			
2B		divn	lock8k	bucket_id <I_12>(1:0)		reference_source_frequency <I_12>(3:0)			
2C		divn	lock8k	bucket_id <I_13>(1:0)		reference_source_frequency <I_13>(3:0)			
2D		divn	lock8k	bucket_id <I_14>(1:0)		reference_source_frequency <I_14>(3:0)			

Table 11. Register Map (continued).

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
30	cnfg_sts_remote_sources_valid (read/write)	Remote status, channels <8:1>							
31				Remote status, channels <14:9>					
32	cnfg_operating_mode (read/write)						Forced operating mode		
33	cnfg_ref_selection (read/write)					force_select_reference_source			
34	cnfg_mode (read/write)	Auto external 2K enable	Phase alarm timeout enable	Clock edge	Holdover Offset enable	External 2K Sync enable	SONET/ SDH I/P	Master/ Slave	Reversion mode
35	cnfg_T4 (read/write)			Squelch	Select T0/T1	Force T1 input source selection (only valid for inputs I_5 to I_10)			
36	cnfg_differential_inputs (read/write)							<I_6> PECL	<I_5> PECL
37	cnfg_uPsel_pins (read only)						Micro-processor type		
38	cnfg_T0_output_enable (read/write)	311.04MHz on T06	1=SONET 0=SDH for Dig2	1=SONET 0=SDH for Dig1	T01	T02	T03 19.44MHz	T04 38.88MHz	T05 77.76MHz
39	cnfg_T0_output_frequencies (read/write)	Digital2		Digital1		T02		T01	
3A	cnfg_differential_outputs (read/write)	T07 Frequency selection		T06 Frequency selection		T07 LVDS enable	T07 PECL enable	T06 LVDS enable	T06 PECL enable
3B	cnfg_bandwidth (read/write)	Auto b/w switch Acq/lock	Acquisition bandwidth			Set to '0'	Normal/locked bandwidth		
3C	cnfg_nominal_frequency (read/write)	Nominal frequency (7:0)							
3D		Nominal frequency (15:8)							
3E	cnfg_holdover_offset (read/write)	Holdover offset (7:0)							
3F		Holdover offset (15:8)							
40		Auto Holdover Averaging					Holdover offset (18:16)		
41	cnfg_freq_limit (read/write)	DPLL Frequency offset limit (7:0)							
42								DPLL Frequency offset limit (9:8)	
43	cnfg_interrupt_mask (read/write)	<I_8> valid change	<I_7> valid change	<I_6> valid change	<I_5> valid change	<I_4> valid change	<I_3> valid change	<I_2> valid change	<I_1> valid change
44		Operating mode	Main ref. failed	<I_14> valid change	<I_13> valid change	<I_12> valid change	<I_11> valid change	<I_10> valid change	<I_9> valid change
45					T4 ref	Ami2 Violation	Ami2 L.O.S	Ami1 Violation	Ami1 L.O.S
46	cnfg_freq_divn (read/write)	Divide-input-by-n ratio (7:0)							
47				Divide-input-by-n ratio (13:8)					