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ACS8514 SETS Buddy

Synchronous Equipment Timing Source Partner IC for 2nd T4 DPLL, Accurate Monitoring & Input Extender

ADVANCED COMMS & SENSING **FINAL** **DATASHEET**

Description

The ACS8514 is an optional partner integrated circuit for applications using the ACS8520/30. It adds an additional BITS clock (T4 path) DPLL to a clock synchronization system, for applications needing two T4 paths (e.g. to GR-253 figure 5-21).

An alternative use for this DPLL is as an input extender such that the ACS8514 automatically selects one of 14 clock sources, its output then feeds the ACS8530/20 which can also select another 13 sources, giving a total input selection range of 27 sources. An additional 13 sources can be added for each ACS8514 added.

An additional highly accurate phase and frequency monitor is also available that can be used to carry out more detailed analysis of standby clock reference sources. This extra monitor is actually another DPLL which under software control could be set to sequentially analyze each input. It can check phase from 0.7° to 23000° and frequency from 0.0003ppm to 80 ppm. An approximate MTIE measurement could be calculated for each reference input as an extra quality check.

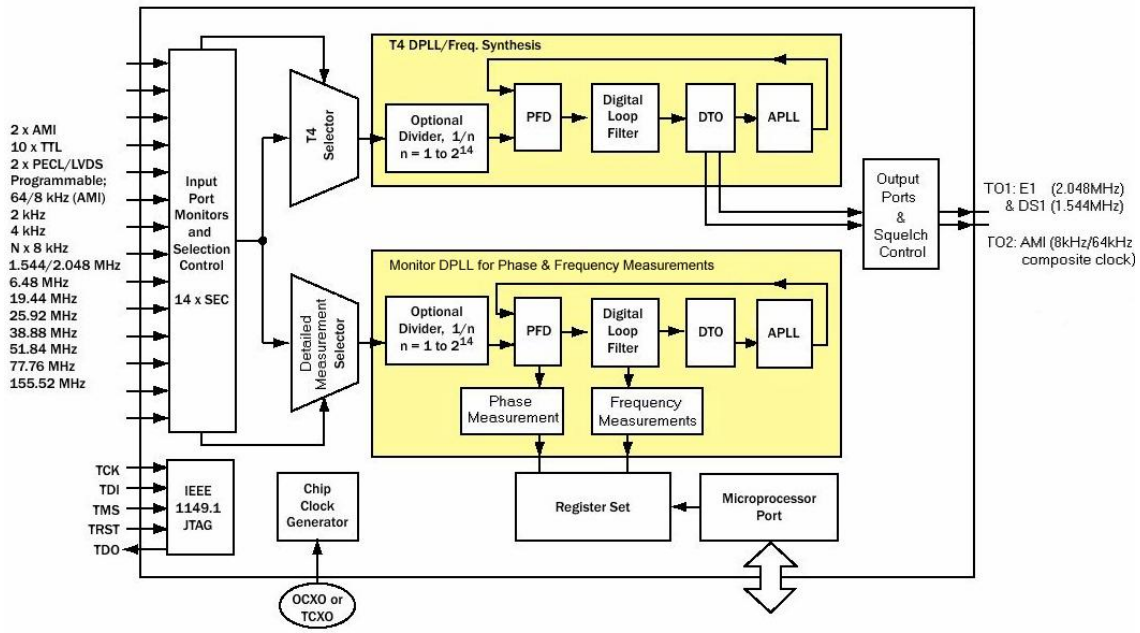
Simultaneous activity and coarse frequency monitoring of all input sources is performed in the same way as on the ACS8520/30. These can be used to automatically qualify and select sources for the extra T4 path or for input selection for the ACS8520/30 when the ACS8514 is used as an input extender.

Features

- Partner to the ACS8520 & ACS8530 for use in SONET Minimum Clock (SMC) or SONET/SDH Equipment Clock (SEC) applications, to provide :
- One Extra independent T4 path for those systems being designed to Figure 5-21 of Bellcore GR253[17],
- An additional DPLL for accurate phase, average phase, frequency and average frequency measuring of any clock source.
- Phase measurement accuracy to 0.7 degrees.
- Frequency measurement accuracy to $3x10^{-10}$
- Aids in enhancing Phase Build-out performance to absorb phase disturbances when switching between noisy input sources, via s/w control.
- Provides the facility to have long term frequency measuring and averaging for BOTH the main and any standby clock source so that the holdover frequency is always accurate for both main and standby clock selections.
- Accepts 14 individual input reference clocks, all with robust input clock source quality monitoring.
- Microprocessor interface - Intel, Motorola, Serial, Multiplexed, or boot from EPROM
- IEEE 1149.1[5] JTAG Boundary Scan
- Single 3.3 V operation. 5 V tolerant
- Lead (Pb)-free version available (ACS8514T), RoHS and WEEE compliant

Block Diagram

Figure 1 Block Diagram of the ACS8514 SETS Buddy



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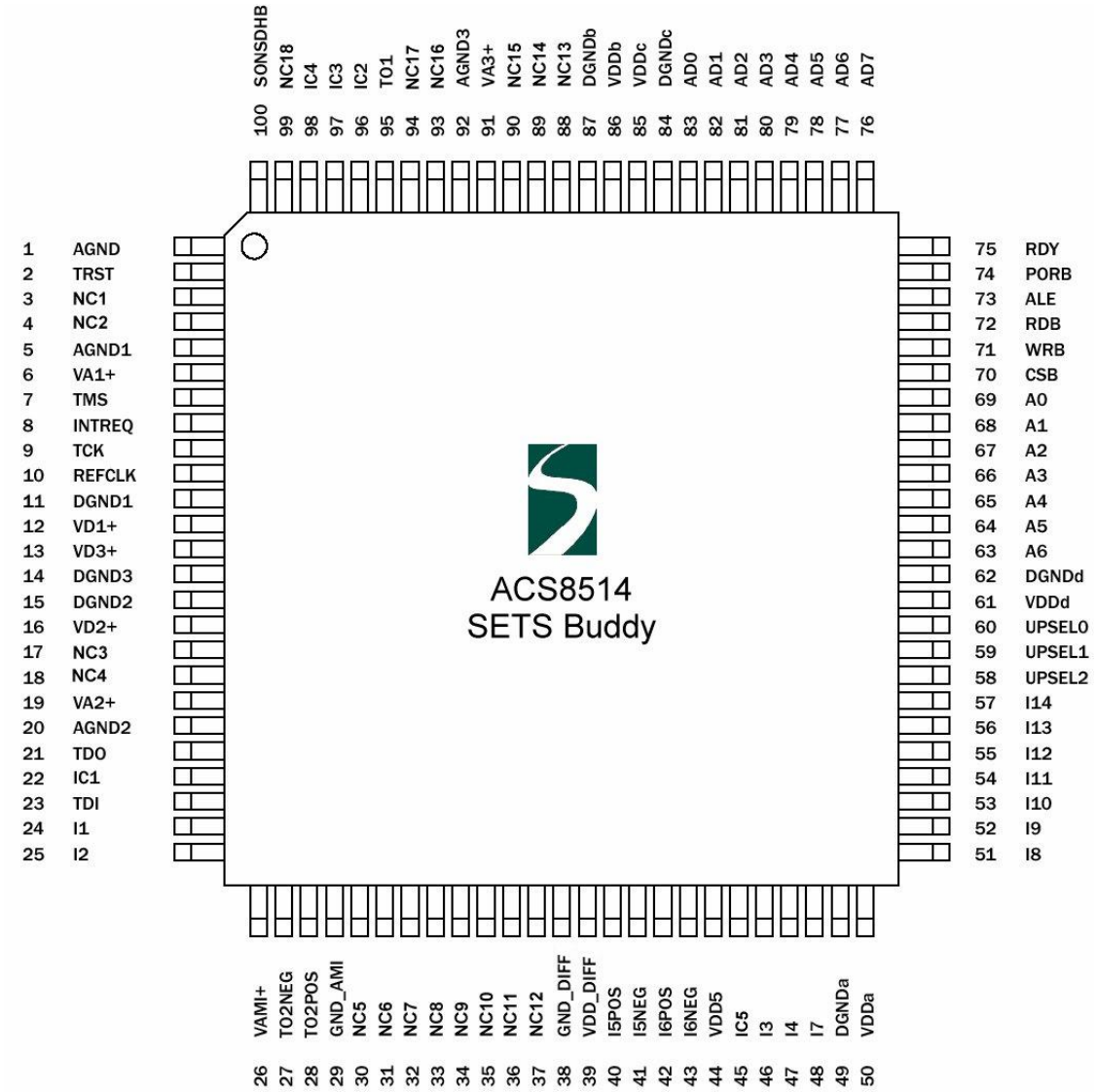
Pin Diagram

Figure 2 ACS8514 Pin Diagram



Pin Description

Table 1 Power Pins

Pin Number	Symbol	I/O	Type	Description
12, 13, 16	VD1+, VD3+, VD2+	P	-	Supply voltage: Digital supply to gates in analog section, +3.3 Volts ± 10%.
26	VAMI+	P	-	Supply voltage: Digital supply to AMI output, +3.3 Volts ± 10%.
39	VDD_DIFF	P	-	Supply voltage: Digital supply for differential ports, +3.3 Volts ± 10%.
44	VDD5	P	-	VDD5: Digital supply for +5 Volts tolerance to input pins. Connect to +5 Volts (± 10%) for clamping to +5 Volts. Connect to VDD for clamping to +3.3 Volts. Leave floating for no clamping, input pins tolerant up to +5.5 Volts.
50, 61, 85, 86	VDDa, VDDd, VDDc, VDDb	P	-	Supply voltage: Digital supply to logic, +3.3 Volts ± 10%.
6	VA1+	P	-	Supply voltage: Analog supply to clock multiplying PLL, +3.3 Volts ± 10%.
19, 91	VA2+, VA3+	P	-	Supply voltage: Analog supply to output PLLs, +3.3 Volts ± 10%.
11, 14, 15,	DGND1, DGND3, DGND2,	P	-	Supply Ground: Digital ground for components in PLLs.
49, 62, 84, 87	DGNDa,DGNDd, DGNDc,DGNDb	P	-	Supply Ground: Digital ground for logic.
29	GND_AMI	P	-	Supply Ground: Digital ground for AMI output.
38	GND_DIFF	P	-	Supply Ground: Digital ground for differential ports.
1, 5, 20, 92	AGND, AGND1, AGND2, AGND3	P	-	Supply Ground: Analog grounds.

Note: I = Input, O = Output, P = Power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor.

Table 2 Internally Connected Pins

Pin Number	Symbol	I/O	Type	Description
22, 45, 96, 97, 98	IC1 - IC5	-	-	Internally Connected: Leave to Float.

Table 3 Not connected Pins

Pin Number	Symbol	I/O	Type	Description
3, 4, 17, 18, 30-37, 88–90, 93, 94, 99	NC1 – NC18	-	-	Not Connected Internally : Leave to float or connect to gnd advised, but may be routed over if necessary.

Table 4 Other Pins

Pin Number	Symbol	I/O	Type	Description
2	TRST	I	TTL D	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 for Boundary Scan stand-by mode, still allowing correct device operation. If not used connect to GND or leave floating.
7	TMS	I	TTL U	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
8	INTREQ	O	TTL/CMOS	Interrupt Request: Active high/low software Interrupt output.
9	TCK	I	TTL D	JTAG Clock: Boundary Scan clock input. If not used connect to GND or leave floating.
10	REFCLK	I	TTL	Reference Clock: 12.8 MHz (refer to section headed Local Oscillator Clock).
21	TDO	O	TTL/CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK. If not used leave floating.
23	TDI	I	TTL U	JTAG Input: Serial test data Input. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
24	I1	I	AMI	Input reference 1: Composite clock 64 kHz + 8 kHz.
25	I2	I	AMI	Input reference 2: Composite clock 64 kHz + 8 kHz.
27	TO2NEG	O	AMI	Output reference 8: Composite clock, 64 kHz + 8 kHz negative pulse.
28	TO2POS	O	AMI	Output reference 8: Composite clock, 64 kHz + 8 kHz positive pulse.
40, 41	I5POS, I5NEG	I	LVDS/PECL	Input reference 5: Programmable, default 19.44 MHz, default type LVDS.
42, 43	I6POS, I6NEG	I	PECL/LVDS	Input reference 6: Programmable, default 19.44 MHz, default type PECL.
46	I3	I	TTL D	Input reference 3: Programmable, default 8 kHz.
47	I4	I	TTL D	Input reference 4: Programmable, default 8 kHz.
48	I7	I	TTL D	Input reference 7: Programmable, default 19.44 MHz.
51	I8	I	TTL D	Input reference 8: Programmable, default 19.44 MHz.
52	I9	I	TTL D	Input reference 9: Programmable, default 19.44 MHz.
53	I10	I	TTL D	Input reference 10: Programmable, default 19.44 MHz.
54	I11	I	TTL D	Input reference 11: Programmable, default (Master mode) 1.544/2.048 MHz, default (Slave mode) 6.48 MHz.
55	I12	I	TTL D	Input reference 12: Programmable, default 1.544/2.048 MHz.
56	I13	I	TTL D	Input reference 13: Programmable, default 1.544/2.048 MHz.
57	I14	I	TTL D	Input reference 14: Programmable, default 1.544/2.048 MHz.
58 - 60	UPSEL(2:0)	I	TTL D	Microprocessor select: Configures the interface for a particular microprocessor type at reset.
63 - 69	A(6:0)	I	TTL D	Microprocessor Interface Address: Address bus for the microprocessor interface registers. A(0) is SDI in Serial mode - output in EPROM mode only.

Table 4 Other Pins (continued)

Pin Number	Symbol	I/O	Type	Description
70	CSB	I	TTL U	Chip Select (Active Low): This pin is asserted Low by the microprocessor to enable the microprocessor interface - output in EPROM mode only.
71	WRB	I	TTL U	Write (Active Low): This pin is asserted Low by the microprocessor to initiate a write cycle. In Motorola mode, WRB = 1 for Read.
72	RDB	I	TTL U	Read (Active Low): This pin is asserted Low by the microprocessor to initiate a read cycle.
73	ALE	I	TTL D	Address Latch Enable: This pin becomes the address latch enable from the microprocessor. When this pin transitions from High to Low, the address bus inputs are latched into the internal registers. ALE = SCLK in Serial mode.
74	PORB	I	TTL U	Power On Reset: Master reset. If PORB is forced Low, all internal states are reset back to default values.
75	RDY	O	TTL/CMOS	Ready/Data acknowledge: This pin is asserted High to indicate the device has completed a read or write operation.
76 - 83	AD(7:0)	IO	TTL D	Address/Data: Multiplexed data/address bus depending on the microprocessor mode selection. AD(0) is SDO in Serial mode.
95	TO1	O	TTL/CMOS	Output reference 9: 1.544/2.048 MHz, as per ITU G.783[9] BITS requirements.
100	SONSDHB	I	TTL D	SONET or SDH frequency select: Sets the initial power up state (or state after a PORB) of the SONET/SDH frequency selection registers, see register address 34h, Bit 2 and address 38h, Bit 5 & 6 and address 64h, bit 4. When set *Low*, SDH rates are selected (2.048 MHz etc.) and when set *High*, SONET rates are selected (1.544 MHz etc.) The register states can be changed after power up by software.

Introduction

The ACS8514 is a highly integrated multiple phase lock loop device designed to partner the ACS8530 and ACS8520 SETS (Synchronous Equipment Timing Source) ICs. It specifically provides one additional BITS / T4 Path to allow a complete clock synchronization system to have two totally independent T4 paths and one T0 path, for those systems constructed to exactly match the configuration as defined in GR253 figure 5-21.

The electrical interfaces for input clocks, configurations and micro-processor interfaces are identical to the ACS8520/30. This allows the same processor interface pins to be shared with this part, with the correct part accessed by using a separate chip select.

All 14 input clocks and the 12.8 MHz TCXO/OCXO system clock can also be shared via parallel connections.

An alternative use for this part is as an input extender for those systems requiring a selection of more than 14 inputs, or more inputs of a particular electrical interface type. The 14 in-built activity monitors and frequency monitors can automatically qualify an input clock and select that clock based on a preset priority. The T4 DPLL output can then be fed on to the ACS8520/30 for subsequent selection according to its priority tables, as required.

The third main set of functions that this part brings to a system is the capability to very precisely measure the phase and frequency at the inputs. Another independently controlled 'monitor DPLL' can be used for this function. This precise measurement capability can measure phase to a 0.7 degrees accuracy with a range up to 23000° degrees and frequency to 0.3 parts per billion (3×10^{-10}), this is in addition to the activity monitoring and coarse frequency monitoring that occurs simultaneously on each of the 14 input pins to a 3.9 ppm frequency accuracy. The measured phase values may be used to give a TIE (Time Interval Error), MTIE (Maximum TIE) and TDEV (Time Deviation) quality assessment of each input using appropriate external software. The phase and frequency measurement DPLL, the Monitor DPLL, can be set to a range of loop bandwidths, down to 0.5 mHz. The phase of an input is measured with respect to the Monitor DPLL output, so varying the DPLL's bandwidth has the effect of changing the maximum observation time for the TIE measurements. A TIE observation period of up to approximately 2000 seconds is allowed for with the 0.5 mHz bandwidth.

Longer observation time measurements of TIE, MTIE and TDEV can be made by using the T4 DPLL since the T4 phase detectors can be configured to measure the phase difference between two independent inputs. This means that there is no limit to the maximum observation time that can be measured.

A Digital Phase Locked Loop (DPLL) incorporating direct digital synthesis (DDS) is used in the device in order to perform frequency translation. This enables the ACS8514 to have overall PLL characteristics that are very stable and consistent, compared to traditional analog PLLs.

In the absence of any input clock after power up the ACS8514 will free-run and generate a stable, low-noise clock signal at a frequency to the same accuracy as the external 12.8 MHz TCXO or OCXO, or it can be made more accurate via software calibration to 0.02 ppm.

Once an input clock source becomes available and is measured and found to be of a good quality, the T4 DPLL will lock to the source with the highest priority (number 1 is the highest priority in the priority table). If all sources subsequently fail then either the last source frequency is held on the T4 DPLL output (holdover) or the output may be automatically turned off (squelched) depending on configuration.

An internal analog PLL (APLL) is used in the feedback path of the DPLLs in order to eliminate digital sampling effect uncertainty at the DPLL PFDs (Phase and Frequency Detectors).

The ACS8514 includes a multi-standard microprocessor port, providing access to the configuration and status registers for device setup and monitoring.

General Description

Overview

The following description refers to the Block Diagram (Figure 1 on page 1).

The ACS8514 SETS device has 14 input clocks and generates 2 output clocks derived from the T4 DPLL path. Of the 14 input references, two are AMI composite clock, two are LVDS/PECL and the remaining ten are TTL/CMOS compatible inputs. All the TTL/CMOS are 3 V and 5 V compatible (with clamping if required by connecting the VDD5 pin). The AMI inputs are ±1 V typically, A.C. coupled. Refer to the electrical characteristics section for more information on the electrical compatibility and details. Input frequencies supported range from 2 kHz to 155.52 MHz.

Common E1, DS1, OC3 and sub-divisions are supported as spot frequencies that the DPLLs will directly lock to. Any input frequency, up to 100 MHz, that is a multiple of 8 kHz, can also be locked to via an inbuilt programmable divider.

An input reference monitor is assigned to each of the 14 inputs. The monitors operate continuously such that at all times the status of all of the inputs to the device is known. Each input can be monitored for both frequency and activity, activity alone, or the monitors can be disabled.

The frequency monitors have a "hard" (rejection) alarm limit and a "soft" (flag only) alarm limit for monitoring frequency. Each input reference can be programmed with a priority number allowing references to be chosen according to the highest priority valid input. The input selection can operate in either automatic mode or external manual source selection mode.

The T4 PLL path supports the following features:

- Automatic source selection according to input priorities and quality level.
- Different quality levels (activity alarm thresholds) for each input
- Variable bandwidth (18, 35 or 70 Hz), lock range (0 – 80 ppm) and damping factor.
- Direct PLL locking to common SONET/SDH input frequencies or any multiple of 8 kHz
- Automatic locking to an available source and either squelch or holdover mode when no source.
- Fast detection on input failure.
- Output holds last frequency (holdover) or output squelch when all input sources failed.
- Frequency translation between input and output rates via direct digital synthesis
- High accuracy digital architecture for stable PLL dynamics..
- Ability to measure a phase difference between two inputs.
- Analog PLL (APLL) used in the feedback path to avoid digital sampling / aliasing effects.

Either external software or an internal state machine controls the T4 DPLL source selection based on input quality and priority.

Input Reference Clock Ports

Table 4 gives details of the input reference ports, showing the input technologies and the range of frequencies supported on each port; the default spot frequencies and default priorities assigned to each port on power-up or by reset are also shown. Note that SDH and SONET networks use different default frequencies; the network type is pin-selectable (using either the SONSDHB pin or via software). Specific frequencies and priorities are set by configuration.

SDH and SONET networks use different default frequencies; the network type is selectable using the register bit *ip_sonsdhb*, at address 34, bit 2.

- For SONET, *ip_sonsdhb* = 1
- For SDH, *ip_sonsdhb* = 0

On power-up or by reset, the default will be set by the state of the SONSDHB pin (pin 100).

The specific frequency selection is programmed via the *cnfg_ref_source* registers (addresses 22 to 2D).

Locking Frequency Modes

There are three locking frequency modes that can be configured: Direct Lock, Lock 8k and DivN.

Direct Lock Mode

In Direct Lock Mode, the internal DPLL can lock to the selected input at the spot frequency of the input, for example 19.44 MHz performs the DPLL phase comparisons at 19.44 MHz.

In Lock8K and DivN modes (and for special case of 155 MHz), an internal divider is used prior to the DPLL to divide the input frequency before it is used for phase comparisons in the DPLL.

Lock8K Mode

Lock8K mode automatically sets the divider parameters to divide the input frequency down to 8 kHz. Lock8K can only be used on the supported spot frequencies (see Table 1, note 0). Lock8k mode is enabled by setting the *Lock8k* bit (Bit 6) in the appropriate register location (at address 22 to 2D). Using lower frequencies for phase comparisons in the DPLL results in a greater tolerance to input jitter. It is possible to choose which edge of the input reference clock to lock to, by setting *8K edge polarity* (Bit 2 of register 03*).*

DivN Mode

DivN mode allows the input to be divided by any integer value. The mode is engaged by bit 7 of registers 22 to 2D allowing any input to use this mode. The divide value is set by register 46 & 47, it must be set so that the frequency after division is 8 kHz.

The DivN function is defined as :

DivN = "Divide by (N+1)", i.e. it is the dividing factor used for the division of the input frequency, and has a value of (N+1) where N is an integer from 1 to 12499 inclusive, as set by registers 46 & 47h.

Therefore, in DivN mode the input frequency can be divided by any integer value between 2 to 12500. Consequently, any input frequency which is a multiple of 8 kHz, between 8 kHz to 100 MHz, can be supported by using DivN mode.

Any reference input can be set to use DivN independently of the frequencies and configurations of the other inputs. However only one value of N is allowed, so all inputs with DivN selected must be running at the same frequency.

DivN Examples

(a) To lock to 2.000 MHz:

(i) Set the cnfg_ref_source_frequency register (address 22 - 2D) to 10XX0000 (binary) to enable DivN, and set the frequency to 8 kHz - the frequency required after division. (XX = "Leaky Bucket" ID for this input).

(ii) To achieve 8 kHz, the 2 MHz input must be divided by 250. So, if DivN=250 = (N + 1) then N must be set to 249. This is done by writing F9 hex (249 decimal) to the DivN register pair at address 46 & 47.

(b) To lock to 10.000 MHz:

(i) The cnfg_ref_source_frequency register (address 22 - 2D) is set to 10XX0000 (binary) to set the DivN and the frequency to 8 kHz, the post-division frequency. (XX = "Leaky Bucket" ID for this input).

(ii) To achieve 8 kHz, the 10 MHz input must be divided by 1,250. So, if DivN, = 250 = (N+1) then N must be set to 1,249. This is done by writing 4E1 hex (1,249 decimal) to the DivN register pair at address 46 & 47.

Direct Lock Mode 155 MHz.

The max frequency allowed for phase comparison is 77.76 MHz, so for the special case of a 155 MHz input set to Direct Lock Mode, there is a divide-by-two function automatically selected to bring the frequency down to within the limits of operation.

PECL/LVDS/AMI Input Port Selection

The choice of PECL or LVDS compatibility is programmed via the cnfg_differential_inputs register, address 36h. Unused PECL differential inputs should be fixed with one input High (VDD) and the other input Low (GND), or set in LVDS mode and left floating, in which case one input is internally pulled High and the other Low .

An AMI port supports a composite clock, consisting of a 64 kHz AMI clock with 8 kHz boundaries marked by deliberate violations of the AMI coding rules, as specified in ITU recommendation G.703[6]. Departures from the nominal pattern are detected within the ACS8514, and may cause reference-switching if too frequent. See section DC Characteristics: AMI Input/Output Port, for more details. If the AMI port is unused, the pins (I1 and I2) should be tied to GND.

Table 5 Input Reference Source Selection and Priority Table for T4 DPLL

Port Number	Channel Number (Bin)	Input Port Technology	Frequencies Supported	Default Priority
I1	0001	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz) Default (SONET): 64/8 kHz Default (SDH): 64/8 kHz	0
I2	0010	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz) Default (SONET): 64/8 kHz Default (SDH): 64/8 kHz	0
I3	0011	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 8 kHz Default (SDH): 8 kHz	0
I4	0100	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 8 kHz Default (SDH): 8 kHz	0
I5	0101	LVDS/PECL LVDS default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	6

Port Number	Channel Number (Bin)	Input Port Technology	Frequencies Supported	Default Priority
I6	0110	PECL/LVDS PECL default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	7
I7	0111	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	8
I8	1000	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	9
I9	1001	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	10
I10	1010	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	11
I11	1011	TTL/CMOS	Up to 100 MHz (see Note 0) Default (Master) (SONET): 1.544 MHz Default (Master) (SDH): 2.048 MHz Default (Slave) 6.48 MHz	12
I12	1100	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	0
I13	1101	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	0
I14	1110	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	0

Notes:

(i) TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies are: 2 kHz, 4 kHz, 8 kHz (and N x 8 kHz), 1.544 MHz (SONET)/2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz. SONET or SDH input rate is selected via register 34 bit 2, ip_sonsdhb).

(ii) PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz.

Clock Quality Monitoring

Clock quality is monitored and used to modify the priority tables of the local and remote ACS8520/30 devices. The following parameters are monitored continuously for all 14 inputs in parallel :

1. Activity (toggling).
2. Frequency to +/- 3.8 ppm accuracy (this monitoring is only performed when there is no irregular operation of the clock or loss of clock condition).

A fine level of frequency monitoring and phase monitoring is also performed in the two DPLLs. Phase is measured down to 0.7 degrees with a maximum range of +/- 8191 cycles or +/- 2.9 x 10^6 degrees. Frequency is measured to a 0.0003 ppm resolution and +/- 80 ppm range (could be up to +/- 500 ppm with software enhanced use of the calibration register (3Ch, 3Dh).

Input ports I1 and I2 carry AMI-encoded composite clocks which are also additionally monitored by the AMI-decoder blocks. Loss of signal is declared by the decoders when either the signal amplitude falls below +0.3 V or there is no activity for 1 ms.

Any reference source that suffers a loss-of-activity or clock-out-of-band condition will be declared as unavailable.

Activity Monitoring

The ACS8514 tests for too much or too little activity via the activity monitors. The ACS8514 uses a Leaky Bucket Accumulator, which is a digital circuit which mimics the operation of an analog integrator, in which input pulses increase the output amplitude but die away over time. Such integrators are used when alarms have to be triggered either by fairly regular defect events, which

occur sufficiently close together, or by defect events which occur in bursts. Events which are sufficiently spread out should not trigger the alarm. By adjusting the alarm setting threshold, the point at which the alarm is triggered can be controlled. The point at which the alarm is cleared depends upon the decay rate and the alarm clearing threshold.

On the alarm setting side, if several events occur close together, each event adds to the amplitude and the alarm will be triggered quickly; if events occur a little more spread out, but still sufficiently close together to overcome the decay, the alarm will be triggered eventually. If events occur at a rate which is not sufficient to overcome the decay, the alarm will not be triggered. On the alarm clearing side, if no defect events occur for a sufficient time, the amplitude will decay gradually and the alarm will be cleared when the amplitude falls below the alarm clearing threshold. The ability to decay the amplitude over time allows the importance of defect events to be reduced as time passes by. This means that, in the case of isolated events, the alarm will not be set, whereas, once the alarm becomes set, it will be held on until normal operation has persisted for a suitable time (but if the operation is still erratic, the alarm will remain set). See Figure 3 .

There is one Leaky Bucket Accumulator per input channel. Each Leaky Bucket can select from one of four Configurations (Leaky Bucket Configuration 0 to 3). Each Leaky Bucket Configuration is programmable for size, alarm set and reset thresholds, and decay rate.

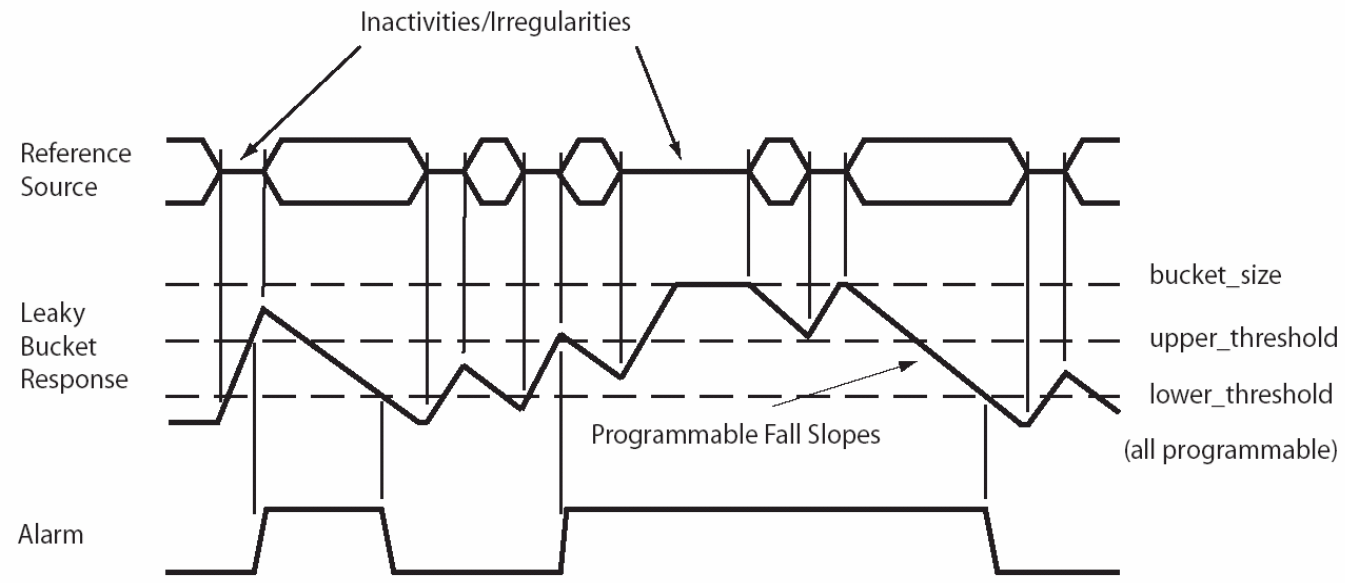
Each source is monitored over a 128 ms period. If, within a 128 ms period, an irregularity occurs that is not deemed to be due to allowable jitter/wander, then the Accumulator is incremented. Irregularity is defined as too much or too little activity (corresponding to +/- 1000ppm on a frequency basis).

The Accumulator will continue to increment up to the point that it reaches the programmed Bucket size. The "fill rate" of the Leaky Bucket is, therefore, 8 units/second. The "leak rate" of the Leaky Bucket is programmable to be in multiples of the fill rate (x 1, x 0.5, x 0.25 and x 0.125) to give a programmable leak rate from 8 units/sec down to 1 unit/sec. A conflict between trying to "leak" at the same time as a "fill" is avoided by preventing a leak when a fill event occurs.

Disqualification of a non-selected reference source is based on inactivity, or on an out-of-band result from the frequency monitors. The currently selected reference source can be disqualified for phase, frequency, inactivity or if the source is outside the DPLL lock range. If the currently selected reference source is disqualified, the next highest priority, qualified reference source is selected.

To avoid the DPLL being pulled off by clock inactivity on a shorter timescale than 128ms, the DPLL contains a fast activity detector such that within approximately two missing input clock cycles, a no-activity flag is raised and the DPLL is frozen in holdover mode, holding the last output frequency value. With the DPLL in holdover mode it is isolated from further disturbances. If the input

Figure 3 Inactivity and Irregularity Monitoring



becomes available again before the activity or frequency monitor rejection alarms have been raised, then the DPLL will continue to lock to the input, with little disturbance. In this scenario, with the DPLL in the "locked" state, the DPLL uses "nearest edge locking" mode (±180° capture) avoiding cycle slips or glitches caused by trying to lock to an edge 360° away, as would happen with traditional PLLs.

Interrupts for Activity Monitors

The loss of the currently selected reference source will eventually cause the input to be considered invalid, triggering an interrupt. The time taken to raise this interrupt is dependant on the Leaky Bucket Configuration of the activity monitors. The fastest Leaky Bucket setting will still take up to 128 ms to trigger the interrupt. The interrupt caused by the brief loss of the currently selected reference source is provided to facilitate very fast source failure detection if desired. It is triggered after missing just a couple of cycles of the reference source. Some applications require the facility to switch downstream devices based on the status of the reference sources. In order to provide extra flexibility, it is possible to flag the mon_ref_failed interrupt (register 06, bit 6) on the pin TDO. This is simply a copy of the status bit in the interrupt register and is independent of the mask register settings. The pin will, therefore, remain high until the interrupt is cleared. This functionality is not enabled by default so the usual JTAG functions can be used. The bit is reset by writing to the interrupt status register in the normal way. This feature can be enabled and disabled by writing to register 48, bit 6.

Leaky Bucket Timing

The time taken (in seconds) to raise an inactivity alarm on a reference source that has previously been fully active (Leaky Bucket empty) will be:

$$(cnfg\_upper\_threshold\_n) / 8$$

where n is the number of the Leaky Bucket Configuration. If an input is intermittently inactive then this time can be longer. The default setting of cnfg_upper_threshold is 6, therefore the default time is 0.75 s.

The time taken (in seconds) to cancel the activity alarm on a previously completely inactive reference source is calculated, for a particular Leaky Bucket, as:

$$[2^{(a)} \times (b - c)] / 8$$

where:

a = cnfg_decay_rate_n
b = cnfg_bucket_size_n
c = cnfg_lower_threshold_n
(where n = the number of the relevant Leaky Bucket Configuration in each case).

The default setting is shown in the following:

$$[2^{1} \times (8 - 4)] / 8 = 1.0 \text{ secs}$$

Frequency Monitoring

The ACS8514 performs frequency monitoring to identify reference sources which have drifted outside the acceptable frequency range measured with respect to the external TCXO/OCXO clock.

The sts_reference_sources (addresses 10 - 16h) out-of-band alarm for a particular reference source is raised when the reference source is outside the acceptable frequency range. With the default register settings a soft alarm is raised if the drift is outside ±11.43 ppm and a hard alarm is raised if the drift is outside ±15.24 ppm. Both of these limits are programmable from 3.8 ppm up to 61 ppm.

The ACS8514 DPLLs have a programmable lock and capture range frequency limit up to ±80 ppm (default is ±9.2 ppm).

The following sections show the frequency monitor features and corresponding registers:

Coarse frequency monitors:

(i) All 14 inputs measured in parallel to a 3.8 ppm resolution. Measured over a 32 second interval.

(ii) Hard (rejection) alarm limit and soft (flag only) alarm limit set in registers 49h & 4Ah. Alarm flags shown in registers 10 h – 16h.

(iii) Makes measurement relative to external TCXO/ OCXO (Must set register 48h, bit7 to '1').

(iv) Reports measured frequency in register 4Ch. Result selected by register 4Bh.

Monitor DPLL:

(v) Measurement to 0.0003 ppm & +/- 80 ppm range. Result at register 0Ch, 0Dh &07h. Register 4Bh, bit 4 at '0' gives monitor DPLL result. Bit 4 at '1' gives T4 DPLL result.

(vi) Measurement Result may be offset or calibrated by registers 3Ch & 3Dh to +/- 500 ppm.

Both the monitor DPLL and the T4 DPLL can be used as a frequency meter. The frequency value measured and reported by the DPLLs corresponds to the integral path value in the DPLLs. As such it is a filtered version of the actual input frequency. The time constant of the filtering is inversely proportional to the DPLL bandwidth. The value is a 19-bit signed number with one LSB representing 0.0003068 ppm (range of ±80 ppm). Reading this regularly can show how the currently locked source is varying in value e.g. due to frequency wander on its input.

Frequency Averagers

Modes are included to provide additional internal filtering on the frequency value from the monitor DPLL. It would also be possible to combine the internal averaging filters with some additional software filtering. For example, the internal fast filter could be used as an anti-aliasing filter and the software could further filter this before determining the actual average frequency. To support this feature, a facility to read out the internally averaged frequency has been provided. By setting register 40h, bit 5, the value read back from the cnfg_average_frequency register (register 3E, 3F, 40) will be the filtered value.

The amount of filtering applied is set by register 40h, bits 6 & 7 and gives additional filter poles of 8 minutes or 110 minutes.

An Example:

Select fast holdover averaging mode by setting register 40h bits 6 & 7 high.

Select to be able to read back filtered output by setting register 40h bit 5 high.

Software reads averaged value from the cnfg_average_ frequency register at address 3Eh, 3Fh & 40h. All bytes of a multi-byte value such as this are frozen internally until all bytes have been read, or until the same byte is read again, in order to correctly build up the multi byte word.

Phase Monitoring

The T4 DPLL will be monitoring the phase of its selected source with respect to its own output and frequency with respect to a calibrated (see register 3Ch, 3Dh) version of the external 12.8 MHz TCXO.

When register 65h, bit 7 is set to '1' the phase detector from T4 DPLL is used to measure the phase between the selected input for the T4 DPLL (set either by priorities in registers 18h to 1Eh or register 35h, bits 3:0) and the selected input for the monitor DPLL (set by register 33). The T4 DPLL outputs are then invalid since the PLL feedback loop is removed.

The monitor DPLL will also be monitoring the phase of its selected source with respect to its own internal output and frequency with respect to a calibrated (see register 3Ch, 3Dh) version of the external 12.8 MHz TCXO. The input phase, as seen at the DPLL phase detector, can be read back from register 77h and 78h. The reporting of the monitor DPLL or T4 DPLL phase detector value is controlled by register 4Bh, bit 4. One LSB corresponds to approximately 0.7 degrees phase difference.

The phase between two inputs may be measured by by the monitor DPLL by switching from source A to source B and recording the measured phase, first at source A (which will be near to zero if the PLL has had time to pull in) and then at source B. Measuring the phase value 30 ms after source B is selected allows enough time for an average phase measurement to be made and reported to register 77h & 78h, but it is before the DPLL loop has had time to pull in the phase back to zero. It is beneficial to set the DPLL bandwidth to the lowest value (e.g. 0.1 Hz when TCXOs used or down to 0.5 mHz with sufficiently stable OCXOs) to slow the rate of this pull-in.

An averaging filter is used in the phase measurement block to get an accurate value. The bandwidth of this filter is 100 Hz (when DPLL bandwidth at 0.5m Hz to 35 Hz) or 200 Hz (when DPLL bandwidth at 70 Hz). Hence around 30 ms is enough for a settled phase value, although this will depend on the magnitude of the phase change.

Using the above method a phase measurement could be made between the most accurate clock source in a system, which would be from an ACS8530 clock output, and any other input clock, such that TIE, MTIE and TDEV could be subsequently calculated by software.

Alternatively the frequency of a selected source could be monitored with respect to the external TCXO/OCXO, as a way of deriving the TIE, MTIE and TDEV result. It may be that the external OCXO is the most stable reference in a system and therefore the most appropriate for input comparisons. A higher monitor DPLL bandwidth of, for example 8 Hz, would allow input wander to be measured, separate from input jitter which would be filtered out according to the setting of the DPLL bandwidth. The frequency accuracy of 0.0003ppm corresponds to a rate of change of phase accuracy of 0.3 ns per second.

The monitor DPLL could be used for accurate analysis of the standby clock sources and the T4 DPLL left to provide the additional T4 path in a system.

Selection of Input Reference Clock Source

The input reference sources for the T4 DPLL may be selected automatically by an order of priority (via registers 18h to 1Eh, register 4Bh, bit4 must be set to '1'). Alternatively it can be forced by external software control (registers 35h, bits 3:0).

The phase and frequency monitor DPLL has its source selected by external control via register 33h, bit 3:0.

Automatic operation selects a reference source based on its pre-defined priority and its current availability. A table is maintained which lists all reference sources in the order of priority. This is initially defined by the default configuration and can be changed via the microprocessor interface by the network manager. In this way, when all the defined sources are active and valid, the source with the highest programmed priority is selected but, if this source fails, the next-highest source is selected, and so on.

The T4 DPLL always operates in revertive mode such that if a valid source has a higher priority than the currently selected reference, a switch over will take place.

Forced Control Selection

For the T4 DPLL register 35 controls both the choice of automatic or forced selection and the selection itself. For automatic choice of source selection, the 4 LSB bit value is set to all zeros. To force a particular input (I_n) , the bit value is set to n (bin).

For the monitor DPLL register 33 controls input selection choice. The power up default has the 4 LSB bit value set to all ones, whereby the DPLL will select the first valid source. The register should be set to a value from 1 to 14 to select the required input for monitoring.

Automatic Control Selection

When an automatic T4 DPLL selection is required, (see above), the priority for each input should be uniquely set in registers 18h to 1Eh (make sure register 4B, bit 4 = 1). Each register holds a 4-bit value which represents the desired priority of that particular port. Unused ports should be given the value, 0000, in the relevant register to indicate they are not to be included in the priority table. On power-up, or following a reset, the whole of the configuration file will be defaulted to the values defined by Table 5. The selection priority values are all relative to each other, with lower-valued numbers taking higher priorities. Each reference source should be given a unique number; the valid values are 1 to 15 (dec). A value of zero disables the reference source. However if two or more inputs are given the same priority number those inputs will be selected on a first in, first out basis. If the first of two same priority number sources goes invalid the second will be switched in. If the first then becomes valid again, it becomes the second source on the first in, first out basis, and there will not be a switch. If a third source with the same priority number as the other two becomes valid, it joins the priority list on the same first in, first out basis.

Modes of Operation

The T4 DPLL in the ACS8514 has three internal modes of operation: Free-run, Locked and Holdover. Only locked or not locked is reported in a status register (register 09, bit6).

After power up and before any sources become qualified and selected the T4 DPLL will either free run, generating an output frequency to the same accuracy as the external TCXO/OCXO or its output will be squelched, depending on register 64h, bit 6. The accuracy of the external oscillator can be calibrated to appear more accurate via registers 3Ch & 3Dh.

Once the T4 DPLL has locked to a source, then when that source fails, it will hold its last output frequency or its output will be squelched, again depending on register 64 hex, bit 6.

Since the outputs from the monitor DPLL are not accessible its internal output frequency and operating modes are less relevant. Indication as to whether it is locked to a source or not are given in register 09h, bits 2:0.

DPLL Architecture and Configuration

A Digital PLL gives a stable and consistent level of performance that can be easily programmed for different dynamic behavior or operating range. It is not affected by operating conditions or silicon process variations. Digital synthesis is used to generate the required SONET/SDH output frequencies. An analog PLL is used to filter the synthesized digital clock before it is fed back to the DPLL input. This avoids any digital sampling induced wander or jitter.

The DPLLs in the ACS8514 are uniquely very programmable for all PLL parameters of bandwidth (from 0.5 mHz up to 70 Hz), damping factor (from 1.2 to 20), frequency acceptance and output range (from 0 to 80 ppm, typically 9.2 ppm) and input frequency (12 common SONET/SDH spot frequencies). There is no requirement to understand the loop filter equations or detailed gain parameters since all high level factors such as overall bandwidth can be set directly via registers in the microprocessor interface. No external critical components are required for either the internal DPLLs or APLLs, providing another key advantage over traditional discrete designs.

The T4 DPLL is similar in structure to the monitor DPLL, but its bandwidth is limited to 18, 35 and 70 Hz.

Monitor DPLL Main Features

- Programmable DPLL bandwidth in 10 steps from 0.5 mHz to 70 Hz.
- Programmable damping factor: For optional faster locking. Factors = 1.2, 2.5, 5, 10 or 20.
- Multiple phase lock detectors.
- Multi-cycle phase detection and locking, programmable up to ±8192 UI (readable up to 23000° as a 16 bit register reports the value).
- Input frequency averaging with a choice of averaging times: 8 minutes or 110 minutes.

T4 DPLL Main Features

- E1 (2.048 MHz) or DS1(1.544 MHz) outputs.
- Programmable DPLL bandwidth in 3 steps from 18 Hz to 70 Hz
- Programmable damping factor: For optional faster locking and peaking control. Factors = 1.2, 2.5, 5, 10 or 20
- Multiple phase lock detectors
- Multi-cycle phase detection and locking, programmable up to ±8192 UI - improves jitter tolerance in direct lock mode
- Can use the phase detector in T4 DPLL to measure the input phase difference between two inputs (+/- 0.5UI).

The following sections detail some component parts of the DPLL.

Monitor DPLL Automatic Bandwidth Controls

In Automatic Bandwidth Selection mode (register 3Bh, bit 7), the monitor DPLL bandwidth setting is selected automatically from the Acquisition Bandwidth or Locked Bandwidth configurations programmed in register 69h and 67h respectively. If this mode is not selected, the DPLL acquires and locks using only the bandwidth set by register 67.

Phase Detectors

A Phase and Frequency detector is used to compare input and feedback clocks. This operates at input frequencies up to 77.76 MHz. The whole DPLL can operate at spot frequencies from 2 kHz up to 77.76 MHz (155.52 MHz is internally divided down to 77.76 MHz). A common arrangement however is to use Lock8k mode (See register 22h to 2Dh, Bit 6) where all input frequencies are divided down to 8 kHz internally. Marginally better MTIE figures may be possible in direct lock mode due to more regular phase updates. This direct locking capability is one of the unique features of the ACS8514.

A multi-phase detector (patent pending) approach is used in order to give an infinitesimally small input phase resolution combined with large jitter tolerance. The following phase detectors are used:

- Phase and frequency detector (±360° or ±180° range)
- An Early/ Late Phase detector for fine resolution
- A multi-cycle phase detector for large input jitter tolerance (up to 8191 UI), which captures and remembers phase differences of many cycles between input and feedback clocks.

The phase detectors can be configured to be immune to occasional missing input clock pulses by using nearest edge detection (±180° capture) or the normal ±360° phase capture range which gives frequency locking. The device will automatically switch to nearest edge locking when the multi-UI phase detector is not enabled and it has detected that phase lock has been achieved. It is possible to disable the selection of nearest edge locking via

register 03h, bit 6 set to 1. In this setting, frequency locking (+/- 360° capture) will always be enabled.

The balance between the first two types of phase detector employed can be adjusted via registers 6Ah to 6Dh. The default settings should be sufficient for all modes. Adjustment of these settings affects only small signal overshoot and bandwidth.

The multi-cycle phase detector is enabled via register 74h, bit 6 set to 1 and the range is set in exponentially increasing steps from ±1 UI, 3 UI, 7 UI, 15 UI ... up to 8191 UI via register 74, bits [3:0].

When this detector is enabled it keeps a track of the correct phase position over many cycles of phase difference to give excellent jitter tolerance. This provides an alternative to switching to Lock8k mode as a method of achieving high jitter tolerance.

An additional control (register 74h, bit 5) enables the multi-phase detector value to be used in the final phase value as part of the DPLL loop. When enabled by setting high, the multi cycle phase value will be used in the loop and gives faster pull in (but more overshoot). The characteristics of the loop will be similar to Lock8k mode where again large input phase differences contribute to the loop dynamics. Setting the bit low only uses a maximum figure of 360 degrees in the loop and will give slower pull-in but gives less overshoot. The final phase position that the loop has to pull in to is still tracked and remembered by the multi-cycle phase detector in either case.

Phase Lock/Loss Detection

Phase lock/loss detection is handled in several ways. Phase loss can be triggered from:

- The fine phase lock detector, which measures the phase between input and feedback clock
- The coarse phase lock detector, which monitors whole cycle slips
- Detection that the DPLL is at min or max frequency
- Detection of no activity on the input.

Each of these sources of phase loss indication is individually enabled via registers bits (register 73h, 74h and 4Dh) and applies to both the T4 DPLL and the monitor DPLL. Phase lock or lost is used to determine whether to switch to nearest edge locking and whether to use acquisition or normal bandwidth settings for the monitor DPLL. Acquisition bandwidth is used for faster pull in from an unlocked state.

The coarse phase lock detector detects phase differences of n cycles between input and feedback clocks, where n is set by register 74h, bits [3:0]; the same register that is used for the coarse phase detector range, since these functions go hand in hand. This detector may be used in the case where it is required that a phase loss indication is not given for reasonable amounts of input jitter and so the fine phase loss detector is disabled and the coarse detector is used instead.

Damping Factor Programmability

The DPLL damping factor is set by default to provide a maximum wander gain peak of around 0.1 dB. The ACS8514 provides a choice of damping factors, with more choice given as the bandwidth setting increases into the frequency regions classified as jitter. Table 6 shows which damping factors are available for selection at the different bandwidth settings and what the corresponding jitter transfer approximate gain peak will be.

Table 6 Available Damping Factors for different DPLL Bandwidths, and associated Jitter Peak Values

Bandwidth	Register 6Bh [2:0]	Damping Factor selected	Gain Peak/ dB
0.5mHz to 4 Hz	1, 2, 3, 4, 5	5	0.1
8 kHz	1	2.5	0.2
	2, 3, 4, 5	5	0.1
18 Hz	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

Local Oscillator Clock

The Master system clock on the ACS8514 should be provided by an external clock oscillator of frequency 12.8 MHz and may be provided by the same oscillator source as used for the partner ACS8520/30 in a system.

Crystal Frequency Calibration

The absolute crystal frequency accuracy is less important than the stability since any frequency offset can be compensated by adjustment of register values in the IC. This allows for calibration and compensation of any crystal frequency variation away from its nominal value. ±50 ppm adjustment would be sufficient to cope with most crystals, in fact the range is an order of magnitude larger due to the use of two 8-bit register locations. The setting of the conf_nominal_frequency register (addr 3Ch, 3Dh) allows for this adjustment. An increase in the register value increases the output frequencies by 0.0196229 ppm for each LSB step.

The default register value (in decimal) = 39321 (9999 hex) = 0 ppm offset. The minimum to maximum offset range of the register is 0 to 65535 dec, giving an adjustment range of -771 ppm to +514 ppm of the output frequencies, in 0.0196229 ppm steps.

Example: If the crystal was oscillating at 12.800 MHz + 5 ppm, then the calibration value in the register to give a - 5 ppm adjustment in output frequencies to compensate for the crystal inaccuracy, would be:

39321 - (5/0.0196229) = 39066 (dec) = 989A (hex).

Output Wander & Jitter

Wander and jitter present on the output depends on::

- The magnitudes of wander and jitter on the selected input reference clock (in Locked mode)
- The internal wander and jitter transfer characteristic (in Locked mode). See below.
- The wander on the local oscillator clock (when the T4 DPLL is free running or holding its frequency).

Jitter and Wander Transfer

The T4 DPLL has a programmable jitter transfer characteristic. This is set by the T4 DPLL bandwidth (register 66). The -3 dB jitter transfer attenuation point can be set to 18, 35 or 70 Hz. The wander and jitter transfer characteristic is shown in Figure 4 .

The monitor DPLL has an effective bandwidth of 0.1 to 70 Hz. The setting of bandwidth for this PLL is mainly used to control how quickly the DPLL follows the input source during input phase and frequency measurements. Since the output clock from the monitor DPLL is not accessible, it's transfer characteristic is not measurable.

Wander on the local oscillator clock will not have a significant effect on the T4 DPLL output clock when locked, since the bandwidth is set high enough so that the DPLL can compensate quickly enough for any frequency changes in the crystal.

In Free-run or frequency holdover wander on the crystal is more significant. Variation in crystal temperature or supply voltage both cause drifts in operating frequency, as does ageing. These effects must be limited by careful selection of a suitable component for the local oscillator.

Input Wander and Jitter Tolerance

The ACS8514 is compliant to the requirements of all relevant standards, principally ITU Recommendation G.825[15], ANSI DS1.101-1999[1], Telcordia GR1244, GR253, G812, G813 and ETS 300 462-5 (1997) in terms of jitter tolerance.

All reference clock inputs have a tight frequency tolerance but a generous jitter tolerance. Using either lock8k mode or direct lock mode and the multi UI phase detector, the jitter tolerance limits can set to exceed all tolerance requirements. When the multi UI phase detector is used, the DPLLs can tolerate and track up to +/- 8191 UI. This limit is programmable (see register 74h).

Pull-in, hold-in and pull-out ranges are shown in Table 7.

Table 7 Input Reference Freq range

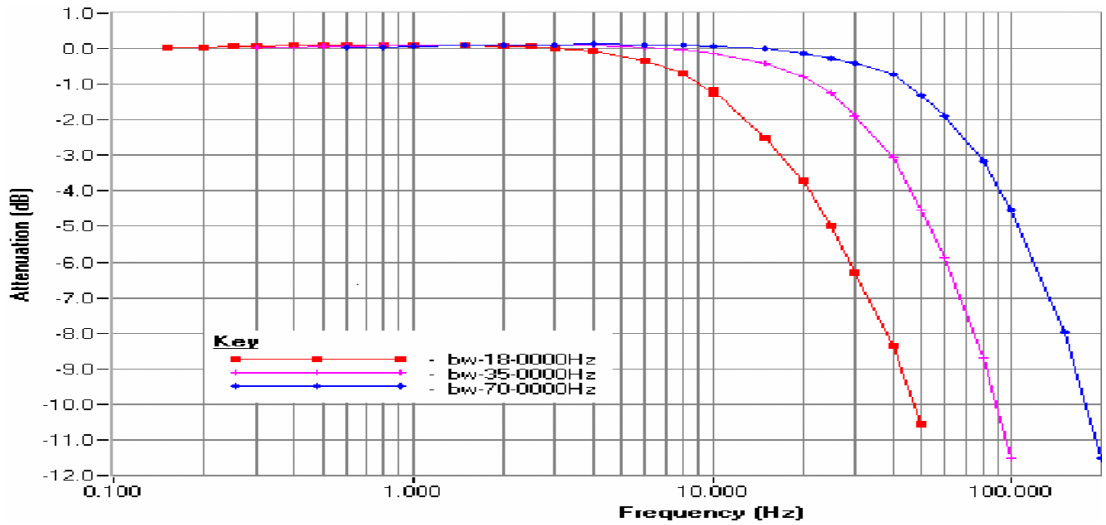
Spec.	Frequency Monitor Acceptance Range	Frequency Acceptance Range (Pull-in)	Frequency Acceptance Range (Hold-in)	Frequency Acceptance Range (Pull-out)
G.703[6]	±16.6 ppm	±4.6 ppm (Note 0) ±9.2 ppm (Note (i))	±4.6 ppm (Note 0) ±9.2 ppm (Note (i))	±4.6 ppm (Note 0) ±9.2 ppm (Note (i))
G.783[9]				
G.823[13]				
GR-1244-CORE[19]				

Notes:

(i) The frequency acceptance and generation range will be ±4.6 ppm around the required frequency when the external crystal frequency accuracy is within a tolerance of ±4.6 ppm.

(ii) The fundamental acceptance range and generation range is ±9.2 ppm with an exact external crystal frequency of 12.800 MHz. This is the default DPLL range; the range is also programmable from 0 to 80 ppm in 0.08 ppm steps.

Figure 4 Measured Jitter Transfer Characteristics T4 DPLL



Replication of Status & Priority Tables

The ACS8514 is designed to partner an ACS8520 or ACS8530. As such there is a need to duplicate the input source quality information and input priorities. A similar need also arises in a redundant system where a slave system shadows a master system.

All devices can independently monitor their reference sources and determine the validity of each source. A facility to make it easier to share the input validity information is provided in the ACS8514, in the form of the *cnfg_sts_remote_sources_valid* register (registers 30 & 31). If one device reports an invalid channel, the same channel can be made invalid in another device by writing a zero to the relevant position in register 30 or 31.

Register *sts_sources_valid (*address 0E & 0F) reports a summary of the input status for each channel. This information can then be written to the *cnfg_sts_remote_sources_valid* register of the other device. This will ensure that any input source considered invalid by one device is also considered invalid by the other.

T4 Generation in Master and Slave ACS8514

As specified by the I.T.U., there is no need to align the phases of the T4 outputs in Master and Slave devices. For a fully redundant system, there is a need, however, to ensure that all devices select the same reference source. As there is no need to guarantee the alignment of phase of the T4 outputs, the Slave devices T4 input does not need to lock to the Masters T4 output, but only needs to ensure that it locks to the same external reference source. There is no defined Holdover requirement for the T4 path.

Output Clock Ports

The device supports outputs from the T4 DPLL in CMOS (TTL compatible) or AMI composite clock format.

TO1 is a CMOS direct digitally synthesized output from the T4 DPLL at E1/SDH (2.048 MHz) or DS1/SONET (1.544 MHz) rate. The output rate is set by register 64, bit 4. Since it is digitally derived it has an output jitter of typically 0.027 UI p-p at 2.048 MHz or 0.020 UI p-p at 1.544 MHz. This is 13 ns p-p and 3.8 ns RMS.

TO2 is an AMI format composite clock, consisting of a 64 kHz AMI clock with 8 kHz boundaries marked by deliberate violations of the AMI coding rules, as specified in ITU recommendation G.703[6]. Departures from the nominal pattern are detected within the ACS8514, and may cause reference-switching if too frequent. The jitter on the TO2 output is < 1ns p-p. See Table 29 for more output details.

The T4 outputs TO1 and TO2 can be enabled/disabled via register 63 bits [5:4].

Table 8 Output Table

Port Name	Output Port Technology	Frequencies Supported
TO1	TTL/CMOS	Fixed frequency, either 1.544 MHz or 2.048 MHz.
TO2	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz), fixed frequency.

Microprocessor Interface

Introduction to Microprocessor Modes

The ACS8514 incorporates a microprocessor interface, which can be configured for all common microprocessor interface types, via the bus interface mode control pins UPSEL(2:0) as defined in Table 9.

These pins are read at power up and set the interface mode.

The optional EPROM mode allows the internal registers to be loaded from the EPROM when the device comes out of "Power-On Reset" mode. The microprocessor interface type can be altered after power up by register 7F, such that for instance the device could boot up in EPROM mode and then switch to Motorola mode, for example, after the EPROM data has preconditioned the device. Reading of Data from the EPROM at boot up time is handled automatically by the ACS8514. The chip select of the EPROM should be driven from the micro in the case of mixed EPROM and micro communication, in order to avoid conflict between EPROM and ACS8514 access from the microprocessor.

The following sections show the interface timings for each interface type.

Table 9 Microprocessor Interface Mode Selection

UPSEL(2:0)	Mode	Description
111 (7)	OFF	Interface disabled
110 (6)	OFF	Interface disabled
101 (5)	SERIAL	Serial uP bus interface
100 (4)	MOTOROLA	Motorola interface
011 (3)	INTEL	Intel compatible bus interface
010 (2)	MULTIPLEXED	Multiplexed bus interface
001 (1)	EPROM	EPROM read mode
000 (0)	OFF	Interface disabled

Timing diagrams for the different microprocessor modes are presented in the following sections.

Motorola Mode

In MOTOROLA mode, the device is configured to interface with a microprocessor using a 680x0 type bus as parallel data + address. Figure 5 and Figure 6 show the timing diagrams of read and write accesses for this mode.

Figure 5 Read Access Timing in MOTOROLA Mode

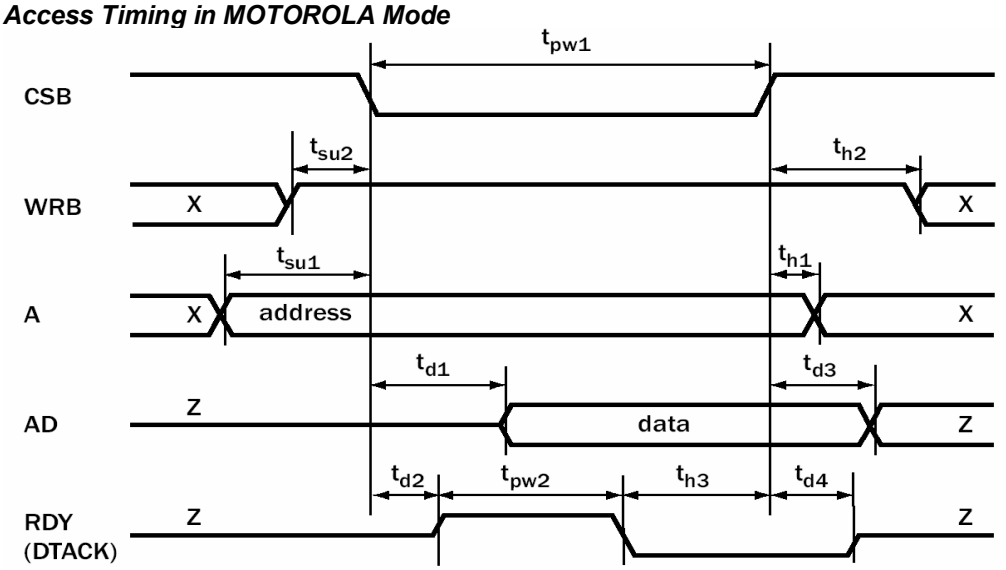


Table 10 Read Access Timing in MOTOROLA Mode (for use with Figure 5)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	4 ns	-	-
t_{su2}	Setup WRB valid to $CSB_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay $CSB_{falling\ edge}$ to AD valid (consecutive Read - Read)	12 ns	-	40 ns
	Delay $CSB_{falling\ edge}$ to AD valid (consecutive Write - Read)	16 ns	-	192 ns
t_{d2}	Delay $CSB_{falling\ edge}$ to $DTACK_{rising\ edge}$	-	-	13 ns
t_{d3}	Delay $CSB_{rising\ edge}$ to AD high-Z	-	-	10 ns
t_{d4}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	9 ns
t_{pw1}	$CSB_{\ Low\ time}$ (consecutive Read - Read)	25 ns	62 ns	-
	$CSB_{\ Low\ time}$ (consecutive Write - Read)	25 ns	193 ns	-
t_{pw2}	$RDY_{\ High\ time}$ (consecutive Read - Read)	12 ns	-	49 ns
	$RDY_{\ High\ time}$ (consecutive Write - Read)	12 ns	-	182 ns
t_{h1}	Hold A valid after $CSB_{rising\ edge}$	0 ns	-	-
t_{h2}	Hold WRB valid after $CSB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold CSB Low after $RDY_{falling\ edge}$	0 ns	-	-
t_p	Time between (consecutive Read - Read) accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	15 ns	-	-
t_p	Time between (consecutive Write - Read) accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	160 ns	-	-

Figure 6 Write Access Timing in MOTOROLA Mode

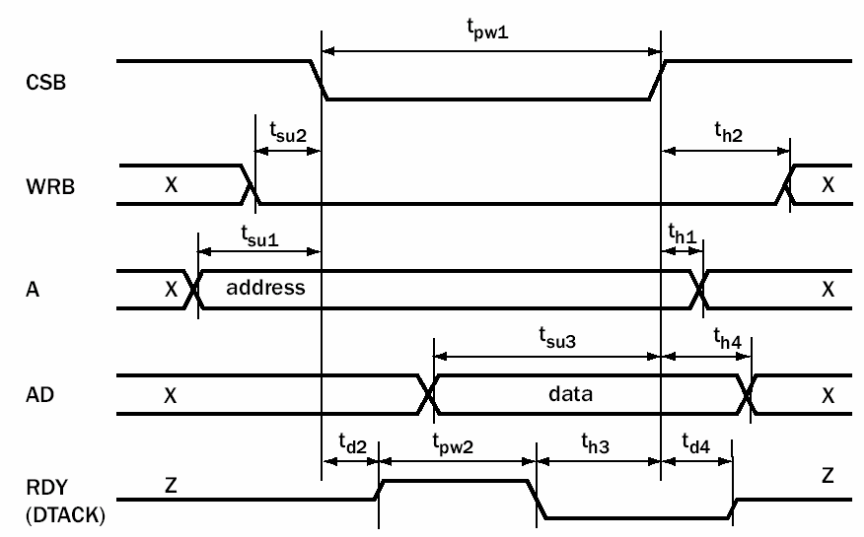


Table 11 Write Access Timing in MOTOROLA Mode (for use with Figure 6)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	4 ns	-	-
t_{su2}	Setup WRB valid to $CSB_{falling\ edge}$	0 ns	-	-
t_{su3}	Setup AD valid before $CSB_{rising\ edge}$	8 ns	-	-
t_{d2}	Delay $CSB_{falling\ edge}$ to $RDY_{rising\ edge}$	-	-	13 ns
t_{d4}	Delay $CSB_{rising\ edge}$ to RDY High -Z	-	-	7 ns
t_{pw1}	$CSB_{Low\ time}$	25 ns	-	180 ns
t_{pw2}	$RDY_{High\ time}$	12 ns	-	166 ns
t_{h1}	Hold A valid after $CSB_{rising\ edge}$	8 ns	-	-
t_{h2}	Hold WRB Low after $CSB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold CSB Low after $RDY_{falling\ edge}$	0 ns	-	-
t_{h4}	Hold AD valid after $CSB_{rising\ edge}$	9 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	160 ns	-	-

Intel Mode

In Intel mode, the device is configured to interface with a microprocessor using a 80x86 type bus as parallel data + address. Figure 7 and Figure 8 show the timing diagrams of read and write accesses for this mode.

Figure 7 Read Access Timing in INTEL Mode

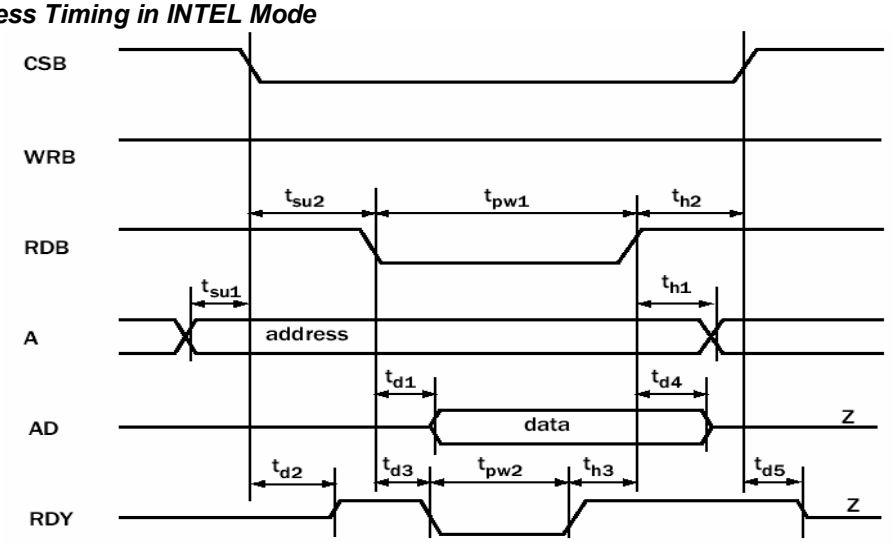


Table 12 Read Access Timing in INTEL Mode (for use with Figure 7)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	4 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $RDB_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay $RDB_{falling\ edge}$ to AD valid (consecutive Read - Read)	12 ns	-	40 ns
	Delay $RDB_{falling\ edge}$ to AD valid (consecutive Write - Read)	12 ns	-	193 ns
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $RDB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	14 ns
t_{d4}	Delay $RDB_{rising\ edge}$ to AD high-Z	-	-	10 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	11 ns
t_{pw1}	RDB Low time (consecutive Read - Read)	35 ns	60 ns	-
	RDB Low time (consecutive Write - Read)	35 ns	195 ns	-
t_{pw2}	RDY Low time (consecutive Read - Read)	20 ns	-	45 ns
	RDY Low time (consecutive Write - Read)	20 ns	-	182 ns
t_{h1}	Hold A valid after $RDB_{rising\ edge}$	0 ns	-	-
t_{h2}	Hold CSB Low after $RDB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold RDB Low after $RDY_{rising\ edge}$	0 ns	-	-
t_p	Time between (consecutive Read - Read) accesses ($RDB_{rising\ edge}$ to $RDB_{falling\ edge}$, or $RDB_{rising\ edge}$ to $WRB_{falling\ edge}$)	15 ns	-	-
t_p	Time between (consecutive Write - Read) accesses (RDBrising edge to $RDB_{falling\ edge}$, or $RDB_{rising\ edge}$ to $WRB_{falling\ edge}$)	160 ns	-	-

Figure 8 Write Access Timing in INTEL Mode

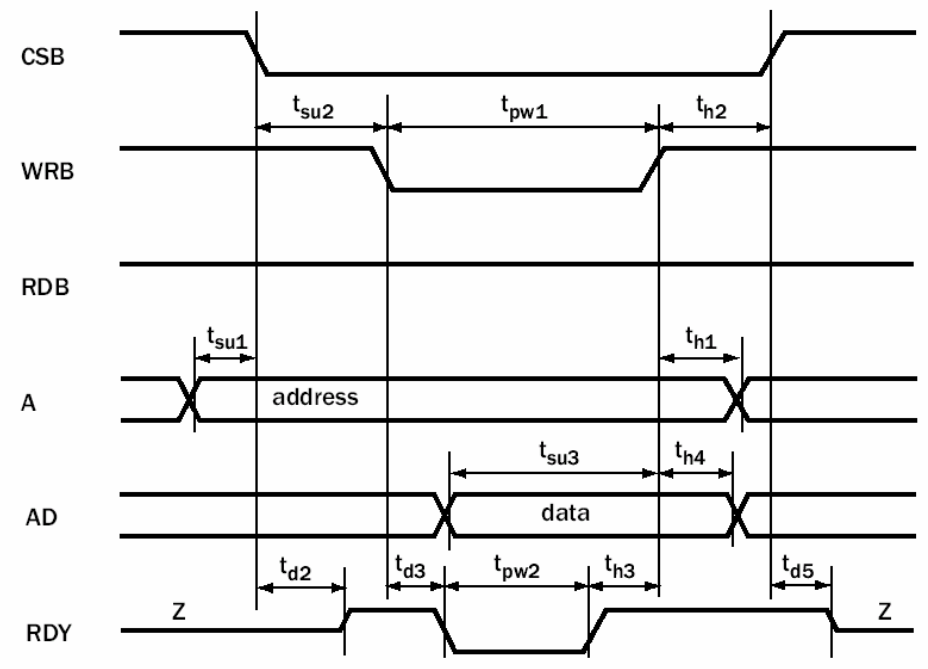


Table 13 Write Access Timing in INTEL Mode (for use with Figure 8)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	4 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $WRB_{falling\ edge}$	0 ns	-	-
t_{su3}	Setup AD valid before $WRB_{rising\ edge}$	6 ns	-	-
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $WRB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	14 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	10 ns
t_{pw1}	WRB Low time	25 ns	185 ns	-
t_{pw2}	RDY Low time	10 ns	-	173 ns
t_{h1}	Hold A valid after $WRB_{rising\ edge}$	12 ns	-	-
t_{h2}	Hold CSB Low after $WRB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold WRB Low after $RDY_{rising\ edge}$	0 ns	-	-
t_{h4}	Hold AD valid after $WRB_{rising\ edge}$	4 ns	-	-
t_p	Time between consecutive accesses ($WRB_{rising\ edge}$ to $WRB_{falling\ edge}$, or $WRB_{rising\ edge}$ to $RDB_{falling\ edge}$)	160 ns	-	-

Multiplexed Mode

In Multiplexed Mode, the device is configured to interface with microprocessors (e.g., Intel's 80x86 family) which share bus signals between address and data. Figure 9 and Figure 10 show the timing diagrams of write and read accesses.

Figure 9 Read Access Timing in MULTIPLEXED Mode

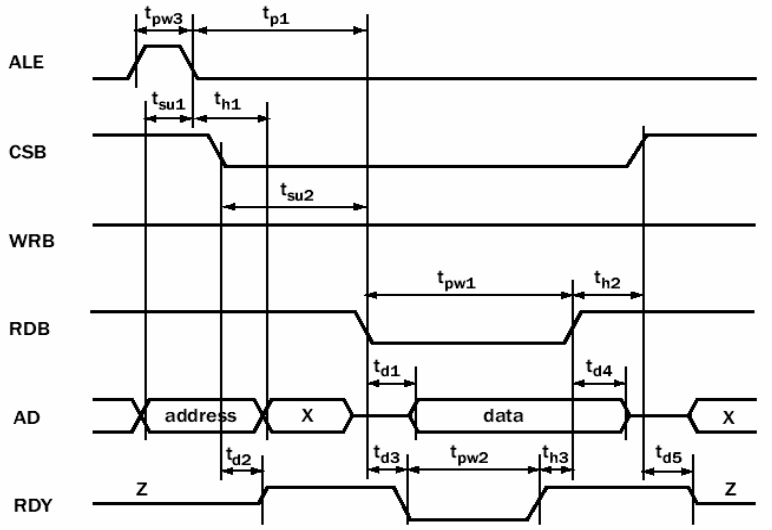


Table 14 Read Access Timing in MULTIPLEXED Mode (for use with Figure 9)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup AD address valid to $ALE_{falling\ edge}$	5 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $RDB_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay $RDB_{falling\ edge}$ to AD data valid (consecutive Read - Read)	12 ns	-	40 ns
	Delay $RDB_{falling\ edge}$ to AD data valid (consecutive Write - Read)	17 ns	-	193 ns
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $RDB_{falling\ edge}$ to RDYfalling edge	-	-	15 ns
t_{d4}	Delay $RDB_{rising\ edge}$ to AD data high-Z	-	-	10 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	10 ns
t_{pw1}	RDB Low time (consecutive Read - Read)	35 ns	60 ns	-
	RDB Low time (consecutive Write - Read)	35 ns	200 ns	-
t_{pw2}	RDY Low time (consecutive Read - Read)	20 ns	-	40 ns
	RDY Low time (consecutive Write - Read)	20 ns	-	185 ns
t_{pw3}	ALE High time	5 ns	-	-
t_{h1}	Hold AD address valid after $ALE_{falling\ edge}$	9 ns	-	-
t_{h2}	Hold CSB Low after $RDB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold RDB Low after $RDY_{rising\ edge}$	0 ns	-	-
t_{p1}	Time between $ALE_{falling\ edge}$ and $RDB_{falling\ edge}$	0 ns	-	-
t_{p2}	Time between (consecutive Read - Read) accesses ($RDB_{rising\ edge}$ to $ALE_{rising\ edge}$)	20 ns	-	-
t_{p2}	Time between (consecutive Write - Read) accesses ($RDB_{rising\ edge}$ to $ALE_{rising\ edge}$)	160 ns	-	-

Figure 10 Write Access Timing in MULTIPLEXED Mode

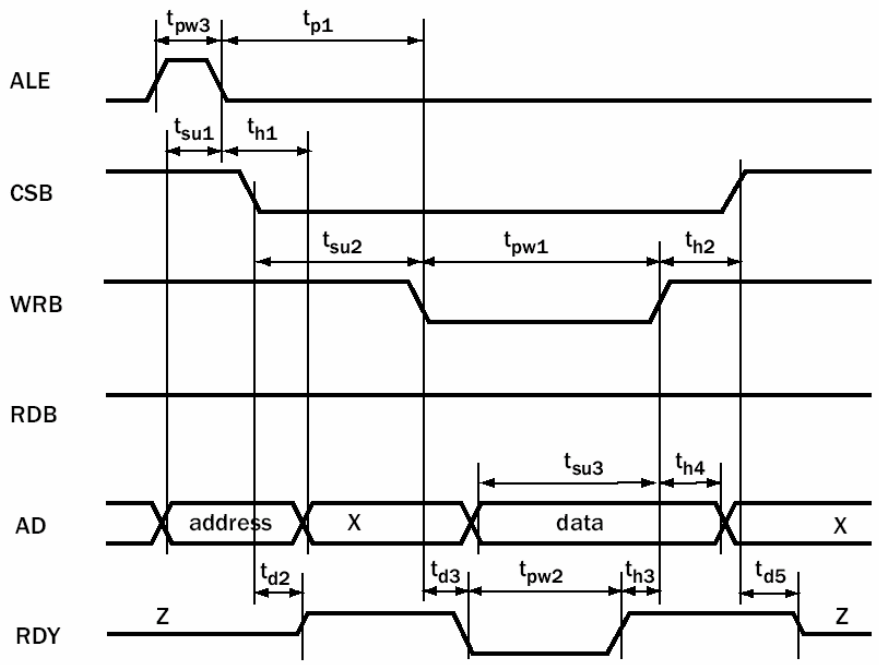


Table 15 Write Access Timing in MULTIPLEXED Mode (For use with Figure 10)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Set up AD address valid to $ALE_{falling\ edge}$	5 ns	-	-
t_{su2}	Set up $CSB_{falling\ edge}$ to $WRB_{falling\ edge}$	0 ns	-	-
t_{su3}	Set up AD data valid to $WRB_{rising\ edge}$	5 ns	-	-
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $WRB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	15 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	9 ns
t_{pw1}	WRB Low time	30 ns	188 ns	-
t_{pw2}	RDY Low time	15 ns	-	173 ns
t_{pw3}	ALE High time	5 ns	-	-
t_{h1}	Hold AD address valid after $ALE_{falling\ edge}$	9 ns	-	-
t_{h2}	Hold CSB Low after $WRB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold WRB Low after $RDY_{rising\ edge}$	0 ns	-	-
t_{h4}	AD data hold valid after $WRB_{rising\ edge}$	7 ns	-	-
t_{p1}	Time between $ALE_{falling\ edge}$ and $WRB_{falling\ edge}$	0 ns	-	-
t_{p2}	Time between consecutive accesses ($WRB_{rising\ edge}$ to $ALE_{rising\ edge}$)	1600 ns	-	-