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Description

The ACS8520 is a highly integrated, single-chip solution for the Synchronous Equipment Timing Source (SETS) function in a SONET or SDH Network Element. The device generates SONET or SDH Equipment Clocks (SEC) and Frame Synchronization clocks. The ACS8520 is fully compliant with the required international specifications and standards.

The device supports Free-run, Locked and Holdover modes. It also supports all three types of reference clock source: recovered line clock, PDH network, and node synchronization. The ACS8520 generates independent SEC and BITS/SSU clocks, an 8 kHz Frame Synchronization clock and a 2 kHz Multi-Frame Synchronization clock.

Two ACS8520 devices can be used together in a Master/Slave configuration mode allowing system protection against a single ACS8520 failure.

A microprocessor port is incorporated, providing access to the configuration and status registers for device setup and monitoring. The ACS8520 supports IEEE 1149.1[5] JTAG boundary scan.

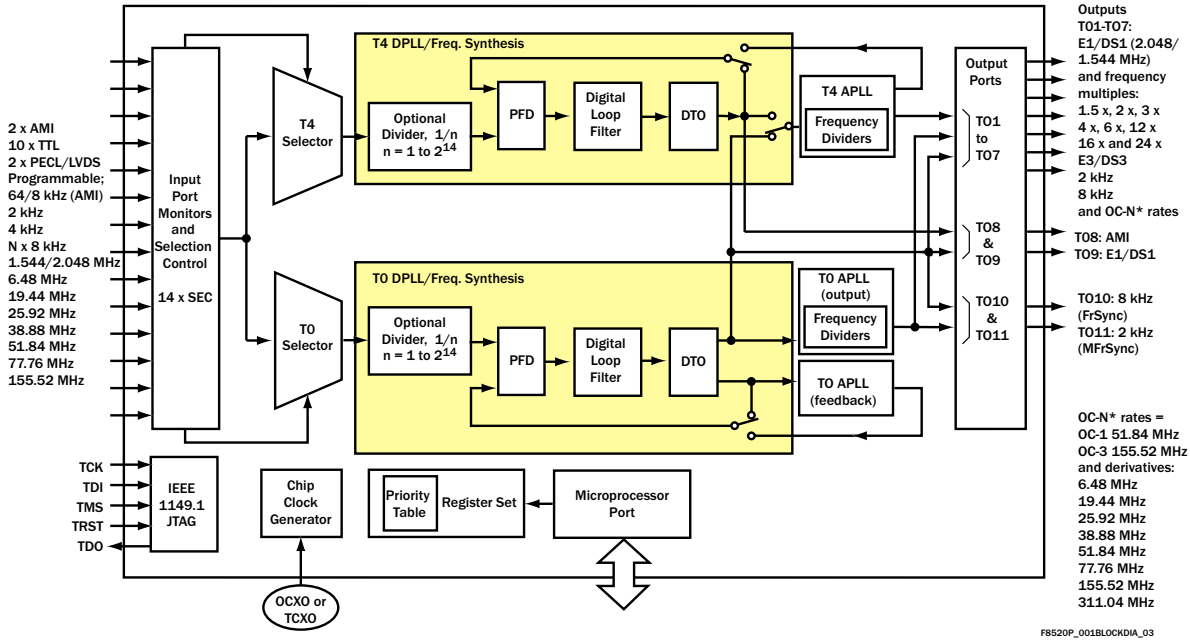
The user can choose between OCXO or TCXO to define the Stratum and/or Holdover performance required.

Features

- Suitable for Stratum 3, 4E, 4 and SONET Minimum Clock (SMC) or SONET/SDH Equipment Clock (SEC) applications
- Meets Telcordia 1244-CORE[19] Stratum 3 and GR-253[17], and ITU-T G.813[11] Options I and II specifications
- Accepts 14 individual input reference clocks, all with robust input clock source quality monitoring.
- Simultaneously generates nine output clocks, plus two Sync pulse outputs
- Absolute Holdover accuracy better than 3×10^{-10} (manual), 7.5×10^{-14} (instantaneous); Holdover stability defined by choice of external XO
- Programmable PLL bandwidth, for wander and jitter tracking/attenuation, 0.1 Hz to 70 Hz in 10 steps
- Automatic hit-less source switchover on loss of input
- Microprocessor interface - Intel, Motorola, Serial, Multiplexed, or boot from EPROM
- Output phase adjustment in 6 ps steps up to ±200 ns
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation. 5 V tolerant
- Available in LQFP 100 package
- Lead (Pb) - free version available (ACS8520T), RoHS and WEEE compliant.

Block Diagram

Figure 1 Block Diagram of the ACS8520 SETS



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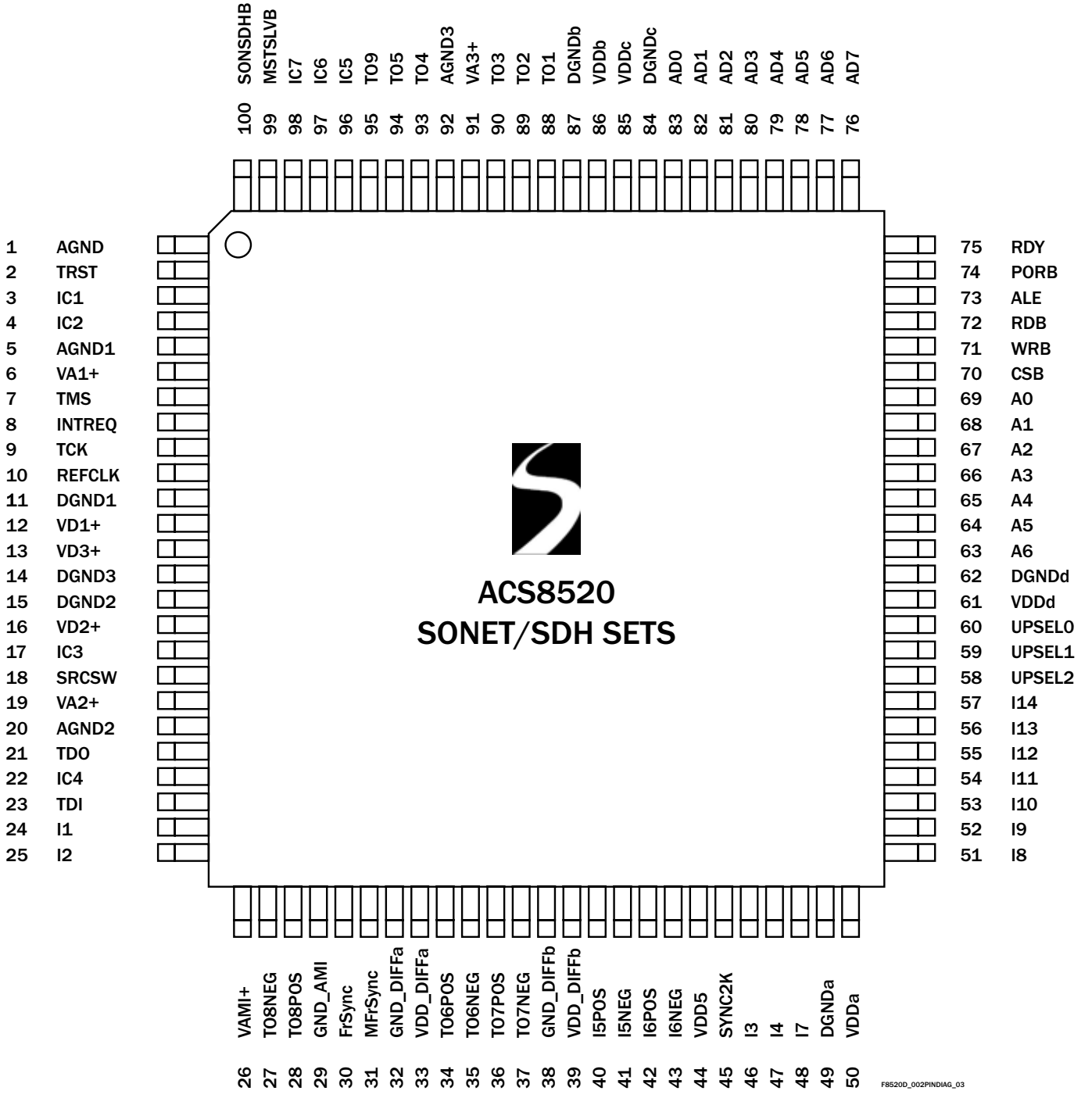
Pin Diagram

Figure 2 ACS8520 Pin Diagram Synchronous Equipment Timing Source for Stratum 3/4E/4 and SMC Systems



Pin Description

Table 1 Power Pins

Pin Number	Symbol	I/O	Type	Description
12, 13, 16	VD1+, VD3+, VD2+	P	-	Supply Voltage: Digital supply to gates in analog section, +3.3 Volts ±10%.
26	VAMI+	P	-	Supply Voltage: Digital supply to AMI output, +3.3 Volts ±10%.
33, 39	VDD_DIFFa, VDD_DIFFb	P	-	Supply Voltage: Digital supply for differential ports, +3.3 Volts ±10%.
44	VDD5	P	-	Digital Supply for +5 Volts Tolerance to Input Pins. Connect to +5 Volts (±10%) for clamping to +5 Volts. Connect to VDD for clamping to +3.3 Volts. Leave floating for no clamping, input pins tolerant up to +5.5 Volts.
50, 61, 85, 86	VDDa, VDDd, VDDc, VDDb	P	-	Supply Voltage: Digital supply to logic, +3.3 Volts ±10%.
6	VA1+	P	-	Supply Voltage: Analog supply to clock multiplying PLL, +3.3 Volts ±10%.
19, 91	VA2+, VA3+	P	-	Supply Voltage: Analog supply to output PLLs, +3.3 Volts ±10%.
11, 14, 15,	DGND1, DGND3, DGND2,	P	-	Supply Ground: Digital ground for components in PLLs.
49, 62, 84, 87	DGNDa, DGNDd, DGNDc, DGNDb	P	-	Supply Ground: Digital ground for logic.
29	GND_AMI	P	-	Supply Ground: Digital ground for AMI output.
32, 38	GND_DIFFa, GND_DIFFb	P	-	Supply Ground: Digital ground for differential ports.
1, 5, 20, 92	AGND, AGND1, AGND2, AGND3	P	-	Supply Ground: Analog grounds.

Note...I = Input, O = Output, P = Power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor.

Table 2 Internally Connected Pins

Pin Number	Symbol	I/O	Type	Description
3, 4, 17, 22, 96, 97, 98	IC1, IC2, IC3, IC4, IC5, IC6, IC7	-	-	Internally Connected: Leave to Float.

Table 3 Other Pins

Pin Number	Symbol	I/O	Type	Description
2	TRST	I	TTL_D	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 for Boundary Scan stand-by mode, still allowing correct device operation. If not used connect to GND or leave floating.
7	TMS	I	TTL^U	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
8	INTREQ	O	TTL/ CMOS	Interrupt Request: Active *High*/ *Low* software Interrupt output.
9	TCK	I	TTL_D	JTAG Clock: Boundary Scan clock input. If not used connect to GND or leave floating.
10	REFCLK	I	TTL	Reference Clock: 12.800 MHz (refer to section headed Local Oscillator Clock).
18	SRCSW	I	TTL_D	Source Switching: Force Fast Source Switching. See "Fast External Switching Mode-SCRSW Pin" on page 15.
21	TDO	O	TTL/ CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK. If not used leave floating.
23	TDI	I	TTL^U	JTAG Input: Serial test data Input. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
24	I1	I	AMI	Input Reference 1: Composite clock 64 kHz + 8 kHz.
25	I2	I	AMI	Input Reference 2: Composite clock 64 kHz + 8 kHz.
27	TO8NEG	O	AMI	Output Reference 8: Composite clock, 64 kHz + 8 kHz negative pulse.
28	TO8POS	O	AMI	Output Reference 8: Composite clock, 64 kHz + 8 kHz positive pulse.
30	FrSync	O	TTL/ CMOS	Output Reference 10: 8 kHz Frame Sync output.
31	MFrSync	O	TTL/ CMOS	Output Reference 11: 2 kHz Multi-Frame Sync output.
34, 35	TO6POS, TO6NEG	O	LVDS/ PECL	Output Reference 6: Programmable, default 38.88 MHz, default type LVDS.
36, 37	TO7POS, TO7NEG	O	PECL/ LVDS	Output Reference 7: Programmable, default 19.44 MHz, default type PECL.
40, 41	I5POS, I5NEG	I	LVDS/ PECL	Input Reference 5: Programmable, default 19.44 MHz, default type LVDS.
42, 43	I6POS, I6NEG	I	PECL/ LVDS	Input Reference 6: Programmable, default 19.44 MHz, default type PECL.
45	SYNC2K	I	TTL_D	External Sync input: 2 kHz, 4 kHz or 8 kHz for frame alignment.
46	I3	I	TTL_D	Input Reference 3: Programmable, default 8 kHz.
47	I4	I	TTL_D	Input Reference 4: Programmable, default 8 kHz.
48	I7	I	TTL_D	Input Reference 7: Programmable, default 19.44 MHz.
51	I8	I	TTL_D	Input Reference 8: Programmable, default 19.44 MHz.
52	I9	I	TTL_D	Input Reference 9: Programmable, default 19.44 MHz.
53	I10	I	TTL_D	Input Reference 10: Programmable, default 19.44 MHz.

Table 3 Other Pins (cont...)

Pin Number	Symbol	I/O	Type	Description
54	I11	I	TTL_D	Input Reference 11: Programmable, default (Master mode) 1.544/2.048 MHz, default (Slave mode) 6.48 MHz.
55	I12	I	TTL_D	Input Reference 12: Programmable, default 1.544/2.048 MHz.
56	I13	I	TTL_D	Input Reference 13: Programmable, default 1.544/2.048 MHz.
57	I14	I	TTL_D	Input Reference 14: Programmable, default 1.544/2.048 MHz.
58 - 60	UPSEL(2:0)	I	TTL_D	Microprocessor Select: Configures the interface for a particular microprocessor type at reset.
63 - 69	A(6:0)	I	TTL_D	Microprocessor Interface Address: Address bus for the microprocessor interface registers. A(0) is SDI in Serial mode - output in EPROM mode only. A(1) is CLKE in serial mode.
70	CSB	I	TTL^U	Chip Select (Active *Low*): This pin is asserted *Low* by the microprocessor to enable the microprocessor interface - output in EPROM mode only.
71	WRB	I	TTL^U	Write (Active *Low*): This pin is asserted *Low* by the microprocessor to initiate a write cycle. In Motorola mode, WRB = 1 for Read.
72	RDB	I	TTL^U	Read (Active *Low*): This pin is asserted *Low* by the microprocessor to initiate a read cycle.
73	ALE	I	TTL_D	Address Latch Enable: This pin becomes the address latch enable from the microprocessor. When this pin transitions from *High* to *Low*, the address bus inputs are latched into the internal registers. ALE = SCLK in Serial mode.
74	PORB	I	TTL^U	Power-On Reset: Master reset. If PORB is forced *Low*, all internal states are reset back to default values.
75	RDY	O	TTL/ CMOS	Ready/ Data Acknowledge: This pin is asserted *High* to indicate the device has completed a read or write operation.
76 - 83	AD(7:0)	IO	TTL_D	Address/ Data: Multiplexed data/ address bus depending on the microprocessor mode selection. AD(0) is SDO in Serial mode.
88	TO1	O	TTL/ CMOS	Output Reference 1: Programmable, default 6.48 MHz.
89	TO2	O	TTL/ CMOS	Output Reference 2: Programmable, default 38.88 MHz.
90	TO3	O	TTL/ CMOS	Output Reference 3: Programmable, default 19.44 MHz.
93	TO4	O	TTL/ CMOS	Output Reference 4: Programmable, default 38.88 MHz.
94	TO5	O	TTL/ CMOS	Output Reference 5: Programmable, default 77.76 MHz.
95	TO9	O	TTL/ CMOS	Output Reference 9: 1.544/2.048 MHz, as per ITU G.783[9] BITS requirements.
99	MSTSLVB	I	TTL^U	Master/ Slave Select: Sets the state of the Master/ Slave selection register, Reg. 34, Bit 1.
100	SONSDHB	I	TTL_D	SONET or SDH Frequency Select: Sets the initial power-up state (or state after a PORB) of the SONET/ SDH frequency selection registers, Reg. 34, Bit 2 and Reg. 38, Bit 5, Bit 6 and Reg. 64 Bit 4.When set *Low*, SDH rates are selected (2.048 MHz etc.) and when set *High*, SONET rates are selected (1.544 MHz etc.) The register states can be changed after power-up by software.

Introduction

The ACS8520 is a highly integrated, single-chip solution for the SETS function in a SONET/ SDH Network Element, for the generation of SEC and Frame/ MultiFrame Synchronization pulses. Digital Phase Locked Loop (DPLL) and direct digital synthesis methods are used in the device so that the overall PLL characteristics are very stable and consistent compared to traditional analog PLLs.

In Free-run mode, the ACS8520 generates a stable, low-noise clock signal at a frequency to the same accuracy as the external oscillator, or it can be made more accurate via software calibration to within ±0.02 ppm. In Locked mode, the ACS8520 selects the most appropriate input reference source and generates a stable, low-noise clock signal locked to the selected reference. In Holdover mode, the ACS8520 generates a stable, low-noise clock signal, adjusted to match the last known good frequency of the last selected reference source. A high level of phase and frequency accuracy is made possible by an internal resolution of up to 54 bits and internal Holdover accuracy of up to 7.5×10^{-14} (instantaneous). In all modes, the frequency accuracy, jitter and drift performance of the clock meet the requirements of ITU G.736[7], G.742[8], G783[9], G.812[10], G.813[11], G.823[13],G.824[14] and Telcordia GR-253-CORE[17] and GR-1244-CORE[19].

The ACS8520 supports all three types of reference clock source: recovered line clock, PDH network synchronization timing, and node synchronization. The ACS8520 generates independent T0 and T4 clocks, an 8 kHz Frame Synchronization clock and a 2 kHz Multi-Frame Synchronization clock.

One key architectural advantage that the ACS8520 has over traditional solutions is in the use of DPLL technology for precise and repeatable performance over temperature or voltage variations and between parts. The overall PLL bandwidth, loop damping, pull-in range and frequency accuracy are all determined by digital parameters that provide a consistent level of performance. An Analog PLL (APLL) takes the signal from the DPLL output and provides a lower jitter output. The APLL bandwidth is set four orders of magnitude higher than the DPLL bandwidth. This ensures that the overall system performance still maintains the advantage of consistent behavior provided by the digital approach.

The DPLLs are clocked by the external Oscillator module (TCXO or OCXO) so that the Free-run or Holdover frequency stability is only determined by the stability of the external oscillator module. This second key advantage confines all temperature critical components to one well defined and pre-calibrated module, whose performance can be chosen to match the application; for example an TCXO for Stratum 3 applications.

All performance parameters of the DPLLs are programmable without the need to understand detailed PLL equations. Bandwidth, damping factor and lock range can all be set directly, for example. The PLL bandwidth can be set over a wide range, 0.1 Hz to 70 Hz in 18 steps, to cover all SONET/ SDH clock synchronization applications.

The ACS8520 supports protection. Two ACS8520 devices can be configured to provide protection against a single ACS8520 failure. The protection maintains alignment of the two ACS8520 devices (Master and Slave) and ensures that both ACS8520 devices maintain the same priority table, choose the same reference input and generate the T0 clock, the 8 kHz Frame Synchronization clock and the 2 kHz Multi-Frame Synchronization clock with the same phase. The ACS8520 includes a multi-standard microprocessor port, providing access to the configuration and status registers for device setup and monitoring.

General Description

Overview

The following description refers to the Block Diagram (Figure 1 on page 1).

The ACS8520 SETS device has 14 input clocks, generates 11 output clocks, and has a total of 55 possible output frequencies. There are two main paths through the device: T0 and T4. Each path has an independent DPLL and APLL pair.

The T0 path is a high quality, highly configurable path designed to provide features necessary for node timing synchronization within a SONET/ SDH network. The T4 path is a simpler and less configurable path designed to give a totally independent path for internal equipment synchronization. The device supports use of either or both paths, either locked together or independent.

Of the 14 input references, two are AMI composite clock, two are LVDS/ PECL and the remaining ten are TTL/ CMOS compatible inputs. All the TTL/ CMOS are 3 V and 5 V compatible (with clamping if required by connecting the

VDD5 pin). The AMI inputs are ±1 V typically A.C. coupled. Refer to the electrical characteristics section for more information on the electrical compatibility and details. Input frequencies supported range from 2 kHz to 155.52 MHz.

Common E1, DS1, OC3 and sub-divisions are supported as spot frequencies that the DPLLs will directly lock to. Any input frequency, up to 100 MHz, that is a multiple of 8 kHz can also be locked to via an inbuilt programmable divider.

An input reference monitor is assigned to each of the 14 inputs. The monitors operate continuously such that at all times the status of all of the inputs to the device are known. Each input can be monitored for both frequency and activity, activity alone, or the monitors can be disabled.

The frequency monitors have a “hard” (rejection) alarm limit and a “soft” (flag only) alarm limit for monitoring frequency, whilst the reference is still within its allowed frequency band. Each input reference can be programmed with a priority number allowing references to be chosen according to the highest priority valid input. The two paths (T0 and T4) have independent priorities to allow completely independent operation of the two paths. Both paths operate either automatic or external source selection.

For automatic input reference selection, the T0 path has a more complex state machine than the T4 path.

The T0 and T4 PLL paths support the following common features:

- Automatic source selection according to input priorities and quality level
- Different quality levels (activity alarm thresholds) for each input
- Variable bandwidth, lock range and damping factor
- Direct PLL locking to common SONET/SDH input frequencies or any multiple of 8 kHz
- Automatic mode switching between Free-run, Locked and Holdover states
- Fast detection on input failure and entry into Holdover mode (holds at the last good frequency value)
- Frequency translation between input and output rates via direct digital synthesis
- High accuracy digital architecture for stable PLL dynamics combined with an APLL for low jitter final output clocks.

There are a number of features supported by the T0 path that are not supported by the T4 path, although these can also all be externally controlled by software.

The additional T0 features supported are:

- Non-revertive mode
- Phase Build-out on source switch (hit-less source switching)
- I/O phase offset control
- Greater programmable bandwidth from 0.1 Hz to 70 Hz in 10 steps (T4 path programmable bandwidth in 3 steps, 18, 35 and 70 Hz)
- Noise rejection on low frequency input
- Manual Holdover frequency control
- Controllable automatic Holdover frequency filtering
- Frame Sync pulse alignment.

Either the software or an internal state machine controls the operation of the DPLL in the T0 path. The state machine for the T4 path is very simple and cannot be manually/externally controlled, however the overall operation can be controlled by manual reference source selection. One additional feature of the T4 path is the ability to measure a phase difference between two inputs.

The T0 path DPLL always produces an output at 77.76 MHz to feed the APLL, regardless of the frequency selected at the output pins. The T4 path can be operated at a number of frequencies. This is to enable the generation of extra output frequencies, which cannot be easily related to 77.76 MHz. When the T4 path is selected to lock to the T0 path, the T4 DPLL locks to the 8 kHz from the T0 DPLL. This is because all of the frequencies of operation of the T4 path can be divided to 8 kHz and this will ensure synchronization of all the frequencies within the two paths.

Both of the DPLLs’ outputs are connected to multiplying and filtering APLLs. The outputs of these APLLs are divided making a number of frequencies simultaneously available for selection at the output clock ports. The various combinations of DPLL, APLL and divider configurations allow for generation of a comprehensive set of frequencies, as listed in Table 14.

To synchronize the lower output frequencies when the T0 PLL is locked to a high frequency reference input, an additional input is provided. The SYNC2K pin (pin 45) is used to reset the dividers that generate the 2 kHz and 8 kHz outputs such that the output 2/8 kHz clocks are lined up with the input 2 kHz. This synchronization

method allows for example, a master and a slave device to be in precise alignment.

The ACS8520 also supports Sync pulse references of 4 kHz or 8 kHz although in these cases frequencies lower than the Sync pulse reference may not necessarily be in phase.

Input Reference Clock Ports

Table 4 gives details of the input reference ports, showing the input technologies and the range of frequencies supported on each port; the default spot frequencies and default priorities assigned to each port on power-up or by reset are also shown. Note that SDH and SONET networks use different default frequencies; the network type is pin-selectable (using either the SONSDHB pin or via software). Specific frequencies and priorities are set by configuration.

SDH and SONET networks use different default frequencies; the network type is selectable using the *cnfg_input_mode* Reg. 34 Bit 2, *ip_sonsdhb*.

- For SONET, *ip_sonsdhb* = 1
- For SDH, *ip_sonsdhb* = 0

On power-up or by reset, the default will be set by the state of the SONSDHB pin (pin 100). Specific frequencies and priorities are set by configuration.

The frequency selection is programmed via the *cnfg_ref_source_frequency* register (Reg. 20 - Reg. 2D).

Locking Frequency Modes

There are three locking frequency modes that can be configured: Direct Lock, Lock 8k and DivN.

Direct Lock Mode

In Direct Lock Mode, the internal DPLL can lock to the selected input at the spot frequency of the input, for example 19.44 MHz performs the DPLL phase comparisons at 19.44 MHz.

In Lock8K and DivN modes (and for special case of 155 MHz), an internal divider is used prior to the DPLL to divide the input frequency before it is used for phase comparisons in the DPLL.

Lock8K Mode

Lock8K mode automatically sets the divider parameters to divide the input frequency down to 8 kHz. Lock8K can only be used on the supported spot frequencies (see Table 4 Note(i)). Lock8k mode is enabled by setting the *Lock8k* bit (Bit 6) in the appropriate *cnfg_ref_source_frequency* register location. Using lower frequencies for phase comparisons in the DPLL results in a greater tolerance to input jitter.It is possible to choose which edge of the input reference clock to lock to, by setting *8K edge polarity* (Bit 2 of Reg. 03, *test_register1)*.

DivN Mode

In DivN mode, the divider parameters are set manually by configuration (Bit 7 of the *cnfg_ref_source_frequency* register), but must be set so that the frequency after division is 8 kHz.

The DivN function is defined as:

DivN = “Divide by N+ 1”, i.e. it is the dividing factor used for the division of the input frequency, and has a value of (N+1) where N is an integer from 1 to 12499 inclusive.

Therefore, in DivN mode the input frequency can be divided by any integer value between 2 to 12500. Consequently, any input frequency which is a multiple of 8 kHz, between 8 kHz to 100 MHz, can be supported by using DivN mode.

Note...Any reference input can be set to use DivN independently of the frequencies and configurations of the other inputs. However only one value of N is allowed, so all inputs with DivN selected must be running at the same frequency.

DivN Examples

(a) To lock to 2.000 MHz:

(i) Set the *cnfg_ref_source_frequency* register to 10XX0000 (binary) to enable DivN, and set the frequency to 8 kHz - the frequency required after division. (XX = “Leaky Bucket” ID for this input).

(ii) To achieve 8 kHz, the 2 MHz input must be divided by 250. So, if DivN = 250 = (N + 1) then N must be set to 249. This is done by writing F9 hex (249 decimal) to the DivN register pair Reg. 46/47.

(b) To lock to 10.000 MHz:

(i) The *cnfg_ref_source_frequency* register is set to 10XX0000 (binary) to set the DivN and the

frequency to 8 kHz, the post-division frequency. (XX = "Leaky Bucket" ID for this input).

(ii) To achieve 8 kHz, the 10 MHz input must be divided by 1,250. So, if DivN, = 250 = (N+1) then N must be set to 1,249. This is done by writing 4E1 hex (1,249 decimal) to the DivN register pair Reg. 46/47.

Direct Lock Mode 155 MHz.

The max frequency allowed for phase comparison is 77.76MHz, so for the special case of a 155 MHz input set to Direct Lock Mode, there is a divide-by-two function automatically selected to bring the frequency down to within the limits of operation.

PECL/ LVDS/ AMI Input Port Selection

The choice of PECL or LVDS compatibility is programmed via the *cnfg_differential_inputs* register. Unused PECL differential inputs should be fixed with one input *High* (VDD) and the other input *Low* (GND), or set in LVDS mode and left floating, in which case one input is internally pulled *High* and the other *Low*.

An AMI port supports a composite clock, consisting of a 64 kHz AMI clock with 8 kHz boundaries marked by deliberate violations of the AMI coding rules, as specified in ITU recommendation G.703[6]. Departures from the nominal pattern are detected within the ACS8520, and may cause reference-switching if too frequent. See section DC Characteristics: AMI Input/ Output Port, for more details. If the AMI port is unused, the pins (I1 and I2) should be tied to GND.

Table 4 Input Reference Source Selection and Priority Table

Port Number	Channel Number (Bin)	Input Port Technology	Frequencies Supported	Default Priority
I1	0001	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz) Default (SONET): 64/8 kHz Default (SDH): 64/8 kHz	2
I2	0010	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz) Default (SONET): 64/8 kHz Default (SDH): 64/8 kHz	3
I3	0011	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 8 kHz Default (SDH): 8 kHz	4
I4	0100	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 8 kHz Default (SDH): 8 kHz	5
I5	0101	LVDS/ PECL LVDS default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	6
I6	0110	PECL/ LVDS PECL default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	7
I7	0111	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	8
I8	1000	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	9
I9	1001	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	10
I10	1010	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	11
I11	1011	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (Master) (SONET): 1.544 MHz Default (Master) (SDH): 2.048 MHz Default (Slave) 6.48 MHz	12/ 1 (Note (iii))
I12	1100	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	13

Table 4 Input Reference Source Selection and Priority Table (cont...)

Port Number	Channel Number (Bin)	Input Port Technology	Frequencies Supported	Default Priority
I13	1101	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	14
I14	1110	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	15

Notes: (i) TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies are: 2 kHz, 4 kHz, 8 kHz (and N x 8 kHz), 1.544 MHz (SONET)/2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz. SONET or SDH input rate is selected via Reg. 34 Bit 2, ip_sonsdhb).

(ii) PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz (and 311.04 MHz for TO6 only).

(iii) Input port I11 is set at priority 12 on the Master SETS IC and priority 1 on the Slave SETS IC, as default on power up (or PORB). The default setup of Master or Slave I11 priority is determined by the MSTSLVB pin.

Clock Quality Monitoring

Clock quality is monitored and used to modify the priority tables of the local and remote ACS8520 devices. The following parameters are monitored:

1. Activity (toggling).
2. Frequency (this monitoring is only performed when there is no irregular operation of the clock or loss of clock condition).

In addition, input ports I1 and I2 carry AMI-encoded composite clocks which are monitored by the AMI-decoder blocks. Loss of signal is declared by the decoders when either the signal amplitude falls below +0.3 V or there is no activity for 1 ms.

Any reference source that suffers a loss-of-activity or clock-out-of-band condition will be declared as unavailable.

Clock quality monitoring is a continuous process which is used to identify clock problems. There is a difference in dynamics between the selected clock and the other reference clocks. Anomalies occurring on non-selected reference sources affect only that source's suitability for selection, whereas anomalies occurring on the selected clock could have a detrimental impact on the accuracy of the output clock.

Anomalies detected by the activity detector are integrated in a Leaky Bucket Accumulator. Occasional anomalies do not cause the Accumulator to cross the alarm setting threshold, so the selected reference source is retained. Persistent anomalies cause the alarm setting threshold to be crossed and result in the selected reference source being rejected.

Anomalies on the currently locked-to input reference clock, whether affecting signal purity or signal frequency, could induce jitter or frequency offsets in the output clock, leading to anomalous behavior. Anomalies on the selected clock, therefore, have to be detected as they occur and the phase locked loop must be temporarily isolated until the clock is once again pure. The clock monitoring process cannot be used for this because the high degree of accuracy required dictates that the process be slow. To achieve the immediacy required by the phase locked loop requires an alternative mechanism. The phase locked loop itself contains a fast activity detector such that within approximately two missing input clock cycles, a no-activity flag is raised and the DPLL is frozen in Holdover mode. This flag can also be read as the *main_ref_failed* bit (from Reg. 06, Bit 6) and can be set to indicate a phase lost state by enabling Reg. 73, Bit 6. With the DPLL in Holdover mode it is isolated from further disturbances. If the input becomes available again before the activity or frequency monitor rejection alarms have been raised, then the DPLL will continue to lock to the input, with little disturbance. In this scenario, with the DPLL in the “locked” state, the DPLL uses “nearest edge locking” mode (±180° capture) avoiding cycle slips or glitches caused by trying to lock to an edge 360° away, as would happen with traditional PLLs.

Activity Monitoring

The ACS8520 has a combined inactivity and irregularity monitor. The ACS8520 uses a Leaky Bucket Accumulator, which is a digital circuit which mimics the operation of an analog integrator, in which input pulses increase the output amplitude but die away over time. Such integrators

are used when alarms have to be triggered either by fairly regular defect events, which occur sufficiently close together, or by defect events which occur in bursts. Events which are sufficiently spread out should not trigger the alarm. By adjusting the alarm setting threshold, the point at which the alarm is triggered can be controlled. The point at which the alarm is cleared depends upon the decay rate and the alarm clearing threshold.

On the alarm setting side, if several events occur close together, each event adds to the amplitude and the alarm will be triggered quickly; if events occur a little more spread out, but still sufficiently close together to overcome the decay, the alarm will be triggered eventually. If events occur at a rate which is not sufficient to overcome the decay, the alarm will not be triggered. On the alarm clearing side, if no defect events occur for a sufficient time, the amplitude will decay gradually and the alarm will be cleared when the amplitude falls below the alarm clearing threshold. The ability to decay the amplitude over time allows the importance of defect events to be reduced as time passes by. This means that, in the case of isolated events, the alarm will not be set, whereas, once the alarm becomes set, it will be held on until normal operation has persisted for a suitable time (but if the operation is still erratic, the alarm will remain set). See Figure 3.

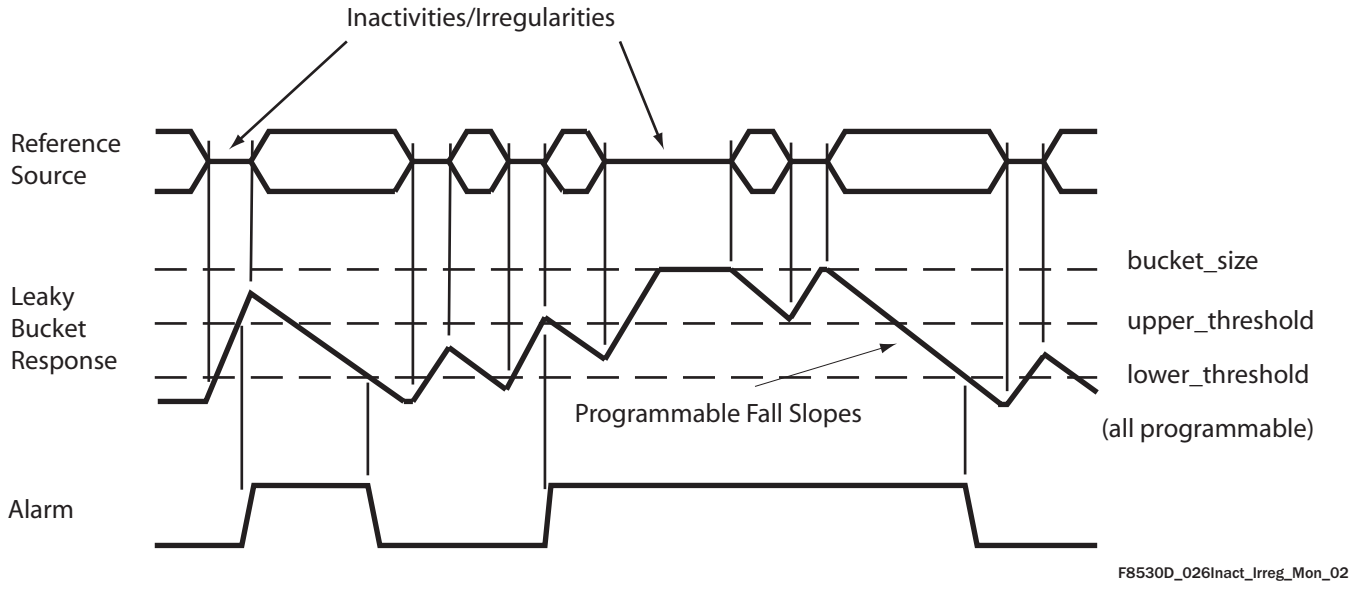
There is one Leaky Bucket Accumulator per input channel. Each Leaky Bucket can select from four Configurations (Leaky Bucket Configuration 0 to 3). Each Leaky Bucket Configuration is programmable for size, alarm set and reset thresholds, and decay rate.

Each source is monitored over a 128 ms period. If, within a 128 ms period, an irregularity occurs that is not deemed to be due to allowable jitter/wander, then the Accumulator is incremented.

The Accumulator will continue to increment up to the point that it reaches the programmed Bucket size. The “fill rate” of the Leaky Bucket is, therefore, 8 units/second. The “leak rate” of the Leaky Bucket is programmable to be in multiples of the fill rate (x 1, x 0.5, x 0.25 and x 0.125) to give a programmable leak rate from 8 units/sec down to 1 unit/sec. A conflict between trying to “leak” at the same time as a “fill” is avoided by preventing a leak when a fill event occurs.

Disqualification of a non-selected reference source is based on inactivity, or on an out-of-band result from the frequency monitors. The currently selected reference source can be disqualified for phase, frequency, inactivity or if the source is outside the DPLL lock range. If the currently selected reference source is disqualified, the next highest priority, qualified reference source is selected.

Figure 3 Inactivity and Irregularity Monitoring



Interrupts for Activity Monitors

The loss of the currently selected reference source will eventually cause the input to be considered invalid, triggering an interrupt. The time taken to raise this interrupt is dependant on the Leaky Bucket Configuration of the activity monitors. The fastest Leaky Bucket setting will still take up to 128 ms to trigger the interrupt. The interrupt caused by the brief loss of the currently selected reference source is provided to facilitate very fast source failure detection if desired. It is triggered after missing just a couple of cycles of the reference source. Some applications require the facility to switch downstream devices based on the status of the reference sources. In order to provide extra flexibility, it is possible to flag the *main_ref_failed* interrupt (Reg. 06 Bit 6) on the pin TDO. This is simply a copy of the status bit in the interrupt register and is independent of the mask register settings. The bit is reset by writing to the interrupt status register in the normal way. This feature can be enabled and disabled by writing to Reg. 48 Bit 6.

Leaky Bucket Timing

The time taken (in seconds) to raise an inactivity alarm on a reference source that has previously been fully active (Leaky Bucket empty) will be:

$$(cnfg\_upper\_threshold\_n) \ / \ 8$$

where n is the number of the Leaky Bucket Configuration. If an input is intermittently inactive then this time can be longer. The default setting of *cnfg_upper_threshold_n* is 6, therefore the default time is 0.75 s.

The time taken (in seconds) to cancel the activity alarm on a previously completely inactive reference source is calculated, for a particular Leaky Bucket, as:

$$[2^{(a)} \times (b - c)] / 8$$

where:

$a = cnfg\_decay\_rate\_n$
$b = cnfg\_bucket\_size\_n$
$c = cnfg\_lower\_threshold\_n$
(where n = the number of the relevant Leaky Bucket Configuration in each case).

The default setting is shown in the following:

$$[2^{1} \times (8 - 4)] / 8 = 1.0 \text{ secs}$$

Frequency Monitoring

The ACS8520 performs frequency monitoring to identify reference sources which have drifted outside the acceptable frequency range measured with respect either to the output clock or to the XO clock.

The *sts_reference_sources* out-of-band alarm for a particular reference source is raised when the reference source is outside the acceptable frequency range. With the default register settings a soft alarm is raised if the drift is outside ±11.43 ppm and a hard alarm is raised if the drift is outside ±15.24 ppm. Both of these limits are programmable from 3.8 ppm up to 61 ppm.

The ACS8520 DPLL has a programmable lock and capture range frequency limit up to ±80 ppm (default is ±9.2 ppm).

Selection of Input Reference Clock Source

Under normal operation, the input reference sources are selected automatically by an order of priority. But, for special circumstances, such as chip or board testing, the selection may be forced by configuration.

Automatic operation selects a reference source based on its pre-defined priority and its current availability. A table is maintained which lists all reference sources in the order of priority. This is initially defined by the default configuration and can be changed via the microprocessor interface by the Network Manager. In this way, when all the defined sources are active and valid, the source with the highest programmed priority is selected but, if this source fails, the next-highest source is selected, and so on.

Restoration of repaired reference sources is handled carefully to avoid inadvertent disturbance of the output clock. For this, the ACS8520 has two modes of operation; Revertive and Non-revertive.

In Revertive mode, if a re-validated (or newly validated) source has a higher priority than the reference source which is currently selected, a switch over will take place. Many applications prefer to minimize the clock switching events and choose Non-revertive mode.

In Non-revertive mode, when a re-validated (or newly validated) source has a higher priority then the selected source will be maintained. The re-validation of the reference source will be flagged in the *sts_sources_valid* register and, if not masked, will generate an interrupt.

Selection of the re-validated source can take place under software control or if the currently selected source fails.

To enable software control, the software should briefly enable Revertive mode to effect a switch-over to the

higher priority source. When there is a reference available with higher priority than the selected reference, there will be NO change of reference source as long as the Non-revertive mode remains on, and the currently selected source is valid. A failure of the selected reference will always trigger a switch-over regardless of whether Revertive or Non-revertive mode has been chosen.

Also, in a Master/ Slave redundancy-protection scheme, the Slave device(s) must follow the Master device. The alignment of the Master and Slave devices is part of the protection mechanism. The availability of each source is determined by a combination of local and remote monitoring of each source. Each input reference source supplied to each ACS8520 device is monitored locally and the results are made available to other devices.

Forced Control Selection

A configuration register, *force_select_reference_source* Reg. 33, controls both the choice of automatic or forced selection and the selection itself (when forced selection is required). For Automatic choice of source selection, the 4 LSB bit value is set to all zeros or all ones (default). To force a particular input (I_n), the Bit value is set to n (bin). Forced selection is not the normal mode of operation, and the *force_select_reference_source* variable is defaulted to the all-ones value on reset, thereby adopting the automatic selection of the reference source.

Automatic Control Selection

When an automatic selection is required, the *force_select_reference_source* register LSB 4 bits must be set to all zeros or all ones. The configuration registers, *cnfg_ref_selection_priority*, held in the µP port block, consist of seven, 8-bit registers organized as one 4-bit register per input reference port. Each register holds a 4-bit value which represents the desired priority of that particular port. Unused ports should be given the value, 0000, in the relevant register to indicate they are not to be included in the priority table. On power-up, or following a reset, the whole of the configuration file will be defaulted to the values defined by Table 4. The selection priority values are all relative to each other, with lower-valued numbers taking higher priorities. Each reference source should be given a unique number; the valid values are 1 to 15 (dec). A value of zero disables the reference source. However if two or more inputs are given the same priority number those inputs will be selected on a first in, first out basis. If the first of two same priority number sources goes invalid the second will be switched in. If the first then becomes valid again, it becomes the second source on the first in, first out basis, and there will not be a switch. If a third source with the same priority number as the other two becomes valid, it joins the priority list on the same first in, first out basis. There is no implied priority based on the channel numbers. Revertive/ Non-revertive mode has no effect on sources with the same priority value.

The input port I11 is also for the connection of the synchronous clock of the T0 output of the Master device (or the active-Slave device), to be used to align the T0 output with the Master (or active-Slave) device if this device is acting in a subordinate-Slave or subordinate-Master role.

Ultra Fast Switching

A reference source is normally disqualified after the Leaky Bucket monitor thresholds have been crossed. An option for a faster disqualification has been implemented, whereby if Reg. 48 Bit 5 (*ultra_fast_switch*) is set, then a loss of activity of just a few reference clock cycles will set the *main_ref_failed* alarm and cause a reference switch. This can be configured (see Reg. 06, Bit 6) to cause an interrupt to occur instead of, or as well as, causing the reference switch.

The *sts_interrupts* register Reg. 06 Bit 6 (*main_ref_failed*) is used to flag inactivity on the reference that the device is locked to much faster than the activity monitors can support. If Reg. 48 Bit 6 of the *cnfg_monitors* register (*los_flag_on_TDO*) is set, then the state of this bit is driven onto the TDO pin of the device.

Note…The flagging of the loss of the main reference failure on TDO is simply allowing the status of the sts_interrupt bit main_ref_failed (Reg. 06 Bit 6) to be reflected in the state of the TDO output pin. The pin will, therefore, remain High until the interrupt is cleared. This functionality is not enabled by default so the usual JTAG functions can be used. When the TDO output from the ACS8520 is connected to the TDI pin of the next device in the JTAG scan chain, the implementation should be such that a logic change caused by the action of the interrupt on the TDI input should not effect the operation when JTAG is not active.

Fast External Switching Mode-SCRSW Pin

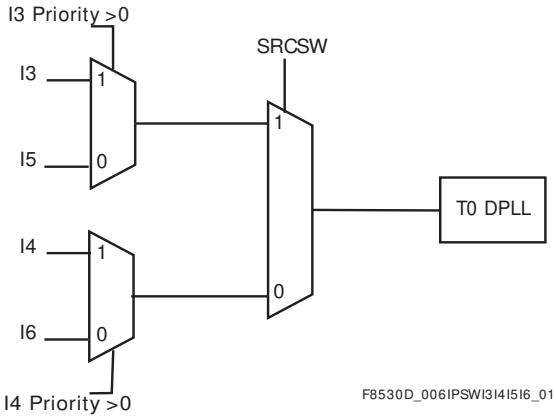
Fast external switching mode, for fast switching between inputs I3 or I5 and I4 or I6, can also be triggered directly from a dedicated pin SRCSW (Figure 4), once the mode has been initialized.

The mode is initialized by either holding SRCSW pin *High* during reset (SRCSW must remain *High* for at least a further 251 ms after PORB has gone *High* - see following Note), or by writing to Reg. 48 Bit 4. After External Protection Switching mode has been initialized, the value on this pin directly selects either I3/I5 (SRCSW *High*) or I4/I6 (SRCSW *Low*). If this mode is initialized at reset by pulling the SRCSW pin *High*, then it configures the default frequency tolerance of I3/I5 and I4/I6 to ±80 ppm (Reg. 41 and Reg. 42) as opposed to the normal frequency tolerance of ±9.2 ppm. Any of these registers can be subsequently set by external software, if required.

Note...The 251 ms comprises 250 ms allowance for the internal reset to be removed plus 1 ms allowance for APLLs to start-up and become stable.

Selection of either input I3 or I5 is determined by the Priority value of I3; if the programmed priority of I3 is 0, then I5 is selected. Similarly, I6 is selected if the programmed priority of I4 is 0.

Figure 4 I3/I5 and I4/I6 Switching



When external protection switching is enabled, the device will operate as a simple switch. All clock monitoring is disabled and the DPLL will simply be forced to try to lock on to the indicated reference source. Consequently the device will always indicate “locked” state in the *sts_operating* register (Reg. 09, Bits [2:0]).

Output Clock Phase Continuity on Source Switchover

If either PBO is selected on (default), or, if DPLL frequency limit is set to less than ±30 ppm or (±9.2 ppm default), the device will always comply with GR-1244-CORE[19] specification for Stratum 3 (maximum rate of phase change of 81 ns/1.326 ms), for all input frequencies.

Modes of Operation

The ACS8520 has three primary modes of operation (Free-run, Locked and Holdover) supported by three secondary, temporary modes (Pre-locked, Lost-phase and Pre-locked2). These are shown in the State Transition Diagram for the T0 DPLL, Figure 5.

The ACS8520 can operate in Forced or Automatic control. On reset, the ACS8520 reverts to Automatic Control, where transitions between states are controlled completely automatically. Forced Control can be invoked by configuration, allowing transitions to be performed under external control. This is not the normal mode of operation, but is provided for special occasions such as testing, or where a high degree of hands-on control is required.

Free-run Mode

The Free-run mode is typically used following a power-on-reset or a device reset before network synchronization has been achieved. In the Free-run mode, the timing and synchronization signals generated from the ACS8520 are based on the 12.800 MHz clock frequency provided from the external oscillator and are not synchronized to an input reference source. By default, the frequency of the output clock is a fixed multiple of the frequency of the external oscillator, and the accuracy of the output clock is equal to the accuracy of the oscillator. However the external oscillator frequency can be calibrated to improve its accuracy by a software calibration routine using register *cnfg_nominal_frequency* (Reg. 3C and 3D). For example a 500 ppm offset crystal could be made to look like one accurate to within ±0.02 ppm.

The transition from Free-run to Pre-locked occurs when the ACS8520 selects a reference source.

Pre-locked Mode

The ACS8520 will enter the Locked state in a maximum of 100 seconds, as defined by GR-1244-CORE[19] specification, if the selected reference source is of good quality. If the device cannot achieve lock within 100 seconds, it reverts to Free-run mode and another reference source is selected.

Locked Mode

The Locked mode is entered from Pre-locked, Pre-locked2 or Phase-lost mode when an input reference source has been selected and the DPLL has locked. The DPLL is

considered to be locked when the phase loss/lock detectors (see "Phase Lock/Loss Detection" on page 21) indicate that the DPLL has remained in phase lock continuously for at least one second. When the ACS8520 is in Locked mode, the output frequency and phase tracks that of the selected input reference source.

Lost-phase Mode

Lost-phase mode is used whenever the phase loss/lock detectors (see "Phase Lock/Loss Detection" on page 21) indicate that the DPLL has lost phase lock. The DPLL will still be trying to lock to the input clock reference, if it exists. If the Leaky Bucket Accumulator calculates that the anomaly is serious, the device disqualifies the reference source. If the device spends more than 100 seconds in Lost-phase mode, the reference is disqualified and a phase alarm is raised on it. If the reference is disqualified, one of the following transitions takes place:

1. Go to Pre-locked2;
   - If a known good stand-by source is available.
2. Go to Holdover;
   - If no stand-by sources are available.

Holdover Mode

Holdover mode is the operating condition the device enters when its currently selected input source becomes invalid, and no other valid replacement source is available. In this mode, the device resorts to using stored frequency data, acquired when the input reference source was still valid, to control its output frequency.

In Holdover mode, the ACS8520 provides the timing and synchronization signals to maintain the Network Element but is not phase locked to any input reference source. Its output frequency is determined by an averaged version of the DPLL frequency when last in the Locked Mode.

Holdover can be configured to operate in either:

- Automatic mode
  (Reg. 34 Bit 4, *cnfg_input_mode: man_holdover* set *Low*), or
- Manual mode
  (Reg. 34 Bit 4, *cnfg_input_mode: man_holdover* set *High*).

Automatic Mode

In Automatic mode, the device can be configured to operate using either:

- Averaged - (Reg. 40 Bit 7, *cnfg_holdover_modes, auto_averaging:* set *High*), or
- Instantaneous - (Reg. 40 Bit 7, *cnfg_holdover_modes, auto_averaging:* set *Low*).

Averaged

In the Averaged mode, the frequency (as reported by *sts_current_DPLL_frequency*, see Reg. 0C, Reg. 0D and Reg. 07) is filtered internally using an Infinite Impulse Response filter, which can be set to either:

- Fast - (Reg. 40 Bit 6, *cnfg_holdover_modes, fast_averaging:* set *High*), giving a -3 dB filter response point corresponding to a period of approximately eight minutes, or
- Slow - (Reg. 40 Bit 6, *cnfg_holdover_modes, fast_averaging:* set *Low*) giving a -3 dB filter response point corresponding to a period of approximately 110 minutes.

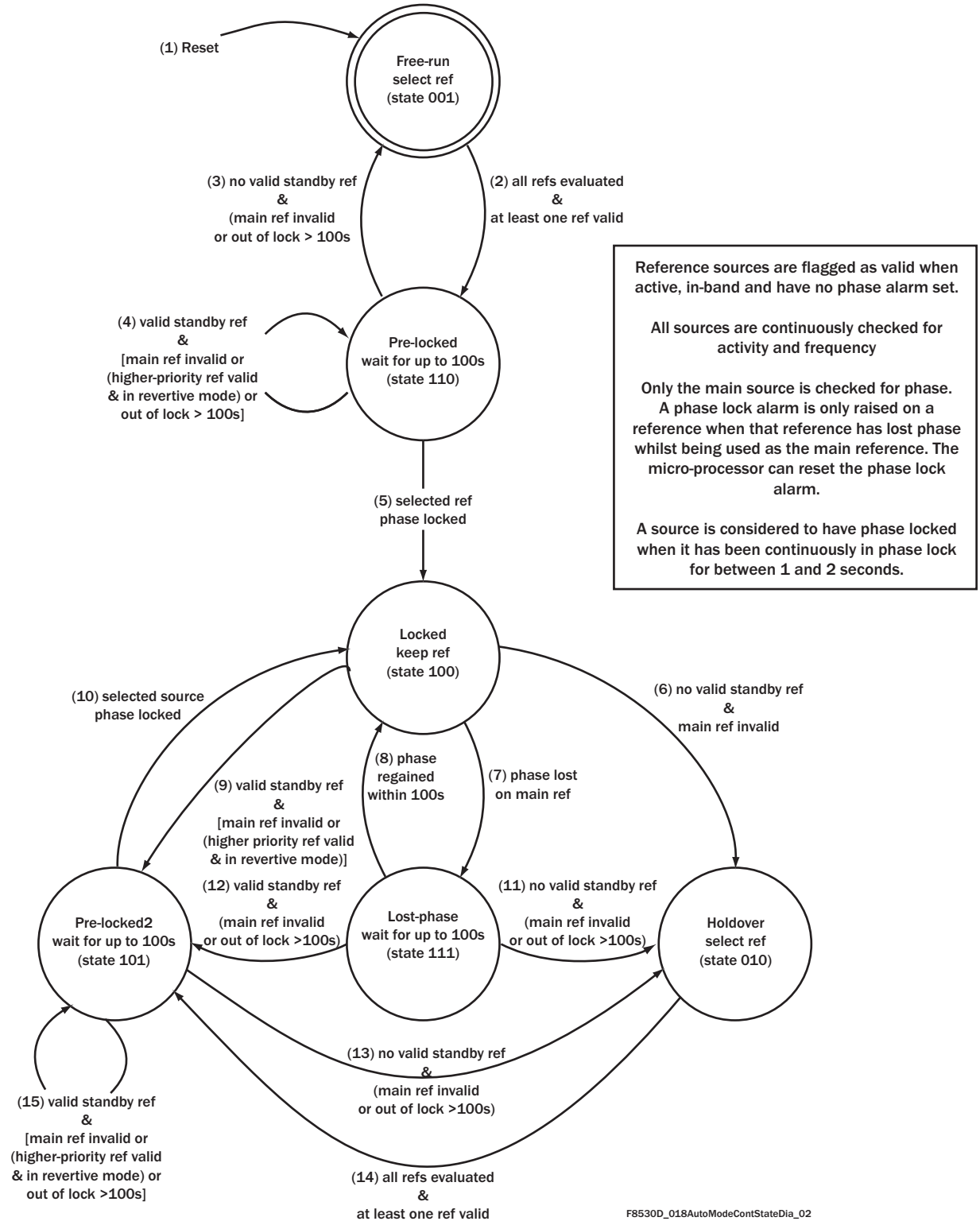
Instantaneous

In Instantaneous mode, the DPLL freezes at the frequency it was operating at the time of entering Holdover mode. It does this by using only its internal DPLL integral path value (as reported in Reg. 0C, 0D, and 07) to determine output frequency. The DPLL proportional path is not used so that any recent phase disturbances have a minimal effect on the Holdover frequency. The integral value used can be viewed as a filtered version of the locked output frequency over a short period of time. The period being in inverse proportion to the DPLL bandwidth setting.

Manual Mode

(Reg. 34 Bit 4, *cnfg_input_mode*, *man_holdover* set *High*.) The Holdover frequency is determined by the value in register *cnfg_holdover_frequency* (Reg. 3E, Reg. 3F, and part of Reg. 40). This is a 19-bit signed number, with a LSB resolution of 0.0003068 ppm, which gives an adjustment range of ±80 ppm. This value can be derived from a reading of register *sts_current_DPLL_frequency* (Reg. 0D, Reg. 0C and Reg. 07), which gives, in the same format, an indication of the current output frequency deviation, which would be read when the device is locked. If required, this value could be read by external software and averaged over time. The averaged value could then be fed to the *cnfg_holdover_frequency* register, ready for setting the averaged frequency value when the device enters Holdover mode. The *sts_current_DPLL_frequency* value is internally derived from the Digital Phase Locked Loop (DPLL) integral path, which represents a short-term average measure of the current frequency, depending on the locked loop bandwidth (Reg. 67) selected.

Figure 5 Automatic Mode Control State Diagram (T0 DPLL)



Note...The state diagram above is for T0 DPLL only, and the 3-bit state value refers to the register sts_operating Reg. 09 Bits [2:0] T0_DPLL_operating _mode. By contrast, the T4 DPLL has only automatic operation and can be in one of only two possible states: "Instantaneous Automatic Holdover" with zero frequency offset (its start-up state), or "Locked". The T4 DPLL states are not configurable by the User and there is no "Free-run" state.

It is also possible to combine the internal averaging filters with some additional software filtering. For example the internal fast filter could be used as an anti-aliasing filter and the software could further filter this before determining the actual Holdover frequency. To support this feature, a facility to read out the internally averaged frequency has been provided. By setting Reg. 40, Bit 5, *cnfg_holdover_modes*, *read_average,* the value read back from the *cnfg_holdover_frequency* register will be the filtered value. The filtered value is available regardless of what actual Holdover mode is selected. Clearly this results in the register not reading back the data that was written to it.

Example: Software averaging to eliminate temperature drift.

Select Manual Holdover mode by setting Reg. 34 Bit 4, *cnfg_input_mode, man_holdover High*.

Select Fast Holdover Averaging mode by setting Reg. 40 Bit 6, *cnfg_holdover_modes*, *auto_averaging High* and Reg. 40 Bit 7 *High*.

Select to be able to read back filtered output by setting Reg. 40 Bit 5, *cnfg_holdover_modes*, *read_average High*.

Software periodically reads averaged value from the *cnfg_holdover_frequency* register and the temperature (not supplied from ACS8520). Software processes frequency and temperature and places data in software look-up table or other algorithm. Software writes back appropriate averaged value into the *cnfg_holdover_frequency* register.

Once Holdover mode is entered, software periodically updates the *cnfg_holdover_frequency* register using the temperature information (not supplied from ACS8520).

Mini-holdover Mode

Holdover mode so far described refers to a state to which the internal state machine switches as a result of activity or frequency alarms, and this state is reported in Reg. 09. To avoid the DPLL's frequency being pulled off as a result of a failed input, then the DPLL has a fast mechanism to freeze its current frequency within one or two cycles of the input clock source stopping. Under these circumstances the DPLL enters Mini-holdover mode; the Mini-holdover frequency used being determined by Reg. 40, Bits [4:3], *cnfg_holdover_modes*, *mini_holdover_mode*.

Mini-holdover mode only lasts until one of the following happens:

- A new source has been selected, or
- The state machine enters Holdover mode, or
- The original fault on the input recovers.

External Factors Affecting Holdover Mode

If the external TCXO/ OCXO frequency is varying due to temperature fluctuations in the room, then the instantaneous value can be different from the average value, and then it may be possible to exceed the 0.05 ppm limit (depending on how extreme the temperature fluctuations are). It is advantageous to shield the TCXO/ OCXO to slow down frequency changes due to drift and external temperature fluctuations.

The frequency accuracy of Holdover mode has to meet the ITU-T, ETSI and Telcordia performance requirements. The performance of the external oscillator clock is critical in this mode, although only the frequency stability is important - the stability of the output clock in Holdover is directly related to the stability of the external oscillator.

Pre-locked2 Mode

This state is very similar to the Pre-Locked state. It is entered from the Holdover state when a reference source has been selected and applied to the phase locked loop. It is also entered if the device is operating in Revertive mode and a higher-priority reference source is restored.

Upon applying a reference source to the phase locked loop, the ACS8520 will enter the Locked state in a maximum of 100 seconds, as defined by GR-1244-CORE[19] specification, if the selected reference source is of good quality.

If the device cannot achieve lock within 100 seconds, it reverts to Holdover mode and another reference source is selected.

DPLL Architecture and Configuration

A Digital PLL gives a stable and consistent level of performance that can be easily programmed for different dynamic behavior or operating range. It is not affected by operating conditions or silicon process variations. Digital synthesis is used to generate all required SONET/ SDH output frequencies. The digital logic operates at 204.8 MHz that is multiplied up from the external 12.800 MHz oscillator module. Hence the best resolution

of the output signals from the DPLL is one 204.8 MHz cycle or 4.9 ns.

Additional resolution and lower final output jitter is provided by a de-jittering Analog PLL that reduces the 4.9 ns p-p jitter from the digital down to 500 ps p-p and 60 ps RMS as typical final outputs measured broadband (from 10 Hz to 1 GHz).

This arrangement combines the advantages of the flexibility and repeatability of a DPLL with the low jitter of an APLL. The DPLLs in the ACS8520 are uniquely very programmable for all PLL parameters of bandwidth (from 0.1 Hz up to 70 Hz), damping factor (from 1.2 to 20), frequency acceptance and output range (from 0 to 80 ppm, typically 9.2 ppm), input frequency (12 common SONET/ SDH spot frequencies) and input-to-output phase offset (in 6 ps steps up to 200 ns). There is no requirement to understand the loop filter equations or detailed gain parameters since all high level factors such as overall bandwidth can be set directly via registers in the microprocessor interface. No external critical components are required for either the internal DPLLs or APLLs, providing another key advantage over traditional discrete designs.

The T4 DPLL is similar in structure to the T0 DPLL, but since the T4 is only providing a clock synthesis and input to output frequency translation function, with no defined requirement for jitter attenuation or input phase jump absorption, then its bandwidth is limited to the high end and the T4 does not incorporate many of the Phase Build-out and adjustment facilities of the T0 DPLL.

TO DPLL Main Features

- Two programmable DPLL bandwidth controls (Locked and Acquisition bandwidth), each with 10 steps from 0.1 Hz to 70 Hz
- Programmable damping factor: For optional faster locking and peaking control. Factors = 1.2, 2.5, 5, 10 or 20
- Multiple phase lock detectors
- Input to output phase offset adjustment (Master/ Slave), ±200 ns, 6 ps resolution step size
- PBO phase offset on source switching - disturbance down to ±5 ns
- Multi-cycle phase detection and locking, programmable up to ±8192 UI - improves jitter tolerance in direct lock mode
- Holdover frequency averaging with a choice of averaging times: 8 minutes or 110 minutes and value can be read out
- Multiple E1 and DS1 outputs supported
- Low jitter MFrSync (2 kHz) and FrSync (8 kHz) outputs.

T4 DPLL Main Features

- A single programmable DPLL bandwidth control: 18 Hz, 35 Hz, or 70 Hz
- Programmable damping factor: For optional faster locking and peaking control. Factors = 1.2, 2.5, 5, 10 or 20
- Multiple phase lock detectors
- Multi-cycle phase detection and locking, programmable up to ±8192 UI - improves jitter tolerance in direct lock mode
- DS3/ E3 support (44.736 MHz / 34.368 MHz) at same time as OC-N rates from T0
- Low jitter E1/ DS1 options at same time as OC-N rates from T0
- Frequencies of n x E1/ DS1 including 16 and 12 x E1, and 16 and 24 x DS1 supported
- Low jitter MFrSync (2 kHz) and FrSync (8 kHz) outputs
- Can use the T4 DPLL as an Independent FrSync DPLL
- Can use the phase detector in T4 DPLL to measure the input phase difference between two inputs.

The structure of the T0 and T4 PLLs are shown later in Figure 11 in the section on output clock ports. That section also details how the DPLLs and particular output frequencies are configured. The following sections detail some component parts of the DPLL.

TO DPLL Automatic Bandwidth Controls

In Automatic Bandwidth Selection mode (Reg. 3B Bit 7), the T0 DPLL bandwidth setting is selected automatically from the Acquisition Bandwidth or Locked Bandwidth configurations programmed in *cnfg_T0_DPLL_acq_bw* Reg. 69 and *cnfg_T0_DPLL_locked_bw* Reg. 67 respectively. If this mode is not selected, the DPLL acquires and locks using only the bandwidth set by .

Phase Detectors

A Phase and Frequency detector is used to compare input and feedback clocks. This operates at input frequencies up to 77.76 MHz. The whole DPLL can operate at spot frequencies from 2 kHz up to 77.76 MHz (155.52 MHz is internally divided down to 77.76 MHz). A common arrangement however is to use Lock8k mode (See Reg. 22 to 2D, Bit 6) where all input frequencies are divided down to 8 kHz internally. Marginally better MTIE figures may be possible in direct lock mode due to more regular phase updates. This direct locking capability is one of the unique features of the ACS8520.

A patented multi-phase detector is used in order to give an infinitesimally small input phase resolution combined with large jitter tolerance. The following phase detectors are used:

- Phase and frequency detector (±360° or ±180° range)
- An Early/ Late Phase detector for fine resolution
- A multi-cycle phase detector for large input jitter tolerance (up to 8191 UI), which captures and remembers phase differences of many cycles between input and feedback clocks.

The phase detectors can be configured to be immune to occasional missing input clock pulses by using nearest edge detection (±180° capture) or the normal ±360° phase capture range which gives frequency locking. The device will automatically switch to nearest edge locking when the multi-UI phase detector is not enabled, and the other phase detectors have detected that phase lock has been achieved. It is possible to disable the selection of nearest edge locking via Reg. 03 Bit 6 set to 1. In this setting, frequency locking will always be enabled.

The balance between the first two types of phase detector employed can be adjusted via registers 6A to 6D. The default settings should be sufficient for all modes. Adjustment of these settings affects only small signal overshoot and bandwidth.

The multi-cycle phase detector is enabled via Reg. 74, Bit 6 set to 1 and the range is set in exponentially increasing steps from ±1 UI, 3 UI, 7 UI, 15 UI ... up to 8191 UI via Reg. 74, Bits [3:0]. When this detector is enabled it keeps a track of the correct phase position over many cycles of phase difference to give excellent jitter tolerance. This provides an alternative to switching to Lock8k mode as a method of achieving high jitter tolerance.

An additional control (Reg. 74 Bit 5) enables the multi-phase detector value to be used in the final phase value as part of the DPLL loop. When enabled by setting *High*, the multi cycle phase value will be used in the loop and gives faster pull in (but more overshoot). The characteristics of the loop will be similar to Lock8k mode where again large input phase differences contribute to the loop dynamics. Setting the bit *Low* only uses a max figure of 360 degrees in the loop and will give slower pull-in but gives less overshoot. The final phase position that the loop has to pull in to is still tracked and remembered by the multi-cycle phase detector in either case.

Phase Lock/ Loss Detection

Phase lock/ loss detection is handled in several ways. Phase loss can be triggered from:

- The fine phase lock detector, which measures the phase between input and feedback clock
- The coarse phase lock detector, which monitors whole cycle slips
- Detection that the DPLL is at min or max frequency
- Detection of no activity on the input.

Each of these sources of phase loss indication is individually enabled via register bits (see Reg. 73, 74 and 4D). Phase lock or lost is used to determine whether to switch to nearest edge locking and whether to use acquisition or normal bandwidth settings for the DPLL. Acquisition bandwidth is used for faster pull in from an unlocked state.

The coarse phase lock detector detects phase differences of n cycles between input and feedback clocks, where n is set by Reg. 74, Bits [3:0]; the same register that is used for the coarse phase detector range, since these functions go hand in hand. This detector may be used in the case where it is required that a phase loss indication is not given for reasonable amounts of input jitter and so the fine phase loss detector is disabled and the coarse detector is used instead.

Damping Factor Programmability

The DPLL damping factor is set by default to provide a maximum wander gain peak of around 0.1 dB. Many of the specifications (e.g. GR-1244-CORE[19], G.812[10] and G.813[11]) specify a wander transfer gain of less than 0.2 dB. GR-253[17] specifies jitter (not wander) transfer of less than 0.1 dB. To accommodate the required levels of transfer gain, the ACS8520 provides a choice of damping

factors, with more choice given as the bandwidth setting increases into the frequency regions classified as jitter. Table 5 shows which damping factors are available for selection at the different bandwidth settings, and what the corresponding jitter transfer approximate gain peak will be.

Table 5 Available Damping Factors for different DPLL Bandwidths, and associated Jitter Peak Values

Bandwidth	Reg. 6B [2:0]	Damping Factor selected	Gain Peak/ dB
0.1 Hz to 4 Hz	1, 2, 3, 4, 5	5	0.1
8 Hz	1	2.5	0.2
	2, 3, 4, 5	5	0.1
18 Hz	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

Local Oscillator Clock

The Master system clock on the ACS8520 should be provided by an external clock oscillator of frequency 12.800 MHz. The clock specification is important for meeting the ITU/ETSI and Telcordia performance requirements for Holdover mode. ITU and ETSI specifications permit a combined drift characteristic, at constant temperature, of all non-temperature-related parameters, of up to 10 ppb per day. The same specifications allow a drift of 1 ppm over a temperature range of 0 to +70° C.

Table 6 ITU and ETSI Specification

Parameter	Value
Tolerance	±4.6 ppm over 20 year lifetime
Drift (Frequency Drift over supply voltage range of +2.7 V to +3.3 V)	±0.05 ppm/ 15 seconds @ constant temp.
	±0.01 ppm/ day @ constant temp.
	±1 ppm over temp. range 0 to +70° C

Telcordia specifications are somewhat tighter, requiring a non-temperature-related drift of less than 40 ppb per day and a drift of 280 ppb over the temperature range 0 to +50° C. Please contact Semtech for information on crystal oscillator suppliers

Table 7 Telcordia GR-1244 CORE Specification

Parameter	Value
Tolerance	±4.6 ppm over 20 year lifetime
Drift (Frequency Drift over supply voltage range of +2.7 V to +3.3 V)	±0.05 ppm/ 15 seconds @ constant temp.
	±0.04 ppm/ 15 seconds @ constant temp.
	±0.28 ppm/ over temp. range 0 to +50° C

Crystal Frequency Calibration

The absolute crystal frequency accuracy is less important than the stability since any frequency offset can be compensated by adjustment of register values in the IC. This allows for calibration and compensation of any crystal frequency variation away from its nominal value. ±50 ppm adjustment would be sufficient to cope with most crystals, in fact the range is an order of magnitude larger due to the use of two 8-bit register locations. The setting of the *conf_nominal_frequency* register allows for this adjustment. An increase in the register value increases the output frequencies by 0.0196229 ppm for each LSB step.

The default register value (in decimal) = 39321 (9999 hex) = 0 ppm offset. The minimum to maximum offset range of the register is 0 to 65535 dec, giving an adjustment range of -771 ppm to +514 ppm of the output frequencies, in 0.0196229 ppm steps.

Example: If the crystal was oscillating at 12.800 MHz + 5 ppm, then the calibration value in the register to give a -5 ppm adjustment in output frequencies to compensate for the crystal inaccuracy, would be:
39321 - (5/ 0.0196229) = 39066 (dec) = 989A (hex).

Output Wander

Wander and jitter present on the output clocks are dependent on:

- The magnitudes of wander and jitter on the selected input reference clock (in Locked mode)
- The internal wander and jitter transfer characteristic (in Locked mode)
- The jitter on the local oscillator clock
- The wander on the local oscillator clock (in Holdover mode).

Wander and jitter are treated in different ways to reflect their differing impacts on network design. Jitter is always strongly attenuated, whilst wander attenuation can be varied to suit the application and operating state. Wander and jitter attenuation is performed using a digital phase locked loop (DPLL) with a programmable bandwidth. This gives a transfer characteristic of a low pass filter, with a programmable pole. It is sometimes necessary to change the filter dynamics to suit particular circumstances - one example being when locking to a new source, the filter can be opened up to reduce locking time and can then be tightened again to remove wander. A change between different bandwidths for locking and for acquisition is handled automatically within the ACS8520.

There may be a phase shift across the ACS8520 between the selected input reference source and the output clock over time, mainly caused by frequency wander in the external oscillator module. Higher stability XOs will give better performance for MTIE. The oscillator becomes more critical at DPLL bandwidth near to or below 0.1 Hz since the rate of change of the DPLL may be slow compared to the rate of change of the oscillator frequency. Shielding of the OCXO or TCXO can further slow down the rate of change of temperature and hence frequency, thus improving output wander performance.

The phase shift may vary over time but will be constrained to lie within specified limits. The phase shift is characterized using two parameters, MTIE (Maximum Time Interval Error) and TDEV (Time Deviation) which, although being specified in all relevant specifications, differ in acceptable limits in each one.

Typical measurements for the ACS8520 are shown in Figure 6, for Locked mode operation. Figure 7 shows a typical measurement of Phase Error accumulation in Holdover mode operation.

The required performance for phase variation during Holdover is specified in several ways and depends on the relevant specification (See “References” on page 146), for example:

1. ETSI ETS-300 462-5[4], Section 9.1, requires that the short-term phase error during switchover (i.e. Locked to Holdover to Locked) be limited to an accumulation rate no greater than 0.05 ppm during a 15 second interval.

2. ETSI ETS-300 462-5[4], Section 9.2, requires that the long-term phase error in the Holdover mode should not exceed
   $\{(a1 + a2)S + 0.5bS^2 + c\}$
   where
   a1 = 50 ns/s (allowance for initial frequency offset)
   a2 = 2000 ns/s (allowance for temperature variation)
   $b = 1.16 \times 10^{-4}$ ns/s^2 (allowance for ageing)
   c = 120 ns (allowance for entry into Holdover mode).
   S = Elapsed time (s) after loss of external ref. input

3. ANSI Tin1.101-1999[1], Section 8.2.2, requires that the phase variation be limited so that no more than 255 slips (of 125 µs each) occur during the first day of Holdover. This requires a frequency accuracy better than:
   ((24x60x60)+(255x125µs))/(24x60x60) = 0.37 ppm
   Temperature variation is not restricted, except to within the normal bounds of 0 to 50° C.

4. Telcordia GR-1244-CORE[19], Section 5.2, shows that an initial frequency offset of 50 ppb is permitted on entering Holdover, whilst a drift over temperature of 280 ppb is allowed; an allowance of 40 ppb is permitted for all other effects.

5. ITU G.822[12], Section 2.6, requires that the slip rate during category (b) operation (interpreted as being applicable to Holdover mode operation) be limited to less than 30 slips (of 125 µs each) per hour.

   ((60 x 60) + (30 x 125 µs))/(60 x 60)) = 1.042 ppm

Figure 6 Maximum Time Interval Error and Time Deviation of T0 PLL Output Port

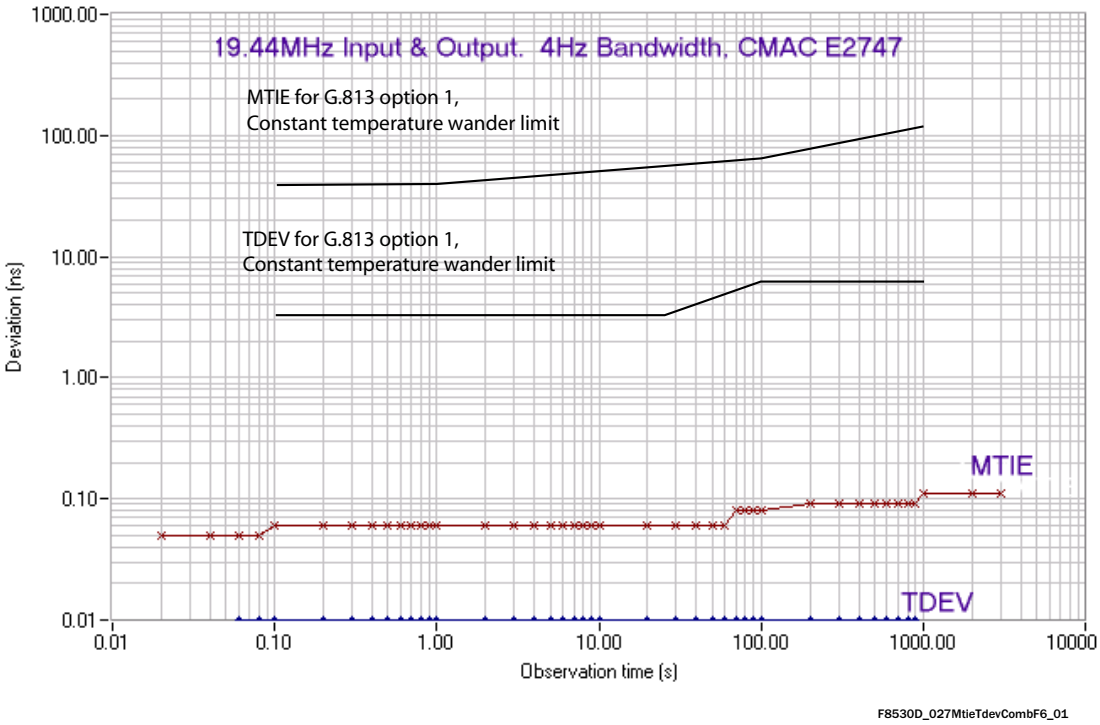
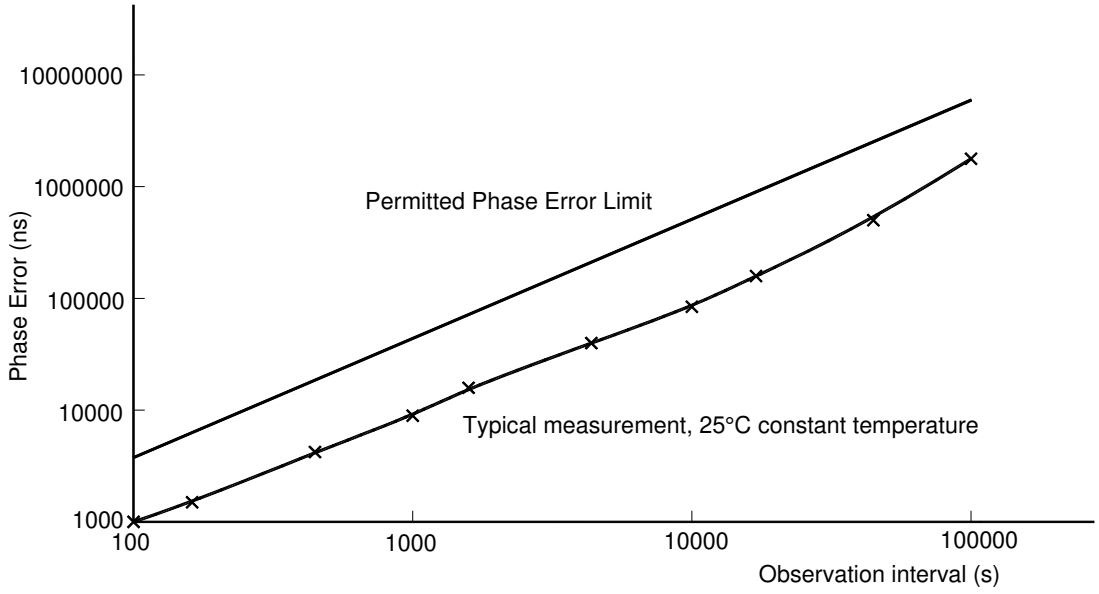


Figure 7 Phase Error Accumulation of T0 PLL Output Port in Holdover Mode



Jitter and Wander Transfer

The ACS8520 has a programmable jitter and wander transfer characteristic. This is set by the DPLL bandwidth. The -3 dB jitter transfer attenuation point can be set in the range from 0.1 Hz to 70 Hz in 10 steps. The wander and jitter transfer characteristic is shown in Figure 8. Wander on the local oscillator clock will not have a significant effect on the output clock whilst in Locked mode, provided that the DPLL bandwidth is set high enough so that the DPLL can compensate quickly enough for any frequency changes in the crystal.

In Free-run or Holdover mode wander on the crystal is more significant. Variation in crystal temperature or supply voltage both cause drifts in operating frequency, as does ageing. These effects must be limited by careful selection of a suitable component for the local oscillator, as specified in the section See Local Oscillator Clock.

Phase Build-out

Phase Build-out (PBO) is the function to minimize phase transients on the output SEC clock during input reference switching. If the currently selected input reference clock source is lost (due to a short interruption, out of frequency detection, or complete loss of reference) the second, next highest priority reference source will be selected, and a PBO event triggered.

ITU-T G.813[11] states that the maximum allowable short-term phase transient response, resulting from a switch from one clock source to another, with Holdover mode entered in between, should be a maximum of 1 µs over a 15 second interval. The maximum phase transient or jump should be less than 120 ns at a rate of change of less than 7.5 ppm and the Holdover performance should be better than 0.05 ppm. The ACS8520 performance is well within this requirement. The typical phase disturbance on clock reference source switching will be less than 5 ns on the ACS8520.

When a PBO event is triggered, the device enters a temporary Holdover state. When in this temporary state, the phase of the input reference is measured, relative to the output. The device then automatically accounts for any measured phase difference and adds the appropriate phase offset into the DPLL to compensate. Following a PBO event, whatever the phase difference on change of input, the output phase transient is minimized to be no greater than 5 ns.

On the ACS8520, PBO can be enabled, disabled or frozen using the microprocessor interface. By default, it is enabled. When PBO is enabled, PBO can also be frozen (at the current offset setting). The device will then ignore any further PBO events occurring on any subsequent

Figure 8 Sample of Wander and Jitter Measured Transfer Characteristics