Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ACS8525 LC/P

Line Card Protection Switch for SONET/SDH Systems

Description

The ACS8525 is a highly integrated, single-chip solution for "Hit-less" protection switching of SEC (SDH/SONET Equipment Clock) + Sync clock "Groups", from Master and Slave SETS clock cards and a third (Stand-by) source, for Line Cards in a SONET or SDH Network Element. The ACS8525 has fast activity monitors on the SEC clock inputs and will implement automatic system protection switching against the Master clock failure. The selection of the Master/Slave input can be forced by a Force Fast Switch pin. If both the Master and Slave input clocks fail, the Stand-by "Group" is selected or, if no Stand-by is available, the device enters Digital Holdover mode.

The ACS8525 can perform frequency translation, converting, for example, an 8 kHz SEC input clock from a backplane into a 155.52 MHz clock for local line cards.

Master and Slave SEC inputs to the device support TTL/CMOS and PECL/LVDS. The Stand-by SEC and three Sync inputs are TTL/CMOS only.

The ACS8525 generates two SEC clock outputs, via one PECL/LVDS and one TTL/CMOS port, with spot frequencies from 2 kHz up to 311.04 MHz (up to 155.52 MHz on the TTL/CMOS port). It also provides an 8 kHz Frame Sync and a 2 kHz Multi-Frame Sync signal output with programmable pulse width and polarity.

The ACS8525 includes a Serial Port, which can be SPI compatible, providing access to the configuration and status registers for device setup.

IEEE 1149.1 JTAG Boundary Scan is supported.

Features

- SONET/SDH applications up to OC-3/STM-1 bit rates
- Switches between grouped inputs (SEC/Sync pairs)
- Inputs: three SECs at any of 2, 4, 8 kHz (and N x 8 kHz multiples up to 155.52 MHz), plus Frame Sync/Multi-Frame Sync
- Outputs: two SEC clocks at any of several spot frequencies from 2 kHz up to 77.76 MHz via the TTL/CMOS port and up to 311.04 MHz via the PECL/LVDS port
- Selectable clock I/O port technologies
- Modes for E3/DS3 and multiple E1/DS1 rate output clocks
- Frequency translation of SEC input clock to a different local line card clock
- Robust input clock source activity monitoring on all inputs
- Supports Free-run, Locked and Digital Holdover modes of operation
- Automatic "Hit-less" source switchover on loss of input
- External force fast switch between SEC1/SEC2 inputs
- Phase Build-out for output clock phase continuity during input switchover
- PLL "Locked" and "Acquisition" bandwidths individually selectable from 18, 35 or 70 Hz
- Serial interface for device set-up
- Single 3.3 V operation, 5 V I/O compatible
- Operating temperature (ambient) of -40 to +85° C
- Available in LQFP 64 package
- Lead (Pb)-free version available (ACS8525T), RoHS and WEEE compliant

Block Diagram

Figure 1 Block Diagram of the ACS8525 LC/P

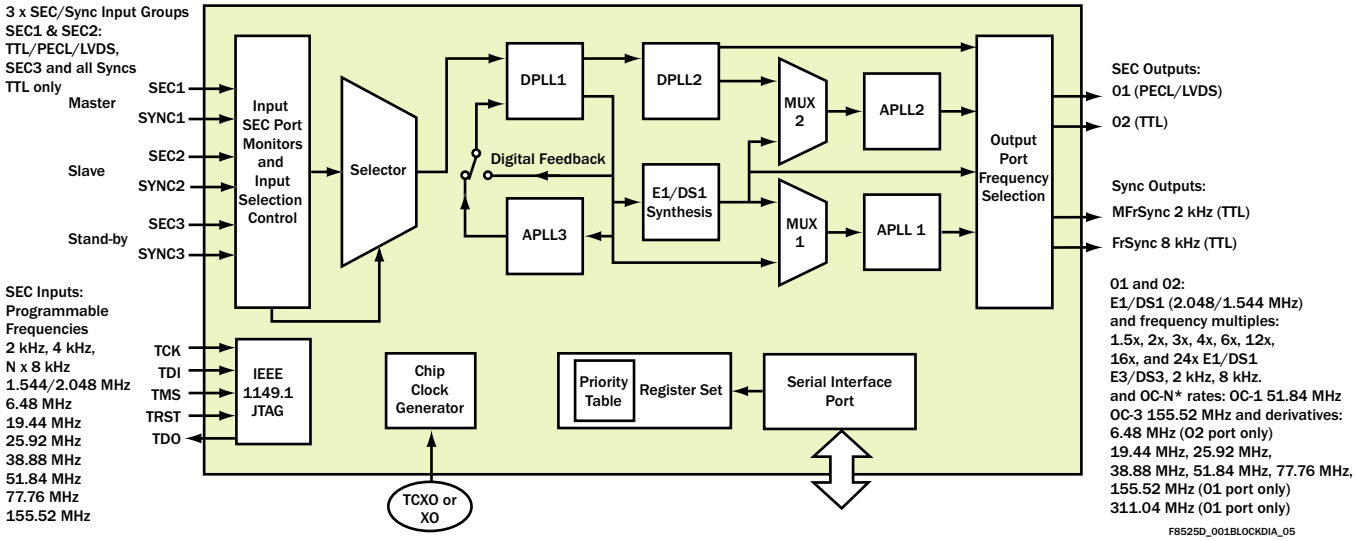


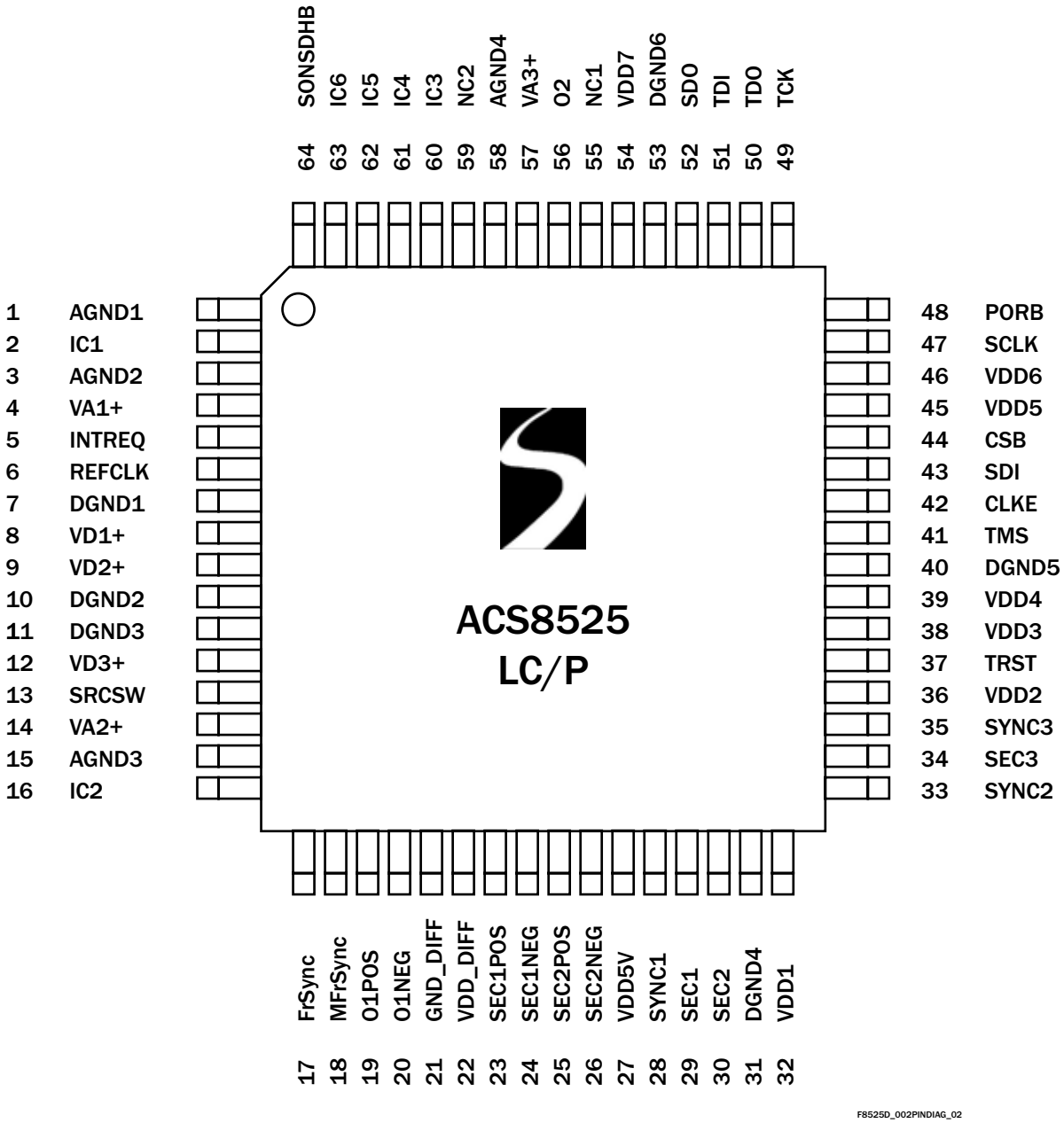
Table of Contents

Section **Page**

Section Page

Pin Diagram

Figure 2 ACS8525 Pin Diagram Line Card Protection Switch for SONET/SDH Systems



Pin Description

Table 1 Power Pins

Pin Number	Symbol	I/O	Type	Description
8, 9, 12	VD1+, VD2+, VD3+	P	-	Supply Voltage: Digital supply to gates in analog section, +3.3 Volts ±10%.
22	VDD_DIFF	P	-	Supply Voltage: Digital supply for differential output pins 19 and 20, +3.3 Volts ±10%.
27	VDD5V	P	-	Digital Supply for +5 Volts Tolerance to Input Pins. Connect to +5 Volts (±10%) for clamping to +5 Volts. Connect to VDD for clamping to +3.3 Volts. Leave floating for no clamping. Input pins tolerant up to +5.5 Volts.
32, 36, 38, 39, 45, 46, 54	VDD1, VDD2, VDD3, VDD4, VDD5, VDD6, VDD7	P	-	Supply Voltage: Digital supply to logic, +3.3 Volts ±10%.
4	VA1+	P	-	Supply Voltage: Analog supply to clock multiplying PLL, +3.3 Volts ±10%.
14, 57	VA2+, VA3+	P	-	Supply Voltage: Analog supply to output PLLs APLL2 and APPL1, +3.3 Volts ±10%.
15, 58	AGND3, AGND4		-	Supply Ground: Analog ground for output PLLs APLL2 and APPL1.
7, 10, 11	DGND1, DGND2, DGND3	P	-	Supply Ground: Digital ground for components in PLLs.
31, 40, 53	DGND4, DGND5, DGND6	P	-	Supply Ground: Digital ground for logic.
21	GND_DIFF	P	-	Supply Ground: Digital ground for differential ports.
1, 3	AGND1, AGND2	P	-	Supply Ground: Analog grounds.

Note ...I = Input, O = Output, P = Power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor.

Table 2 Internally Connected

Pin Number	Symbol	I/O	Type	Description
2, 16, 60, 61, 62, 63	IC1, IC2, IC3, IC4, IC5, IC6,	-	-	Internally Connected: Leave to float.
55, 59	NC1, NC2	-	-	Not Connected: Leave to float.

Table 3 Other Pins

Pin Number	Symbol	I/O	Type	Description
5	INTREQ	O	TTL/CMOS	Interrupt Request: Active *High*/*Low* software Interrupt output.
6	REFCLK	I	TTL	Reference Clock: 12.800 MHz (refer to section headed Local Oscillator Clock).
13	SRCSW	I	TTL_D	Source Switching: Force Fast Source Switching on SEC1 and SEC2.

Table 3 Other Pins (cont...)

Pin Number	Symbol	I/O	Type	Description
17	FrSync	O	TTL/CMOS	Output Reference: 8 kHz Frame Sync output.
18	MFrSync	O	TTL/CMOS	Output Reference: 2 kHz Multi-Frame Sync output.
19, 20	O1POS, O1NEG	O	LVDS/PECL	Output Reference: Programmable, default 38.88 MHz, LVDS.
23, 24	SEC1_POS, SEC1_NEG	I	PECL/LVDS	Input Reference: Programmable, default 19.44 MHz, PECL.
25, 26	SEC2_POS, SEC2_NEG	I	PECL/LVDS	Input Reference: Programmable, default 19.44 MHz PECL.
28	SYNC1	I	TTL_D	(Master) Multi-Frame Sync 2kHz Input: Connect to 2 or 8 kHz Multi-Frame Sync output of Master SETS.
29	SEC1	I	TTL_D	(Master) Input Reference: Programmable, default 8 kHz.
30	SEC2	I	TTL_D	(Slave) Input Reference: Programmable, default 8 kHz.
33	SYNC2	I	TTL_D	(Slave) Multi-Frame Sync 2 kHz: Connect to 2 or 8 kHz Multi-Frame Sync output of Slave SETS.
34	SEC3	I	TTL_D	(Stand-by) Input Reference: External stand-by reference clock source, programmable, default 19.44MHz.
35	SYNC3	I	TTL_D	(Stand-by) Input Reference: External stand-by 2 or 8 kHz Multi-Frame Sync clock source.
37	TRST	I	TTL_D	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 is Boundary Scan stand-by mode, still allowing normal device operation (JTAG logic transparent). NC if not used.
41	TMS	I	TTL_D	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. NC if not used.
42	CLKE	I	TTL_D	SCLK Edge Select: SCLK active edge select, CLKE = 1, selects falling edge of SCLK to be active.
43	SDI	I	TTL_D	Serial Interface Address: Serial Data Input.
44	CSB	I	TTL^U	Chip Select (Active *Low*): This pin is asserted *Low* by the microprocessor to enable the microprocessor interface.
47	SCLK	I	TTL_D	Serial Data Clock. When this pin goes *High* data is latched from SDI pin.
48	PORB	I	TTL^U	Power-On Reset: Master reset. If PORB is forced *Low*, all internal states are reset back to default values.
49	TCK	I	TTL_D	JTAG Clock: Boundary Scan clock input.
50	TDO	O	TTL/CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK.
51	TDI	I	TTL_D	JTAG Input: Serial test data Input. Sampled on rising edge of TCK.
52	SDO	O	TTL_D	Interface Address: SPI compatible Serial Data Output.
56	O2	O	TTL/CMOS	Output Reference: Programmable, default 19.44 MHz.
64	SONSDHB	I	TTL_D	SONET or SDH Frequency Select: Sets the initial power-up state (or state after a PORB) of the SONET/SDH frequency selection registers, Reg. 34, Bit 2 and Reg. 38, Bit 5, Bit 6 and Reg. 64 Bit 4. When set *Low*, SDH rates are selected (2.048 MHz etc.) and when set *High*, SONET rates are selected (1.544 MHz etc.) The register states can be changed after power-up by software.

Introduction

The ACS8525 is a highly integrated, single-chip solution for "Hit-less" protection switching of SEC + Sync clock "Groups", from Master and Slave SETS clock cards and a third (Stand-by) source, for Line Cards in a SONET or SDH Network Element. The ACS8525 has fast activity monitors on the SEC clock inputs and will implement automatic system protection switching against failure of the selected clock. The selection of the Master/Slave input can be forced by a Force Fast Switch pin. The Stand-by "Group" is selected if both the Master and Slave input clocks fail, or, if not available, the device enters a Digital Holdover mode.

Digital Phase Locked Loop (DPLL) and Direct Digital Synthesis (DDS) methods are used in the device so that the overall PLL characteristics are very stable and consistent compared to traditional analog PLLs.

The ACS8525 has three SEC/SYNC input groups from which it can select any group as input. It generates independent clocks on outputs 01 and 02, with a total of 53 possible output frequencies, and generates two Sync outputs on outputs FrSync and MFrSync: 8 kHz Frame Synchronization (FrSync) signal and 2 kHz Multi-Frame Synchronization (MFrSync) signal.

The device has three main operating modes (states); Free-run, Locked, or Digital Holdover. In Free-Run mode, the ACS8525 generates a stable, low-noise clock signal at a frequency to the same accuracy as the external oscillator, or it can be made more accurate via software calibration to within ±0.02 ppm. In Locked mode, the ACS8525 selects the most appropriate of the three input SECs and generates a stable, low-noise clock signal locked to the selected reference. In Digital Holdover mode, the ACS8525 generates a stable, low-noise clock signal, adjusted to match the frequency of the last selected SEC.

One key architectural advantage that the ACS8525 has over traditional solutions is in the use of DPLL technology for precise and repeatable performance over temperature or voltage variations and between parts. The overall PLL bandwidth, loop damping, pull-in range and frequency accuracy are all determined by digital parameters that provide a consistent level of performance. An Analog PLL (APLL) takes the signal from the DPLL output and provides a lower jitter output. The APLL bandwidth is set four orders of magnitude higher than the DPLL bandwidth. This ensures that the overall system performance still maintains the advantage of consistent behavior provided by the digital approach.

The DPLLs are clocked by the external Oscillator module (TCXO or XO) so that the Free-run or Digital Holdover frequency stability is only determined by the stability of the external oscillator module. This second key advantage confines all temperature critical components to one well defined and pre-calibrated module, whose performance can be chosen to match the application.

All performance parameters of the DPLLs are programmable without the need to understand detailed PLL equations. Bandwidth, damping factor and lock range can all be set directly.

The ACS8525 includes an SPI compatible serial interface port, providing access to the configuration and status registers for device setup, external control and monitoring. The device is primarily controlled according to values in this Register block.

Each register (8-bit wide data field) is identified and referred to by its two-digit hexadecimal address and name, e.g. Reg. 7D *cnfg_interrupt*. The "Register Map" on page 38 summarizes the content of all of the registers, and each register is individually described in the subsequent Register Tables, organized in order of ascending Address (hexadecimal), in the "Register Descriptions" from page 42 onwards.

An Evaluation Board and intuitive GUI-based software package is available for this device to help designers learn how to use the ACS8525 and rapidly configure the device for particular applications. This has its own documentation: "ACS8525-EVB".

General Description

The following description refers to the Block Diagram (Figure 1 on page 1).

Inputs

The ACS8525 SETS device has input ports for input clock groups from three sources, typically Master, Slave and Stand-by, where each clock group comprises one SEC and optionally one Sync signal. This is so that when any SEC input changeover is made, the corresponding Sync signal changeover is also made.

TTL/CMOS and PECL/LVDS ports are provided for the Master and Slave SEC inputs to the device. The Stand-by SEC input and three Frame Sync/Multi-frame Sync inputs to the device are via TTL Ports. All the TTL/CMOS parts are 3 V and 5 V compatible (with clamping if required by connecting the VDD5V pin). Refer to the "Electrical

Specifications" on page 98 for more information on electrical compatibility.

Input frequencies supported range from 2 kHz to 155.52 MHz. Common E1, DS1, OC-3 and sub-divisions are supported as spot frequencies that the DPLLs will directly lock to. Any input frequency, up to 100 MHz, that is a multiple of 8 kHz can also be locked to via an inbuilt programmable divider.

Preconfiguring Inputs

Each input device has to be preconfigured with:

- Expected input frequency *cnfg_ref_source_frequency* register (Reg. 22 to 25 and Reg. 28)
- Technology (TTL or PECL/ LVDS) where applicable, via *cnfg_differential_inputs* (Reg. 36)
- Selection Priority (Reg. 19, 1A and 1C).

Table 4 gives details of the input reference ports, showing the input technologies and the range of frequencies supported on each port; the default spot frequencies and default priorities assigned to each port on power-up or by reset are also shown.

SDH and SONET networks use different default frequencies; the network type is selectable using the *cnfg_input_mode* Reg. 34 Bit 2, *ip_sonsdhb*.

- For SONET, *ip_sonsdhb* = 1
- For SDH, *ip_sonsdhb* = 0

On power-up or by reset, the default will be set by the state of the SONSDHB pin (pin 64). Specific frequencies and priorities are set by configuration.

The frequency selection is programmed via the *cnfg_ref_source_frequency* register (Reg. 22 - Reg. 28).

Table 4 Input Reference Source Selection and Priority Table

Port Name	Channel Number (Bin)	Input Port Technology	Frequencies Supported	Default Priority
SEC1 TTL	0011	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 8 kHz Default (SDH): 8 kHz	2
SEC2 TTL	0100	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 8 kHz Default (SDH): 8 kHz	3
SEC1 DIFF	0101	PECL/ LVDS PECL default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	0
SEC2 DIFF	0110	PECL/ LVDS PECL default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	0
SYNC1	0111	TTL/ CMOS	2/ 4/ 8 kHz auto-sensing	n/ a
SYNC2	1000	TTL/ CMOS	2/ 4/ 8 kHz auto-sensing	n/ a
SEC3	1001	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	4
SYNC3	1010	TTL/ CMOS	2/ 4/ 8 kHz auto-sensing	n/ a

Notes: (i) TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies are: 2 kHz, 4 kHz, 8 kHz (and N x 8 kHz), 1.544 MHz (SONET)/2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz. SONET or SDH input rate is selected via Reg. 34 Bit 2, ip_sonsdhb).

(ii) PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz (and 311.04 MHz for Output O1 only).

(iii) SEC1 TTL and SEC2 TTL ports are on pins SEC1 and SEC2. SEC1 DIFF (Differential) port uses pins SEC1POS and SEC1NEG, similarly SEC2DIFF uses pins SEC2POS and SEC2NEG.

PECL/ LVDS Input Port Selection

The choice of PECL or LVDS compatibility is programmed via the *cnfg_differential_inputs* register. Unused PECL differential inputs should be fixed with one input *High* (VDD) and the other input *Low* (GND), or set in LVDS mode and left floating, in which case one input is internally pulled *High* and the other *Low*.

Input Locking Frequency Modes

Each input port has to be configured to receive the expected input frequency. To achieve this, three Input Locking Frequency modes are provided: Direct Lock, Lock8K and DivN.

Direct Lock Mode

In Direct Lock mode, DPLL1 can lock to the selected input at the spot frequency of the input, for example 19.44 MHz performs the DPLL phase comparisons at 19.44 MHz.

In Lock8K and DivN modes (and for the special case of 155 MHz), an internal divider is used prior to DPLL1 to divide the input frequency before it is used for phase comparisons.

Direct Lock Mode 155 MHz.

The max frequency allowed for phase comparison is 77.76 MHz, so for the special case of a 155 MHz input set to Direct Lock mode, there is a divide-by-two function automatically selected to bring the frequency down to within the limits of operation.

Lock8K Mode

Lock8K mode automatically sets the divider parameters to divide the input frequency down to 8 kHz. Lock8K can only be used on the supported spot frequencies (see Table 4 Note(i)). Lock8k mode is enabled by setting the *Lock8k* bit (Bit 6) in the appropriate *cnfg_ref_source_frequency* register location. Using lower frequencies for phase comparisons in the DPLL results in a greater tolerance to input jitter. It is possible to choose which edge of the input reference clock to lock to, by setting *8K Edge Polarity* (Bit 2 of Reg. 03, *test_register1*).

DivN Mode

In DivN mode, the divider parameters are set manually by configuration (Bit 7 of the *cnfg_ref_source_frequency* register), but must be set so that the frequency after division is 8 kHz.

The DivN function is defined as:

DivN = "Divide by N + 1", i.e. it is the dividing factor used for the division of the input frequency, and has a value of (N + 1) where N is an integer from 1 to 15624 inclusive.

Therefore, in DivN mode the input frequency can be divided by any integer value between 2 to 15625. Consequently, any input frequency which is a multiple of 8 kHz, between 8 kHz and 125 MHz, can be supported by using DivN mode.

Note...Any reference input can be set to use DivN independently of the frequencies and configurations of the other inputs. However only one value of N is allowed, so all inputs with DivN selected must be running at the same frequency.

DivN Examples

(a) To lock to 2.000 MHz:

(i) Set the *cnfg_ref_source_frequency* register to 10XX0000 (binary) to enable DivN, and set the frequency to 8 kHz - the frequency required after division. (XX = "Leaky Bucket" ID for this input).

(ii) To achieve 8 kHz, the 2 MHz input must be divided by 250. So, if DivN = 250 = (N + 1) then N must be set to 249. This is done by writing F9 hex (249 decimal) to the DivN register pair Reg. 46/47.

(b) To lock to 10.000 MHz:

(i) The *cnfg_ref_source_frequency* register is set to 10XX0000 (binary) to set the DivN and the frequency to 8 kHz, the post-division frequency. (XX = "Leaky Bucket" ID for this input).

(ii) To achieve 8 kHz, the 10 MHz input must be divided by 1,250. So, if DivN, = 250 = (N+1) then N must be set to 1,249. This is done by writing 4E1 hex (1,249 decimal) to the DivN register pair Reg. 46/47.

Input SEC Activity Monitors

An input reference activity monitor is assigned to each of the three SEC inputs. The monitors operate continuously such that at all times the activity status of each SEC input is known.

SEC activity monitoring is used to declare whether or not an input is valid. Any SEC that suffers a loss-of-activity will be declared as invalid and unavailable for selection.

SEC activity monitoring is a continuous process which is used to identify clock problems. There is a difference in

dynamics between the selected clock and the other reference clocks. Anomalies occurring on non-selected SECs affect only that source's suitability for selection, whereas anomalies occurring on the selected clock could have a detrimental impact on the accuracy of the output clock.

Leaky Bucket Accumulator

Anomalies detected by the Activity Monitor are integrated in a Leaky Bucket Accumulator. There is one Leaky Bucket Accumulator per SEC input. Each Leaky Bucket can be programmed with a Bucket ID (0 to 3) which assigns to the Leaky Bucket the corresponding Leaky Bucket Configuration (from four available Configurations). Each Leaky Bucket Configuration comprises the following programmable parameters (See Reg. 50 to Reg. 5F):

- Bucket size
- Alarm trigger (set threshold)
- Alarm clear (reset threshold)
- Leak rate (decay rate)

There are occasional anomalies that do not cause the Accumulator to cross the alarm setting threshold, so the selected SEC is retained. Persistent anomalies cause the alarm setting threshold to be crossed and result in the selected SEC being rejected.

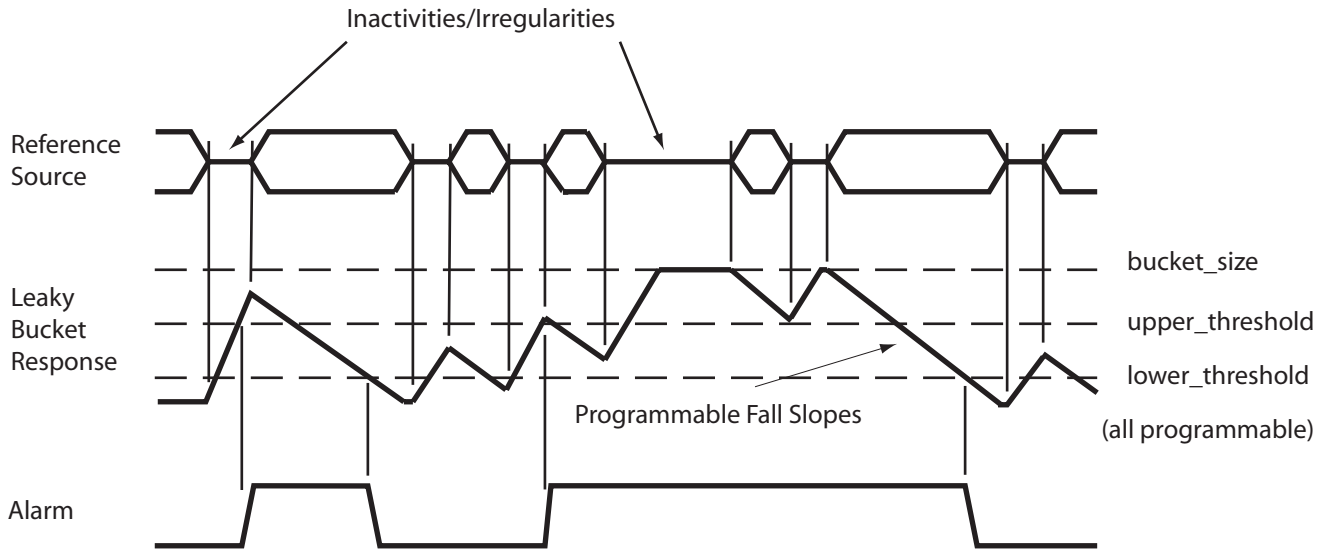
Each Leaky Bucket Accumulator is a digital circuit which mimics the operation of an analog integrator. If several events occur close together, each event adds to the amplitude and the alarm will be triggered quickly; if events occur over a greater time period but still sufficiently close together to overcome the decay, the alarm will be triggered eventually. If events occur at a rate which is not sufficient to overcome the decay, the alarm will not be triggered. Similarly, if no defect events occur for a sufficient time, the amplitude will decay gradually and the alarm will be cleared when the amplitude falls below the alarm clearing threshold. The ability to decay the amplitude over time allows the importance of defect events to be reduced as time passes by. This means that, in the case of isolated events, the alarm will not be set, whereas, once the alarm becomes set, it will be held on until normal operation has persisted for a suitable time (but if the operation is still erratic, the alarm will remain set).

Figure 3 illustrates the behavior of the Leaky Bucket Accumulator.

Each SEC input is monitored over a 128 ms period. If, within a 128 ms period, an irregularity occurs that is not deemed to be due to allowable jitter/ wander, then the accumulator is incremented.

The Accumulator will continue to increment up to the point that it reaches the programmed Bucket size. The “fill rate” of the Leaky Bucket is, therefore, 8 units/ second. The “leak rate” of the Leaky Bucket is programmable to be in multiples of the fill rate (x 1, x 0.5, x 0.25 and x 0.125) to give a programmable leak rate from 8 units/ sec down to 1 unit/ sec. A conflict between trying to “leak” at the same time as a “fill” is avoided by preventing a leak when a fill event occurs.

Figure 3 Inactivity and Irregularity Monitoring



Disqualification of a non-selected SEC is based on inactivity noted by the Activity Monitors. The currently selected SEC can be disqualified for being out-of phase, inactive, or if the source is outside the DPLL lock range.

If the currently selected SEC is disqualified, the next highest priority qualified SEC is selected.

Interrupts for Activity Monitors

The loss of the currently selected SEC will eventually cause the input to be considered invalid, triggering an interrupt. The time taken to raise this interrupt is dependant on the Leaky Bucket Configuration of the activity monitors. The fastest Leaky Bucket setting will still take up to 128 ms to trigger the interrupt. The interrupt caused by the brief loss of the currently selected SEC is provided to facilitate very fast source failure detection if desired. It is triggered after missing just a couple of cycles of the SEC. Some applications require the facility to switch downstream devices based on the status of the SECs. In order to provide extra flexibility, it is possible to flag the *main_ref_failed* interrupt (Reg. 06 Bit 6) on the pin TDO. This is simply a copy of the status bit in the interrupt register and is independent of the mask register settings. The bit is reset by writing to the interrupt status register in the normal way. This feature can be enabled and disabled by writing to Reg. 48 Bit 6.

Leaky Bucket Timing

The time taken (in seconds) to raise an inactivity alarm on an SEC that has previously been fully active (Leaky Bucket empty) will be:

$$(cnfg\_upper\_threshold\_n) \ / \ 8$$

where n is the number of the Leaky Bucket Configuration. If an input is intermittently inactive then this time can be longer. The default setting of *cnfg_upper_threshold_n* is 6, therefore the default time is 0.75 s.

The time taken (in seconds) to cancel the activity alarm on a previously completely inactive SEC is calculated, for a particular Leaky Bucket, as:

$$[2^{(a)} \times (b - c)] / 8$$

where:

a = cnfg_decay_rate_n
b = cnfg_Bucket_size_n
c = cnfg_lower_threshold_n
(where n = the number of the relevant Leaky Bucket Configuration in each case).

The default setting is shown in the following:

$$[2^{1} \times (8 - 4)] / 8 = 1.0 \text{ secs}$$

Fast Activity Monitor

Anomalies on the selected clock have to be detected as they occur and the PLL must be temporarily isolated until the clock is once again pure. The SEC activity monitoring process cannot be used for this because the high degree of accuracy required dictates that the process be slow. To achieve the immediacy required, the PLL requires an alternative mechanism. The phase locked loop itself contains a fast activity detector such that within approximately two missing input clock cycles, a no-activity flag is raised and the DPLL is frozen in Digital Holdover mode. This flag can also be read as the *DPLL1 main_ref_failed* bit (from Reg. 06 *sts_interrupts*, Bit 6) and can be set to indicate a phase lost state by enabling Reg. 73, Bit 6. With the DPLL in Digital Holdover mode it is isolated from further disturbances. If the input becomes available again before the activity monitor rejection alarm has been raised, then the DPLL will continue to lock to the input, with little disturbance. In this scenario, with the DPLL in the "locked" state, the DPLL uses "nearest edge locking" mode (±180° capture) avoiding cycle slips or glitches caused by trying to lock to an edge 360° away, as would happen with traditional PLLs.

Selector

This block has two main functions:

- Selection of the Input reference clock source via Reg. 33 *force_select_reference_source*
- Forcing of the Operating mode of the device, via Reg. 32 *cnfg_operating_mode*

Selection of Input SECs

Under normal operation, the input SECs are selected automatically by an order of priority given in the Priority Table. For special circumstances however, such as chip or board testing, the selection may be forced by configuration.

Automatic operation selects an SEC based on its predefined priority and its current validity. A table is maintained which lists all valid SECs in the order of priority. This is initially downloaded into the ACS8525 via the Serial interface by the Network Manager, and is subsequently modified by the results of the ongoing quality monitoring. In this way, when all the defined

sources are active and valid, the source with the highest programmed priority is selected, but if this source fails, the next-highest source is selected, and so on.

Restoration of repaired SECs is handled carefully to avoid inadvertent disturbance of the output clock. For this, the ACS8525 has two modes of operation; Revertive and Non-revertive.

In Revertive mode, if a re-validated (or newly validated) source has a higher priority than the SEC which is currently selected, a switchover will take place. Many applications prefer to minimize the clock switching events and choose Non-revertive mode.

In Non-revertive mode, when a re-validated (or newly validated) source has a higher priority, then the selected source will be maintained. The re-validation of the SEC will be flagged in the *sts_sources_valid* register (*Reg. 0E* and 0F) and, if not masked, will generate an interrupt. Selection of the re-validated source can take place under software control or if the currently selected source fails.

To enable software control, the software should briefly enable Revertive mode to effect a switch-over to the higher priority source. When there is a reference available with higher priority than the selected reference, there will be NO change of SEC as long as the Non-revertive mode remains on, and the currently selected source is valid. A failure of the selected reference will always trigger a switch-over regardless of whether Revertive or Non-revertive mode has been chosen.

Forced Control Selection

A configuration register, *force_select_reference_source* Reg. 33, controls both the choice of automatic or forced selection and the selection itself (when forced selection is required). For Automatic choice of source selection, the 4 LSB bit value *force_select_SEC_input* is set to all zeros or all ones (default). To force a particular input, the bit value is set according to the description for Reg. 33. Forced selection is not the normal mode of operation, and *force_select_SEC_input* defaults to the all-ones value on reset, thereby adopting the automatic selection of the SEC.

Automatic Control Selection - Priority Table

When an automatic selection is required, the *force_select_reference_source* register LSB 4 bits (*force_select_SEC_input*) must be set to all zeros or all ones.

The Priority Table register *cnfg_ref_selection_priority*, occupying three 8-bit register addresses (Reg. 19, 1A and 1C), is organized as one 4-bit word per input SEC port. Each 4 bit word represents the desired priority of that particular port. Unused ports should be given the value 0000 in the relevant register to indicate they are not to be included in the priority table. On power-up, or following a reset, the input priority configuration is set to the default values defined by Table 4. The selection priority values are all relative to each other, with lower-valued numbers taking higher priorities. Each SEC should be given a unique number; the valid values are 1 to 15 (dec). A value of 0 disables the SEC. However if two or more inputs are given the same priority number those inputs will be selected on a first in, first out basis. If the first of two same priority number sources goes invalid the second will be switched in. If the first then becomes valid again, it becomes the second source on the first in, first out basis, and there will not be a switch. If a third source with the same priority number as the other two becomes valid, it joins the priority list on the same first in, first out basis. There is no implied priority based on the channel numbers. Revertive/Non-revertive mode has no effect on sources with the same priority value.

The priority of Sync inputs is determined by the priority of their associated SEC inputs. The Sync inputs do not have their own separate priority table.

Ultra Fast Switching

An SEC is normally disqualified after the Leaky Bucket monitor thresholds have been crossed. An option for a faster disqualification has been implemented, whereby if Reg. 48 Bit 5 (*ultra_fast_switch*) is set, then a loss of activity of just two or three reference clock cycles causes a reference switch, and sets the *DPLL1_main_ref_failed* bit (see Reg. 06 Bit 6) which raises an interrupt (if not masked).

The *sts_interrupts* register Reg. 06 Bit 6 (*DPLL1_main_ref_failed*) is used to flag inactivity on the reference that the device is locked to much faster than the activity monitors can support. If Reg. 48 Bit 6 of the *cnfg_monitors* register (*los_flag_on_TDO*) is set, then the state of this bit is driven onto the TDO pin of the device.

Note...The flagging of the loss of the main reference failure on TDO is simply allowing the status of the sts_interrupts bit DPLL1_main_ref_failed to be reflected in the state of the TDO output pin. The pin will, therefore, remain High until the interrupt is cleared. This functionality is not enabled by default so the usual JTAG functions can be used. When the TDO output from the ACS8525 is connected to the TDI pin of the next

device in the JTAG scan chain, the implementation should be such that a logic change caused by the action of the interrupt on the TDI input should not effect the operation when JTAG is not active.

External Protection Switching Mode-SRCSW pin

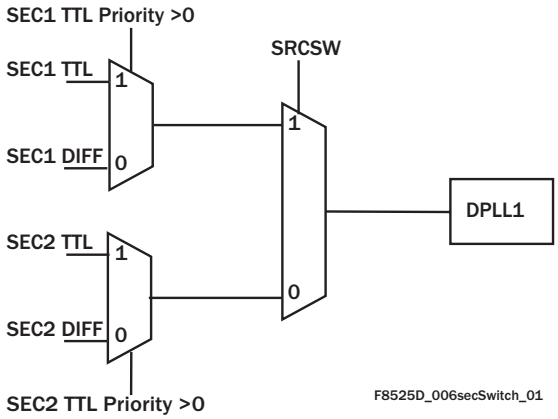
External Protection Switching mode, for fast switching between inputs SEC1 or SEC2, can be triggered directly from the dedicated pin SRCSW, once the mode has been initialized.

The mode is initialized by either holding SRCSW pin *High* during reset (SRCSW must remain *High* for at least a further 251 ms after PORB has gone *High* - see following Note), or by writing to Reg. 48 Bit 4. After External Protection Switching mode has been initialized, the value on this pin directly selects either SEC1 (SRCSW *High*) or SEC2 (SRCSW *Low*). If this mode is activated at reset by pulling the SRCSW pin *High*, then it configures the default frequency tolerance of SEC1 and SEC2 to ±80 ppm (Reg. 41 and Reg. 42), as opposed to the normal frequency tolerance of ±9.2 ppm. These registers can be subsequently set by external software, if required.

Note...The 251 ms comprises 250 ms allowance for the internal reset to be removed plus 1 ms allowance for APLLs to start-up and become stable.

The control of TTL or DIFF selection for inputs SEC1 and SEC2 is independently determined by the priority values of the TTL inputs; if the programmed priority of SEC1 TTL is 0, then SEC1 DIFF is available for selection by SRCSW pin; similarly, if SEC2 TTL is 0 priority, SEC2 DIFF is available for selection by SRCSW pin (See Reg. 19 and 1A *cnfg_ref_selection_priority* and Figure 4).

Figure 4 SEC1 and SEC2 Switching



When external protection switching is enabled, the device will operate as a simple switch. All clock monitoring is disabled and the DPLL will simply be forced to try to lock on to the indicated reference source. Consequently the device will always indicate "Locked" state in the operating mode register (Reg. 09, Bits 2:0).

Output Clock Phase Continuity on Source Switchover

If either PBO is selected on (default), or, if DPLL frequency limit set to less than ±30 ppm (±9.2 ppm default), the device will always comply with GR-1244-CORE[13] specifications for Stratum 3 (max rate of phase change of 81 ns/1.326 ms), for all input frequencies.

A well designed system would have Master and Slave clock from the clock sync cards aligned to within a few nanoseconds. In which case a complete system using the Semtech SETS clock card parts (ACS8530, ACS8520 or ACS8510) and this Line Card part would be fully compliant to GR-1244-CORE[13] specifications under all conditions due to the low frequency range and bandwidth set at the clock card end. These parts and the ACS8525 LC/P also allow easy frame sync (8 kHz) alignment both at the clock card and at the Line Card end through the use of dedicated frame sync (8 kHz) inputs, in addition to the main clock inputs.

Forcing of the Operating Mode of the Device

The Selector can force the following Operating modes, (*cnfg_operating_mode*, Reg. 32):

- Auto
- Free-run
- Holdover
- Locked
- Lost-phase
- Pre-locked
- Pre-locked2

See "Operating Modes (States) of the Device" on page 30.

Phase Locked Loops (PLLs)

PLL Overview

Figure 1 shows the PLL circuitry to comprise two Digital PLLs (DPLL1 and DPLL2), two output multiplying and filtering Analog PLLs (APLL1 and APLL2), output frequency dividers in an Output Port Frequency Selection block, a synthesis block, multiplexers MUX1 and MUX2, and a feedback Analog PLL (APLL3). These functional blocks, and their interconnections are highly configurable,

via register control, which provides a range of output frequencies and levels of jitter performance.

The DPLLs give a stable and consistent level of performance that can be easily programmed for different dynamic behavior or operating range. They are not affected by operating conditions or silicon process variations. Digital Synthesis is used to generate all required SONET/SDH output frequencies. The digital logic operates at 204.8 MHz that is multiplied up from the external 12.800 MHz oscillator module. Hence the best resolution of the output signals from the DPLLs is one 204.8 MHz cycle or 4.9 ns.

Additional resolution and lower final output jitter is provided by a de-jittering APLL that reduces the 4.9 ns p-p jitter from the digital down to 500 ps p-p and 60 ps RMS as typical final outputs measured broadband (from 10 Hz to 1 GHz).

This arrangement combines the advantages of the flexibility and repeatability of a DPLL with the low jitter of an APLL. The DPLLs in the ACS8525 are programmable for PLL parameters of bandwidth (18, 35 and 70 Hz), damping factor (from 1.2 to 20), frequency acceptance and output range (from 0 to 80 ppm, typically 9.2 ppm), input frequency (12 common SONET/SDH spot frequencies) and input-to-output phase offset (in 6 ps steps up to 200 ns). There is no requirement to understand the loop filter equations or detailed gain parameters since all high level factors such as overall bandwidth can be set directly via registers in the microprocessor interface. No external critical components are required for either the internal DPLLs or APLLs, providing another key advantage over traditional discrete designs.

Either the software or an internal state machine controls the operation of DPLL1. The state machine for DPLL2 is very simple and cannot be manually/externally controlled. One additional feature of DPLL2 is the ability to measure a phase difference between two inputs.

DPLL1 always produces an output at 77.76 MHz to feed the APLL, regardless of the frequency selected at the output pins or the locking frequency (frequency at the input of the Phase and Frequency Detector- PFD).

DPLL2 can be operated at a number of frequencies. This is to enable the generation of extra output frequencies, which cannot be easily related to 77.76 MHz. If DPLL2 is enabled, it locks to the 8 kHz from DPLL1. This is because all of the frequencies of operation of DPLL2 can be divided to 8 kHz and this will ensure synchronization of frequencies, from 8kHz upwards, within the two DPLLs.

Both of the DPLLs' outputs can be connected to multiplying and filtering APLLs. The outputs of these APLLs are divided making a number of frequencies simultaneously available for selection at the output clock ports. The various combinations of DPLL, APLL and divider configurations allow for generation of a comprehensive set of frequencies, as listed in Table 7, "Output Frequency Selection," on page 22.

A function is provided to synchronize the lower output frequencies when DPLL1 is locked to a high frequency reference input. The dividers that generate the 2 kHz and 8 kHz outputs are reset such that the output 2/8 kHz clocks are lined up with the input 2 kHz.

The ACS8525 also supports Sync pulse references of 4 kHz or 8 kHz although in these cases frequencies lower than the Sync pulse reference may not necessarily be in phase.

The PLL configurations for particular output frequencies is described in "Output Frequency Selection and PLL Configuration" on page 22.

PLL Architecture

Figure 5 shows the PLL arrangement in more detail. Each DPLL comprises a generic Phase and Frequency Detector (PFD), a Digital Loop filter, and a Digital Timed Oscillator (DTO- not shown); together with Forward, Feedback, and Low Frequency (LF) (DPLL1 only) Digital Frequency Synthesis (DFS) blocks. The DPLL architecture for DPLL1.

is actually more complex than that of DPLL2, and provides greater functionality.

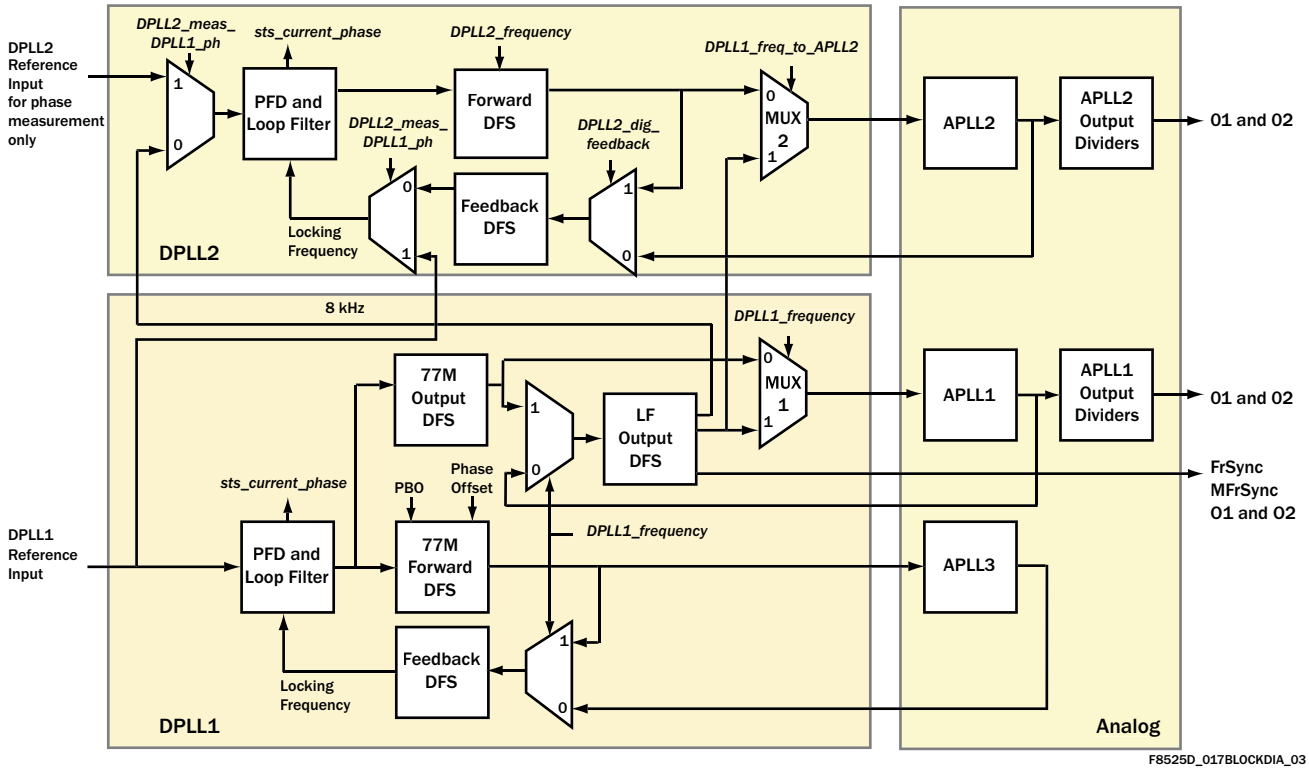
The selected SEC input is always supplied to DPLL1. DPLL1 may use either digital feedback or analog feedback (via APLL3).

DPLL2 always takes its feed from DPLL1 and cannot be used to select a different input to that of DPLL1, except in the case where the device is being used to measure phase difference between input sources. In this case, the PFD of DPLL2 is used for phase measurement and the DPLL2 normal output is rendered unusable.

DPLL1 and APLLs

DPLL1 always produces 77.76 MHz regardless of either the reference frequency (frequency at the input pin of the device) or the locking frequency (frequency at the input of the DPLL PFD).

Figure 5 PLL Block Diagram



The input reference is either passed directly to the PFD or via a pre-divider (not shown) to produce the reference input. The feedback 77.76 MHz is either divided or synthesized to generate the locking frequency.

Any Digital Frequency Synthesis (DFS) generated clock will inherently have jitter on it equivalent to one period of the generating clock (p-p). The DPLL1 77M Forward DFS block uses DFS clocked by the 204.8 MHz system clock to synthesize the 77.76 MHz and, therefore, has an inherent 4.9 ns of p-p jitter. There is an option to use a feedback APLL (APLL3) to filter out this jitter before the 77.76 MHz is used to generate the feedback locking frequency in the DPLL1 feedback DFS block. This analog feedback option allows a lower jitter (<1 ns) feedback signal to give maximum performance.

The DPLL1 77M Forward DFS block is also the block that handles Phase Build-out and any phase offset programmed into the device. Hence, the DPLL1 77M Forward DFS and the DPLL1 77M Output DFS blocks are locked in frequency but may be offset in phase.

The DPLL1 77M Output DFS block also uses the 204.8 MHz system clock and always generates 77.76 MHz for the output clocks (with inherent 4.9 ns of jitter). This is fed to DPLL1 LF Output DFS block and to APLL1. The low frequency DPLL1 LF Output DFS block is used to produce three frequencies; two of them, Digital1 and Digital2, are available for selection to be produced at outputs O1 and O2, and the third frequency can produce multiple E1/DS1 rates via the filtering APLLs. The input clock to the DPLL1 LF Output DFS block is either 77.76 MHz from APLL1 (post jitter filtering) or 77.76 MHz direct from the DPLL1 77M Output DFS.

Utilizing the clock from APLL1 will result in lower jitter outputs from the DPLL1 LF Output DFS block. However, when the input to the APLL1 is taken from the DPLL1 LF Output DFS block, the input to that block comes directly from the DPLL1 77M Output DFS block so that a “loop” is not created.

APLL1 is for multiplying and filtering. The input to APLL1 can be either 77.76 MHz from the DPLL1 77M Output DFS block or an alternative frequency from the DPLL1 LF

Output DFS block (offering 77.76 MHz, 12E1, 16E1, 24DS1 or 16DS1). The frequency from APLL1 is four times its input frequency i.e. 311.04 MHz when used with a 77.76 MHz input. APLL1 is subsequently divided by 1, 2, 4, 6, 8, 12, 16 and 48 and these are available at the O1 and O2 Outputs.

DPLL2 & APLLs

DPLL2 is simpler than DPLL1. DPLL2 offers no PBO or phase offset. The DPLL2 input can only be used to lock to DPLL1. Unlike DPLL1, the DPLL2 Forward DFS block does not always generate 77.76 MHz. The possible frequencies are listed in Table 10, "APLL2 Frequencies," on page 27. Similar to DPLL1, the output of the DPLL2 Forward DFS block is generated using DFS clocked by the 204.8 MHz system clock and will have an inherent jitter of 4.9 ns.

The DPLL2 feedback DFS also has the facility to be able to use the post APLL2 (jitter-filtered) clock to generate the feedback locking frequency. Again, this will give the maximum performance by using a low jitter feedback.

APLL2 block is also for multiplying and filtering. The input to APLL2 can come either from the DPLL2 Forward DFS block or from DPLL1. The input to APLL2 can be programmed to be one of the following:

(a) Output from the DPLL2 Forward DFS block (12E1, 24DS1, 16E1, 16DS1, E3, DS3, OC-N),

(b) 12E1 from DPLL1,

(c) 16E1 from DPLL1,

(d) 24DS1 from DPLL1,

(e) 16DS1 from DPLL1.

The frequency generated from the APLL2 is four times its input frequency i.e. 311.04 MHz when used with a 77.76 MHz input. APLL2 is subsequently divided by 2, 4, 8, 12, 16, 48 and 64 and these are available at the O1 and 02 Outputs.

"Digital" Frequencies

The DPLL1 LF Output DFS block shown in the diagram, clocked either by the DPLL1 77M Output DFS block or via the APLL1, generates the single frequencies Digital1 and Digital2 (see Table 11 and Table 12). The input clock frequency of the DFS is always 77.76 MHz and as such has a period of approximately 12 ns. The jitter generated on the Digital outputs is relatively high, because they do not pass through an APLL for jitter filtering. The minimum level of jitter is when DPLL1 is in analog feedback mode, when the p-p jitter will be approximately 13 ns (equivalent to a period of the DFS clock). The maximum jitter is generated when in digital feedback mode, when the total is approximately 18 ns.

The E1/DS1 Synthesis block generates the E1/DS1 rates for the APLLs, using the output from DPLL1. It can generate 12E1, 16E1, 16DS1 or 24DS1, for selection by the multiplexers.

FrSync, MFrSync, 2 kHz and 8 kHz Clock Outputs

Whilst the FrSync and MFrSync Outputs are always supplied from DPLL1, the 2 kHz and 8 kHz options available from the O1 and O2 Outputs can be supplied from either DPLL1 or DPLL2 (Reg. 7A Bit 7).

Multiplexers

Multiplexers MUX1 and MUX2 are used to select the appropriate inputs to the Analog PLLs. The function they represent is controlled by Reg. 65 *cnfg_DPLL1_frequency*.

APLL2 Input Selection using MUX 2

- DPLL2 selected for input to APLL2 (Reg. 65 Bit 6 = 0) The input frequency is selected from the operating frequency of DPLL2 (Reg. 64 Bits [2:0])
- DPLL1 + LF Output DFS selected for Input to APLL2
  - 12E1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 00)
  - 16E1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 01)
  - 24DS1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 10)
  - 16DS1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 11)

APLL1 Input Selection using MUX 1

- DPLL1 (77.76 MHz) output fed to input of APLL1. Analog feedback used in DPLL1 (Reg. 65 Bits [2:0] set to 000)
- DPLL1 (77.76 MHz) output fed to input of APLL1. Digital feedback used in DPLL1 (Reg. 65 Bits [2:0] set to 001)
- DPLL1 + LF Output DFS selected for input to APLL1
  - 12E1 (Reg. 65 Bits [2:0] set to 010)
  - 16E1 (Reg. 65 Bits [2:0] set to 011)
  - 24DS1 (Reg. 65 Bits [2:0] set to 100)
  - 16DS1 (Reg. 65 Bits [2:0] set to 101)

Notes: (i) DPLL2 output cannot be selected for input to APLL1

(ii) If both multiplexers select LF Output DFS, the same frequency value must be selected in Reg. 65 Bits [2:0] and Reg. 65 Bits [5:4].

APLLs

There are three main APLLs. APLL1 and APLL2 provide a lower final output jitter reducing the 4.9 ns p-p jitter from the digital down to 500 ps p-p and 60 ps rms as typical final outputs measured broadband (from 10 Hz to 1 GHz). The feedback APLL (APLL3) is selected by default; it provides improved performance over the digital feedback.

APLL Output Dividers

Each APLL has its own divider. Each divider simultaneously outputs a series of fixed ratios of its APLL input. Any of these divided outputs may be selected as the output on Output Ports O1 or O2 by configuring Reg. 61 and Reg. 62, with the following exceptions: (APLL1)/2 and (APLL1)/1 only available for Output 01 (differential port), and (APLL1)/48 only available for Output 02.

PFD and Loop Filters

The PFD compares the input reference with that of the locking frequency (feedback) giving a phase error which is then filtered by a 100 Hz low pass filter, to give the average phase error for input into a loop filter. The PFD is quite complex and has several programmable options to determine what phase error value is fed to the loop (see "Phase and Frequency Detectors" on page 18) depending on the type of jitter/wander expected.

The loop filter bandwidth and damping is programmable to optimize the locking time/ability to track the input. See "Damping Factor Programmability" on page 18 and Figure 6 on page 18.

PLL Operational Controls

The main factors controlling the operation of the PLL are:

1. The operating mode of the device. See "Operating Modes (States) of the Device" on page 30.
2. Input reference and feedback frequency selection. See "PLL Architecture" on page 14 and "Input Locking Frequency Modes" on page 9.
3. Loop Bandwidth (Input Acquisition/Locked Bandwidth) and Damping factor of the DPLLs - these determine how fast the device can to lock to the selected input, or how tightly it can track the input. See from "Input Acquisition Bandwidth" to "Damping Factor Programmability" next.
4. PFD settings - these affect the input phase error to the Loop filter and relate to jitter and wander tolerance. See "Phase/Frequency/Lock Detection" on page 18.
5. Phase compensation functions - See "Phase Compensation Functions" on page 19.

Input Acquisition Bandwidth

DPLL1 has programmable acquisition bandwidth of 18, 35 or 70 Hz. The default is set to 70 Hz.

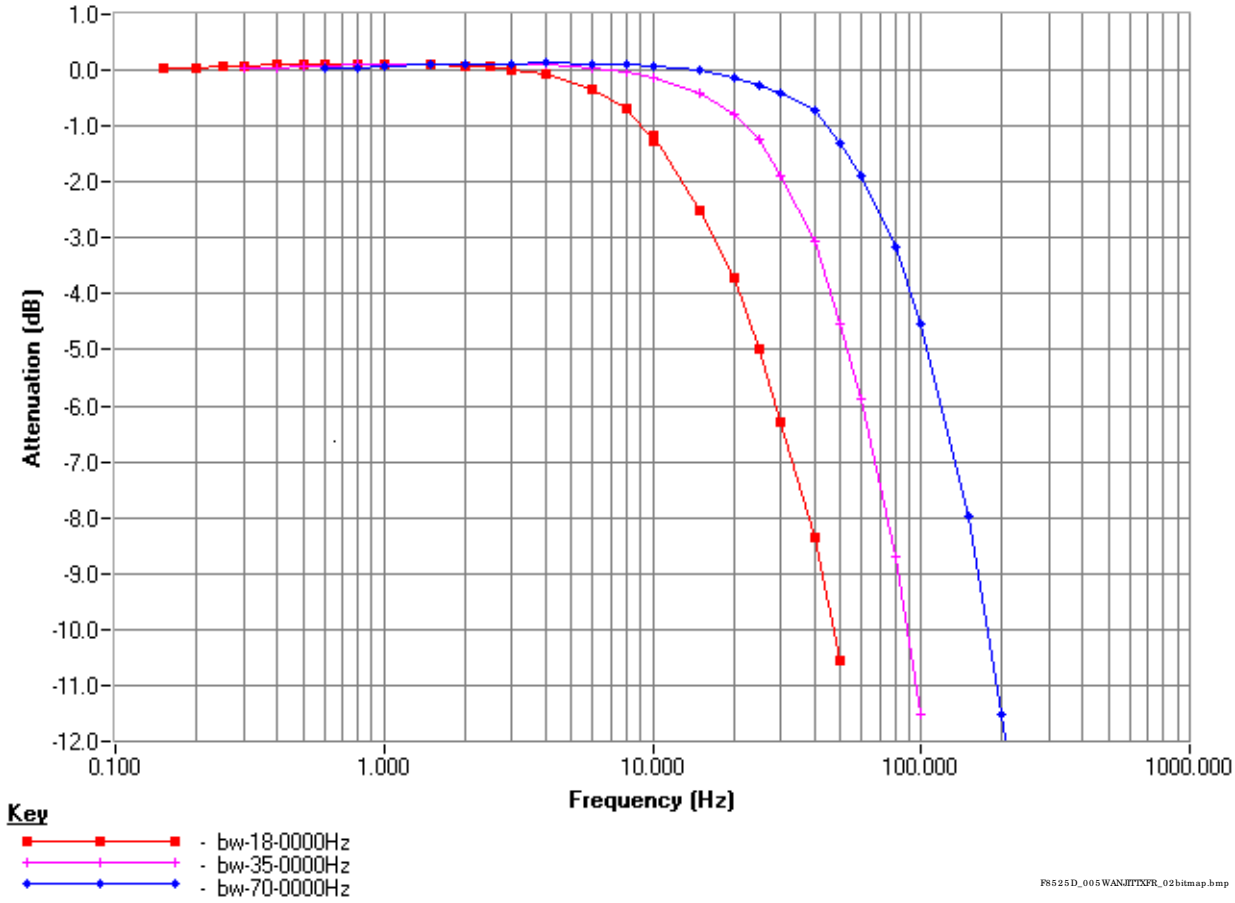
Input Locked Bandwidth

The ACS8525 has programmable Locked Bandwidth of 18, 35 or 70 Hz. These bandwidth settings correspond to the -3 dB jitter attenuation point on the ACS8525's jitter transfer characteristic shown in Figure 6. If the ACS8525 is used with only DPLL1, the highest bandwidth setting is recommended to ensure the closest tracking of the input SEC. If DPLL2 is also to be used, DPLL1 should be set to a lower bandwidth setting than DPLL2. The lowest bandwidth setting will provide the highest jitter attenuation although this is not the main function of the ACS8525 device.

Table 5 Available Damping Factors for different DPLL Bandwidths, and Associated Gain Peak Values

Bandwidth/Hz	Reg. 6B [2:0]	Damping Factor selected	Gain Peak/dB
18	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

Figure 6 DPLL1 Jitter Transfer Characteristic, (Freq = 1.544 MHz, Jitter = 0.2 UI p-p, Damping Factor = 5)



Damping Factor Programmability

The DPLL damping factor is set by default to provide a maximum wander gain peak of around 0.1 dB. Many of the specifications (e.g. GR-1244-CORE [13], G.812 [7] and G.813 [8]) specify a wander transfer gain of less than 0.2 dB. GR-253 [11] specifies jitter (not wander) transfer of less than 0.1 dB. To accommodate the required levels of transfer gain, the ACS8525 provides a choice of damping factors, with more choice given as the bandwidth setting increases into the frequency regions classified as jitter. Table 5 shows which damping factors are available for selection at the different bandwidth settings, and what the corresponding jitter transfer approximate gain peak will be.

Phase/ Frequency/ Lock Detection

Two main types of detector are used in the ACS8525:

- Phase and frequency detectors, and
- Phase Loss/ Lock detectors.

Phase and Frequency Detectors

There are two multi-phase and frequency detectors, one for each DPLL. The multi-phase and frequency detectors are used to compare input and feedback clocks. They operate at input frequencies up to 77.76 MHz. DPLL1 can lock to input spot frequencies from 2 kHz up to 77.76 MHz (155.52 MHz is internally divided down to 77.76 MHz). A common arrangement however is to use Lock8k mode (See Bit 6 of Reg. 22 to Reg. 28), where all input frequencies are divided down to 8 kHz internally. Marginally better MTIE figures may be possible in direct lock mode due to more regular phase updates. This direct locking capability is one of the unique features of the ACS8525.

A patented multi-phase detector is used in order to give an infinitesimally small input phase resolution combined with large jitter tolerance. A multi-phase detector comprises the following phase detectors:

- Phase and frequency detector (±360° or ±180° range)

- An Early/Late phase detector for fine resolution
- A multi-cycle phase detector for large input jitter tolerance (up to 8191 UI), which captures and remembers phase differences of many cycles between input and feedback clocks.

The phase detectors can be configured to be immune to occasional missing input clock pulses by using nearest edge detection (±180° capture) or the normal ±360° phase capture range which gives frequency locking. The device will automatically switch to nearest edge locking when the multi-UI phase detector is not enabled, and the other phase detectors have detected that phase lock has been achieved. It is possible to disable the selection of nearest edge locking via Reg. 03 Bit 6 (set to 1). In this setting, frequency locking will always be enabled.

The balance between the first two types of phase detector employed can be adjusted via Reg. 6A to 6D. The default settings should be sufficient for all modes. Adjustment of these settings affects only small signal overshoot and bandwidth.

The multi-cycle phase detector (wide-range) is enabled via Reg. 74, Bit 6 set to 1 and the range is set in exponentially increasing steps from ±1 UI up to 8191 UI via Reg. 74, Bits [3:0].

When this detector is enabled it keeps a track of the correct phase position over many cycles of phase difference to give excellent jitter tolerance. This provides an alternative to switching to Lock8k mode as a method of achieving high jitter tolerance.

An additional control (Reg. 74 Bit 5) enables the multi-phase detector value to be used in the final phase value as part of the DPLL loop. When enabled by setting *High*, the multi cycle phase value will be used in the loop and gives faster pull-in (but more overshoot). The characteristics of the loop will be similar to Lock8k mode where again large input phase differences contribute to the loop dynamics. Setting the bit *Low* only uses a max figure of 360° in the loop and will give slower pull-in but gives less overshoot. The final phase position that the loop has to pull in to is still tracked and remembered by the multi-cycle phase detector in either case.

Phase Lock/Loss Detectors

Phase lock detection is handled in several ways. Phase loss can be triggered from:

- The fine phase lock detector, which measures the phase between input and feedback clock
- The coarse phase lock detector, which monitors whole cycle slips
- Detection that the DPLL is at min. or max. frequency
- Detection of no activity on the input

Each of these sources of phase loss indication is individually enabled via register bits (see Reg. 73 and 74). Phase lock or lost is used to determine whether to switch to nearest edge locking and whether to use acquisition or normal bandwidth settings for the DPLL. Acquisition bandwidth is used for faster pull-in from an unlocked state.

The coarse phase lock detector detects phase differences of n cycles between input and feedback clocks, where n is set by Reg. 74 Bits [3:0]; the same register that is used for the coarse phase detector range, since these functions go hand in hand. This detector may be used in the case where it is required that a phase loss indication is not given for reasonable amounts of input jitter and so the fine phase loss detector is disabled and the coarse detector is used instead.

Phase Compensation Functions

The ACS8525 has the following phase compensation functions and controls:

- Phase Build-out (PBO)
- PBO Phase Offset
- Input-to-Output Phase Adjustment

Phase Build-out

Phase Build-out (PBO) is the function to minimize phase transients on the output SEC clock during input reference switching. If the currently selected input reference clock source is lost (due to a short interruption or complete loss of reference), the next highest priority SEC will be selected, and a PBO event triggered. When a PBO event is triggered, the device enters a temporary Holdover state. When in this temporary state, the phase of the input reference is measured, relative to the output. The device then automatically accounts for any measured phase difference and adds the appropriate phase offset into the DPLL to compensate.

Following a PBO event, whatever the phase difference on change of input, the output phase transient is minimized to be typically less than ±2.5 ns (in digital feedback mode).

On the ACS8525, PBO can be enabled, disabled or frozen using the Serial interface. By default, it is enabled. When

PBO is enabled, PBO can also be frozen (at the current offset setting). The device will then ignore any further PBO events occurring on any subsequent reference switch, and maintain the current phase offset. If PBO is disabled while the device is in the Locked mode, there may be a phase shift on the output SEC clocks as the DPLL locks back to 0° phase error. The rate of phase shift will depend on the programmed bandwidth. Enabling PBO whilst in the Locked stated will also trigger a PBO event.

PBO Phase Offset

In order to minimize the systematic (average) phase error for PBO, a PBO Phase Offset can be programmed in 0.101 ns steps in the *cnfg_PBO_phase_offset* register, Reg. 72. The range of the programmable PBO phase offset is restricted to ±1.4 ns. This can be used to eliminate an accumulation of phase shifts in one direction.

Input to Output Phase Adjustment

When PBO is off such that the system always tries to align the outputs to the inputs at the 0° position, there is a mechanism provided in the ACS8525 for precise fine tuning of the output phase position with respect to the input. This can be used to compensate for circuit and board wiring delays. The output phase can be adjusted in 6 ps steps up to 200 ns in a positive or negative direction. The phase adjustment actually changes the phase position of the feedback clock so that the DPLL adjusts the output clock phases to compensate. The rate of change of phase is therefore related to the DPLL bandwidth. For the DPLL to track large instant changes in phase, either Lock8k mode should be on, or the coarse phase detector should be enabled. Register *cnfg_phase_offset* at Reg. 70 and 71 controls the output phase, which is only used when Phase Build-out is off (Reg. 48, Bit 2 = 0, and Reg. 76, Bit 4 = 0).

DPLL Feature Summary

DPLL1 is the more feature rich of the two DPLLs. The features of the two DPLLs are summarized here. Refer to the Register Descriptions for more information.

DPLL1 Main Features

- Multiple E1 and DS1 outputs supported
- Low jitter MFrSync (2 kHz) and FrSync (8 kHz) outputs
- Multiple phase loss and multiple phase detectors (see "DPLL1 Advanced Features" on page 20")
- Direct PLL locking to common SONET/SDH input frequencies or any multiple of 8 kHz
- Automatic mode switching between Free-run, Locked and Digital Holdover states (see "Operating Modes (States) of the Device" on page 30)
- Fast detection on input failure and entry into Digital Holdover mode (holds at the last good frequency value)
- Frequency translation between input and output rates via direct digital synthesis
- High accuracy digital architecture for stable PLL dynamics combined with an APLL for low jitter final output clocks
- Non-revertive mode
- Frame Sync pulse alignment
- Selectable Automatic DPLL bandwidth control (auto selects either Locked bandwidth, or Acquisition bandwidth), or Locked DPLL bandwidth (Reg. 3B Bit 7)
- Two programmable bandwidth controls:
  - Locked bandwidth: 18, 35 or 70 Hz (Reg. 67)
  - Acquisition bandwidth: 18, 35 or 70 Hz (Reg. 69)
- Programmable damping factor (for optional faster locking and peaking control). Factors = 1.2, 2.5, 5, 10 or 20. (Reg. 6B, Bits [2:0])
- Programmable DPLL pull-in frequency range (Reg. 41, Reg. 42)
- Phase Build-out on source switching (hit-less source switching), on/off (Reg. 48 Bit 3)
- Freeze Phase Build-out, on/off (Reg. 48 Bit 2)

DPLL1 Advanced Features

Phase Loss Indicators

- Phase loss fine limit. on/off (Reg. 73 Bit 7) and programmable range 0 to 7 dec (Reg. 73 Bits [2:0])
- Multi-cycle phase loss course limit, on/off (Reg. 74 Bit 7) and selectable range from ±1 to 8191 UI in 13 steps (Reg. 74 Bits [3:0])

Output Phase Adjustment

- Programmable Input to Output phase offset adjustment, ±200 ns, 6 ps resolution step size (Reg. 70 and 71)
- Programmable mean offset on Phase Build-out event (PBO phase offset on source switching) - disturbance down to ±5 ns. (Reg. 72 Bits [5:0]). Requires PBO to be on (Reg. 48 Bit 3)

Phase Detector Controls

- Multi-cycle phase detection - Course phase lock & capture range on/off (Reg. 74 Bit 6) and selectable range from ±1 to 8191 UI in 13 steps (Reg. 74 Bits [3:0]). If selected, this feature increases jitter and wander tolerance to a maximum of 8192 UI (normally limited to ±0.5 UI)
- Use of coarse phase detector result in DPLL algorithm, on/off (Reg. 74 Bit 6) - speeds up phase locking
- Limit DPLL1 Integral when at DPLL frequency limit, on/off (Reg. 3B Bit 3) - reduces overshoot
- Anti-noise filter for low frequency inputs, on/off (Reg. 76 Bit 7)

Advanced Phase Detector Controls

The phase detector actually comprises two different phase detector types, PD1 and PD2. Their interworking and selection algorithms are beyond the scope of this datasheet, however it should be noted the gain of only PD2 is adjustable by configuration, in the following feature:

- DPLL1 PD2 gain control enable, on/off (Reg. 6D Bit 7)
  If on, this allows automatic gain selection according to the type of feedback to the DPLL (For the digital feedback setting, the gain used for PD2 is given by Reg. 6D Bits [2:0]). If off, PD2 is not used.
- Adjustable gain settings for PD2 (with auto switching enabled), for the following feedback cases:
  - Digital feedback (Reg. 6D Bits [2:0])
  - Analog feedback (all frequencies above 8 kHz) (Reg. 6D Bits [6:4])
  - Analog 8k (or less) feedback (Reg. 6B Bits [2:0])

Phase Monitors

- Input phase measured at DPLL1 or DPLL2. DPLL select (Reg. 4B Bit 4), 16-bit phase status (Reg. 77/Reg. 78)
- Phase measured between two inputs (uses DPLL2's PFD (Reg. 65 Bit 7))

DPLL2 Main Features

The main features of DPLL2 are:

- Always locked to DPLL1
- A single programmable bandwidth control: 18, 35 or 70 Hz
- Damping factor, (For optional faster locking and peaking control) Factors = 1.2, 2.5, 5, 10 or 20.
- Digital feedback, on/off (Reg. 35 Bit 6)
- Output frequency selection (Reg. 64)
  - DS3/E3 support (44.736 MHz / 34.368 MHz) independent of rates from DPLL1
  - Low jitter E1/DS1 options independent of rates from DPLL1
  - Frequencies of n x E1/DS1 including 16 and 12 x E1, and 16 and 24 x DS1 supported
  - Squelched (clock off)
- Can provide the source for the 2 kHz and 8 kHz outputs available at Outputs 01 and 02 (Reg. 7A Bit 7)
- Can use the phase detector in DPLL2 to measure the input phase difference between two inputs
- Selectable DPLL2 digital feedback, on/off (Reg. 64 Bit 6)

DPLL2 Advanced Features

The advanced features are the same as those for DPLL1, with DPLL2 using the configuration values for DPLL1, with the following exceptions:

Advanced Phase Detector Controls

- PD2 gain control enable, on/off (Reg. 6C, Bit 7)
  If on, this allows automatic gain selection according to the type of feedback to the DPLL (For the digital feedback setting, the gain used for PD2 is given by (Reg. 6C Bits [2:0]). If off, PD2 is not used.
- Adjustable gain settings for PD2 (with auto switching enabled), for the following feedback cases:
  - Digital feedback (Reg. 6C Bits [2:0])
  - Analog feedback (all frequencies above 8K) (Reg. 6C Bits [6:4])
  - Analog 8k (or less) feedback (Reg. 6A Bits [2:0])

Outputs

The ACS8525 delivers four output signals on the following ports: Two clocks, one each on ports Output O1 and Output O2; and two Sync signals, on ports FrSync and MFrSync. Output O1 and Output O2 are independent of each other and are individually selectable. Output 01 is a differential port (pins O1POS and O1NEG), and can be selected PECL or LVDS. Output O2 (pin O2) and the Sync outputs are TTL/CMOS.

The two Sync outputs, FrSync (8 kHz) and MFrSync (2 kHz), are derived from DPLL1.

PECL/LVDS Output Port Selection

The choice of PECL or LVDS compatibility for Output 01 is programmed via the *cnfg_differential_output* register, Reg. 3A.

Output Frequency Selection and PLL Configuration

The output frequency at many of the outputs is controlled by a number of inter-dependent parameters (refer to "PLL Architecture" on page 14). The frequencies of the output clocks are selectable from a range of pre-defined spot frequencies/port technologies, as defined in Tables 6 and 7.

Outputs O1 & O2 Frequency Configuration Steps

The output frequency selection is performed in the following steps:

6. Refer to Table 8, Frequency Divider Look-up, to choose a set of output frequencies.
7. Refer to the Table 8 to determine the required APLL frequency to support the frequency set.
8. Refer to Table 9, APLL1 Frequencies, and Table 10, APLL2 Frequencies, to determine in what mode DPLL1 and DPLL2 need to be configured, considering the output jitter level.
9. Refer to Table 11, O1 and O2 Output Frequency Selection, and the column headings in Table 8, Frequency Divider Look-up, to select the appropriate frequency from either of the APLLs on each output as required.

Table 6 Output Reference Source Selection Table

Port Name	Output Port Technology	Frequencies Supported
Output O1	LVDS/PECL (LVDS default)	Frequency selection as per Table 7 and Table 11
Output O2	TTL/CMOS	
FrSync	TTL/CMOS	FrSync, 8 kHz programmable pulse width and polarity, see Reg. 7A.
MFrSync	TTL/CMOS	MFrSync, 2 kHz programmable pulse width and polarity, see Reg. 7A.

Note...1.544 MHz/2.048 MHz are shown for SONET/SDH respectively. Pin SONSDHB controls default, when High SONET is default

Table 7 Output Frequency Selection

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (Typ)	
				rms (ps)	p-p (ns)
2 kHz	77.76 MHz Analog	-	-	60	0.6
2 kHz	Any digital feedback mode	-	-	1400	5
8 kHz	77.76 MHz Analog	-	-	60	0.6
8 kHz	Any digital feedback mode	-	-	1400	5

Table 7 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)		DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (Typ)	
					rms (ps)	p-p (ns)
1.536		-	12E1 mode	Select DPLL2	500	2.3
1.536		-	-	Select DPLL1 12E1	250	1.5
1.544		-	16DS1 mode	Select DPLL2	200	1.2
1.544		-	-	Select DPLL1 16DS1	150	1.0
1.544	via Digital1 or Digital2 (not Output O1)	77.76 MHz Analog	-	-	3800	13
1.544	via Digital1 or Digital2 (not Output O1)	Any digital feedback mode	-	-	3800	18
2.048		-	12E1 mode	Select DPLL2	500	2.3
2.048		-	-	Select DPLL1 12E1	250	1.5
2.048		-	16E1 mode	Select DPLL2	400	2.0
2.048		-	-	Select DPLL1 16E1	220	1.2
2.048	(not Output O1)	12E1 mode	-	-	900	4.5
2.048	via Digital1 or Digital2 (not Output O1)	77.76 MHz Analog	-	-	3800	13
2.048	via Digital1 or Digital2 (not Output O1)	Any digital feedback mode	-	-	3800	18
2.059		-	16DS1 mode	Select DPLL2	200	1.2
2.059		-	-	Select DPLL1 16DS1	150	1.0
2.059	(not Output O1)	16DS1 mode	-	-	760	2.6
2.316		-	24DS1 mode	Select DPLL2	110	0.75
2.316		-	-	Select DPLL1 24DS1	110	0.75
2.731		-	16E1 mode	Select DPLL2	400	1.5
2.731		-	-	Select DPLL1 16E1	220	1.2
2.731	(not Output O1)	16E1 mode	-	-	250	1.6
2.796		-	DS3 mode	Select DPLL2	110	1.0
3.088		-	24DS1 mode	Select DPLL2	110	0.75
3.088		-	-	Select DPLL1 24DS1	110	0.75
3.088	(not Output O1)	24DS1 mode	-	-	110	0.75
3.088	via Digital1 or Digital2 (not Output O1)	77.76 MHz Analog	-	-	3800	13
3.088	via Digital1 or Digital2 (not Output O1)	Any digital feedback mode	-	-	3800	18
3.728		-	DS3 mode	Select DPLL2	110	1.0
4.096	via Digital1 or Digital2 (not Output O1)	77.76 MHz Analog	-	-	3800	13
4.096	via Digital1 or Digital2 (not Output O1)	Any digital feedback mode	-	-	3800	18
4.296		-	E3 mode	Select DPLL2	120	1.0

Table 7 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (Typ)	
				rms (ps)	p-p (ns)
4.86	-	77.76 MHz mode	Select DPLL2	60	0.6
5.728	-	E3 mode	Select DPLL2	120	1.0
6.144	12E1 mode	-	-	900	4.5
6.144	-	12E1 mode	Select DPLL2	500	2.3
6.144	-	-	Select DPLL1 12E1	250	1.5
6.176	16DS1 mode	-	-	760	2.6
6.176	-	16DS1 mode	Select DPLL2	200	1.2
6.176	-	-	Select DPLL1 16DS1	150	1.0
6.176 via Digital1 or Digital2 (not Output O1)	77.76 MHz Analog	-	-	3800	13
6.176 via Digital1 or Digital2 (not Output O1)	Any digital feedback mode	-	-	3800	18
6.48	-	77.76 MHz mode	Select DPLL2	60	0.6
6.48 (not Output O1)	77.76 MHz analog	-	-	60	0.6
6.48 (not Output O1)	77.76 MHz digital	-	-	60	0.6
8.192	12E1 mode	-	-	900	4.5
8.192	16E1 mode	-	-	250	1.6
8.192	-	16E1 mode	Select DPLL2	400	2.0
8.192	-	-	Select DPLL1 16E1	220	1.2
8.192 via Digital1 or Digital2 (not Output O1)	77.76 MHz Analog	-	-	3800	13
8.192 via Digital1 or Digital2 (not Output O1)	Any digital feedback mode	-	-	3800	18
8.235	16DS1 mode	-	-	760	2.6
9.264	24DS1 mode	-	-	110	0.75
9.264	-	24DS1 mode	Select DPLL2	110	0.75
9.264	-	-	Select DPLL1 24DS1	110	0.75
10.923	16E1 mode	-	-	250	1.6
11.184	-	DS3 mode	Select DPLL2	110	1.0
12.288	12E1 mode	-	-	900	4.5
12.288	-	12E1 mode	Select DPLL2	500	2.3
12.288	-	-	Select DPLL1 12E1	250	1.5
12.352	24DS1 mode	-	-	110	0.75
12.352	16DS1 mode	-	-	760	2.6
12.352	-	16DS1 mode	Select DPLL2	200	1.2

Table 7 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (Typ)	
				rms (ps)	p-p (ns)
12.352	-	-	Select DPLL1 16DS1	150	1.0
12.352 via Digital1 or Digital2 (not Output O1)	77.76 MHz Analog	-	-	3800	13
12.352 via Digital1 or Digital2 (not Output O1)	Any digital feedback mode	-	-	3800	18
16.384	12E1 mode	-	-	900	4.5
16.384	16E1 mode	-	-	250	1.6
16.384	-	16E1 mode	Select DPLL2	400	2.0
16.384	-	-	Select DPLL1 16E1	220	1.2
16.384 via Digital1 or Digital2 (not Output O1)	77.76 MHz Analog	-	-	3800	13
16.384 via Digital1 or Digital2 (not Output O1)	Any digital feedback mode	-	-	3800	18
16.469	16DS1 mode	-	-	760	2.6
17.184	-	E3 mode	Select DPLL2	120	1.0
18.528	24DS1 mode	-	-	110	0.75
18.528	-	24DS1 mode	Select DPLL2	110	0.75
18.528	-	-	Select DPLL1 24DS1	110	0.75
19.44	77.76 MHz analog	-	-	60	0.6
19.44	77.76 MHz digital	-	-	60	0.6
19.44	-	77.76MHz mode	Select DPLL2	60	0.6
21.845	16E1 mode	-	-	250	1.6
22.368	-	DS3 mode	Select DPLL2	110	1.0
24.576	12E1 mode	-	-	900	4.5
24.576	-	12E1 mode	Select DPLL2	500	2.3
24.576	-	-	Select DPLL1 12E1	250	1.5
24.704	24DS1 mode	-	-	110	0.75
24.704	16DS1 mode	-	-	760	2.6
24.704	-	16DS1 mode	Select DPLL2	200	1.2
24.704	-	-	Select DPLL1 16DS1	150	1.0
25.92	77.76 MHz analog	-	-	60	0.6
25.92	77.76 MHz digital	-	-	60	0.6
32.768	16E1 mode	-	-	250	1.6
32.768	-	16E1 mode	Select DPLL2	400	2.0
32.768	-	-	Select DPLL1 16E1	220	1.2