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ACS8526 LC/P LITE

Line Card Protection Switch for PDH, SONET or SDH Systems

Description

The ACS8526 is a highly integrated single-chip solution for protection switching between two SECs (SDH/SONET Equipment Clocks) from Master and Slave SETS clock cards, for line cards in a PDH, SONET or SDH Network Element. The ACS8526 has fast activity monitors on the inputs and will raise a flag on a pin if there is a loss of activity on the currently selected input. The protection switching between the input reference clock sources is controlled by an external pin.

The ACS8526 has two SEC reference clock input ports, configured for expected frequency by setting hardware pins or by writing to registers via the serial interface.

The ACS8526 can perform frequency translation, converting, for example, an 8 kHz SEC input clock from a backplane into a 155.52 MHz clock for local line cards.

The ACS8526 generates two independent SEC clock outputs, one on a PECL/LVDS port and one on a TTL/CMOS port, at spot frequencies configured by hardware pins, or by writing to registers via the serial interface. The hardware selectable spot frequencies range from 1.544 MHz up to 155.52 MHz, with further options for N x E1/DS1 and 311.04 MHz via register selection. The ACS8526 also provides an 8 kHz Frame Sync output and 2 kHz Multi-Frame Sync output, both with programmable pulse width and polarity.

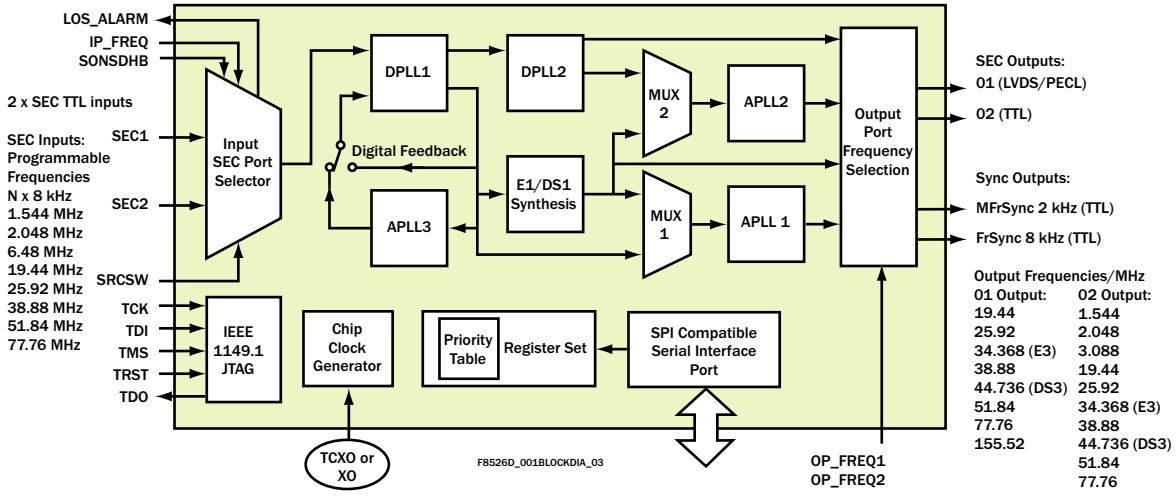
Advanced configuration possibilities are available via the serial port (which can be SPI compatible), however the basic configuration of I/O frequencies and SONET/SDH selection by hardware make the device suitable for standalone operation, i.e., no need for a microprocessor.

Features

- Line card protection switch - partners Semtech SETS devices for Stratum 3E/3/4E/4 PDH, SONET or SDH applications
- High performance DPLL/APLL solution
- Output jitter compliant to STM-1
- Two independent SEC inputs ports (TTL)
- Four independent output ports:
  - Two clock ports: one PECL/LVDS, one TTL
  - Two Syncs (TTL): 8 kHz FrSync & 2 KHz MFrSync
- TTL I/O ports: spot frequencies 2 kHz to 77.76 MHz
- PECL/LVDS port: spot frequencies 2 kHz to 311 MHz
- N x E1/DS1 mode
- Programmable pulse width and polarity on Syncs
- SONET/SDH frequency translation
- Digital Holdover mode on input failure
- Separate activity monitors and register alarms on each input.
- “Loss of activity” on selected input flagged on dedicated pin
- Source switch under external hardware control
- PLL “Locked” and “Acquisition” bandwidth selectable from 18, 35 or 70 Hz
- Configurable via serial interface or hardware pins
- Output clock phase continuity to GR-1244-CORE[13]
- Single 3.3 V operation, 5 V I/O compatible
- IEEE 1149.1 JTAG Boundary Scan is supported
- Operating temperature (ambient) of -40 to +85 °C
- Available in LQFP 64 package
- Lead (Pb)-free version available (ACS8526T), RoHS and WEEE compliant.

Block Diagram

Figure 1 Block Diagram of the ACS8526 LC/P LITE



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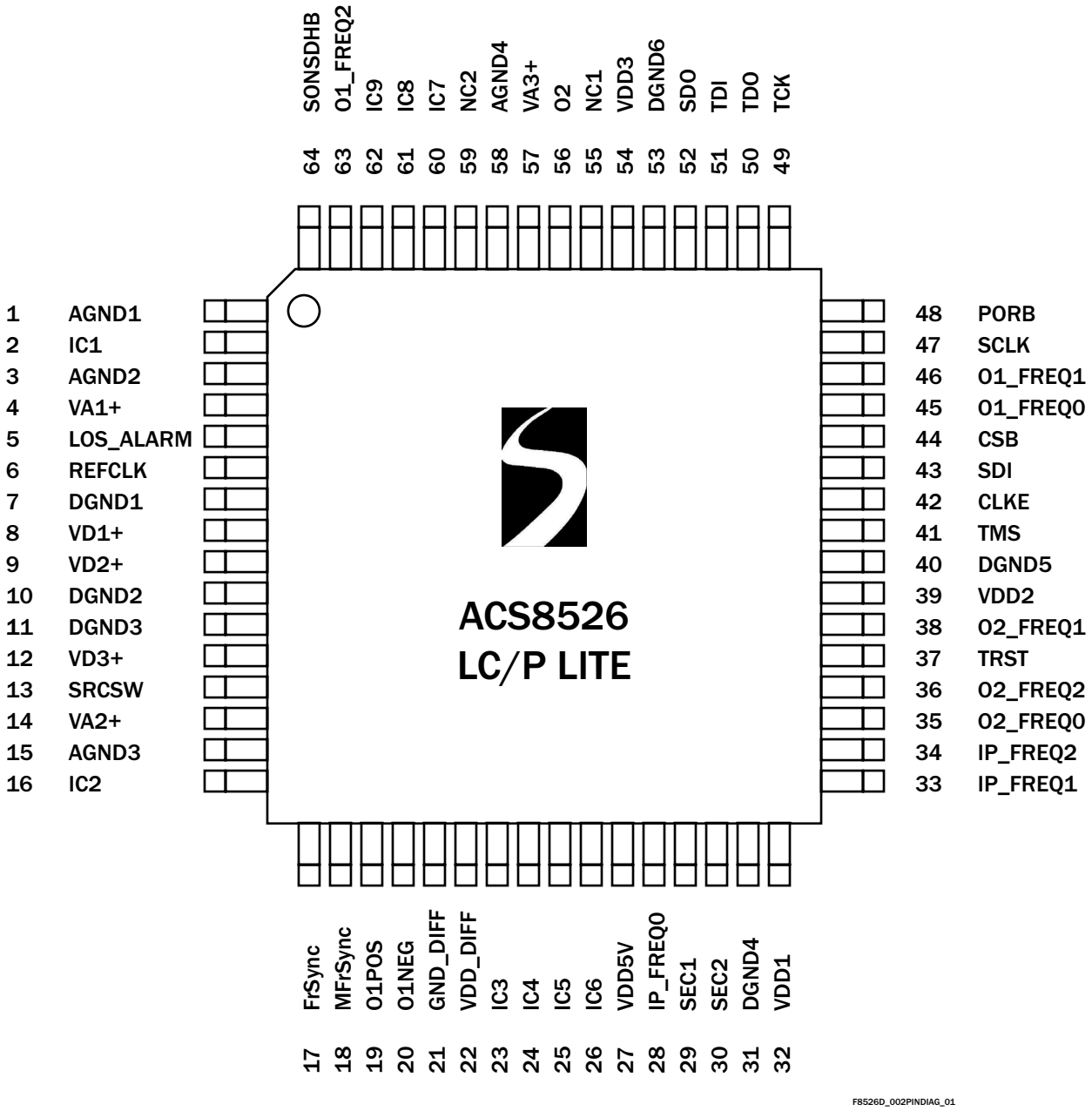
Pin Diagram

Figure 2 ACS8526 Pin Diagram



Pin Description

Table 1 Power Pins

Pin Number	Symbol	I/O	Type	Description
8, 9, 12	VD1+, VD2+, VD3+	P	-	Supply Voltage: Digital supply to gates in analog section, +3.3 Volts ±10%.
22	VDD_DIFF	P	-	Supply Voltage: Digital supply for differential output pins 19 and 20, +3.3 Volts ±10%.
27	VDD5V	P	-	Digital Supply for +5 Volts tolerance to input pins. Connect to +5 Volts (±10%) for clamping to +5 Volts. Connect to VDD for clamping to +3.3 Volts. Leave floating for no clamping, input pins tolerant up to +5.5 Volts.
32, 39, 54	VDD1, VDD2, VDD3,	P	-	Supply Voltage: Digital supply to logic, +3.3 Volts ±10%.
4	VA1+	P	-	Supply Voltage: Analog supply to clock multiplying PLL, +3.3 Volts ±10%.
14, 57	VA2+, VA3+	P	-	Supply Voltage: Analog supply to output PLLs APLL2 and APLL1, +3.3 Volts ±10%.
15, 58	AGND3, AGND4		-	Supply Ground: Analog ground for output PLLs APLL2 and APLL1.
7, 10, 11	DGND1, DGND2, DGND3	P	-	Supply Ground: Digital ground for components in PLLs.
31, 40, 53	DGND4, DGND5, DGND6	P	-	Supply Ground: Digital ground for logic.
21	GND_DIFF	P	-	Supply Ground: Digital ground for differential output pins 19 and 20.
1, 3	AGND1, AGND2	P	-	Supply Ground: Analog grounds.

Note...I = Input, O = Output, P = Power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor.

Table 2 Internally Connected

Pin Number	Symbol	I/O	Type	Description
2, 16, 23, 24, 25, 26, 60, 61, 62	IC1, IC2, IC3, IC4, IC5, IC6, IC7, IC8 IC9	-	-	Internally Connected: Leave to float.
55, 59	NC1, NC2	-	-	Not Connected: Leave to float.

Table 3 Other Pins

Pin Number	Symbol	I/O	Type	Description
5	LOS_ALARM	O	TTL/CMOS	LOS_Alarm: Flag to indicate loss of activity of currently selected reference source.
6	REFCLK	I	TTL	Reference Clock: 12.800 MHz (refer to section headed Local Oscillator Clock).
13	SRCSW	I	TTL_D	Source Switching: Controls switchover between SEC1 and SEC2 inputs as the selected reference. SRCSW must be held *High* on power-up or reset, and for a further 251 ms after PORB has gone *High*. See “Initialization” on page 8.
17	FrSync	O	TTL/CMOS	Output Reference: 8 kHz Frame Sync output.

Table 3 Other Pins (cont...)

Pin Number	Symbol	I/O	Type	Description
18	MFrSync	O	TTL/CMOS	Output Reference: 2 kHz Multi-Frame Sync output.
19, 20	O1POS, O1NEG	O	LVDS/PECL	Output Reference 1: Differential output., default LVDS.
28	IP_FREQ0	I	TTL_D	Input Reference Frequency Select: Frequency select for input SEC1 and SEC2.
29	SEC1	I	TTL_D	Input Reference 1: Primary input.
30	SEC2	I	TTL_D	Input Reference 2: Secondary input.
33	IP_FREQ1	I	TTL_D	Input Reference Frequency Select: Frequency select for input SEC1 and SEC2.
34	IP_FREQ2	I	TTL_D	Input Reference Frequency Select: Frequency select for input SEC1 and SEC2.
35	O2_FREQ0	I	TTL_D	Output O2 Frequency Select: Frequency select for output O2.
36	O2_FREQ2	I	TTL_D	Output O2 Frequency Select: Frequency select for output O2.
37	TRST	I	TTL_D	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 for normal device operation (JTAG logic transparent). NC if not used.
38	O2_FREQ1	I	TTL_D	Output O2 Frequency Select: Frequency select for output O2.
41	TMS	I	TTL_D	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. NC if not used.
42	CLKE	I	TTL_D	SCLK Edge Select: SCLK active edge select, CLKE = 1, selects falling edge of SCLK to be active.
43	SDI	I	TTL_D	Interface Address: SPI compatible Serial Data Input.
44	CSB	I	TTL^U	Chip Select (Active *Low*): This pin is asserted *Low* by the external device (microprocessor) to enable the Serial interface.
45	O1_FREQ0	I	TTL^U	Output O1 Frequency Select: Frequency select for output O1.
46	O1_FREQ1	I	TTL^U	Output O1 Frequency Select: Frequency select for output O1.
47	SCLK	I	TTL_D	Serial Data Clock: The *Low* to *High* transition on this input latches the data on the SDI input into the internal registers. The active clock edge (defined by CLKE) latches the data out of the internal registers onto the SDO output.
48	PORB	I	TTL^U	Power-On Reset: Master reset. If PORB is forced *Low*, all internal states are reset back to default values.
49	TCK	I	TTL_D	JTAG Clock: Boundary Scan clock input.
50	TDO	O	TTL/CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK.
51	TDI	I	TTL_D	JTAG Input: Serial test data Input. Sampled on rising edge of TCK. NC if not used.
52	SDO	O	TTL_D	Interface Address: SPI compatible Serial Data Output.
56	O2	O	TTL/CMOS	Output Reference: Programmable, default 19.44 MHz.
63	O1_FREQ2	I	TTL^U	Output O1 Frequency Select: Frequency select for output O1.
64	SONSDHB	I	TTL_D	SONET or SDH frequency select: Sets the initial power-up state (or state after a PORB) of the SONET/SDH frequency selection registers, Reg. 34, Bit 2 and Reg. 38, Bit 5, Bit 6 and Reg. 64 Bit 4. The register states can be changed after power-up by software. When set *Low*, SDH rates are selected (2.048 MHz etc.) and when set *High*, SONET rates are selected (1.544 MHz etc.) The register states can be changed after power-up by software.

Introduction

The ACS8526 is a highly integrated, single-chip solution for protection switching of two SEC inputs from, for example, Master and Slave SETS clock cards sources, for Line Cards in a SONET or SDH Network Element. The ACS8526 has fast activity monitors on the SEC clock inputs.

The ACS8526 can be used as a standalone part without the serial interface where all input and output frequencies are set by external control using the IP_FREQ and OP_FREQ pins. These pins determine the default power-up or reset state of internal registers, that in turn determine the I/O frequencies.

If more detailed control is required, then the registers within the device can be re-configured, after an initialization period, by writes through the serial interface. The SRCSW pin is used to select one of the two SEC inputs to lock to. The SRCSW pin must remain *High* for at least 251 ms following power-up or reset (251 ms after the PORB signal has gone *High*). SRCSW *Low* following a power-up or reset is not supported.

The ACS8526 has two SEC inputs from which it can generate independent clocks on outputs 01 and 02 with a total of 53 possible output frequencies. In addition, there are two Sync outputs; 8 kHz Frame Synchronization (FrSync) signal and a 2 kHz Multi-Frame Synchronization (MFrSync) signal.

Initially the ACS8526 generates a stable, low-noise clock signal at a frequency to the same accuracy as the external oscillator, or it can be made more accurate via software calibration to within ±0.02 ppm. The device always attempts to lock to one of its inputs (according to the value on the SRCSW pin). Once locked to a reference the accuracy of the output clock is determined directly by the accuracy of the input reference. In the absence of any input references the device simply maintains its most recent frequency in a Digital Holdover mode. However, as soon as the DPLL detects an input presence, it will attempt to lock to it and will not “qualify” it first. As soon as the DPLL detects a failure on the input, the DPLL freezes its operating frequency and raises the LOS alarm on device pin LOS_ALARM.

The overall PLL loop bandwidth, damping, pull-in range and frequency accuracy are all determined by digital parameters that provide a consistent level of performance. An Analog PLL (APLL) takes the signal from the DPLL output and provides a lower jitter output. The APLL bandwidth is set four orders of magnitude higher than the DPLL bandwidth. This ensures that the overall system performance still maintains the advantage of consistent behavior provided by the digital approach. The DPLLs are clocked by the external oscillator module (TCXO or XO) so that prior to initial lock (with no input reference) or in Digital Holdover, the frequency stability is only determined by the stability of the external oscillator module. This gives the key advantage of confining all temperature critical components to one well defined and pre-calibrated oscillator module, whose performance can be chosen to match the application. All performance parameters of the DPLLs are programmable without the need to understand detailed PLL equations. Bandwidth, damping factor and lock range can all be configured under software control.

The hardware set-up configures a subset of the registers in the register block, with the remainder adopting their default settings. If hardware set-up alone is insufficient for configuring, controlling and monitoring the device for a particular application, then access to the full set of registers for these purposes is provided by an SPI compatible serial interface port.

Each register (8-bit wide data field) is identified by and referred to by its hexadecimal address and name, e.g. Reg. 7D *cnfg_LOS_alarm*. The “Register Map” on page 30 summarizes the content of all of the registers, and each register is individually described in the subsequent Register Tables, organized in order of ascending Address (hexadecimal), in the “Register Descriptions” from page 32 onwards.

An Evaluation board and intuitive GUI-based software package is available for device introduction. This has its own documentation “ACS8526-EVB”.

General Description

The following description refers to the Block Diagram (Figure 1 on page 1).

Inputs

The ACS8526 SETS device has two TTL/CMOS compatible SEC input ports. They are 3 V and 5 V compatible (with clamping if required by connecting the VDD5V pin). Refer to the “Electrical Specifications” on page 61 for more information on electrical compatibility.

Input frequencies supported range from 2 kHz to 155.52 MHz. Common E1, DS1, OC-3 and sub-divisions are supported as spot frequencies that the DPLLs will directly lock to. Any input frequency, up to 100 MHz, that is a multiple of 8 kHz can also be locked to via an inbuilt programmable divider.

In addition to the SEC inputs, there are four configuration pins IP_FREQ [2:0] and SONSDHB used to configure the input to expect a particular input frequency (same value applies to both inputs), and a control pin SRCSW for switching between SEC1 and SEC2 as the selected input reference to which the device tries to lock.

Preconfiguring Inputs - Expected Input Frequency

The inputs SEC1 and SEC2 must be preconfigured to expect a particular input frequency.

The expected input frequencies can be selected from a range of spot frequencies by either:

- Hardware selection: configuring the hardware pins IP_FREQ [2:0] and SONSDHB, which are read on reset
- Register programming: writing to the *cnfg_ref_source_frequency* and *cnfg_input_mode* registers.

Hardware Selection of Expected I/P Frequency

The combined pin states of IP_FREQ [2:0] and SONSDHB represent a 4-bit word which addresses a particular frequency value as given in Table 4.

The frequency selected by the hardware configuration is always applied to both inputs on Power-up or Reset, so both will be preconfigured to expect the same frequency. If SEC1 and SEC2 are required to expect different frequencies, then these inputs must be subsequently reconfigured by programming the appropriate registers.

Register Programming of Expected I/P Frequency

The expected input frequencies can be programmed by writing to the *cnfg_ref_source_frequency* registers (Reg. 22 and 23) and *ip_sonsdhb* (Bit 2 of *cnfg_input_mode*,Reg. 34), via the serial interface. This must not be done until after the end of the initialization period (see “Initialization” on page 8).

Note...Any subsequent reset will cause these registers to be overwritten by values that equate to the single hardware selected frequency on the pins at the time of reset, i.e both inputs will be configured to expect the same input frequency. After a reset and initialization period, any change of state on IP_FREQ [2:0] or SONSDHB will have no effect on the device configuration, as these are only read during the reset period.

The register programming approach provides a greater range of frequencies than the hardware selection method: more spot frequencies, plus frequencies derived using DivN Mode up to 100 MHz (TTL technology limit).

Table 4 Hardware Configuration for Selecting Expected Input Frequency on SEC1 and SEC2

IP_FREQ Pins			SONSDHB Pin	Input frequency
2	1	0		
0	0	0	X	8 kHz
0	0	1	0	2.048 MHz
			1	1.544 MHz
0	1	0	X	6.48 MHz
0	1	1	X	19.44 MHz
1	0	0	X	25.92 MHz
1	0	1	X	38.88 MHz
1	1	0	X	51.84 MHz
1	1	1	X	77.76 MHz

Preconfiguring Inputs- SONET/SDH

The *cnfg_input_mode* register bit *ip_sonsdhb* is used to select SDH or SONET mode for the entire device and its setting affects parameters other than just the expected input frequency selection, e.g. output frequency. To set the device for use in a SONET network, set *ip_sonsdhb* = 1. For SDH, set *ip_sonsdhb* = 0.

Input Locking Frequency Modes

Each input port has to be configured to receive the expected input frequency. To achieve this, three input locking frequency modes are provided: Direct Lock, Lock8K and DivN.

Direct Lock Mode

In Direct Lock mode, DPLL1 can lock to the selected input at the spot frequency of the input, for example 19.44 MHz performs the DPLL phase comparisons at 19.44 MHz.

In Lock8K and DivN modes an internal divider is used prior to DPLL1 to divide the input frequency before it is used for phase comparisons.

Lock8K Mode

Lock8K mode automatically sets the divider parameters to divide the input frequency down to 8 kHz. Lock8K can only be used on the supported spot frequencies. See *divn_SEC1* and *2* descriptions (Bit 7 of Reg. 22 and 23, *cnfg_ref_source_frequency*). Lock8k mode is enabled by setting the *Lock8k* bit (Bit 6) in the appropriate *cnfg_ref_source_frequency* register. Using lower frequencies for phase comparisons in the DPLL results in a greater tolerance to input jitter. It is possible to choose which edge of the input reference clock to lock to, by setting *8K Edge Polarity*, (Bit 2 of Reg. 03, *test_register1*).

DivN Mode

In DivN mode, the divider parameters are set manually by configuration (Bit 7 of the *cnfg_ref_source_frequency* register), but must be set so that the frequency after division is exactly 8 kHz.

The DivN function is defined as:

DivN = "Divide by N+ 1", i.e. it is the dividing factor used for the division of the input frequency, and has a value of (N+1) where N is an integer from 1 to 12499 inclusive.

Therefore, in DivN mode the input frequency can be divided by any integer value between 2 to 12499. Consequently, any input frequency which is a multiple of 8 kHz, between 8 kHz to 125 MHz, can be supported by using DivN mode.

Note...Both reference inputs can be set to use DivN independently of the frequency and configuration of the other input. However only one value of N is allowed, so if both inputs have DivN selected, they must be running at the same frequency.

DivN Examples

(a) To lock to 2.000 MHz:

(i) Set the *cnfg_ref_source_frequency* register to 10XX0000 (binary) to enable DivN, and set the frequency to 8 kHz - the frequency required after division. (XX = "Leaky Bucket" ID for this input).

(ii) To achieve 8 kHz, the 2 MHz input must be divided by 250. So, if DivN = 250 = (N + 1) then N must be set to 249. This is done by writing F9 hex (249 decimal) to the DivN register pair Reg. 46/47.

(b) To lock to 10.000 MHz:

(i) The *cnfg_ref_source_frequency* register is set to 10XX0000 (binary) to set the DivN and the frequency to 8 kHz, the post-division frequency. (XX = "Leaky Bucket" ID for this input).

(ii) To achieve 8 kHz, the 10 MHz input must be divided by 1,250. So, if DivN, = 250 = (N+1) then N must be set to 1,249. This is done by writing 4E1 hex (1,249 decimal) to the DivN register pair Reg. 46/47.

Selection of Input SECs

Initialization

Switching between inputs SEC1 and SEC2 is triggered directly from a dedicated pin (SRCSW), though for the device to operate properly, the device must first be initialized by holding the pin *High* during reset and for at least a further 251 ms after PORB has gone *High* (250 ms allowance for the internal reset to be removed plus 1 ms allowance for APLLs to start-up and become stable). A simple external circuit to set SCRSW high for the required period is shown in the "Simplified Application Schematic" on page 70. If SCRSW is held *Low* at any time during the 251 ms initialization period, this will result in incorrect device operation.

SEC Selection - SRCSW pin

After the ACS8526 has been initialized (see previous "Initialization" section), then the value of SRCSW pin directly selects either SEC1 (SRCSW *High*) or SEC2 (SRCSW *Low*). The default frequency tolerance of SEC1 and SEC2 is ±80 ppm (Reg. 41 and Reg. 42) with respect to the local (calibrated) oscillator clock. These registers can be subsequently set by external software, if required.

After initialization, the output clocks are stable and the device will operate as a simple switch, with the DPLL trying to lock on to the selected reference source.

Output Clock Phase Continuity on Source Switchover

A phase offset between SEC inputs will be seen as a phase shift on the output on source switchover equal to the input phase offset.

Note...The ACS8526 has no Phase Build-out function to accommodate this. If this function is required, it is available on the AS8525 LC/P device.

The rate of change of phase on the output, during the time between input switchover and the output settling to a steady state, is dependent on factors of: input frequency,

input phase change, DPLL bandwidth, DPLL frequency limit, and phase detector capture range. The ACS8526 always complies with GR-1244-CORE[13] spec for Stratum 3 (max rate of phase change of 81 ns/1.326 ms), for input frequencies at 6.48 MHz or higher, with the default 1UI phase detector capture range.

For inputs at a lower frequency than 6.48 MHz (e.g. 8 kHz) with the DPLL frequency limit set to greater than ±30 ppm (note default is ±80 ppm), then to ensure compliance with GR-1244-CORE[13] at DPLL bandwidth settings of 18, 35 or 70 Hz, the input phase difference between the Master and Slave inputs to the line card PLL should be limited to less than 600, 330 ns or 190 ns respectively. Alternatively, the DPLL frequency range should be set <±30 ppm. A well designed system would have Master and Slave clock from the clock sync cards aligned to within a few nanoseconds. In which case a complete system using the Semtech SETS clock card parts (ACS8530, ACS8520 or ACS8510) and this line card part would be fully compliant to GR-1244-CORE[13] specifications under all conditions due to the lower frequency range and bandwidth set at the clock card end.

Activity Monitors

Two types of Activity monitors are incorporated in the ACS8526:

- SEC Activity Monitors, which raise flags in Reg. 11, *sts_reference_sources* for each SEC in event of no input activity, as defined by the configuration of Leaky Bucket accumulator.
- Fast Activity Monitor (part of DPLL), which raises LOS alarm on pin LOS_ALARM in event of two missing cycles of input activity on the selected source.

SEC Activity Monitors

There is a SEC activity monitor assigned to each SEC input. Each has a programmable Leaky Bucket Accumulator which is used to determine at what point the period of inactivity is deemed sufficient to raise or clear an alarm. Each SEC has its own no activity alarm bit in Reg. 11, *sts_reference_sources,*. The monitors operate continuously such that at all times the activity status of each SEC input is known.

Leaky Bucket Accumulator

Anomalies detected by the Activity Monitor are integrated in a Leaky Bucket Accumulator. There is one Leaky Bucket Accumulator per SEC input. The accumulators share a set of configuration parameters which can be programmed via Reg. 50 to Reg. 53. They are:

- Bucket size
- Alarm trigger (set threshold)
- Alarm clear (reset threshold)
- Leak rate (decay rate)

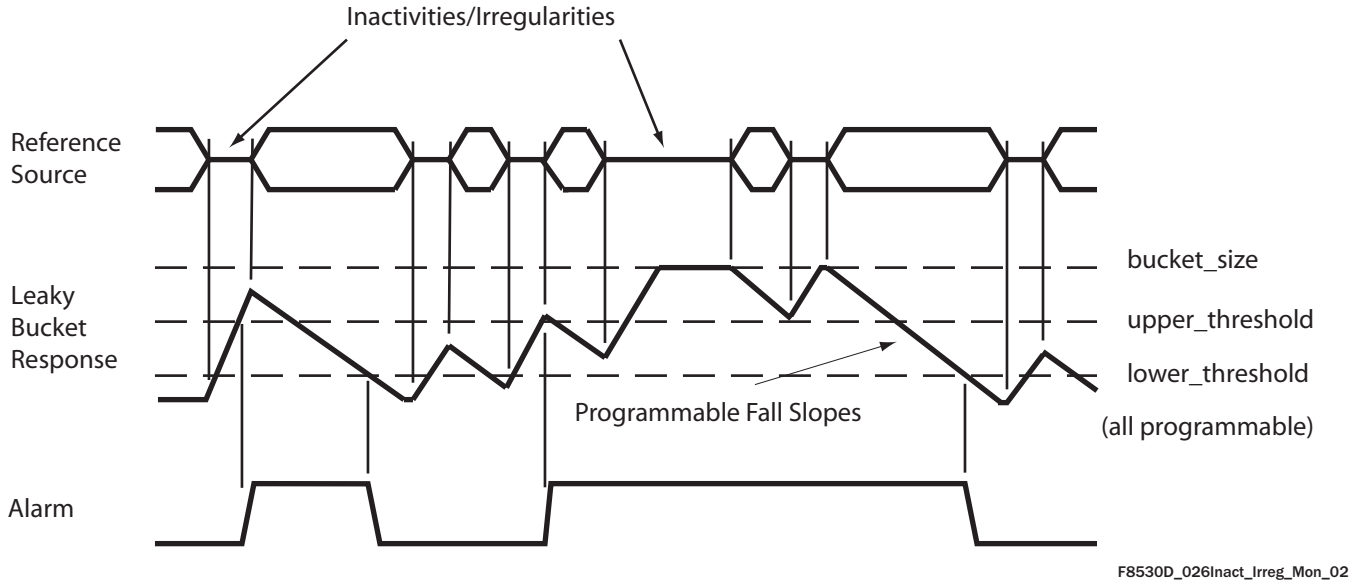
There are occasional anomalies that do not cause the Accumulator to cross the alarm setting threshold, but if the Bucket fills faster than it leaks it will eventually cross the alarm setting threshold and the associated *SEC Input Activity Alarm* bit in Reg. 11, *sts_reference_sources*, will change to 1 (Alarm active).

Each Leaky Bucket Accumulator is a digital circuit which mimics the operation of an analog integrator. If several events occur close together, each event adds to the amplitude and the alarm will be triggered quickly; if events occur over a greater time period but still sufficiently close together to overcome the decay, the alarm will be triggered eventually. If events occur at a rate which is not sufficient to overcome the decay, the alarm will not be triggered. Similarly, if no defect events occur for a sufficient time, the amplitude will decay gradually and the alarm will be cleared when the amplitude falls below the alarm clearing threshold. The ability to decay the amplitude over time allows the importance of defect events to be reduced as time passes by. This means that, in the case of isolated events, the alarm will not be set, whereas, once the alarm becomes set, it will be held on until normal operation has persisted for a suitable time (but if the operation is still erratic, the alarm will remain set). Figure 3 illustrates the behavior of the Leaky Bucket Accumulator.

Each SEC input is monitored over a 128 ms period. If, within a 128 ms period, an irregularity occurs that is not deemed to be due to allowable jitter/wander, then the Accumulator is incremented.

The Accumulator continues to increment up to the point that it reaches the programmed Bucket size. The “fill rate” of the Leaky Bucket is, therefore, 8 units/second. The “leak rate” of the Leaky Bucket is programmable to be in multiples of the fill rate (x 1, x 0.5, x 0.25 and x 0.125) to give a programmable leak rate from 8 units/sec down to 1 unit/sec. A conflict between trying to “leak” at the same time as a “fill” is avoided by preventing a leak when a fill event occurs.

Figure 3 Inactivity and Irregularity Monitoring



Leaky Bucket Timing

The time taken (in seconds) to raise an inactivity alarm on an SEC that has previously been fully active (Leaky Bucket empty) will be:

(cnfg_upper_threshold) / 8

If an input is intermittently inactive then this time can be longer. The default setting of *cnfg_upper_threshold* is 6, therefore the default time is 0.75 s.

The time taken (in seconds) to cancel the activity alarm on a previously completely inactive SEC is calculated, for a particular Leaky Bucket, as:

$[2^{(a)} \times (b - c)]/ 8$

where:

a = cnfg_decay_rate
b = cnfg_bucket_size
c = cnfg_lower_threshold
The default setting is shown in the following:

$[2^1 \times (8 - 4)] /8 = 1.0$ *secs*

Fast Activity Monitor

Anomalies on the selected clock have to be detected as they occur and the PLL must be temporarily isolated until the clock is once again pure. The SEC activity monitor cannot be used for this because the high degree of accuracy required dictates that the process be slow. To achieve the immediacy required, the PLL uses an alternative mechanism. The phase locked loop itself contains an additional fast activity monitor such that within approximately two missing input clock cycles, a no-activity flag is raised and the DPLL is frozen in Digital Holdover mode. This flag generates LOS (Loss of Signal) alarm on pin LOS_ALARM.

With the DPLL in Digital Holdover mode it is isolated from further disturbances. If the input becomes active again then the DPLL will continue to lock to the input, with little disturbance.

Phase Locked Loops (PLLs)

This section is in four parts;

- Overview description of the PLLs
- Architectural description, introducing the sub-blocks and their interconnection options for different frequency selection and jitter filtering
- Description of PLL controls- phase error detector options, Loop bandwidth and damping selection
- DPLL summary feature list.

PLL Overview

The PLL circuitry comprises the following blocks shown in Figure 1: Two Digital PLLs (DPLL1 and DPLL2), two output multiplying and filtering Analog PLLs (APLL1 and APLL2), output frequency dividers in an Output Port Frequency Selection block, a synthesis block, multiplexers MUX1 and MUX2, and a feedback Analog PLL (APLL3).

These functional blocks, and their interconnections, are highly configurable, via register control, which provides a

range of output frequencies and levels of jitter performance. However if the device is configured by hardware alone, then the PLLs are configured as shown in Table 7 and 8.

Digital Synthesis is used to generate all required SONET/SDH output frequencies. The digital logic operates at 204.8 MHz that is multiplied up from the external 12.800 MHz oscillator module. Hence the best resolution of the output signals from the DPLLs is one 204.8 MHz cycle or 4.9 ns.

Additional resolution and lower final output jitter is provided by a de-jittering APLL that reduces the 4.9 ns p-p jitter from the digital down to 500 ps p-p and 60 ps RMS as typical final outputs measured broadband (from 10 Hz to 1 GHz). This arrangement combines the advantages of the flexibility and repeatability of a DPLL with the low jitter of an APLL.

The DPLLs in the ACS8526 are programmable for parameters of bandwidth (18, 35 and 70 Hz) and damping factor (from 1.2 to 20). See Sections “DPLL1 Jitter Transfer Characteristic, (Freq. = 1.544 MHz, Jitter = 0.2 UI p-p, Damping Factor = 5)” on page 14, and “Damping Factor Programmability” on page 15.

DPLL1 input frequency is programmable with 12 common SONET/SDH spot frequencies. See *cnfg_nominal_frequency* Reg. 3C and Reg. 3D

The DPLL has programmable frequency acceptance and output range (from 0 to 80 ppm) set by the allowable offset between the expected input frequency and the calibrated external frequency, Reg. 41 and Reg. 42).

There is no requirement to understand the loop filter equations or detailed gain parameters since all high level factors such as overall bandwidth can be set directly in registers via the microprocessor interface. No external critical components are required for either the internal DPLLs or APLLs, providing another key advantage over traditional discrete designs.

DPLL1 always produces an output at 77.76 MHz to feed the APLL, regardless of the frequency selected at the output pins or the locking frequency (frequency at the input of the Phase and Frequency Detector- PFD).

DPLL2 can be operated at a number of frequencies. This is to enable the generation of extra output frequencies, which cannot be easily related to 77.76 MHz. If DPLL2 is enabled, it locks to the 8 kHz from DPLL1. This is because all of the frequencies of operation of DPLL2 can be divided to 8 kHz and this will ensure synchronization of frequencies, from 8kHz upwards, within the two DPLLs.

Both of the DPLLs’ outputs can be connected to multiplying and filtering APLLs. The outputs of these APLLs are divided making a number of frequencies simultaneously available for selection at the output clock ports. The various combinations of DPLL, APLL and divider configurations allow for generation of a comprehensive set of frequencies, as listed in Table 9, “Output Frequency Selection,” on page 19.

A function is provided to synchronize the lower output frequencies when DPLL1 is locked to a high frequency reference input. The dividers that generate the 2 kHz and 8 kHz outputs are reset such that the output 2/8 kHz clocks are lined up with the input 2 kHz.

The PLL configurations required for particular output frequencies are described in “Output Frequency Selection by Hardware” on page 17, and “Output Frequency Selection by Register Programming” on page 17.

An advanced feature of the device is its ability to control the amount of jitter and wander that is tolerated on the input. This is achieved by the configuration of the Phase and Frequency detectors within the DPLLs, which determines the phase error input to the Digital Loop Filter. For basic operation, the configuration should not be changed from the default settings.

PLL Architecture

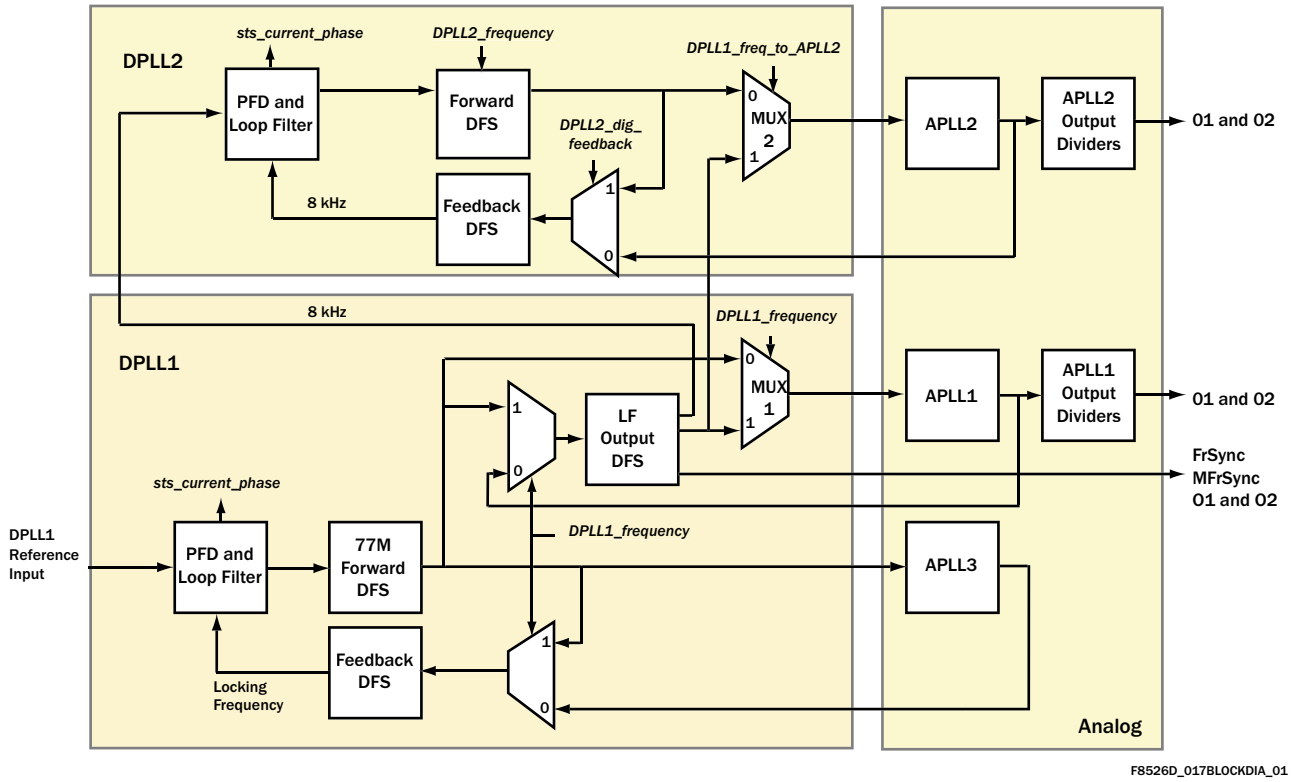
Figure 4 shows the PLL arrangement in more detail. Each DPLL comprises a generic Phase and Frequency Detector (PFD) with a Digital Loop filter, together with Forward, Feedback, and Low Frequency (LF) (DPLL1 only) Digital Frequency Synthesis (DFS) blocks. The Forward DFS block represents a Digital Timed Oscillator (DTO).

The DPLL architecture for DPLL1 is more complex than that of DPLL2. See “DPLL Feature Summary” on page 16..

The selected SEC input is always supplied to DPLL1. DPLL1 may use either digital feedback or analog feedback (via APLL3).

DPLL2 always takes its feed from DPLL1 and cannot be used to select a different input to that of DPLL1.

Figure 4 PLL Block Diagram



DFS is a technique for generating an output frequency using a higher frequency system clock (204.8 MHz in the case of the 77.76 MHz synthesis). However, the edges of the output clock are not ideally placed in time, since all edges of the output clock will be aligned to the active edge of the system clock. This means that the generated clock will inherently have jitter on it equivalent to one period of the system clock.

DPLL1 and APLLs

DPLL1 always produces 77.76 MHz. The input reference is either passed directly to the PFD or via a pre-divider (not shown) to produce the reference input. The feedback 77.76 MHz is either divided or synthesized to generate the locking frequency.

The DPLL1 77M Forward DFS block uses DFS clocked by the 204.8 MHz system clock to synthesize the 77.76 MHz and, therefore, has an inherent 4.9 ns of p-p jitter. There is an option to use a feedback APLL (APLL3) to filter out this jitter before the 77.76 MHz is used to generate the feedback locking frequency in the DPLL1 feedback DFS block. This analog feedback option allows a lower jitter (<1 ns) feedback signal to give maximum performance.

The 77.76 MHz is fed to DPLL1 LF Output DFS block and to APLL1. The low frequency DPLL1 LF Output DFS block is used to produce three frequencies; two of them, Digital1 and Digital2, are available for selection to be produced at outputs 01 and 02, and the third frequency can produce multiple E1/DS1 rates via the filtering APLLs. The input clock to the DPLL1 LF Output DFS block is 77.76 MHz from APLL1 (post jitter filtering) or 77.76 MHz direct from the DPLL1 77M Forward DFS.

Utilizing the clock from APLL1 will result in lower jitter outputs from the DPLL1 LF Output DFS block. However, when the input to the APLL1 is taken from the DPLL1 LF Output DFS block, the input to that block comes directly from the DPLL1 77M Forward DFS block so that a “loop” is not created.

APLL1 is for multiplying and filtering. The input to APLL1 is controlled by MUX 1 (see “Multiplexers” on page 13). The frequency from APLL1 is four times its input frequency i.e. 311.04 MHz when used with a 77.76 MHz input. APLL1 is subsequently divided by 1, 2, 4, 6, 8, 12, 16 and 48 and these are available at the 01 and 02 Outputs.

DPLL2 & APLLs

DPLL2 is simpler than DPLL1. DPLL2 offers no low frequency output. The DPLL2 input can only be used to lock to DPLL1. Unlike DPLL1, the DPLL2 Forward DFS block does not always generate 77.76 MHz. The possible

frequencies are listed in Table 12, “APLL2 Frequencies,” on page 24. Similarly to DPLL1, the output of the DPLL2 Forward DFS block is generated using DFS clocked by the 204.8 MHz system clock and will have an inherent jitter of 4.9 ns.

The DPLL2 feedback DFS also has the facility to be able to use the post APLL2 (jitter-filtered) clock to generate the feedback locking frequency. Again, this will give the maximum performance by using a low jitter feedback.

APLL2 block is also for multiplying and filtering. The input to APLL2 is controlled by MUX 2 (see “Multiplexers” on page 13) and can come either from the DPLL2 Forward DFS block or from DPLL1.

The frequency generated from the APLL2 is four times its input frequency i.e. 311.04 MHz when used with a 77.76 MHz input. APLL2 is subsequently divided by 2, 4, 8, 12, 16, 48 and 64 and these are available at the 01 and 02 Outputs.

“Digital” Frequencies

DFS is also carried out by DPLL1 LF Output DFS block in Figure 4 (E1/DS1 Synthesis block in Figure 1). This block is clocked either by the DPLL1 77M Forward DFS block or via the APLL1, and generates the single frequencies Digital1 and Digital2 (see Table 13 and Table 14). The input clock frequency of the DFS is always 77.76 MHz and as such has a period of approximately 12 ns. The jitter generated on the Digital outputs is relatively high, because they do not pass through an APLL for jitter filtering. The minimum level of jitter is when DPLL1 is in analog feedback mode, when the p-p jitter will be approximately 13 ns (equivalent to a period of the DFS clock). The maximum jitter is generated when in digital feedback mode, when the total is approximately 18 ns.

The E1/DS1 Synthesis block generates the E1/DS1 rates for the APLLs, using the output from DPLL1. It generates 12E1, 16E1, 16DS1 or 24DS1, for selection by MUX1.

FrSync, MFrSync, 2 kHz and 8 kHz Clock Outputs

Whilst the FrSync and MFrSync Outputs are always supplied from DPLL1, the 2 kHz and 8 kHz options available from the 01 and 02 Outputs can be supplied from either DPLL1 or DPLL2 (Reg. 7A Bit 7).

Multiplexers

Multiplexers MUX1 and MUX2 are used to select the appropriate inputs to the Analog PLLs. The function they represent is controlled by *cnfg_DPLL1_frequency* Reg. 65.

APLL2 Input Selection using MUX 2

- DPLL2 selected for input to APLL2 (Reg. 65 Bit 6 = 0) The input frequency is selected from the operating frequency of DPLL2 (Reg. 64 Bits [2:0])
- DPLL1 + LF Output DFS selected for Input to APLL2
  - 12E1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 00)
  - 16E1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 01)
  - 24DS1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 10)
  - 16DS1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 11)

APLL1 Input Selection using MUX 1

- DPLL1 (77.76 MHz) output fed to input of APLL1. Analog feedback used in DPLL1 (Reg. 65 Bits [2:0] set to 000)
- DPLL1 (77.76 MHz) output fed to input of APLL1. Digital feedback used in DPLL1 (Reg. 65 Bits [2:0] set to 001)
- DPLL1 + LF Output DFS selected for input to APLL1
  - 12E1 (Reg. 65 Bits [2:0] set to 010)
  - 16E1 (Reg. 65 Bits [2:0] set to 011)
  - 24DS1 (Reg. 65 Bits [2:0] set to 100)
  - 16DS1 (Reg. 65 Bits [2:0] set to 101)

Notes: (i) DPLL2 output cannot be selected for input to APLL1

(ii) If both multiplexers select LF Output DFS, the same frequency value must be selected in Reg. 65 Bits [2:0] and Reg. 65 Bits [5:4].

APLLs

There are three main APLLs. APLL1 and APLL2 provide a lower final output jitter reducing the 4.9 ns p-p jitter from the digital down to 500 ps p-p and 60 ps RMS as typical final outputs measured broadband (from 10 Hz to 1 GHz). The feedback APLL (APLL3) is selected by default; it provides improved performance over the digital feedback.

APLL Output Dividers

Each APLL has its own divider. Each divider simultaneously outputs a series of fixed ratios of its APLL input. Any of these divided outputs may be selected as the output on Outputs 01 or 02 by configuring Reg. 61 and Reg. 62, with the following exceptions: (APLL1)/2 and (APLL1)/1 only available for Output 01 (differential port), and (APLL1)/48 only available for Output 02.

PFD and Loop Filters

The PFD compares the input reference with that of the locking frequency (feedback) giving a phase error which is then filtered by a 100Hz low pass filter, to give the average phase error for input into a loop filter. The PFD is quite complex and has several programmable options to determine what phase error value is fed to the loop (See "Phase and Frequency Detectors" on page 15.") depending on the type of jitter/wander expected.

The loop filter bandwidth and damping is programmable to optimize the locking time/ability to track the input. See Figure 5 and "Damping Factor Programmability" on page 15.

PLL Operational Controls

The main factors controlling the operation of the PLL are:

1. Input reference and feedback frequency selection - See "PLL Architecture" on page 11., and "Input Locking Frequency Modes" on page 7.
2. Loop Bandwidth and Damping factor of the DPLLs - these determine how fast the device can to lock to the selected input, or how tightly it can track the input.
3. PFD settings - these affect the input phase error to the Loop filter and relate to jitter and wander tolerance - See "Phase/Frequency/Lock Detection" on page 15.

DPLL1 initially tries to lock to the input frequency of the selected input SEC. By default, it uses a wide "acquisition" bandwidth setting until it has achieved frequency lock, then DPLL1 switches to using a narrower "Locked" bandwidth setting as it locks to the phase of the input.

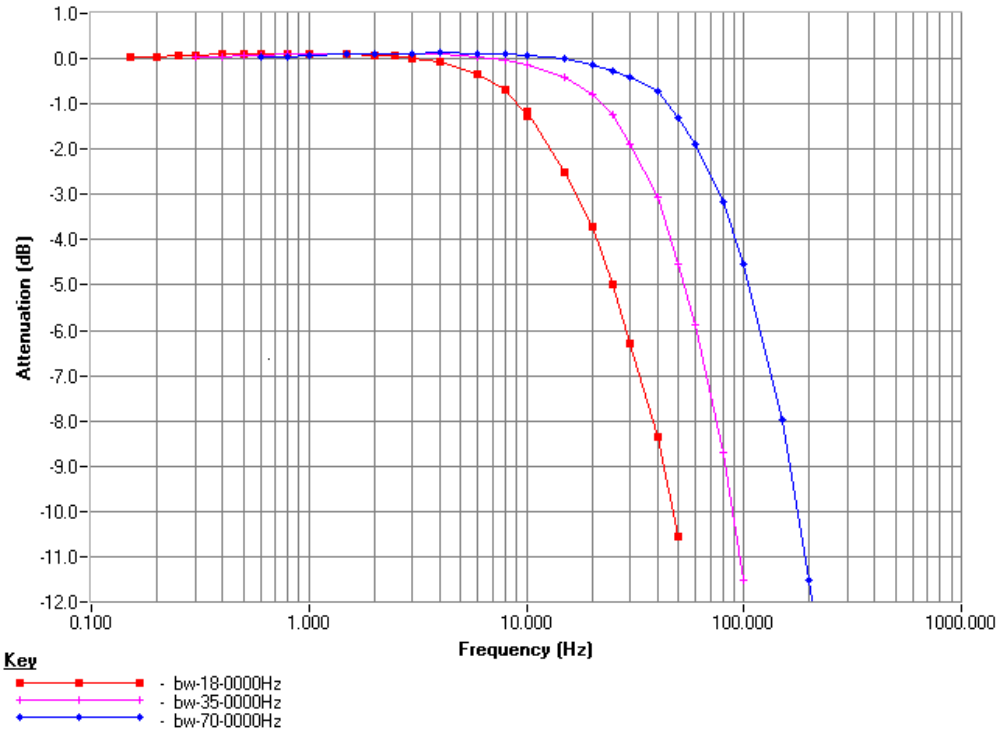
Input Acquisition Bandwidth

DPLL1 has programmable acquisition bandwidth of 18, 35 or 70 Hz. The default is set to 70 Hz.

Input Locked Bandwidth

The ACS8526 has programmable "Locked" bandwidth of 18, 35 or 70 Hz. These bandwidth settings correspond to the -3 dB jitter attenuation point on the ACS8526's jitter transfer characteristic shown in Figure 5. If the ACS8526 is used with only DPLL1, the highest bandwidth setting is recommended to ensure the closest tracking of the input SEC. If DPLL2 is also to be used, DPLL1 should be set to a lower bandwidth setting than DPLL2. The lowest bandwidth setting will provide the highest jitter attenuation, although this is not the main function of the ACS8526 device.

Figure 5 DPLL1 Jitter Transfer Characteristic, (Freq. = 1.544 MHz, Jitter = 0.2 UI p-p, Damping Factor = 5)



Damping Factor Programmability

The DPLL damping factor is set by default to provide a maximum wander gain peak of around 0.1 dB. Many of the specifications (e.g. GR-1244-CORE [13], G.812[7] and G.813[8]) specify a wander transfer gain of less than 0.2 dB. GR-253[11] specifies jitter (not wander) transfer of less than 0.1 dB. To accommodate the required levels of transfer gain, the ACS8526 provides a choice of damping factors, with more choice given as the bandwidth setting increases into the frequency regions classified as jitter. Table 5 shows which damping factors are available for selection at the different bandwidth settings, and the corresponding jitter transfer approximate gain peak.

Table 5 Available Damping Factors for different DPLL Bandwidths, and Associated Gain Peak Values

Bandwidth/Hz	Reg. 6B [2:0]	Damping Factor selected	Gain Peak/dB
18	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

Phase/Frequency/Lock Detection

Two main types of detector are available in the ACS8526:

- Phase and frequency detectors, and
- Phase Loss/Lock detectors.

Phase and Frequency Detectors

There are two multi-phase and frequency detectors, one for each DPLL. The multi-phase and frequency detectors are used to compare input and feedback clocks. They operate at input frequencies up to 77.76 MHz (155.52 MHz is internally divided down to 77.76 MHz).

A common arrangement however is to use Lock8k mode (See Bit 6 of Reg. 22 and 23), where all input frequencies are divided down to 8 kHz internally. Marginally better MTIE figures may be possible in direct lock mode due to more regular phase updates. This direct locking capability is one of the unique features of the ACS8526.

A multi-phase detector (patent pending) approach is used in order to give an infinitesimally small input phase resolution combined with large jitter tolerance. A multi-phase detector comprises the following phase detectors:

- Phase and frequency detector (±360°, or ±180° range).
- An Early/Late phase detector for fine resolution.
- A multi-cycle phase detector for large input jitter tolerance (up to 8191 UI), which captures and remembers phase differences of many cycles between input and feedback clocks.

The phase detectors can be configured to be immune to occasional missing input clock pulses by using nearest edge detection (±180° capture) or the normal ±360° phase capture range which gives frequency locking. The device will automatically switch to nearest edge locking when the multi-UI phase detector is not enabled, and the other phase detectors have detected that phase lock has been achieved. It is possible to disable the selection of nearest edge locking via Reg. 03 Bit 6 (set to 1). In this setting, frequency locking will always be enabled.

The balance between the first two types of phase detector employed can be adjusted via Reg. 6A to 6D. The default settings should be sufficient for all modes. Adjustment of these settings affects only small signal overshoot and bandwidth.

The multi-cycle phase detector (wide-range) is enabled via Reg. 74, Bit 6 set to 1 and the range is set in exponentially increasing steps from ±1 UI up to 8191 UI via Reg. 74, Bits [3:0].

When this detector is enabled it keeps a track of the correct phase position over many cycles of phase difference to give excellent jitter tolerance. This provides an alternative to switching to Lock8k mode as a method of achieving high jitter tolerance.

An additional control (Reg. 74 Bit 5) enables the multi-phase detector value to be used in the final phase value as part of the DPLL loop. When enabled by setting *High*, the multi cycle phase value will be used in the loop and gives faster pull-in (but more overshoot).

The characteristics of the loop will be similar to Lock8k mode where again large input phase differences contribute to the loop dynamics. Setting the bit *Low* only uses a max figure of 360° in the loop and will give slower pull-in but gives less overshoot. The final phase position that the loop has to pull in to is still tracked and remembered by the multi-cycle phase detector in either case.

Phase Lock/Loss Detectors

Phase lock/loss detection is handled in several ways. Phase loss can be triggered from:

- The fine phase lock detector, which measures the phase between input and feedback clock
- The coarse phase lock detector, which monitors whole cycle slips
- Detection that the DPLL is at min. or max. frequency
- Detection of no activity on the input.

Each of these sources of phase loss indication is individually enabled via registers bits (see Reg. 73 and 74). Phase lock or loss is used to determine whether to switch to nearest edge locking and whether to use acquisition or normal bandwidth settings for the DPLL. Acquisition bandwidth is used for faster pull-in from an unlocked state.

The coarse phase lock detector detects phase differences of n cycles between input and feedback clocks, where n is set by Reg. 74, Bits [3:0]; the same register that is used for the coarse phase detector range, since these functions go hand in hand. This detector may be used in the case where it is required that a phase loss indication is not given for reasonable amounts of input jitter and so the fine phase loss detector is disabled and the coarse detector is used instead.

DPLL Feature Summary

(* = hardware default selection)

DPLL1 Main Features

- Multiple E1 and DS1 outputs supported
- Low jitter MFrSync (2 kHz) and FrSync (8 kHz) outputs
- Multiple phase loss and multiple phase detectors (see “DPLL1 Advanced Features”)
- Direct PLL locking to common SONET/SDH input frequencies or any multiple of 8 kHz
- Fast detection on input failure and entry into Digital Holdover mode (holds at the current frequency value)
- Frequency translation between input and output rates via direct digital synthesis
- High accuracy digital architecture for stable PLL dynamics combined with an APLL for low jitter final output clocks
- Selectable Automatic DPLL bandwidth control (auto* selects either Locked bandwidth, or Acquisition bandwidth), or Locked DPLL bandwidth (Reg. 3B Bit 7)
- Two programmable bandwidth controls:
  - Locked bandwidth: 18, 35* or 70 Hz (Reg. 67)
  - Acquisition bandwidth: 18, 35 or 70* Hz (Reg. 69)
- Programmable damping factor, (For optional faster locking and peaking control) Factors = 1.2, 2.5, 5, 10* or 20 (Reg. 6B, Bits [2:0])
- Programmable DPLL pull-in frequency range (Reg. 41, Reg. 42).

DPLL1 Advanced Features

Phase Loss Indicators

- Phase loss fine limit. on*/off (Reg. 73 Bit 7) and programmable range 0 to 7 Dec. (Reg. 73 Bits [2:0])
- Multi-cycle phase loss course limit, on*/off (Reg. 74 Bit 7) and selectable range from ±(1 to 8191) UI in 13 steps (Reg. 74 Bits [3:0]).

Phase Detector Controls

- Multi-cycle phase detector - Course phase detector & capture range on*/off (Reg. 74 Bit 6) and selectable range from ±(1 to 8191) UI in 13 steps (Reg. 74 Bits [3:0]). If selected, this feature increases jitter and wander tolerance to a maximum of 8192 UI (normally limited to ±0.5 UI)
- Use of coarse phase detector result in DPLL algorithm, on*/off (Reg. 74 Bit 5) - speeds up phase locking
- Limit DPLL1 Integral when at DPLL frequency limit, on*/off (Reg. 3B Bit 3) - reduces overshoot
- Anti-noise filter for low frequency inputs, on/off* (Reg. 76 Bit 7).

Advanced Phase Detector Controls

- DPLL1 PD2 gain enable, on*/off (Reg. 6D Bit 7)
  If on, this allows automatic gain selection according to the type of feedback to the DPLL (For the digital feedback setting, the gain used for PD2 is given by Reg. 6D Bits [2:0]). If off, PD2 is not used.

- Adjustable gain settings for PD2 (when enabled), for the following feedback cases:
  - Digital feedback (Reg. 6D Bits [2:0])
  - Analog feedback (all frequencies above 8 kHz) (Reg. 6D Bits [6:4])
  - Analog 8k (or less) feedback (Reg. 6B Bits [2:0]).

DPLL2 Main Features

- Always locked to DPLL1
- A single programmable bandwidth control: 18*, 35 or 70 Hz
- Programmable damping factor, (For optional faster locking and peaking control) Factors = 1.2, 2.5, 5*, 10 or 20.
- Digital feedback, on*/off (Reg. 35 Bit 6)
- Output frequency selection (Reg. 64)
  - DS3/E3 support (44.736 MHz / 34.368 MHz) independent of rates from DPLL1
  - Low jitter E1/DS1 options independent of rates from DPLL1
  - Frequencies of n x E1/DS1 including 16 and 12 x E1, and 16 and 24 x DS1 supported
  - Squelched (clock off)
- Can provide the source for the 2 kHz and 8 kHz outputs available at Outputs 01 and 02 (Reg. 7A Bit 7).

DPLL2 Advanced Features

The advanced features are the same as those for DPLL1, with DPLL2 using the configuration values for DPLL1, with the following exceptions:

Advanced Phase Detector Controls

- PD2 gain control enable, on*/off (Reg. 6C Bit 7)
  If on, this allows automatic gain selection according to the type of feedback to the DPLL (For the digital feedback setting, the gain used for PD2 is given by (Reg. 6C Bits [2:0]). If off, PD2 is not used
- Adjustable gain settings for PD2 (with auto switching enabled), for the following feedback cases:
  - Digital feedback (Reg. 6C Bits [2:0])
  - Analog feedback (all frequencies above 8K) (Reg. 6C Bits [6:4])
  - Analog 8k (or less) feedback (Reg. 6A Bits [2:0]).

Outputs

The ACS8526 delivers four output signals on the following ports: Two clocks, one each on Output 01 and 02, and two Sync signals, one each on output ports FrSync and MFrSync. Outputs 01 and 02 are independent of each other and are individually selectable. Output 01 is a differential port (pins 01POS and 01NEG), and can be selected to be PECL or LVDS via Reg. 3A *cnfg_differential_output*. Output 02 (pin 02) and the Sync outputs are TTL/CMOS compatible.

The two Sync outputs, FrSync (8 kHz) and MFrSync (2 kHz), are derived from DPLL1.

The frequencies available on the outputs can be selected from a range of spot frequencies by either:

- Hardware selection: configuring the hardware pins OP_FREQ1 [2:0], OP_FREQ2[2:0] and SONSDH, which are read on reset, or
- Register programming: writing to the registers after the end of the initialization period.

Output Frequency Selection by Hardware

Tables 6 and 7 show the hardware settings for selecting particular output frequencies on Outputs 01 and 02. Note that the hardware frequency selection method provides only a subset (11) of the total number of frequencies (55) available when selecting by register programming.

Output Frequency Selection by Register Programming

The output frequencies on 01 and 02 are controlled by a number of interdependent parameters (refer to “PLL Architecture” on page 11). The frequencies of the output clocks are selectable from a range of pre-defined spot frequencies/port technologies, as defined in Table 8.

Outputs 01 & 02 Frequency Configuration Steps

The output frequency selection is performed in the following steps:

1. Refer to Table 10, Frequency Divider Look-up, to choose a set of output frequencies.
2. Refer to the Table 10 to determine the required APLL frequency to support the frequency set.
3. Refer to Table 11, APLL1 Frequencies, and Table 12, APLL2 Frequencies, to determine in what mode DPLL1 and DPLL2 need to be configured, considering the output jitter level.

4. Refer to Table 13, 01 and 02 Output Frequency Selection, and the column headings in Table 10, Frequency Divider Look-up, to select the appropriate frequency from either of the APLLs on each output as required.

Table 6 Output 01 Frequency Selection by Hardware Configuration

01_FREQ			SONSDHB Pin	Output Frequency/ MHz	DPLL Selected	DPLL Mode	Jitter Level (typ)	
2	1	0					rms (ps)	p-p (ns)
0	0	0	X	0	-	-	-	-
0	0	1	0	34.368	DPLL2	E3	120	1
			1	44.736	DPLL2	DS3	110	1
0	1	0	X	19.44	DPLL1	Analog feedback	60	0.6
0	1	1	X	25.92	DPLL1	Analog feedback	60	0.6
1	0	0	X	38.88	DPLL1	Analog feedback	60	0.6
1	0	1	X	51.84	DPLL1	Analog feedback	60	0.6
1	1	0	X	77.76	DPLL1	Analog feedback	60	0.6
1	1	1	X	155.52	DPLL1	Analog feedback	60	0.6

Table 7 Output 02 Frequency Selection by Hardware Configuration

02_FREQ			SONSDHB Pin	01_FREQ = "001"	Output Frequency/ MHz	DPLL Selected	DPLL Mode	Jitter Level (typ)	
2	1	0						rms (ps)	p-p (ns)
0	0	0	X	X	0	-	-	-	-
0	0	1	0	FALSE	2.048	DPLL2	16E1	400	2
			1		1.544	DPLL2	16DS1	200	1.2
0	0	1	0	TRUE	2.048	DPLL1	12E1	900	0.45
			1		3.088	DPLL1	24DS1	110	0.75
0	1	0	0	X	34.368	DPLL2	E3	120	1
			1	X	44.736	DPLL2	DS3	110	1
0	1	1	X	X	19.44	DPLL1	Analog feedback	60	0.6
1	0	0	X	X	25.92	DPLL1	Analog feedback	60	0.6
1	0	1	X	X	38.88	DPLL1	Analog feedback	60	0.6
1	1	0	X	X	51.84	DPLL1	Analog feedback	60	0.6
1	1	1	X	X	77.76	DPLL1	Analog feedback	60	0.6

Table 8 Output Reference Source Selection Table

Port Name	Output Port Technology	Frequencies Supported
Output 01	LVDS/PECL (LVDS default)	Frequency selection as per Table 9 and Table 13
Output 02	TTL/CMOS	
FrSync	TTL/CMOS	FrSync, 8 kHz programmable pulse width and polarity, see Reg. 7A.
MFrSync	TTL/CMOS	MFrSync, 2 kHz programmable pulse width and polarity, see Reg. 7A.

Note...1.544 MHz/2.048 MHz are shown for SONET/SDH respectively. Pin SONSDHB controls default. When High, SONET is default.

Table 9 Output Frequency Selection

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
2 kHz	77.76 MHz Analog	-	-	60	0.6
2 kHz	Any digital feedback mode	-	-	1400	5
8 kHz	77.76 MHz Analog	-	-	60	0.6
8 kHz	Any digital feedback mode	-	-	1400	5
1.536	-	12E1 mode	Select DPLL2	500	2.3
1.536	-	-	Select DPLL1 12E1	250	1.5
1.544	-	16DS1 mode	Select DPLL2	200	1.2
1.544	-	-	Select DPLL1 16DS1	150	1.0
1.544 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
1.544 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
2.048	-	12E1 mode	Select DPLL2	500	2.3
2.048	-	-	Select DPLL1 12E1	250	1.5
2.048	-	16E1 mode	Select DPLL2	400	2.0
2.048	-	-	Select DPLL1 16E1	220	1.2
2.048 (not Output 01)	12E1 mode	-	-	900	4.5
2.048 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
2.048 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
2.059	-	16DS1 mode	Select DPLL2	200	1.2
2.059	-	-	Select DPLL1 16DS1	150	1.0

Table 9 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
2.059 (not Output 01)	16DS1 mode	-	-	760	2.6
2.316	-	24DS1 mode	Select DPLL2	110	0.75
2.316	-	-	Select DPLL1 24DS1	110	0.75
2.731	-	16E1 mode	Select DPLL2	400	1.5
2.731	-	-	Select DPLL1 16E1	220	1.2
2.731 (not Output 01)	16E1 mode	-	-	250	1.6
2.796	-	DS3 mode	Select DPLL2	110	1.0
3.088	-	24DS1 mode	Select DPLL2	110	0.75
3.088	-	-	Select DPLL1 24DS1	110	0.75
3.088 (not Output 01)	24DS1 mode	-	-	110	0.75
3.088 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
3.088 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
3.728	-	DS3 mode	Select DPLL2	110	1.0
4.096 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
4.096 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
4.296	-	E3 mode	Select DPLL2	120	1.0
4.86	-	77.76 MHz mode	Select DPLL2	60	0.6
5.728	-	E3 mode	Select DPLL2	120	1.0
6.144	12E1 mode	-	-	900	4.5
6.144	-	12E1 mode	Select DPLL2	500	2.3
6.144	-	-	Select DPLL1 12E1	250	1.5
6.176	16DS1 mode	-	-	760	2.6
6.176	-	16DS1 mode	Select DPLL2	200	1.2
6.176	-	-	Select DPLL1 16DS1	150	1.0
6.176 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
6.176 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
6.48	-	77.76 MHz mode	Select DPLL2	60	0.6
6.48 (not Output 01)	77.76 MHz analog	-	-	60	0.6
6.48 (not Output 01)	77.76 MHz digital	-	-	60	0.6

Table 9 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
8.192	12E1 mode	-	-	900	4.5
8.192	16E1 mode	-	-	250	1.6
8.192	-	16E1 mode	Select DPLL2	400	2.0
8.192	-	-	Select DPLL1 16E1	220	1.2
8.192 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
8.192 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
8.235	16DS1 mode	-	-	760	2.6
9.264	24DS1 mode	-	-	110	0.75
9.264	-	24DS1 mode	Select DPLL2	110	0.75
9.264	-	-	Select DPLL1 24DS1	110	0.75
10.923	16E1 mode	-	-	250	1.6
11.184	-	DS3 mode	Select DPLL2	110	1.0
12.288	12E1 mode	-	-	900	4.5
12.288	-	12E1 mode	Select DPLL2	500	2.3
12.288	-	-	Select DPLL1 12E1	250	1.5
12.352	24DS1 mode	-	-	110	0.75
12.352	16DS1 mode	-	-	760	2.6
12.352	-	16DS1 mode	Select DPLL2	200	1.2
12.352	-	-	Select DPLL1 16DS1	150	1.0
12.352 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
12.352 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
16.384	12E1 mode	-	-	900	4.5
16.384	16E1 mode	-	-	250	1.6
16.384	-	16E1 mode	Select DPLL2	400	2.0
16.384	-	-	Select DPLL1 16E1	220	1.2
16.384 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
16.384 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
16.469	16DS1 mode	-	-	760	2.6
17.184	-	E3 mode	Select DPLL2	120	1.0

Table 9 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
18.528	24DS1 mode	-	-	110	0.75
18.528	-	24DS1 mode	Select DPLL2	110	0.75
18.528	-	-	Select DPLL1 24DS1	110	0.75
19.44	77.76 MHz analog	-	-	60	0.6
19.44	77.76 MHz digital	-	-	60	0.6
19.44	-	77.76MHz mode	Select DPLL2	60	0.6
21.845	16E1 mode	-	-	250	1.6
22.368	-	DS3 mode	Select DPLL2	110	1.0
24.576	12E1 mode	-	-	900	4.5
24.576	-	12E1 mode	Select DPLL2	500	2.3
24.576	-	-	Select DPLL1 12E1	250	1.5
24.704	24DS1 mode	-	-	110	0.75
24.704	16DS1 mode	-	-	760	2.6
24.704	-	16DS1 mode	Select DPLL2	200	1.2
24.704	-	-	Select DPLL1 16DS1	150	1.0
25.92	77.76 MHz analog	-	-	60	0.6
25.92	77.76 MHz digital	-	-	60	0.6
32.768	16E1 mode	-	-	250	1.6
32.768	-	16E1 mode	Select DPLL2	400	2.0
32.768	-	-	Select DPLL1 16E1	220	1.2
34.368	-	E3 mode	Select DPLL2	120	1.0
37.056	24DS1 mode	-	-	110	0.75
37.056	-	24DS1 mode	Select DPLL2	110	0.75
37.056	-	-	Select DPLL1 24DS1	110	0.75
38.88	77.76 MHz analog	-	-	60	0.6
38.88	77.76 MHz digital	-	-	60	0.6
38.88	-	77.76 MHz mode	Select DPLL2	60	0.6
44.736	-	DS3 mode	Select DPLL2	110	1.0
49.152 (Output 01 only)	12E1 mode	-	-	900	4.5
49.408 (Output 01 only)	16DS1 mode	-	-	760	2.6
51.84	77.76 MHz analog	-	-	60	0.6

Table 9 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
51.84	77.76 MHz digital	-	-	60	0.6
65.536 (Output 01 only)	16E1 mode	-	-	250	1.6
68.736	-	E3 mode	Select DPLL2	120	1.0
74.112 (Output 01 only)	24DS1 mode	-	-	110	0.75
77.76	77.76 MHz analog	-	-	60	0.6
77.76	77.76 MHz digital	-	-	60	0.6
77.76	-	77.76 MHz mode	Select DPLL2	60	0.6
98.304 (Output 01 only)	12E1 mode	-	-	900	4.5
98.816 (Output 01 only)	16DS1 mode	-	-	760	2.6
131.07 (Output 01 only)	16E1 mode	-	-	250	1.6
148.22 (Output 01 only)	24DS1 mode	-	-	110	0.75
155.52 (Output 01 only)	77.76 MHz analog	-	-	60	0.6
155.52 (Output 01 only)	77.76 MHz digital	-	-	60	0.6
311.04 (Output 01 only)	77.76 MHz analog	-	-	60	0.6
311.04 (Output 01 only)	77.76 MHz digital	-	-	60	0.6

Table 10 Frequency Divider Look-up

Transmission Rate	APLL Frequency	APLL/2	APLL/4	APLL/6	APLL/8	APLL/12	APLL/16	APLL/48	APLL/64
OC-N Rates	311.04	155.52	77.76	51.84	38.88	25.92	19.44	6.48	4.86
E3	274.944	137.472	68.376	-	34.368	-	17.184	5.728	4.296
DS3	178.944	89.472	44.736	-	22.368	-	11.184	3.728	2.796
24DS1	148.224	74.112	37.056	24,704	18.528	12.352	9.264	3.088	2.316
16E1	131.072	65.536	32.768	21.84533	16.384	10.92267	8.192	2.730667	2.048
16DS1	98.816	49.408	24.704	16.46933	12.352	8.234667	6.176	2.058667	1.544
12E1	98.304	49.152	24.576	16.384	12.288	8.192	6.144	2.048	1.536

Note...All frequencies in MHz.

Table 11 APLL1 Frequencies

APLL1 Frequency	Synthesis/MUX setting for APLL1 input	DPLL1 Frequency Control Reg. 65 Bits[2:0]	Output Jitter Level ns (p-p)
311.04	Normal (digital feedback)	000	<0.5
311.04 MHz	Normal (analog feedback)	001	<0.5
98.304 MHz	12E1 (digital feedback)	010	<2
131.072 MHz	16E1 (digital feedback)	011	<2
148.224 MHz	24DS1 (digital feedback)	100	<2
98.816 MHz	16DS1 (digital feedback)	101	<2
-	Do not use	110	-
-	Do not use	111	-

Table 12 APLL2 Frequencies

APLL2 Frequency	DPLL Mode	DPLL2 Forward DFS Frequency (MHz)	DPLL2 Freq Control Register Bits Reg. 64 Bits [2:0]	APLL2 Input from DPLL1 or 2. Reg. 65 Bit 6	DPLL1 + Synthesis Freq to APLL2 Register Bits Reg. 65 Bits [5:4]	Output Jitter Level ns (p-p)
311.04 MHz	DPLL2-Squelched	77.76	000	0 (DPLL2 selected)	XX	<0.5
311.04 MHz	DPLL2-Normal	77.76	001	0 (DPLL2 selected)	XX	<0.5
98.304 MHz	DPLL2-12E1	24.576	010	0 (DPLL2 selected)	XX	<0.5
131.072 MHz	DPLL2-16E1	32.768	011	0 (DPLL2 selected)	XX	<0.5
148.224 MHz	DPLL2-24DS1	37.056 (2*18.528)	100	0 (DPLL2 selected)	XX	<0.5
98.816 MHz	DPLL2-16DS1	24.704	101	0 (DPLL2 selected)	XX	<0.5
274.944 MHz	DPLL2-E3	68.736 (2*34.368)	110	0 (DPLL2 selected)	XX	<0.5
178.944 MHz	DPLL2-DS3	44.736	111	0 (DPLL2 selected)	XX	<0.5
98.304 MHz	DPLL1-12E1	-	XXX	1 (DPLL1 selected)	00	<2
131.072 MHz	DPLL1-16E1	-	XXX	1 (DPLL1 selected)	01	<2
148.224 MHz	DPLL1-24DS1	-	XXX	1 (DPLL1 selected)	10	<2
98.816 MHz	DPLL1-16DS1	-	XXX	1 (DPLL1 selected)	11	<2

Note...If using Synthesis for inputs to both APLL1 and APLL2, then they must both use the same synthesis settings.

"Digital" Frequencies

Table 13, "O1 and O2 Output Frequency Selection," lists Digital1 and Digital2 as available for selection. Digital1 is a single frequency selected from the range shown in Table 14. Digital2 is another single frequency selected from the same range.

Table 13 O1 and O2 Output Frequency Selection

Value in Register	Output Frequency for given "Value in Register" for each Output Port's *Cnf_output_frequency* Register	
	Output O2 Reg. 61 Bits [3:0]	**Output O1 Reg. 62 Bits [7:4]**
0000	Off	Off
0001	2 kHz	2 kHz
0010	8 kHz	8 kHz
0011	Digital2	APLL1/2
0100	Digital1	Digital1
0101	APLL1/48	APLL1/1
0110	APLL1/16	APLL1/16
0111	APLL1/12	APLL1/12
1000	APLL1/8	APLL1/8
1001	APLL1/6	APLL1/6
1010	APLL1/4	APLL1/4
1011	APLL2/64	APLL2/64
1100	APLL2/48	APLL2/48
1101	APLL2/16	APLL2/16
1110	APLL2/8	APLL2/8
1111	APLL2/4	APLL2/4

Using Output O2 to Control Pulse Width of 2/8 kHz on FrSync, MFrSync and O1 Outputs

It can be seen from Table 13 (O1 and O2 Output Frequency Selection) that frequencies listed as 2 kHz and 8 kHz can be selected. Whilst the FrSync and MFrSync outputs are always supplied from DPLL1, the 2 kHz and 8 kHz options available from the O1 and O2 outputs are all supplied via DPLL1 or DPLL2 (Reg. 7A Bit 7).

The outputs can be either clocks (50:50 mark-space) or pulses, and can be inverted. When pulse configuration is used, the pulse width will be one cycle of the rate selected on Output O2 (Output O2 must be configured to generate at least 1,544 kHz to ensure that pulses are generated correctly). Figure 6 shows the various options with the 8 kHz controls in Reg. 7A. There is an identical arrangement with Reg. 7A Bits [1:0] for the 2 kHz O1 and MFrSync outputs. Outputs FrSync and MFrSync can be disabled via Reg. 63 Bits [7:6].

Power-On Reset

The Power-On Reset (PORB) pin resets the device if forced *Low*. The reset is asynchronous, the minimum *Low* pulse width is 5 ns. Reset is needed to initialize all of the register values to their defaults. Reset must be asserted at power on, and may be re-asserted at any time to restore defaults. This is implemented simply using an external capacitor to GND along with the internal pull-up resistor. The ACS8526 is held in a reset state for 250 ms after the PORB pin has been pulled *High*. In normal operation PORB should be held *High*.