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ACS8595 ATCA

Line Card Protection Switch for SONET/ SDH AdvancedTCA Systems

Description

The ACS8595 ATCA is a highly integrated, single-chip solution for "Hit-less" protection switching of SEC (SDH/ SONET Equipment Clock) + Sync clock "Groups", from Master and Slave SETS clock cards and a third (Stand-by) source, for line cards/ blades in a SONET or SDH ATCA (Advanced Telecommuncications Computing Architecture) Network Element. The ACS8595 has fast activity monitors on the SEC clock inputs and will implement automatic system protection switching against the Master clock failure. The selection of the Master/ Slave input can be forced by a Force Fast Switch pin. If both the Master and Slave input clocks fail, the Stand-by "Group" is selected or, if no Stand-by is available, the device enters Digital Holdover mode.

The ACS8595 can perform frequency translation, converting, for example, an 8 kHz SEC input clock from the ATCA backplane into a range of spot frequencies from 2 kHz up to 311.04 MHz (up to 77.76 MHz on the TTL/ CMOS ports). The output frequency is independently programmable on each of the six SEC output ports, so the ACS8595 ATCA has the potential to supply simultanously up to six different SEC frequencies, for example, to meet the individual requirements of several Advanced Mezzanine Cards (AMCs).

The ACS8595 has one PECL/ LVDS output port and five TTL/ CMOS ports. It also provides an 8 kHz Frame Sync and a 2 kHz Multi-Frame Sync TTL/ CMOS signal output with programmable pulse width and polarity.

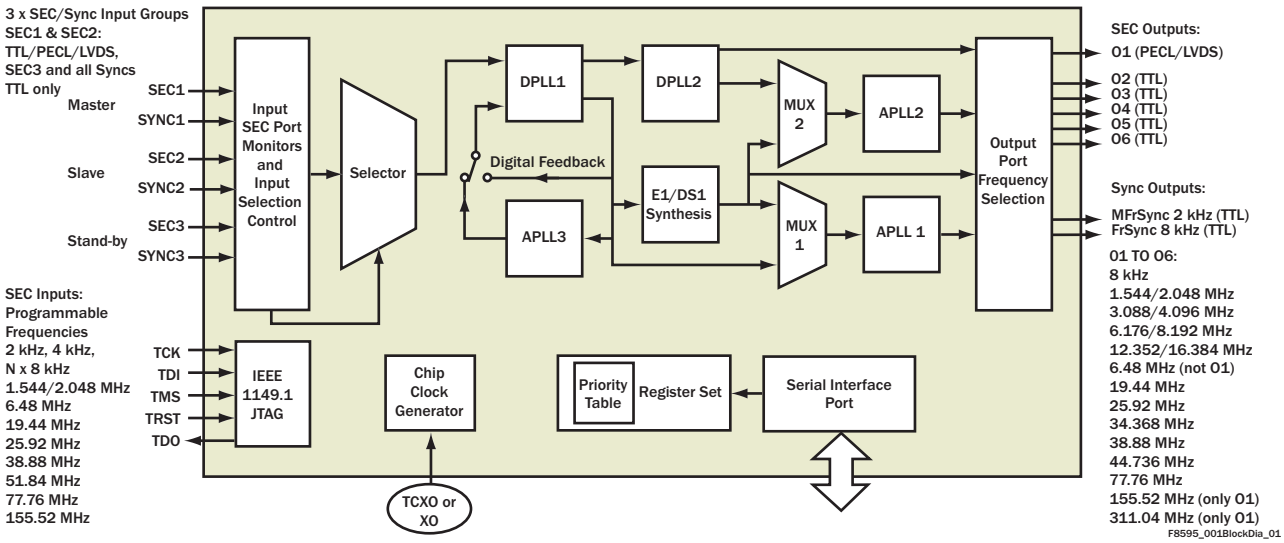
The ACS8595 includes a Serial Port, which can be SPI compatible, providing access to the configuration and status registers for device setup.

Features

- SONET/ SDH applications up to OC-3/ STM-1 bit rates
- Switches between grouped inputs (SEC/ Sync pairs)
- Inputs: three SECs at any of 2, 4, 8 kHz (and N x 8 kHz multiples up to 155.52 MHz), plus Frame Sync/ Multi-Frame Sync
- Outputs: Six SEC clocks at any of several spot frequencies from 2 kHz up to 77.76 MHz via the TTL/ CMOS port and up to 311.04 MHz via the PECL/ LVDS port
- Modes for E3/ DS3 and multiple E1/ DS1 rate output clocks
- Generates 8 kHz Frame Sync and 2 kHz Multi-Frame Sync output clocks with programmable pulse width and polarity
- Frequency translation of SEC input clock to different local line card clocks
- Robust activity monitoring on all clock inputs
- Supports Free-run, Locked and Digital Holdover modes of operation
- Automatic "Hit-less" source switchover on loss of input
- External force fast switch between SEC1/ SEC2 inputs
- Phase Build-out for output clock phase continuity during input switchover
- PLL "Locked" and "Acquisition" bandwidths individually selectable from 18, 35 or 70 Hz
- Serial interface for device set-up
- IEEE 1149.1 JTAG Boundary Scan is supported.
- Single 3.3 V operation, 5 V I/O compatible
- Operating temperature (ambient) of -40 to +85° C
- Available in 100-pin LQFP package
- Lead (Pb)-free version (ACS8595T), RoHS and WEEE compliant

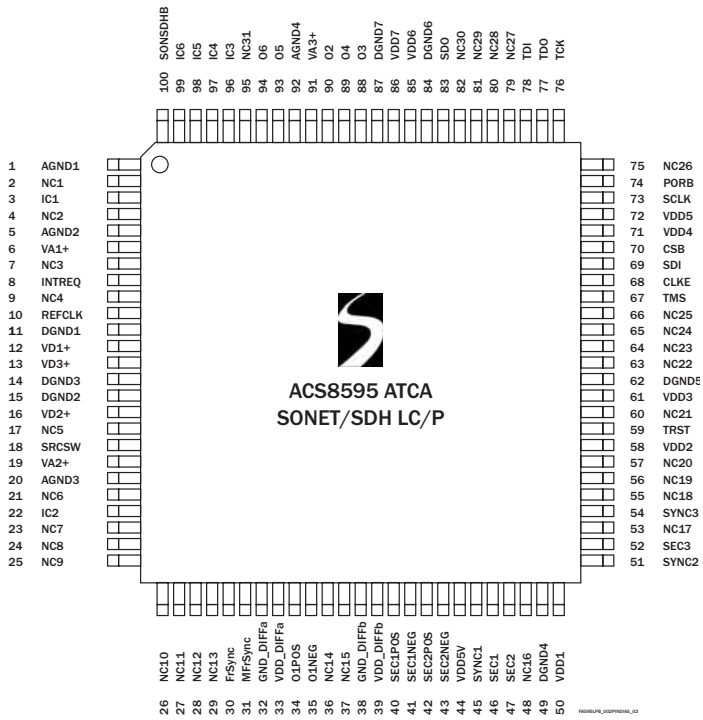
Block Diagram

Figure 1 Block Diagram of the ACS8595 ATCA



Pin Diagram

Figure 2 ACS8595 Pin Diagram



Pin Description

Table 1 Power Pins

Pin No.	Symbol	I/O	Type	Description
12,16, 13,	*VD1+, VD2+, VD3+*	*P*	-	*Supply Voltage: Digital supply to gates in analog section, +3.3 Volts ±10%.*
33, 39	*VDD_DIFFa, VDD_DIFFb*	*P*	-	*Supply Voltage: Digital supply for differential output pins 19 and 20, +3.3 Volts ±10%.*
44	*VDD5V*	*P*	-	*Digital Supply for +5 Volts Tolerance to Input Pins. Connect to +5 Volts (±10%) for clamping to +5 Volts. Connect to VDD for clamping to +3.3 Volts. Leave floating for no clamping. Input pins tolerant up to +5.5 Volts.*
50, 58, 61, 71 72, 85, 86	*VDD1, VDD2, VDD3, VDD4 VDD5, VDD6, VDD7*	*P*	-	*Supply Voltage: Digital supply to logic, +3.3 Volts ±10%.*
6	*VA1+*	*P*	-	*Supply Voltage: Analog supply to clock multiplying PLL, +3.3 Volts ±10%.*
19, 91	*VA2+, VA3+*	*P*	-	*Supply Voltage: Analog supply to output PLLs APLL2 and APPL1, +3.3 Volts ±10%.*
1, 5	*AGND1, AGND2*	*P*	-	*Supply Ground: Analog grounds.*

Table 1 Power Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
20, 92	*AGND3, AGND4*		-	*Supply Ground: Analog ground for output PLLs APLL2 and APPL1.*
11, 15, 14	*DGND1, DGND2, DGND3*	*P*	-	*Supply Ground: Digital ground for components in PLLs.*
49, 62, 84, 87	*DGND4, DGND5, DGND6, DGND7*	*P*	-	*Supply Ground: Digital ground for logic.*
32, 38	*GND_DIFFa, GND_DIFFb*	*P*	-	*Supply Ground: Digital ground for differential ports.*

Note ...I = Input, O = Output, P = Power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor.

Table 2 Internally Connected and Not Connected Pins

Pin No.	Symbol	I/O	Type	Description
3, 22, 96,97, 98, 99	*IC1, IC2, IC3, IC4, IC5, IC6,*	-	-	*Internally Connected: Leave to float.*
2,4, 7,9, 17,21, 23,24, 25,26, 27,28, 29,36, 37,48, 53,55, 56,57, 60,63, 64,65, 66,75, 79,80, 81, 82, 95	*NC1, NC2, NC3,NC4, NC5,NC6, NC7, NC8, NC9, NC10, NC11, NC12, NC13,NC14, NC15, NC16, NC17, NC18, NC19, NC20, NC21, NC22, NC23, NC24, NC25, NC26, NC27, NC28, NC29, NC30, NC31*	-	-	*Not Connected: Leave to float.*

Table 3 Other Pins

Pin No.	Symbol	I/O	Type	Description
8	*INTREQ*	*O*	*TTL/CMOS*	*Interrupt Request: Active High/Low software Interrupt output.*
10	*REFCLK*	*I*	*TTL*	*Reference Clock: 12.800 MHz.*
18	*SRCSW*	*I*	TTL_D	*Source Switching: Force Fast Source Switching on SEC1 and SEC2.*
30	*FrSync*	*O*	*TTL/CMOS*	*Output Reference: 8 kHz Frame Sync output.*
31	*MFrSync*	*O*	*TTL/CMOS*	*Output Reference: 2 kHz Multi-Frame Sync output.*
34, 35	*O1POS, O1NEG*	*O*	*LVDS/PECL*	*Output Reference: Programmable, default 38.88 MHz, LVDS.*

Table 3 Other Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
40, 41	SEC1_POS, SEC1_NEG	I	PECL/LVDS	Input Reference: Programmable, default 19.44 MHz, PECL.
42, 43	SEC2_POS, SEC2_NEG	I	PECL/LVDS	Input Reference: Programmable, default 19.44 MHz PECL.
45	SYNC1	I	TTL_D	(Master) Multi-Frame Sync 2 kHz Input: Connect to 2 or 8 kHz Multi-Frame Sync output of Master SETS.
46	SEC1	I	TTL_D	(Master) Input Reference: Programmable, default 8 kHz.
47	SEC2	I	TTL_D	(Slave) Input Reference: Programmable, default 8 kHz.
51	SYNC2	I	TTL_D	(Slave) Multi-Frame Sync 2 kHz: Connect to 2 or 8 kHz Multi-Frame Sync output of Slave SETS.
52	SEC3	I	TTL_D	(Stand-by) Input Reference: External stand-by reference clock source, programmable, default 19.44 MHz.
54	SYNC3	I	TTL_D	(Stand-by) Input Reference: External stand-by 2 or 8 kHz Multi-Frame Sync clock source.
59	TRST	I	TTL_D	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 is Boundary Scan stand-by mode, still allowing normal device operation (JTAG logic transparent). NC if not used.
67	TMS	I	TTL_D	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. NC if not used.
68	CLKE	I	TTL_D	SCLK Edge Select: SCLK active edge select, CLKE = 1, selects falling edge of SCLK to be active.
69	SDI	I	TTL_D	Serial Interface Address: Serial Data Input.
70	CSB	I	TTL^U	Chip Select (Active Low): This pin is asserted Low by the microprocessor to enable the microprocessor interface.
73	SCLK	I	TTL_D	Serial Data Clock. When this pin goes High data is latched from SDI pin.
74	PORB	I	TTL^U	Power-On Reset: Master reset. If PORB is forced Low, all internal states are reset back to default values.
76	TCK	I	TTL_D	JTAG Clock: Boundary Scan clock input.
77	TDO	O	TTL/CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK.
78	TDI	I	TTL_D	JTAG Input: Serial test data Input. Sampled on rising edge of TCK.

Table 3 Other Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
83	SDO	O	TTL_D	Interface Address: SPI compatible Serial Data Output.
88	O3	O	TTL/CMOS	Output Reference: Programmable, disabled by default.
89	O4	O	TTL/CMOS	Output Reference: Programmable, disabled by default.
90	O2	O	TTL/CMOS	Output Reference: Programmable, default 19.44 MHz.
93	O5	O	TTL/CMOS	Output Reference: Programmable, disabled by default.
94	O6	O	TTL/CMOS	Output Reference: Programmable, disabled by default.
100	SONSDHB	I	TTL_D	SONET or SDH Frequency Select: Sets the initial power-up state (or state after a PORB) of the SONET/SDH frequency selection registers, Reg. 34, Bit 2 and Reg. 38, Bit 5, Bit 6 and Reg. 64 Bit 4. When set Low, SDH rates are selected (2.048 MHz etc.) and when set High, SONET rates are selected (1.544 MHz etc.) The register states can be changed after power-up by software.

Introduction

The ACS8595 ATCA is a Line Card Protection device designed to complement the Semtech SETS devices which maintain the SETS functions in both SONET and SDH Network Elements. The ACS8595 ATCA extends this functionality on to the Line Card, for which it has been specifically designed. The ACS8595 ATCA uses “Hit-less” group switching between Master and Slave inputs or a third (Stand-by) input group, to generate and maintain accurate and stable SEC and frame synchronization pulse outputs for distribution on the Line Card, typically for Advanced Mezzaninie Cards (AMCs) on AdvancedTCA equipment.

The ACS8595 provides a simple, compact, yet flexible solution, which can be easily tailored for use with a range of transmission formats and rates, via software configuration.

The ACS8595 employs various mechanisms to maintain the integrity of its output clocks when its input clocks fail or fall below the required specification levels. By smoothing out the effects of these input anomalies, the ACS8595 improves the overall stability and reliability of

the downstream system synchronization, which translates to improved quality of service.

The key architectural advantage that the ACS8595 has over traditional solutions is in the use of Digital Phase Locked Loop (DPLL) technology for precise and repeatable performance over temperature or voltage variations and between parts.

Semtech can provide an Evaluation Board so that designers can rapidly appraise the ACS8595 ATCA device and see for themselves the benefits that a Semtech ATCA solution can bring to their designs.

General Description

Inputs

The ACS8595 SETS device has input ports for clock groups from three sources, typically Master, Slave and Stand-by, where each clock group comprises one SEC and optionally one Sync signal. This means that when any SEC input changeover is made, the corresponding Sync signal changeover is also made. Master and Slave SEC inputs to the device support TTL/ CMOS and PECL/ LVDS. The Stand-by SEC and three Sync inputs are TTL/ CMOS only.

All the TTL/ CMOS ports are 3 V and 5 V compatible (with clamping if required by connecting the VDD5V pin).

Input frequencies supported range from 2, 4, 8 kHz (and n x 8 kHz) up to 155.52 MHz. Common E1, DS1, OC-3/ STM-1 and sub-divisions are supported as spot frequencies to which the DPLLs will directly lock. Any input frequency, up to 100 MHz, that is a multiple of 8 kHz can also be locked to via a built-in programmable divider. Refer to Table 4 for details of each input port.

Input Locking Frequency Modes

Each input port has to be configured to receive the expected input frequency. To achieve this, three Input Locking Frequency Modes are provided: Direct Lock, Lock8K and DivN.

SEC Activity Monitors

A monitoring function constantly appraises the activity of each input SEC, and reports anomalous behavior. Each of the input monitors is individually configurable, allowing flags or interrupts to be raised which can influence both the operating state of the device, and which inputs are available for selection by the PLL circuitry. Any Input SEC which suffers a loss-of-activity will be declared as unavailable.

Anomalies detected by the Activity Monitor are integrated in a Leaky Bucket Accumulator. Occasional anomalies do not cause the accumulator to cross the alarm setting threshold, so the selected reference source is retained.

Table 4 Input Reference Source Selection and Priority Table

Port Name	Channel Number	Input Port Technology	Frequencies Supported	Default Priority
SEC1 TTL	0011	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 8 kHz Default (SDH): 8 kHz	2
SEC2 TTL	0100	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 8 kHz Default (SDH): 8 kHz	3
SEC1 DIFF	0101	PECL/ LVDS PECL default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	0
SEC2 DIFF	0110	PECL/ LVDS PECL default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	0
SYNC1	0111	TTL/ CMOS	2/ 4/ 8 kHz auto-sensing	n/ a
SYNC2	1000	TTL/ CMOS	2/ 4/ 8 kHz auto-sensing	n/ a
SEC3	1001	TTL/ CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	4
SYNC3	1010	TTL/ CMOS	2/ 4/ 8 kHz auto-sensing	n/ a

Notes: (i) TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies are: 2 kHz, 4 kHz, 8 kHz (and N x 8 kHz), 1.544 MHz (SONET)/ 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz. SONET or SDH input rate is selected via Reg. 34 bit 2, ip_sonsdhb).

(ii) PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz (and 311.04 MHz for Output O1 only).

(iii) SEC1 TTL and SEC2 TTL ports are on pins SEC1 and SEC2. SEC1 DIFF (Differential) port uses pins SEC1POS and SEC1NEG, similarly SEC2 DIFF uses pins SEC2POS and SEC2NEG.

Persistent anomalies cause the alarm setting threshold to be crossed and result in the selected SEC (and Sync) being rejected.

There is one Leaky Bucket Accumulator per SEC input. Each Leaky Bucket Accumulator can be programmed with a Bucket ID (0 to 3) which assigns to the Leaky Bucket the corresponding Leaky Bucket Configuration (from four available Configurations). Each Leaky Bucket Configuration comprises the following programmable parameters:

- Bucket size
- Alarm trigger (set threshold)
- Alarm clear (reset threshold)
- Leak rate (decay rate

Phase Locked Loops (PLLs)

Figure 1 shows the PLL circuitry which comprises two Digital PLLs (DPLL1 and DPLL2), two output multiplying and filtering Analog PLLs (APLL1 and APLL2), output frequency dividers in an Output Port Frequency Selection block, a Synthesis block, multiplexers MUX1 and MUX2, and a feedback Analog PLL (APLL3). These functional blocks and their interconnections are highly configurable, via register control, providing a range of output frequencies and a choice of levels of jitter performance.

The DPLLs give a stable and consistent level of performance that can be easily programmed for different dynamic behavior or operating range. They are not affected by operating conditions or silicon process variations. Digital Synthesis is used to generate all required SONET/SDH output frequencies. The digital logic operates at 204.8 MHz that is multiplied up from the external 12.800 MHz oscillator module. Hence the best resolution of the output signals from the DPLLs is one 204.8 MHz cycle or 4.9 ns.

Both of the DPLLs' outputs can be connected to multiplying and filtering APLLs. The outputs of these APLLs are divided making a number of frequencies simultaneously available for selection at the output clock ports. The various combinations of DPLL, APLL, Multiplexer and divider configurations allow for generation of a comprehensive set of frequencies, as listed in Table 5 and Table 6.

DPLLs

DPLL1 is the more feature rich of the two DPLLs. The main features of the two DPLLs are summarized here. Refer to the Register Descriptions in the datasheet for advanced features and more information.

DPLL1 Main Features

- Multiple E1 and DS1 outputs supported
- Low jitter MFrSync (2 kHz) and FrSync (8 kHz) outputs
- Multiple phase loss and multiple phase detectors
- Direct PLL locking to common SONET/SDH input frequencies or any multiple of 8 kHz
- Automatic mode switching between Free-run, Locked and Digital Holdover modes (states)
- Fast detection on input failure and entry into Digital Holdover mode (holds at the last good frequency value)
- Frequency translation between input and output rates via direct digital synthesis
- High accuracy digital architecture for stable PLL dynamics combined with an APLL for low jitter final output clocks
- Non-revertive mode
- Frame Sync pulse alignment
- Selectable automatic DPLL bandwidth control (auto selects either Locked bandwidth, or Acquisition bandwidth), or Locked DPLL bandwidth
- Two programmable bandwidth controls:
  - Locked bandwidth: 18, 35 or 70 Hz
  - Acquisition bandwidth: 18, 35 or 70 Hz
- Programmable damping factor, (For optional faster locking and peaking control) Factors = 1.2, 2.5, 5, 10 or 20
- Programmable DPLL pull-in frequency range
- Phase Build-out on source switching (hit-less source switching), on/off
- Freeze Phase Build-out, on/off

DPLL2 Main Features

The main features of DPLL2 are:

- Always locked to DPLL1
- Single programmable bandwidth control: 18, 35 or 70 Hz
- Programmable damping factor, (For optional faster locking and peaking control) Factors = 1.2, 2.5, 5, 10 or 20.
- Digital feedback, on/off
- Output frequency selection

- DS3/E3 support (44.736 MHz / 34.368 MHz) independent of rates from DPLL1
  - Low jitter E1/DS1 options independent of rates from DPLL1
  - Frequencies of n x E1/DS1 including 16 and 12 x E1, and 16 and 24 x DS1 supported
  - Squelched (clock off)
- Can provide the source for the 2 kHz and 8 kHz outputs available at Outputs 01 to 06
- Can use its phase detector to measure the input phase difference between two inputs
- Selectable digital feedback, on/off

Either the software or an internal state machine controls the operation of DPLL1. The state machine for DPLL2 is very simple and cannot be manually/externally controlled. One additional feature of DPLL2 is the ability to measure a phase difference between two inputs.

DPLL1 always produces an output at 77.76 MHz to feed the APLL, regardless of the frequency selected at the output pins or the locking frequency (frequency at the input of the Phase and Frequency Detector — PFD).

DPLL2 can be operated at a number of frequencies. This is to enable the generation of extra output frequencies, which cannot be easily related to 77.76 MHz. If DPLL2 is enabled, it locks to the 8 kHz from DPLL1. This is because all of the frequencies of operation of DPLL2 can be divided to 8 kHz and this will ensure synchronization of frequencies, from 8 kHz upwards, within the two DPLLs.

APLLs

There are three APLLs. APLL1 and APLL2 provide a lower final output jitter reducing the 4.9 ns p-p jitter from the digital down to 500 ps p-p and 60 ps rms as typical final outputs measured broadband (from 10 Hz to 1 GHz). The feedback APLL (APLL3) is selected by default; it provides improved performance over the digital feedback.

Each APLL has its own divider. Each divider simultaneously outputs a series of fixed ratios of its APLL input. These divided outputs are available on Output Ports O1 to O6.

Outputs

The ACS8595 delivers eight output signals on the following ports: Six clocks, one each on ports O1 to O6; and two Sync signals, on ports FrSync and MFrSync. Outputs O1 to O6 are independent of each other and are individually selectable. Output 01 is a differential port (pins O1POS and O1NEG), and can be selected PECL or LVDS. All other outputs are TTL/CMOS.

Table 5 Output Port Frequencies and Technologies

Port Name	Output Port Technology	Frequencies Supported
O1	LVDS/PECL (LVDS default)	Frequencies as per Table 6
O2, O3, O4, O5 and O6	TTL/CMOS	
FrSync	TTL/CMOS	FrSync, 8 kHz programmable pulse width and polarity, see Reg. 7C.
MFrSync	TTL/CMOS	MFrSync, 2 kHz programmable pulse width and polarity, see Reg. 7C.

Table 6 Output Frequencies/Lowest Jitter Configuration (Typical Conditions)

Frequency (MHz)		Jitter Level (typ)	
		rms (ps)	p-p (ns)
2 kHz		60	0.6
8 kHz		60	0.6
1.536	(not O5/O6)	250	1.5
1.544	(not O5/O6)	150	1.0
2.048		220	1.2
2.0586667		150	1.0
2.316	(not O5/O6)	110	0.75
2.7306667		220	1.2
2.796	(not O5/O6)	110	1.0
3.088		110	0.75
3.728		110	1.0
4.096	via Digital1 or Digital2 (not O1)	3800	13
4.296	(not O5/O6)	120	1.0
4.86	(not O5/O6)	60	0.6
5.728		120	1.0
6.144		250	1.5
6.176		150	1.0
6.48		60	0.6
8.192		220	1.2
8.2346667		760	2.6
9.264		110	0.75
10.922667		250	1.6
11.184		110	1.0
12.288		250	1.5
12.352		110	0.75
16.384		220	1.2
16.46933		760	2.6
17.184		120	1.0
18.528		110	0.75
19.44		60	0.6
21.84533		250	1.6
22.368		110	1.0
24.576		250	1.5
24.704		110	0.75
25.92		60	0.6
32.768		220	1.2
34.368		120	1.0
37.056		110	0.75

Table 6 Output Frequencies/Lowest Jitter Configuration (Typical Conditions) (cont...)

Frequency (MHz)		Jitter Level (typ)	
		rms (ps)	p-p (ns)
38.88		60	0.6
44.736		110	1.0
49.152	(O5/O6 only)	250	1.5
49.152	(O1 only)	900	4.5
49.408	(O5/O6 only)	150	1.0
49.408	(O1 only)	760	2.6
51.84		60	0.6
65.536	(O5/O6 only)	220	1.2
65.536	(O1 only)	120	1.0
68.736		120	1.0
74.112	(O5/O6 only)	110	0.75
74.112	(O1 only)	110	0.75
77.76		60	0.6
89.472	(O5/O6 only)	110	1.0
98.304	(O1 only)	900	4.5
98.304	(O1 only)	900	4.5
98.816	(O1 only)	760	2.6
131.072	(O1 only)	250	1.6
137.472	(O5/O6 only)	120	1.0
148.224	(O1 only)	110	0.75
155.52		60	0.6
311.04	(O1 only)	60	0.6

Modes of Operation

The device has three principle modes of operation:

- Free-run
- Locked
- Digital Holdover

The Free-run mode is typically used following a power-on-reset or a device reset before network synchronization has been achieved. In the Free-run mode, the timing and synchronization signals generated from the ACS8595 are based on the 12.800 MHz clock frequency provided from the external oscillator and are not synchronized to an input SEC. The accuracy can be enhanced via software calibration to within ±0.0196229 ppm.

The Locked mode is used when an input SEC has been selected and the PLL has had time to lock. When the Locked mode is achieved, the output signal is in phase and is locked to the selected input SEC. The priority table determines which input SEC is selected. When the ACS8595 is in Locked mode, the output frequency and phase follows that of the selected input SEC.

In Digital Holdover mode, the ACS8595 provides the timing signals to maintain the Line Card when its currently selected input source becomes invalid, and no other valid replacement source is available. Digital Holdover operates instantaneously, which means the DPLL freezes at the frequency it was operating at the time of entering Digital Holdover mode.

Input Selection Priorities

Each input SEC can be programmed with a priority number (see Table 4) allowing references to be chosen according to the highest priority valid input. Under normal operation, the input SECs are selected automatically, according to availability and in order of priority. For special circumstances, such as chip or board testing, the selection may be forced by configuration.

The priority table is initially defined by the default configuration and can be changed via the Serial interface by the Network Manager. In this way, when all the defined sources are active and valid, the source with the highest programmed priority is selected but, if this source fails, the next-highest source is selected, and so on.

Table 4 gives details of the input reference ports. Specific frequencies and priorities are set by configuration.

Ultra Fast Switching

SEC inputs are monitored using a leaky bucket approach to allow source qualification criterion to be monitored. A reference source is normally disqualified after the leaky bucket monitor thresholds have been crossed. An option for a faster disqualification has been implemented so that a loss of activity of just a few reference clock cycles will raise an alarm and cause a reference switch.

External Forced Fast Protection Switching

External Forced Fast Protection Switching mode, for fast switching between inputs SEC1 or SEC2, can be triggered directly from the dedicated pin SRCSW.

Restoration

Restoration of repaired reference sources is handled carefully to avoid inadvertent disturbance of the output clock. For this, the ACS8595 has two modes of operation; Revertive and Non-revertive.

Sync Reference Sources

The ACS8595 provides the facility to have a Sync reference source associated with each SEC.

The Sync inputs (SYNC1, SYNC2 and SYNC3) are used for Frame Sync output alignment and can be 2, 4 or 8 kHz (automatically detected frequency).

As in all the Semtech ACS85xx series of parts supporting such a mechanism, the Sync is treated as an additional part of the SEC clock. The failure of a Sync input will never cause a source disqualification. The Sync input is used to internally align the generation of the output 2 kHz and 8 kHz Sync pulses.

Serial Interface

The ACS8595 device has an SPI compatible serial interface, providing access to the configuration and status registers for device set-up and monitoring.

Performance

Conformance

The ACS8595 is designed for use in Line Cards in Network Elements which must meet the requirements of the following specifications:

ITU: G. 736, G.742, G.812, G.813, G.824, K.41.
Telcordia: GR-253-CORE, GR-499-CORE, GR-1244-CORE.
ANSI: T1.101-1999.
ETSI: ETSI 300 462-3, ETSI 300 462-5.

Performance Benefits from DPLL/APLL Technology

The use of Digital Phase Locked Loop technology ensures precise and repeatable performance over temperature or voltage variations, and between parts. The overall PLL bandwidth, loop damping, pull-in range and frequency accuracy are all determined by digital parameters that provide a consistent level of performance. An Analog PLL takes the signal from the DPLL output and provides a lower jitter output. The APLL bandwidth is set four orders of magnitude higher than the DPLL bandwidth. This ensures that the overall system performance still maintains the advantage of consistent behavior provided by the digital approach.

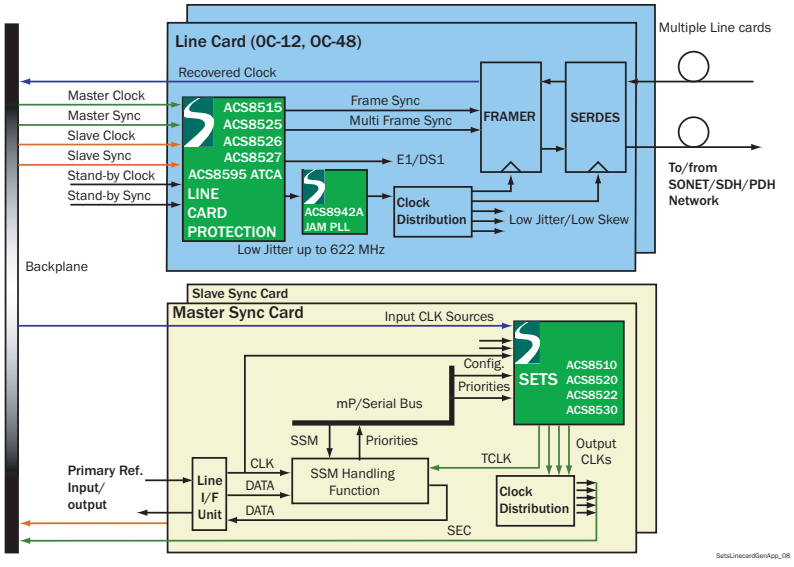
The DPLLs are clocked by the external oscillator module therefore the Free-run or Digital Holdover frequency stability is only determined by the stability of the external oscillator module. This key advantage confines all temperature critical components to one well defined and pre-calibrated module, whose performance can be chosen to match the application.

All performance parameters of the DPLLs are programmable without the need to understand detailed PLL equations. Bandwidth, damping factor and lock range, for example, can all be set directly.

A high level of phase and frequency accuracy is made possible in the ACS8595 by an internal resolution of up to 54 bits and internal Holdover accuracy of up to 7.5×10^{-14} ppb (instantaneous).

Typical Application

Figure 3 Semtech's Product Family Solution for a Typical SONET/SDH Architecture



Register Map

Table 7 Register Map

Register Name RO = Read Only R/W = Read/Write	Address (hex)	Default (hex)	Data Bit 7 (MSB)	6	5	4	3	2	1	0 (LSB)
chip_id (RO)	00	4D	chip_id[7:0], 8 LSBs of Chip ID							
	01	21	chip_id[15:8], 8 MSBs of Chip ID							
chip_revision (RO)	02	00	chip_revision[7:0]							
test_register1 (R/W)	03	14	Phase_alarm	Disable_180		Resync_ analog	Set to 0	8K Edge Polarity	Set to 0	Set to 0
test_register2 (R/W)	04	12	Do not use							
sts_interrupts (R/W)	05	FF			status_SEC2_ DIFF	status_SEC1_ DIFF	status_SEC2_ TTL	status_SEC1_ TTL		
	06	3F	operating_ mode	DPLL1_main_ ref_failed						status_SEC3
sts_current_DPLL_frequency, see OC/OD	07	00						Bits [18:16] of sts_current_DPLL_frequency		
sts_interrupts (R/W)	08	10	Sync_alarm_ int							
sts_operating_mode (RO)	09	01	Sync_alarm	DPLL2_Lock	DPLL1_freq_ soft_alarm	DPLL2_freq_ soft_alarm		DPLL1_operating_mode		
sts_priority_table (RO)	0A	00	Highest priority validated source				Currently selected source			
	0B	00	3rd highest priority validated source				2nd highest priority validated source			
sts_current_DPLL_frequency[7:0]	0C	00	Bits [7:0] of sts_current_DPLL_frequency							
(RO) [15:8]	0D	00	Bits [15:8] of sts_current_DPLL_frequencyy							
[18:16]	07	00						Bits [18:16] of sts_current_DPLL_frequency		
sts_sources_valid (RO)	0E	00			SEC2 DIFF	SEC1 DIFF	SEC2 TTL	SEC1 TTL		
	0F	00								SEC3
sts_reference_sources (RO) Alarm Status on inputs: SEC1 & SEC2 TTL	11	22			No Activity SEC2 TTL	Phase Lock SEC2 TTL			No Activity SEC1 TTL	Phase Lock SEC1 TTL
SEC1 & SEC2 DIFF	12	22			No Activity SEC2 DIFF	Phase Lock SEC2 DIFF			No Activity SEC1 DIFF	Phase Lock SEC1 DIFF
SEC3	14	22							No Activity SEC3	Phase Lock SEC3
cnfg_ref_selection_priority (R/W) SEC1 & SEC2 TTL	19	32	programmed_priority_SEC2_TTL				programmed_priority_SEC1_TTL			
SEC1 & SEC2 DIFF	1A	00	programmed_priority_SEC2_DIFF				programmed_priority_SEC1_DIFF			
SEC3	1C	04					programmed_priority_SEC3			
cnfg_ref_source_frequency_ <input> (R/W), where <input> = SEC1 TTL	22	00	divn_SEC1 TTL	lock8k_SEC1 TTL	Bucket_id_SEC1 TTL		reference_source_frequency_SEC1 TTL			
SEC2 TTL	23	00	divn_SEC2 TTL	lock8k_SEC2 TTL	Bucket_id_SEC2 TTL		reference_source_frequency_SEC2 TTL			
SEC1 DIFF	24	03	divn_SEC1 DIFF	lock8k_SEC1 DIFF	Bucket_id_SEC1 DIFF		reference_source_frequency_SEC1 DIFF			
SEC2 DIFF	25	03	divn_SEC2 DIFF	lock8k_SEC2 DIFF	Bucket_id_SEC2 DIFF		reference_source_frequency_SEC2 DIFF			
SEC3	28	03	divn_SEC3	lock8k_SEC3	Bucket_id_SEC3		reference_source_frequency_SEC3			
cnfg_operating_mode (R/W)	32	00						DPLL1_operating_mode		
force_select_reference_source (R/W)	33	0F					forced_select_SEC_input			
cnfg_input_mode (R/W)	34	CA	auto_extsync_ en	phalarm_ timeout	XO_ edge		extsync_en	ip_sonsdhb		reversion_ mode
cnfg_DPLL2_path (R/W)	35	A0		DPLL2_dig_ feedback						
cnfg_differential_inputs (R/W)	36	03							SEC2_DIFF_ PECL	SEC1_DIFF_ PECL
cnfg_dig_outputs_sonsdh (R/W)	38	04		dig2_sonsdh	dig1_sonsdh					
cnfg_digtial_frequencies (R/W)	39	08	digital2_frequency		digital1_frequency					
cnfg_differential_output (R/W)	3A	C2							Output O1 _LVDS_PECL	
cnfg_auto_bw_sel	3B	98	auto_BW_sel				DPLL1_lim_int			

Table 7 Register Map (cont...)

Register Name *RO = Read Only* *R/W = Read/Write*	Address (hex)	Default (hex)	Data Bit 7 (MSB)	6	5	4	3	2	1	0 (LSB)
cnfg_nominal_frequency [7:0]	3C	99	*Bits[7:0] of cnfg_nominal_frequency*							
(R/W) [15:8]	3D	99	*Bits[15:8] of cnfg_nominal_frequency*							
cnfg_DPLL_freq_limit (R/W) [7:0]	41	76	*Bits[7:0] of cnfg_DPLL_freq_limit*							
cnfg_DPLL_freq_limit (R/W) [9:8]	42	00							*Bits[9:8] of cnfg_DPLL_freq_limit*	
cnfg_interrupt_mask (R/W) [7:0]	43	00	*Set to 0*	*Set to 0*	*SEC2 DIFF*	*SEC1 DIFF*	*SEC2 TTL*	*SEC1 TTL*		
[15:8]	44	00	*operating_mode*	*main_ref_failed*				*Set to 0*		*SEC3*
[23:16]	45	00	*Sync_ip_alarm*							
cnfg_freq_divn (R/W) [7:0].	46	FF	*divn_value [7:0] (divide Input frequency by n)*							
[13:8]	47	3F			*divn_value [13:8] (divide Input frequency by n)*					
cnfg_monitors (R/W)	48	04		*los_flag_on_TDO*	*ultra_fast_switch*	*ext_switch*	*PBO_freeze*	*PBO_en*		
cnfg_registers_source_select (R/W)	4B	00				*DPLL1_DPLL2_select*				
cnfg_freq_lim_ph_loss	4D		*freq_lim_ph_loss*							
cnfg_upper_threshold_0 (R/W)	50	06	*upper_threshold_0_value (Activity alarm, Config. 0, Leaky Bucket - set threshold)*							
cnfg_lower_threshold_0 (R/W)	51	04	*lower_threshold_0_value (Activity alarm, Config. 0, Leaky Bucket - reset threshold)*							
cnfg_bucket_size_0 (R/W)	52	08	*Bucket_size_0_value (Activity alarm, Config. 0, Leaky Bucket - size)*							
cnfg_decay_rate_0 (R/W)	53	01							*decay_rate_0_value (Activity alarm, Config. 0, Leaky Bucket - leak rate)*	
cnfg_upper_threshold_1 (R/W)	54	06	*upper_threshold_1_value (Activity alarm, Config. 1, Leaky Bucket - set threshold)*							
cnfg_lower_threshold_1 (R/W)	55	04	*lower_threshold_1_value (Activity alarm, Config. 1, Leaky Bucket - reset threshold)*							
cnfg_bucket_size_1 (R/W)	56	08	*Bucket_size_1_value (Activity alarm, Config. 1, Leaky Bucket - size)*							
cnfg_decay_rate_1 (R/W)	57	01							*decay_rate_1_value (Activity alarm, Config. 1, Leaky Bucket - leak rate)*	
cnfg_upper_threshold_2 (R/W)	58	06	*upper_threshold_2_value (Activity alarm, Config. 2, Leaky Bucket - set threshold)*							
cnfg_lower_threshold_2 (R/W)	59	04	*lower_threshold_2_value (Activity alarm, Config. 2, Leaky Bucket - reset threshold)*							
cnfg_bucket_size_2 (R/W)	5A	08	*Bucket_size_2_value (Activity alarm, Config. 2, Leaky Bucket - size)*							
cnfg_decay_rate_2 (R/W)	5B	01							*decay_rate_2_value (Activity alarm, Config. 2, Leaky Bucket - leak rate)*	
cnfg_upper_threshold_3 (R/W)	5C	06	*upper_threshold_3_value (Activity alarm, Config. 3, Leaky Bucket - set threshold)*							
cnfg_lower_threshold_3 (R/W)	5D	04	*lower_threshold_3_value (Activity alarm, Config. 3, Leaky Bucket - reset threshold)*							
cnfg_bucket_size_3 (R/W)	5E	08	*Bucket_size_3_value (Activity alarm, Config. 3, Leaky Bucket - size)*							
cnfg_decay_rate_3 (R/W)	5F	01							*decay_rate_3_value (Activity alarm, Config. 3, Leaky Bucket - leak rate)*	
cnfg_output_frequency (R/W) Outputs O4 & 03	60	00	*output_freq_O4*				*output_freq_O3*			
Outputs O5 & O2	61	06	*output_freq_O5*				*output_freq_O2*			
Outputs O1 & 06	62	80	*output_freq_O1*				*output_freq_O6*			
(MFrSync/FrSync)	63	C0	*MFrSync_en*	*FrSync_en*						
cnfg_DPLL2_frequency (R/W)	64	00						*DPLL2_frequency*		
cnfg_DPLL1_frequency (R/W)	65	01	*DPLL2_meas_DPLL1_ph*	*APLL2_for_DPLL1_E1/DS1*	*DPLL1_freq_to_APLL2*			*DPLL1_frequency*		
cnfg_DPLL2_bw (R/W)	66	00							*DPLL2_bandwidth*	
cnfg_DPLL1_locked_bw (R/W)	67	10							*DPLL1_locked_bandwidth*	
cnfg_DPLL1_acq_bw (R/W)	69	11							*DPLL1_acquisition_bandwidth*	
cnfg_DPLL2_damping (R/W)	6A	13		*DPLL2_PD2_gain_alog_8k*				*DPLL2_damping*		
cnfg_DPLL1_damping (R/W)	6B	13		*DPLL1_PD2_gain_alog_8k*				*DPLL1_damping*		
cnfg_DPLL2_PD2_gain (R/W)	6C	C2	*DPLL2_PD2_gain_enable*	*DPLL2_PD2_gain_alog*				*DPLL2_PD2_gain_digital*		
cnfg_DPLL1_PD2_gain (R/W)	6D	C2	*DPLL1_PD2_gain_enable*	*DPLL1_PD2_gain_alog*				*DPLL1_PD2_gain_digital*		

Table 7 Register Map (cont...)

Register Name RO = Read Only R/W = Read/Write	Address (hex)	Default (hex)	Data Bit 7 (MSB)	6	5	4	3	2	1	0 (LSB)
cnfg_phase_offset (R/W) [7:0]	70	00	phase_offset_value [7:0]							
[15:8]	71	00	phase_offset_value[15:8]							
cnfg_PBO_phase_offset (R/W)	72	00			PBO_phase_offset					
cnfg_phase_loss_fine_limit (R/W)	73	A2	fine_limit_en	noact_ph_loss	narrow_en			phase_loss_fine_limit		
cnfg_phase_loss_coarse_limit (R/W)	74	85	coarse_lim_ phaseloss_en	wide_range_ en	multi_ph_resp		phase_loss_coarse_limit			
cnfg_ip_noise_window (R/W)	76	06	ip_noise_ window_en							
sts_current_phase (RO) [7:0]	77	00	current_phase[7:0]							
[15:8]	78	00	current_phase[15:8]							
cnfg_phase_alarm_timeout (R/W)	79	32			timeout_value (in two-second intervals)					
cnfg_sync_pulses (R/W)	7A	00	2k_8k_from_ DPLL2				8k_invert	8k_pulse	2k_invert	2k_pulse
cnfg_sync_phase (R/W)	7B	00	Indep_FrSync/ MFrSync	Sync_OC-N_ rates	Sync_phase_SYNC3		Sync_phase_SYNC2		Sync_phase_SYNC1	
cnfg_sync_monitor (R/W)	7C	2B	ph_offset_ ramp	Sync_monitor_limit						
cnfg_interrupt (R/W)	7D	02						Interrupt GPO_en	Interrupt tristate_en	Interrupt int_polarity
cnfg_protection(R/W)	7E	85	protection_value							

Ordering Information

Table 8 Parts List

Part Number	Description
ACS8595	ATCA Line Card Protection Switch for SONET/ SDH AdvancedTCA Systems
ACS8595T	Lead (Pb)-free package version of ACS8595; RoHs and WEEE compliant
ACS8595 EVB	Evaluation Board and Software

Disclaimers

Life support- This product is not designed or intended for use in life support equipment, devices or systems, or other critical applications. This product is not authorized or warranted by Semtech for such use.

Right to change- Semtech Corporation reserves the right to make changes, without notice, to this product. Customers are advised to obtain the latest version of the relevant information before placing orders.

Compliance to relevant standards- Operation of this device is subject to the User's implementation and design practices. It is the responsibility of the User to ensure equipment using this device is compliant to any relevant standards.

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