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30V Buck-Boost Charger with Integrated MOSFETs and OTG

BENEFITS and FEATURES

- **Wide VIN Range: 3.9V to 29V (No Dead Zone)**
- **Supports 2 to 5 Cell Lithium-ion Batteries**
- **Supports OTG Function (5V ~ 22.5V Input) with wide range of output voltages**
- **OTG output supports QC3.0 / USB PD + PPS output levels and transition times**
- **Programmable Frequency: 125KHz, 250KHz, 500kHz, and 1MHz**
- **2V ~ 5V/100mA Programmable Output LDO**
- **Precision 0.5% Voltage Reference**
- **+/-4% Output Constant Current Regulation**
- **< 5 µA Leakage Current from Battery in Shipping Mode**
- **Programmable Charge Voltage via I2C**
- **Programmable Charge Current via Pin and I2C**
- **Programmable Soft-Start**
- **Programmable Safety Timer**
- **Battery Path Impedance Compensation**
- **JEITA Compliant**
- **Cycle-by-Cycle Current Limit**
- **Built in ADC for Temperature, Input and Output Voltage and Current monitoring**
- **Thermal Regulation and Protection**
- **25mΩ FET from VIN to SW1**
- **25mΩ FET from SW2 to VOUT**
- **35mΩ FET from SW1 to PGND**
- **35mΩ FET from SW2 to PGND**
- **Low Output Ripple**
- **Thermally Enhanced 32-Lead 4mx4mm QFN**

APPLICATIONS

- Multi Cell Battery Charger
- Portable Battery-Powered Devices
- Car Charger
- Power Bank
- 24V Industrial Applications
- Automotive Power Systems
- Multiple Power Source Supplies
- DC UPS
- Solar Powered Devices
- Solid-State Lighting

GENERAL DESCRIPTION

The ACT286x is a buck-boost charger with 4 integrated MOSFETs. It offers a high efficiency, low component counts, compact solution for 2 to 5 cell battery charging application. It can operate from an input voltage range from 3.9V to 29V.

The 4 internal low resistance NMOS switches minimize the size of the application circuit and reduce power losses to maximize efficiency. Internal high side gate drivers, which require only the addition of two small external capacitors, further simplify the design process. An advanced switch control algorithm allows the buck-boost converter to maintain output voltage regulation with input voltages that are above, below or equal to the output voltage. Transitions between these operating modes are seamless and free of transients and subharmonic switching.

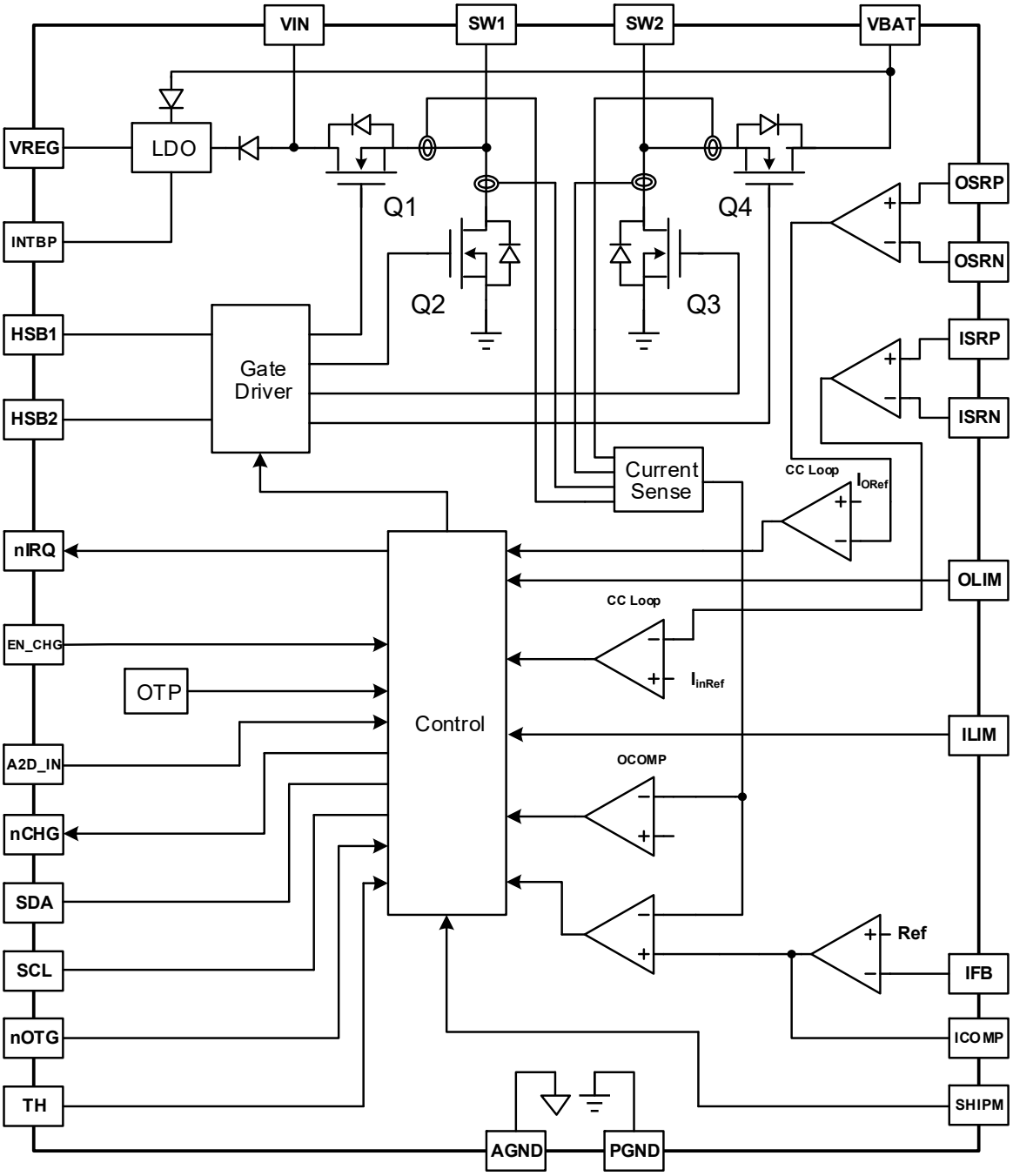
The ACT286x has been optimized to reduce input current in shipping, shutdown, and standby for applications which are sensitive to quiescent current draw, such as battery-powered devices.

Both the input side and output side voltages and currents can be configured by resistors or the I^2C serial interface. The system can be monitored and configured by I^2C as well. The build-in ADC can be read for the information of input/output voltages and currents, and the die temperature. With a MCU, it can easy to charge a multi cell battery pack from a variety of input power sources.

The IC provides various safety features for system operation. The thermal regulation reduces output current when the junction temperature exceeds 120°C (programmable).

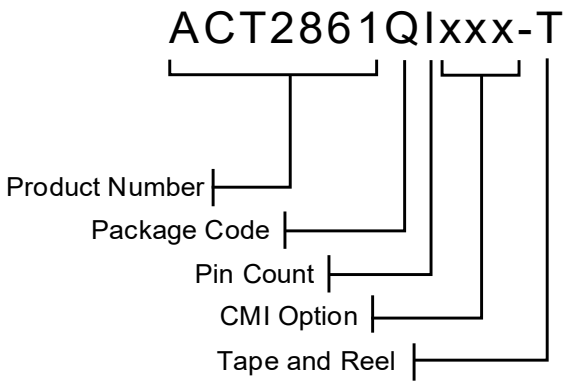
The ACT286x is available in 32-pin, 4x4 mm QFN package.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	Cell Count	Termination Voltage	OTG Voltage	LDO	Fsw	JEITA	PACKAGE
ACT2861QI201-T	2	8.40V	5.1V	5.0V	500kHz	Enabled	FCQFN4x4-32
ACT2861QI301-T	3	12.6V	5.1V	5.0V	500kHz	Enabled	FCQFN4x4-32
ACT2861QI401-T	4	16.8V	5.1V	5.0V	500kHz	Enabled	FCQFN4x4-32



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

Note 3: Package Code designator “Q” represents QFN

Note 4: Pin Count designator “I” represents 32 pins

PIN CONFIGURATION

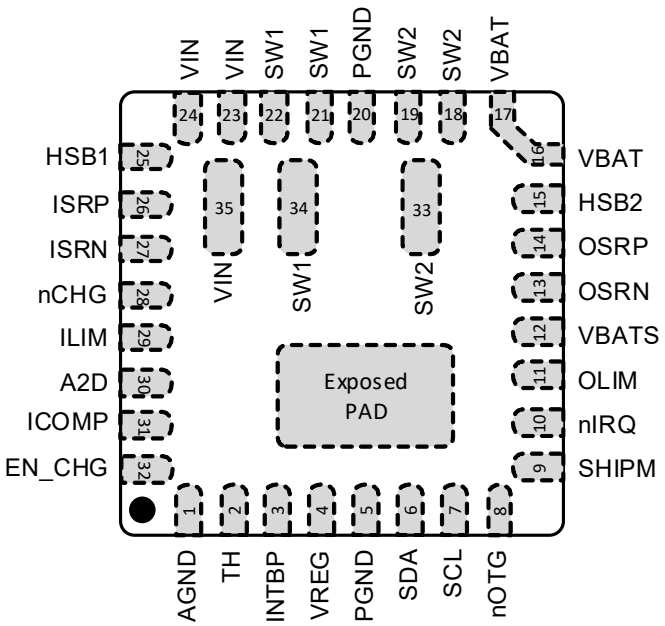


Figure 1: Pin Configuration – Top View – QFN4x4-32

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	AGND	Analog Ground. Kelvin connect AGND to the PGND plane.
2	TH	Battery temperature sensing input. Connect a negative temperature coefficient thermistor from TH to AGND. This pin provides a constant current output and the voltage at this pin is used for temperature calculation. If temperature sensing is not used, leave TH open and set register bit “DIS_TH” to a 1
3	INTBP	Internal Voltage Bypass - Connect a 100nF ceramic capacitor between INTBP and AGND
4	VREG	Internal VREG LDO output. The output voltage is programmable from 2V to 5V. Connect a 1.0uF between VREG and AGND. The maximum current capability for this pin is 100mA.
5, 20	PGND	Power Ground. Connect to large ground plane on PCB with thermal vias.
6	SDA	I^2C Data Input and Output. Needs an external pull up resistor.
7	SCL	I^2C Clock Input. Needs an external pull up resistor.
8	nOTG	OTG Enable Input. The OTG mode is active when this pin is pulled low and the EN_OTG bit = 1. In OTG mode, the converter works in reverse operation mode, and power is transferred from battery to VIN.
9	SHIPM	Shipping Mode input. Shorting this pin to GND for 32ms enables the IC. If not used, connect SHIPM to AGND.
10	nIRQ	Interrupt Open-Drain Output. nIRQ goes low to indicate a fault condition. nIRQ is referenced to AGND.
11	OLIM	Output Fast charge current setting pin. Connect a resistor from OLIM to AGND to program the output current in normal charge mode.
12	VBATS	VBAT Sense Input – Kelvin connect close the battery to sense the battery voltage.
13	OSRN	Output current sense resistor negative input.
14	OSRP	Output current sense resistor positive input.
15	HSB2	High Side Bias Boot-strap pin. This provides power to the internal high-side MOSFET gate driver circuitry. Connect a 47nF capacitor from HSB2 to SW2 pin
16, 17	VBAT	Charging Power Output pin. Connect this pin to 22uF-100uF ceramic capacitors placed as close to the IC as possible.
18, 19, 33	SW2	Power switching output to external inductor.
21, 22, 34	SW1	Power switching output to external inductor.
23, 24, 35	VIN	Input voltage pin. Place a 22uF to 44uF decoupling capacitor between VIN and PGND.
25	HSB1	High Side Bias Boot-strap pin. This provides power to the internal high-side MOSFET gate driver circuitry. Connect a 47nF capacitor from HSB1 to SW1 pin
26	ISRP	Input current sense resistor positive input.
27	ISRN	Input current sense resistor negative input
28	nCHG	Open drain charge status indicator. nCHG = L indicates charging is in progress. nCHG = HIZ indicates charge complete or charger disabled. nCHG = H to L at 1Hz indicates a fault condition.
29	ILIM	Input current limit and OTG output current setting pin. Connect a resistor from ILIM to AGND to program the input current when operating in normal mode and to program the output current when operating in OTG Mode.

30	A2D	A2D input pin
31	ICOMP/GPIO	OTG mode Error Amplifier Output. This pin is used to compensate the converter when operating in OTG mode.
32	EN_CHG	Charge Enable pin. Charging is enabled when EN_CHG is above 0.8V. Connect a resistor divider to EN_CHG to program charging input UVLO.
Exposed Pad	PGND	Power Ground. Connect to large ground plane on PCB with thermal vias.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE	UNIT
VIN	-0.3 to +31	V
ISRP, ISRN	-0.3 to VIN + 0.3	V
VBAT	-0.3 to +23	V
OSRP, OSRN	-0.3 to VBAT + 0.3	V
VBATS	-0.3 to OSRN + 0.3	V
SW1	-0.3 to VIN + 0.3	V
SW2	-0.3 to VBAT + 0.3	V
HSB1	V_{SW1} - 0.3 to V_{SW1} + 5.5	V
HSB2	V_{SW2} - 0.3 to V_{SW2} + 5.5	V
SCL, SDA, VREG, nCHG, EN_CHG, nOTG, TH, nIRQ, ICOMP, ILIM, OLIM, SHIPM, A2D	-0.3 to +6	V
AGND to PGND	-0.3 to +0.3	V
Junction to Ambient Thermal Resistance (θ_{JA})	35	°C/W
Operating Junction Temperature (T_J)	-40 to 150	°C
Operating Ambient Temperature Range (T_A)	-40 to 85	°C
Store Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

Note1: Measured on Active-Semi Evaluation Kit

Note2: Do not exceed these limits to prevent damage to the IC. Exposure to absolute maximum rating conditions for long periods may affect IC reliability.

SYSTEM CHARACTERISTICS

(VIN = 12V, VBAT = 7.6V, T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage						
Input voltage Range	V_{IN}		4		29	V
Input Over Voltage Protection	V_{IN_OVP}	Rising Measured at VIN Pin	29	30	31	V
Input Over Voltage Hysteresis				2		V
Input Over Voltage Response Time	T_{VIN_OVP}	VIN step from 20V to 31V		250		ns
VIN UVLO Threshold	V_{IN_UVLO}	VIN Rising Measured at VIN Pin	3.725	3.9	4.075	V
VIN UVLO Hysteresis	$V_{IN\_UVLO\_HYST}$	VIN Falling Measured at VIN Pin		200		mV
EN_CHG INPUT Threshold	V_{EN_IN}	EN_CHG Rising	0.7	0.8	0.9	V
EN_CHG INPUT Hysteresis	$V_{EN\_IN\_HYST}$	EN_CHG Falling		160		mV
CURRENT REGULATION - VIN INPUT AND CURRENT REGULATION IN CHARGE MODE						
Input Voltage Regulation Accuracy	$V_{INLIM\_REG\_ACC}$	Measured from VIN Pin to AGND Pin Relative to the factory default Register Setting	-2	V_{INLIM}	+2	%
Input Current Regulation Range	I_{INLIM_RANGE}	With I_{IN_LIM}=100% register setting	0.5		5	A
Input Current Regulation Accuracy	I_{IN_ILIM}	I_{IN_LIM} = 0.5A to 1A Rsense = 0.01Ohms	-20	I_{IN_ILIM}	+20	%
	I_{IN_ILIM}	I_{IN_LIM} = 1A to 2A Rsense = 0.01Ohms	-15	I_{IN_ILIM}	+15	%
	I_{IN_ILIM}	I_{IN_LIM} > 2A Rsense = 0.01Ohms	-10	I_{IN_ILIM}	+10	%
VIN INPUT QUIESCENT CURRENTS						
Input Supply Current HIZ	I_{IN_HIZ1}	VIN=12V, VBAT=8.4V, EN Low, converter off, I2C on, VREG is OFF		35		μA
	I_{IN_HIZ2}	VIN=12V, VBAT=8.4V, EN Low, converter off, I2C on, VREG is ON		50		μA
	I_{IN_HIZ3}	VIN=12V, VBAT=8.4V, EN Low, converter off, I2C on, VREG is on, A2D Enabled, Fault Monitor Enabled, TH Enabled		1000		μA
Input Supply Current at No Load	I_{IN_NOLOAD}	VIN=5V, Charger Mode, converter switching, I2C on, VREG on, no load, 500kHz		1		mA
VBAT INPUT QUIESCENT CURRENTS						

Battery Current Ship Mode	I_{BAT_SHIP}	VBAT = 8.4V, no VIN, Shipping mode, Converter off, I2C off, VREG off, SHIPM Pin Enabled		1	2.5	µA
Battery Current in HIZ	I_{BAT_HIZ1}	VBAT=8.4V, VIN < VBAT, Converter off, I2C on, VREG off		20		µA
	I_{BAT_HIZ2}	VBAT=8.4V, VIN < VBAT, Converter off, I2C on, VREG on		35		µA
	I_{BAT_HIZ3}	VBAT=8.4V, VIN < VBAT, Converter off, I2C on, VREG on, A2D Enabled, Fault Monitor Enabled, TH Enabled		1100		µA
Battery Current OTG	I_{BAT_OTG}	VBAT=8.4V, V_{OTG_OUT}=5V		1		mA
INTERNAL MOSFETS						
VIN to SW1 FET Resistance	R_{DSONQ1}	T_J = 25C		25		mΩ
SW1 to PGND FET Resistance	R_{DSONQ2}	T_J = 25C		35		mΩ
SW2 to PGND FET Resistance	R_{DSONQ3}	T_J = 25C		35		mΩ
VBAT to SW2 FET Resistance	R_{DSONQ4}	T_J = 25C		25		mΩ
Cycle By Cycle Current Limit	I_{FET_ILIM}	FET_ILIM=0 Q1, Q2, Q3, or Q4 in any mode	6.5	8.5	10.5	A
		FET_ILIM=1 Q1, Q2, Q3, or Q4 in any mode	7.75	10	12.25	A

BATTERY CHARGER

(VIN = 12V, VBAT = 7.6V, T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Battery Regulation Voltage Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT} = VBAT Register Setting Measured at VBATS Pin	-0.5		0.5	%
Fast Charge Current Range	$I_{FCHG\_REG\_RANGE}$	With I_{CHG}=100% register setting	0.5		5	A
Fast Charge Current Regulation Accuracy (10mΩ current sensing resistor)	$I_{FCHG\_REG\_ACC}$	VBAT= V_{BAT_LOW}, ICHG=2A	-5		+5	%
		VBAT= V_{BAT_LOW}, ICHG=1A	-10		+10	%
		VBAT= V_{BAT_LOW} ICHG=500mA	-20		+20	%
Pre-charge Current Regulation Accuracy (10mΩ current sensing resistor)	I_{PRECHG_ACC}	VBAT= V_{BAT_LOW}, ICHG=250mA	-30		+30	%
		VBAT= V_{BAT_LOW}, ICHG=125mA	-40		+40	%
Termination Voltage Accuracy (default factory setting)	V_{TERM_ACC}	$V_{BATSHORT}$<VBAT<V_{BAT_LOW} I_{TERM} = 250mA	-30		+30	%
Battery Short Charge Current (default factory setting for I_{SHRT} and $V_{BATSHORT}$)	I_{SHRT}	$V_{BATSHORT}$<VBAT<V_{BAT_LOW} I_{SHRT}=200mA	120	200	280	mA
		V_{BAT} < $V_{BATSHORT}$ -100mV V_{BAT} > 3V I_{SHRT}=400mA	300	400	400	mA
Minimum Battery Voltage for Active I^2C	V_{BAT_UVLOZ}	V_{BAT} rising Measured at VBATS Pin	3.75	3.9	4.15	V
Battery LOW Threshold	V_{BAT_LOW}	Pre-Charge to Fast Charge with V_{BAT} Rising Relative to the factory default V_{BAT_LOW} Register Setting Measured at VBATS Pin	-3.3	V_{BAT_LOW}	+ 3.3	%
Battery LOW Hysteresis	$V_{BAT\_LOW\_HYST}$	Fast Charge to Pre-Charge with V_{BAT} Falling Relative to the factory default V_{BAT_LOW} Register Setting Referenced to actual V_{BAT_LOW} measurement Measured at VBATS Pin	3.3	6	8.6	%
Battery Short Voltage	$V_{BATSHORT}$	BAT Short Charge level to Pre-Charge level with V_{BAT} rising Relative to the factory default $V_{BATSHORT}$ Register Setting Measured at VBATS Pin	–2.5	$V_{BATSHORT}$	+ 2.5	%
Battery Short Voltage Hysteresis	$V_{BATSHORT\_HYST}$	BAT Pre-Charge to Short Charge level with V_{BAT} Falling Relative to the actual $V_{BATSHORT}$ measurement Measured at VBATS Pin	4	5	6	%

Battery Good Voltage	$V_{BATGOOD}$	V_{BAT} Rising Relative to the factory default $V_{BATGOOD}$ Register Setting Measured at VBATS Pin	-3%	V_{BAT_GOOD}	+3%	%
Battery Good Voltage Hysteresis	$V_{BATGOOD\_HYST}$	VBAT falling Relative to the actual $V_{BATGOOD}$ measurement Measured at VBATS Pin	3	4	5	%
Battery SHORT to Precharge and Pre-Charge to Short De-glitch Time	$t_{VBATSHORT}$	Battery voltage rising and falling at $V_{BATSHORT}$ threshold		16		ms
Battery Pre-Charge to Fast Charge and Fast Charge to Pre-Charge deglitch time	t_{VBAT_LOW}	Battery voltage rising and falling at V_{BAT_LOW} threshold		16		ms
Battery Charge Termination Current detection delay	$t_{VBATTERM}$	Termination current below and above I_{TERM} threshold		750		ms
Battery Good Detection deglitch Time	$t_{VBATGOOD}$	Battery voltage rising and falling at $V_{BATGOOD}$ threshold		16		ms
Battery Path Compensation	R_{BAT_COMP}	I_{CHG} = 1A At default programmed setting for $R_{VBAT\_PATH\_COMP}$	-20	$R_{VBAT\_PATH\_COMP}$	+20	%
		I_{CHG} = 2A At default programmed setting for $R_{VBAT\_PATH\_COMP}$	-15	$R_{VBAT\_PATH\_COMP}$	+15	%
		I_{CHG} = 3A At default programmed setting for $R_{VBAT\_PATH\_COMP}$	-10	$R_{VBAT\_PATH\_COMP}$	+10	%
Battery Path Compensation Voltage Clamp	$V_{BAT\_COMP\_CLAMP}$	Enable Measured at VBATS Pin	-20	$V_{BAT\_COMP\_CLAMP}$	+20	mV
Dead Battery Voltage	$V_{DBATTERY}$	Measured at VBATS Pin	2.8	3	3.2	V
Dead Battery Hysteresis	$V_{DBATTERY\_HYST}$	Measured at VBATS Pin		100		mV
Dead Battery Current	$I_{DBATTERY}$	Charge Current from VBAT pin	5	10	20	mA
BATTERY OVER-VOLTAGE PROTECTION						
Battery over-voltage threshold	V_{BATOVP}	V_{BAT} rising, as percentage of V_{BAT_REG} Measured at VBATS Pin	102	104	106	%
Battery over-voltage hysteresis	V_{BATOVP_HYST}	V_{BAT} falling, as percentage of V_{BAT_REG} Measured at VBATS Pin		2		%
Battery over-voltage deglitch time to disable charge	t_{BATOVP}	VBAT_OV_DEGLITCH_EN Register =0		5		us
		VBAT_OV_DEGLITCH_EN Register =1		40		msec
PWM OPERATION						
Programmable Frequency Range	F_{SW}		125		1000	kHz

Operation Frequency Accuracy	F_{SW}		-10		+10	%
Maximum PWM Duty Cycle	D_{MAX}			97		%

LDO

(VIN = 12V, VBAT = 7.6V, T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Normal Mode						
VREG Regulation Voltage	VREG		2		5.1	V
VREG Regulation Accuracy	$VREG_{ACC}$	At Default Factory Setting	-2		2	%
VREG Dropout	$VREG_{DROPOUT}$	I_{OUT} = 100mA			300	mV
VREG UVLO Threshold	$VREG_{UVLO}$	VREG Falling	84	88	93	%
VREG UVLO Hysteresis	$VREG_{UVLO\_HYST}$			2		%
VREG Current Limit	$VREG_{ILIM}$	V_{VIN} = 12V, VREG = 5V	100	175	250	mA
VREG Current Limit Deglitch	$VREG_{ILIM\_DG}$	In current limit		50		us
VREG Current Limit Off Time	$VREG_{ILIM\_OFF}$	After Deglitch Time		100		ms
VREG Soft Start	$VREG_{SS}$			250		us

OTG

(VIN = 12V, VBAT = 7.6V, T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
OTG Output Voltage	$V_{OTG\_REG\_ACC}$	Internal Feedback Mode VOTG_I2C Register = 0 Relative to the factory default setting. OTG output in PWM Mode. Measured at VIN Pin	-1		1	%
OTG Reference Voltage	$V_{OTG\_REF\_ACC}$	External Feedback VOTG_I2C Register = 1	1.99	2	2.01	V
OTG Battery Cut Off Voltage	$V_{OTG\_BAT\_CUTOFF}$	VBAT Rising Relative to the factory default $V_{OTG\_VBAT\_CUTOFF}$ Register setting Measured at VBATS Pin	-3.0	$V_{OTG\_VBAT\_CUTOFF}$	3.0	%
OTG Battery Cut Off Voltage Hysteresis	$V_{OTG\_BAT\_CUTOFF\_HSYT}$	VBAT Falling Relative to the actual $V_{OTG\_VBAT\_CUTOFF}$ voltage Measured at VBATS Pin	3	4	5	%
OTG Battery OV Threshold	$V_{OTG\_BAT\_OV}$	VBAT Rising Measured at VBATS Pin	22.75	23.5	24.25	V
OTG Battery OV Hysteresis	$V_{OTG\_BAT\_OV\_HYST}$	VBAT Falling Measured at VBATS Pin		300		mV
OTG Output Current Range	I_{OTG_RANGE}	With I_{CHG} = 100% register setting	0.5		5	A
OTG Mode Output Constant Current (measured at ISRN and ISRP pins using 10mΩ current sensing resistor)	I_{OTG_OCP}	I_{OTG_OCP} = 0.5A to 1A	-20	I_{OTG}	+20	%
		I_{OTG_OCP} = 1A to 2A	-15	I_{OTG}	+15	%
		I_{OTG_OCP} > 2A	-10	I_{OTG}	+10	%
OTG Mode Output Constant Current Undervoltage Protection Threshold	V_{OTG_UVP}	V_{OTG} Falling Enters Hiccup Mode Measured at VIN pin	2.62	2.72	2.82	V
OTG Mode Output Constant Current Undervoltage Protection Deglitch Time	t_{OTG_UVP}	V_{OTG} Falling		7		us
OTG Hiccup Mode Off-Time	t_{OTC_HICCUP}	Off-time after V_{OTG} falls below V_{OTG_UVP}		3		secs
OTG Overvoltage Threshold	$V_{OTG\_OVP\_INT}$	Reference to OTG_VOUT Register Setting Measured at VIN Pin	105	108	111	%
OTG Overvoltage Threshold Hysteresis	$V_{OTG\_OVP\_HYS}$	Falling Threshold		2		%
OTG Soft Start Time	t_{OTG_SS}	Relative to the factory default OTG_SS Register Setting. From 0 to 100%	-30	OTG_SS Setting	30	%
OTG Pulldown Current Source	I_{OTG_PD}	V_{OTG} Output > 2.0V	30	65	120	mA
OTG Off-Delay Timer	$t_{OTG\_OFF\_DLY}$	OFF DLY is enabled	-10	OTG_OFF_DLY	+10	%

				Setting		
OTG Off-Delay Current	$I_{OTG\_OFF\_LOAD}$	OTG in Buck Mode Only and OTG Output less than 6V $V_{BAT} > V_{OTG} + 0.5V$	3	4	6	mA
OTG Cord Compensation Accuracy	V_{OTG_CC}	OTG Cord Compensation Enabled OTG_CORD_COMP: 00: Disabled 01: 100mV 10: 200mV 11: 300mV Measured at VIN Pin	-15	OTG_CORD_COMP Setting	+15	%
OTG Output Slew Accuracy	t_{OTG_SLEW}	OTG Output Slew Setting OTG_OUTPUT_SLEW 00: 1.0V/ms 01: 0.5V/ms 10: 0.3V/ms 11: 0.1V/ms Internal Feedback Only VOTG_I2C Register = 0	-20	OTG_OUTPUT_SLEW Setting	+20	%
OTG Battery ILIM	I_{OTG_BAT}	I_{OTG_BAT} = 0.5A to 1A	-20	I_{OTG_BAT}	+20	%
		I_{OTG_BAT} = 1A to 2A	-15	I_{OTG_BAT}	+15	%
		I_{OTG_BAT} > 2A	-10	I_{OTG_BAT}	+10	%

THERMAL PROTECTION

(VIN = 12V, VBAT = 7.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Thermal Regulation and Shutdown						
Charger Mode Junction Temperature Regulation Accuracy	T_{REG}	00: Disabled 01: 80 °C 10: 100 °C 11: 120 °C	-20	T_{REG}	+20	°C
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature Increasing		160		°C
Thermal Shutdown Hysteresis	T_{SHUT_HYS}			30		°C
Thermal Shutdown Deglitch		Enter or Exit Thermal Shutdown		32		us
NTC Thermistor Input						
NTC TH Current Source	I_{TH}	When TH Pin Enabled	64.8	67.5	70.2	uA
NTC TH Current Source Leakage	$I_{TH\_DISABLE}$	When TH Pin Disable			1	uA
NTC TH -10°C Voltage	V_{TH-10C}		2.770	2.870	2.970	V
NTC TH 0°C Voltage	V_{TH0C}		1.780	1.840	1.900	V
NTC TH 10°C Voltage	V_{TH10C}		1.165	1.21	1.255	V
NTC TH 45°C Voltage	V_{TH45C}		0.317	0.332	0.347	V

NTC TH 55°C Voltage	V_{TH55C}		0.223	0.238	0.253	V
NTC TH 60°C Voltage	V_{TH60C}		0.188	0.203	0.218	V
NTC TH 65°C Voltage	V_{TH65C}		0.160	0.175	0.190	V
Deglitch time for each range transition				16		ms
TH Detect Battery or Very Cold Temp Threshold	$V_{TH\_NO\_BAT}$	When TH Pin Enabled		INTBP -150		mV
TH Detect Battery or Very Cold Temp Threshold Hysteresis	$V_{TH\_NO\_BAT\_HYST}$	When TH Pin Enabled		50		mV

ADC CONVERTER

(VIN = 12V, VBAT = 7.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Total Error	$A2D_{ERROR}$	12 Bit Range			0.5	LSB
Conversion Time	$A2D_{tCONV}$	All 6 Channels			100	ms
Conversion Time	$A2D_{tCONV}$	1 Channel			15	ms
Input Capacitance	$A2D_{CIN}$			5		pF
A2D Full Scale Input EXT_IN	$A2D_{FS}$			2.5		V
A2D Full Scale VIN	$A2D_{VIN}$	Measurement input at VIN pin	0		32.5	V
A2D Full Scale VBAT	$A2D_{VBAT}$	Measurement input at VBATS Pin	1.5		25	V
A2D Full Scale OLIM, ILIM	$A2D_{OLIM}$, $A2D_{ILIM}$			2.5		V
A2D Full Scale TH	$A2D_{TH}$	Battery NTC Voltage			3.5	V

SHIP MODE

(VIN = 12V, VBAT = 7.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SHIPM Deglitch Time Exit	t_{SHIPM_EXIT}	Ship Mode Enabled From SHIPM pin or VIN threshold	12	32	60	ms
SHIPM Pullup Resistor Exit	R_{SHIPM_PU}	Ship Mode Enabled	1	1.35	2	MΩ
SHIPM Pullup Voltage Exit	V_{SHIPM_PU}	Ship Mode Enabled		3		V
SHIPM Input low threshold Exit	V_{SHIPM_L}	Ship Mode Enabled	1.5			V
SHIPM Input Hysteresis Exit	V_{SHIPM_HYST}	Ship Mode Enabled	100			mV
SHIPM VIN Threshold Exit	V_{SHIP_VIN}	Ship Mode Enabled		3.9		V
SHIPM Pull Down Resistor	R_{SHIPM_PD}	Ship Mode Disabled	0.7	1	1.3	MΩ
SHIPM Enter Voltage to Re-enter Ship Mode	V_{SHIP_ENTER}	Voltage on SHIPM Pin Ship Mode Disabled		4.5		V
SHIPM Deglitch Time to Re-enter Ship Mode	t_{SHIPM_ENTER}	Ship Mode Disabled	20	32	45	ms
SHIPM Delay entering Ship Mode using I^2C Register Bit	$t_{SHIPM\_ENTER\_I2C}$	Ship Mode Disabled	0.8	1	1.2	s

LOGIC PIN CHARACTERISTICS – NOTG, NCHG, NIRQ, GPIO

(VIN = 12V, VBAT = 7.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
nOTG, GPIO Input low threshold	V_{ILO}				0.4	V
nOTG, GPIO Input high threshold	V_{IHI}		1.25			V
nCHG, nIRQ , GPIO Output Low Voltage	V_{OL}	Sink Current = 5 mA			0.4	V
nCHG, nIRQ, GPIO High Level Leakage Current	I_{OH}	Output = 5V			1	uA

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(VIN = 12V, VBAT = 7.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{ILO}	V_{IO} = 1.8V			0.4	V
SCL, SDA Input High	V_{IHI}	V_{IO} = 1.8V	1.25			V
SDA Leakage Current	I_{OH}	SDA = 5V			1	μA
SDA Output Low	V_{OL}	I_{OL} = 5mA			0.4	V
SCL Clock Frequency	f_{SCL}		0		1000	kHz
SCL Low Period	t_{SCL_LOW}		0.5			us
SCL High Period	t_{SCL_HI}		0.26			us
SDA Data Setup Time	t_{SU}		50			ns
SDA Data Hold Time	t_{HD}		0			ns
Start Setup Time	t_{ST}		260			ns
Stop Setup Time	t_{SP}		260			ns
Capacitance on SCL or SDA PIN	C_{IN}				10	pF
Noise suppression on SCL and SDA	$t_{DEGLITCH}$				50	ns
I²C Timeout Function	t_{out}	Total time required for I²C communication to cause I²C state machine to reset		100		ms

Note1: Comply with I²C timings for 1MHz operation - “Fast Mode Plus”.
Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering UV/POR State.
Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the IC.
Note4: IC Address is factory configurable to 7’h24, 7’h66.

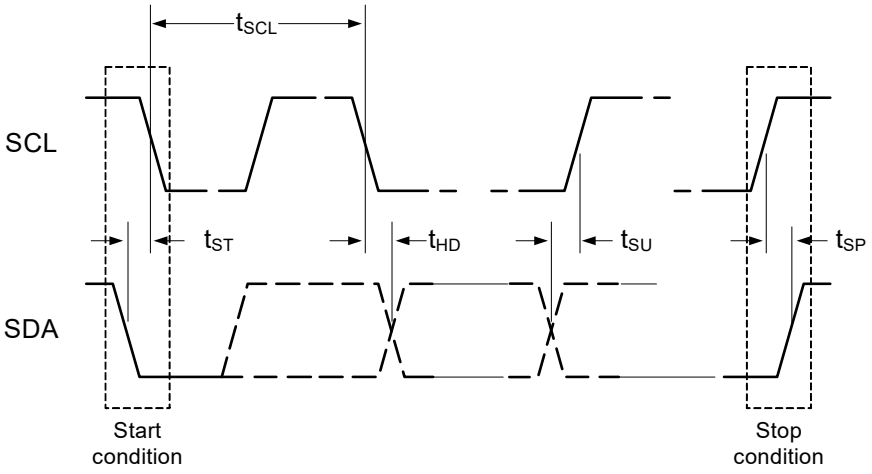


Figure 2: I²C Data Transfer

FUNCTIONAL DESCRIPTION

General

ACT2861 is a buck-boost charger with integrated MOSFETs. It provides a high efficiency, low external component count, minimal size solution for 2 to 5 cell battery charging applications. Its wide input operating range of 3.9V to 29V allows charging from many input sources.

The ACT2861 also operates in OTG (On-The-Go) mode where it operates in reverse operation by converting the battery voltage to a regulated output voltage on the VIN pin. It autonomously switches between buck, buck-boost, and boost modes depending on the input and output voltages. It is optimized for minimum quiescent current in shipping, shutdown, and standby modes. This makes it ideal for battery powered applications. SHIP mode reduces the total quiescent current to 1uA. It automatically resumes normal operation when the SHIPM pin is pulled low or power is applied to VIN.

The ACT2861 can be operated in both stand-alone and host-controlled applications. External resistors set the fast charge current, input current limit, and OTG current limit. Using host controlled I²C operation, the user has full control over voltage, current, and fault settings. The IC can be configured to charge any battery chemistry.

I²C operation gives the host full control of operating parameters as well as full knowledge of the operating parameters and fault conditions. A built in ADC provides input voltage, output voltage, input current, output current, and die temperature. The ADC also has one general purpose input to measure an external analog signal.

The ACT2861 is highly flexible and contains many I²C configurable functions. The IC's default functionality is defined by its default CMI (Code Matrix Index), but much of this functionality can be changed via I²C. I²C functionality includes OV and UV fault thresholds, switching frequencies, current limits, precharge and fast charge current settings, charging termination voltage, JEITA settings, and more. The CMI Options section shows the default settings for each available CMI option. Contact sales@active-semi.com for additional information about other configurations.

I²C Serial Interface

To ensure compatibility with a wide range of systems, the ACT2861 uses standard I²C commands. It supports clock speeds up to 1MHz. The ACT2861 always operates as a slave device, and can be factory configured to one of two 7-bit slave addresses. The 7-bit slave address is followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC's slave address

Table 1: ACT2861 I²C Addresses

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x24h	010 0100b	0x48h	0x49h
0x66h	110 0110b	0xCCh	0xCDh

The I²C packet processing state machine has a 100ms timeout function for each I²C command. If there is greater than 100ms between a start bit and a stop bit, the ACT2861 resets the I²C packet processing and sets the I²C_FAULT bit in register 0x06h. Any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet. The I²C functionality is operational in all states except RESET.

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pull-up resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics. For more information regarding the I²C 2-wire serial interface, refer to the NXP website: http://www.nxp.com.

I²C Registers

The ACT2861 has an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, switching frequency, fault thresholds, fault masks, etc. These registers give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult

sales@active-semi.com for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected IC behavior.

STATE MACHINE

ACT2861 contains an internal state machine with four internal states: SHIP MODE, HIZ, OTG MODE, and CHARGE MODE.

SHIP MODE State

SHIP MODE is the IC's lowest power state. The ACT2861 always starts up in SHIP MODE. This mode is designed to reduce battery current during shipping. In this state, the IC is completely disabled except for the SHIPM pin and the input voltage detection circuitry. This results in 1uA of quiescent current from the battery. The IC can enter SHIP MODE via I²C, the SHIPM pin, or after a full power down of both input and battery voltage. See the SHIP MODE section for more details.

HIZ State

HIZ mode is a low power state with the switching converter disabled. In this mode, I²C is active and the IC configuration can be changed. The IC enters HIZ from SHIP MODE and then either stays in HIZ or transitions to OTG MODE or CHARGE MODE depending on the external voltages, the EN_CHG pin, and the nOTG pin settings. Note that the HIZ Register overrides the EN_CHG and nOTG pin settings and holds the IC in HIZ mode. See the HIZ section for more details.

CHARGE MODE

In CHARGE MODE, the ACT2861 transfers power from VIN to VBAT to charge the battery. The IC follows the Charge State Machine. While in CHARGE MODE, the nOTG pin is ignored until charge mode is disabled. See the CHARGE MODE section for more details.

OTG MODE

In OTG MODE, the ACT2861 transfers power from VBAT to VIN to provide a regulated supply from the battery. The IC enters this mode with the nOTG Pin or the OTG_EN_OVERRIDE register. Once in OTG Mode, the IC follows the OTG State Machine. While in OTG MODE, the EN_CHG input is ignored. See the OTG MODE section for more details.

CHARGE STATE MACHINE

When the ACT2861 is in CHARGE MODE, it follows a dedicated charging state machine that autonomously handles complete battery charge control. This state machine is pre-configured for Li-Ion batteries. The ACT2861 can be configured to charge any battery topology using I²C.

Reset State (RESET)

All charging starts in the RESET State. In this state, all charging is completely disabled. The IC waits until the VIN voltage is within specification and then starts the Startup Delay timer. This timer is controlled by I²C bits VIN_STRT_DLY[1:0] in register 0x0Dh.

During this state the nCHG pin is pulled low to indicate charging is in progress.

The Low Battery Safety timer and the Fast Charge Safety Timer are both held in reset in this state.

Dead Battery Condition State (SCOND_DB)

This charging state protects against dead batteries or battery packs where the internal battery FET has opened. The ACT2861 always enters this state after a valid input voltage is applied and the Startup Delay timer is expired. If the total battery voltage is less than 3V, the IC stays in this state and sources 10mA to the battery. In many cases, the internal battery FET is opened and the 10mA source current will reset the battery FET. The IC exits this state when the battery voltage increases above 3V for > 256us. The Low Battery Safety Timer runs in this mode.

During this state the nCHG pin is pulled low to indicate charging is in progress.

Battery Short Condition State (SCOND)

This state also protects against dead batteries. It provides a reduced charge current to protect over-discharged batteries. The default charging current is 100mA, but this can be modified via I²C bits VBAT_SHORT_CURRENT in register 0x0Bh.

During normal charging, the charger enters SCOND when the battery voltage is greater than 3V for 16ms.

The system continuously monitors the battery voltage and if the battery voltage is greater than the VBATSHORT voltage threshold for 16ms, the charger exits the SCOND state and moves to the Precondition state. The battery short detection voltage, VBAT_SHORT, is adjustable by I²C bits VBAT_SHORT in register 0x0Bh. Note: If the battery

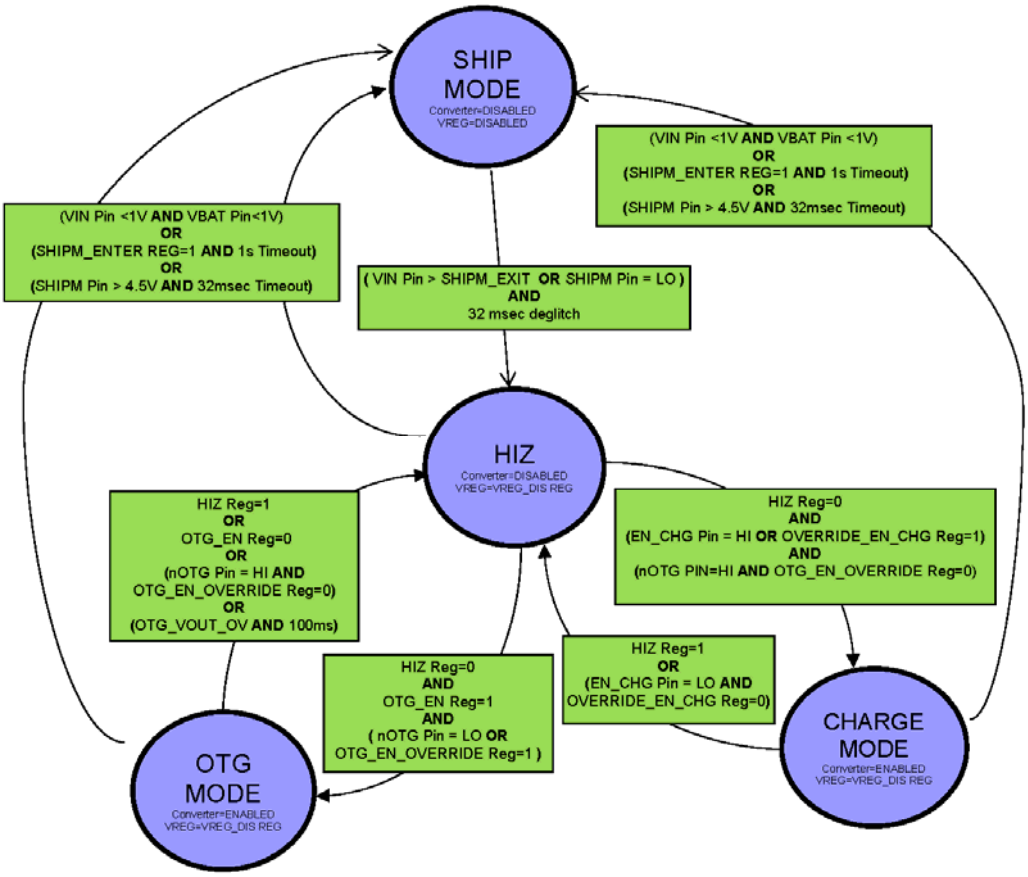


Figure 3: Operating Modes State Machine

voltage is above the VBATSHORT voltage when entering this state, the charger still charges at the ISHRT current for 16ms before moving to the Precondition state.

During this state, the Low Battery Safety Timer is running to detect fault conditions or bad battery. See the Charge Safety Timers section for further details. The Low Battery Safety Timer is a cumulative timer for the SCOND, and PCOND states and is fixed at 2 hours.

A Safety Timer timeout or Battery OV during this state causes the charger to move to the Fault State, which disables charging. An input voltage OV or UV condition also moves the state machine into the Fault state. Finally, a fault on the VREG LDO, which is not masked with the DIS_CHG_VREG_FLT register also moves the state machine into the Fault state.

During this state, the VIN voltage and VIN Current regulation loops are active to ensure the input supply power ratings are not exceeded. Additionally, the thermal regulation loop is active to keep the ACT2861 junction temperature at or below the desired maximum junction temperature. See the appropriate sections for more details.

During this state the nCHG pin is pulled low to indicate charging is in progress.

Battery Short Condition Temp Suspend (SCSUSPEND)

This state prevents charging when the battery temperature measured by the TH pin exceeds the JEITA or Battery Temp registers settings for Hot or Cold. All switching stops and charging is suspended. The state machine only enters SCSUSPEND from the SCOND state. The charger transitions back to the SCOND state and

resumes charging when the temperature returns to allowable levels. The system can force the IC out of the SCSUSPEND state by disabling the TH input via I²C.

In this state, the Low Battery Safety Timer is suspended, but held at its current value, in SCSUSPEND state. The timer resumes counting when charging resumes.

During this state the nCHG output pin blinks at 1HZ to indicate a fault condition.

Battery Precondition Condition State (PCOND)

The PCOND state preconditions the battery with a low charge current to avoid damage to fully discharged batteries. In this state the charger charges the battery at the IPRECHG level. The default precharge current is 10% of the fast charge current which is set by the OLIM resistor. It is adjustable between 5% and 20% of the fast charge current using the I2C bits IPRECHG[3:0] in register 0x19h.

During normal charging, the charger enters PCOND when the battery voltage is greater than VBATSHORT for 16ms.

The system continuously monitors the battery voltage and if the battery voltage is greater than the VBAT_LOW voltage threshold for 16ms, the charger exits the PCOND state and moves to the Fast Charge state. Note: If the battery voltage is above the VBAT_LOW voltage when entering this state, the charger still charges at the IPRECHG current for 16ms before moving to the Fast Charge state.

During this state, the Low Battery Safety Timer is running to detect a fault conditions or bad battery. See the Fast Charge Safety Timers section for further details. The Low Battery Safety Timer is a cumulative timer for the SCOND and PCOND states and is fixed at 2 hours.

A Low Battery Safety Timer timeout or Battery OV fault during this state causes the charger to move to the Fault State, and disable charging. An input voltage UV or OV condition also moves the state machine into the Fault state. Finally, a fault on the VREG LDO, which is not masked with the DIS_CHG_VREG_FLT register moves the state machine into the Fault state.

During this state, the VIN voltage and VIN Current regulation loops are active to ensure the input supply power ratings are not exceeded. Additionally, the thermal regulation loop is active to keep the ACT2861 junction temperature at or below the desired maximum junction temperature. See the appropriate sections for more details.

During this state the nCHG pin is pulled low to indicate charging is in progress.

Battery Precondition BAT Temp Suspend (PCSUSPEND)

This state prevents charging when the battery temperature measured by the TH pin exceeds the JEITA or Battery Temp registers settings for Hot or Cold. The state machine only enters PCSUSPEND from the PCOND state. The charger transitions back to the PCOND state and resumes charging when the temperature returns to allowable levels. The system can force the IC out of the PCSUSPEND state by disabling the TH input via I²C.

In this state, the Low Battery Safety Timer is suspended, but held at its current value. The timer resumes counting when charging resumes.

During this state the nCHG output pin blinks at 1HZ to indicate a fault condition.

Battery Fast Charge State (FASTCHG)

The Fast Charge state is the state where charger provides full charging current to the battery. The ACT2861 voltage and temperature protections ensure that the battery only enters the Fast Charge state when the conditions are safe for fast charging.

During normal charging, the charger enters FASTCHG when the battery voltage is greater than VBAT_LOW for 16ms.

If the charge current drops below ITERM for 750ms, the charger assumes the battery is charged and the state machines moves to either Charge Termination state or the Charge Full State.

In the FASTCHG state, the charger regulates the constant charging current, ICHG, until the battery voltage reaches the VBAT_REG voltage. Then it regulates the battery voltage to a constant voltage. If in voltage regulation mode and current is pulled from the battery causing its voltage to drop below VBAT_REG, the charger seamlessly switches back into constant current mode. When the battery voltage reaches the VBAT_REG voltage, the current slowly decays as the battery “tops off”. When the current drops to the termination current, ITERM, the battery is fully charged.

The VBAT_REG battery voltage can be adjusted using the I²C bits VTERM[10:0] bits in registers 0x11h and 0x12h.

The ICHG current can be controlled with the external resistor on the OLIM pin and by the I²C bits IFCHG[6:0] in register 0x18h. The I²C current adjustable is programmed as a percentage of the full current level set by the OLIM resistor.

The termination current can be adjusted using the I²C bits ITERM[3:0] in register 0x19h.

In this state, the Low Battery Safety Timer is turned off and reset. The Fast Charge Safety Timer starts running at the nominal rate to detect faults with battery charging. This timer can be adjusted between 30 minutes and 16 hours, using the I²C bits FC_SAFETY_TIMER in register 0x1Bh. If a battery temperature fault condition is detected, the charger moves to the FAULT state. See the Charge Safety Timers section for further details.

A Fast Charge Safety Timer timeout or Battery OV fault during this state causes the charger to move to the Fault State, and disable charging. An input voltage UV or OV condition also moves the state machine into the Fault state. Finally, a fault on the VREG LDO, which is not masked with the DIS_CHG_VREG_FLT register moves the state machine into the Fault state.

If the battery voltage drops below the VBAT_LOW voltage for 16ms, the charger goes back into the Battery Precondition state.

During this state, the VIN voltage and VIN Current regulation loops are active to ensure the input supply power ratings are not exceeded. Additionally, the thermal regulation loop is active to keep the ACT2861 junction temperature at or below the desired maximum junction temperature. See the appropriate sections for more details.

During this state the nCHG pin is pulled low to indicate charging is in progress.

Fast Charge Temp Suspend (FCSUSPEND)

This state prevents charging when the battery temperature measured by the TH pin exceeds the JEITA or Battery Temp registers settings for Hot or Cold. The state machine only enters FCSUSPEND from the FASTCHG state. The charger transitions back to the FASTCHG state and resumes charging when the temperature returns to allowable levels. The system can force the IC out of the FCSUSPEND state by disabling the TH input via I²C.

In this state, the Fast Charge Safety Timer is suspended, but held at its current value. The timer resumes counting when charging resumes.

During this state the nCHG output blinks at 1HZ to indicate a fault condition.

Charge Full State (CHGFULL)

The Charge Full state functionality is the same as the FASTCHG state. The charger can stay in the CHGFULL state indefinitely. It keeps a fully charged battery regulated to the VBAT_REG voltage. If something pulls current from the battery, the charger supplies current to maintain the battery voltage at VBAT_REG. The maximum charge current is still limited by the external OLIM resistor and the IFCHG[6:0] register.

During normal charging, the charger enters CHGFULL state from the FASTCHG state when the charging current drops below ITERM for greater than 750ms AND the I²C bit EN_TERM = 0.

If the charge current exceeds the ITERM current for 16ms, or if the battery voltage drops below VBAT_GOOD for 16ms, the IC exits the Charge Full state and moves back to the FASTCHG state.

A Battery Temp or Battery OV fault during this state causes the charger to move to the Fault state and disable charging. An input UV or OV condition also moves the state machine into the Fault state. Finally, a fault on the VREG LDO, which is not masked with the DIS_CHG_VREG_FLT register moves the state machine into the Fault state.

In this state, the Fast Charge Safety Timer and the Low Battery Safety Timer are reset and held at 0.

During this state the nCHG pin is HIZ to indicate the charging has completed and the Fast Charge Safety Timer is reset and held at 0.

Charge Full Suspend (CFSUSPEND)

This state prevents charging when the battery temperature measured by the TH pin exceeds the JEITA or Battery Temp registers settings for Hot or Cold. The state machine only enters CFSUSPEND from the CHGFULL state. The charger transitions back to the CHGFULL state and resumes charging when the temperature returns to allowable levels. The system can force the IC out of the CFSUSPEND state by disabling the TH input via I²C.

In this state, the Fast Charge Safety Timer is still held at 0.

During this state the nCHG output blinks at 1HZ to indicate a fault condition.

Battery Termination State (CHGTERM)

In this state, the charger is disabled and does not supply any current to the battery. It monitors the battery voltage to check for the condition when the battery voltage drops to VTERM-VRECHARGE. The VRECHARGE voltage is typically 100mV or 150mV per cell. Once the battery voltage drops below the threshold, the IC enters the Fast Charge state and recharges the battery.

During normal charging, the charger enters this state when the charging current drops below ITERM for greater than 750ms AND the I²C bit EN_TERM = 1.

In this state, the Fast Charge Safety Timer and the Low Battery Safety Timer are reset and held at 0.

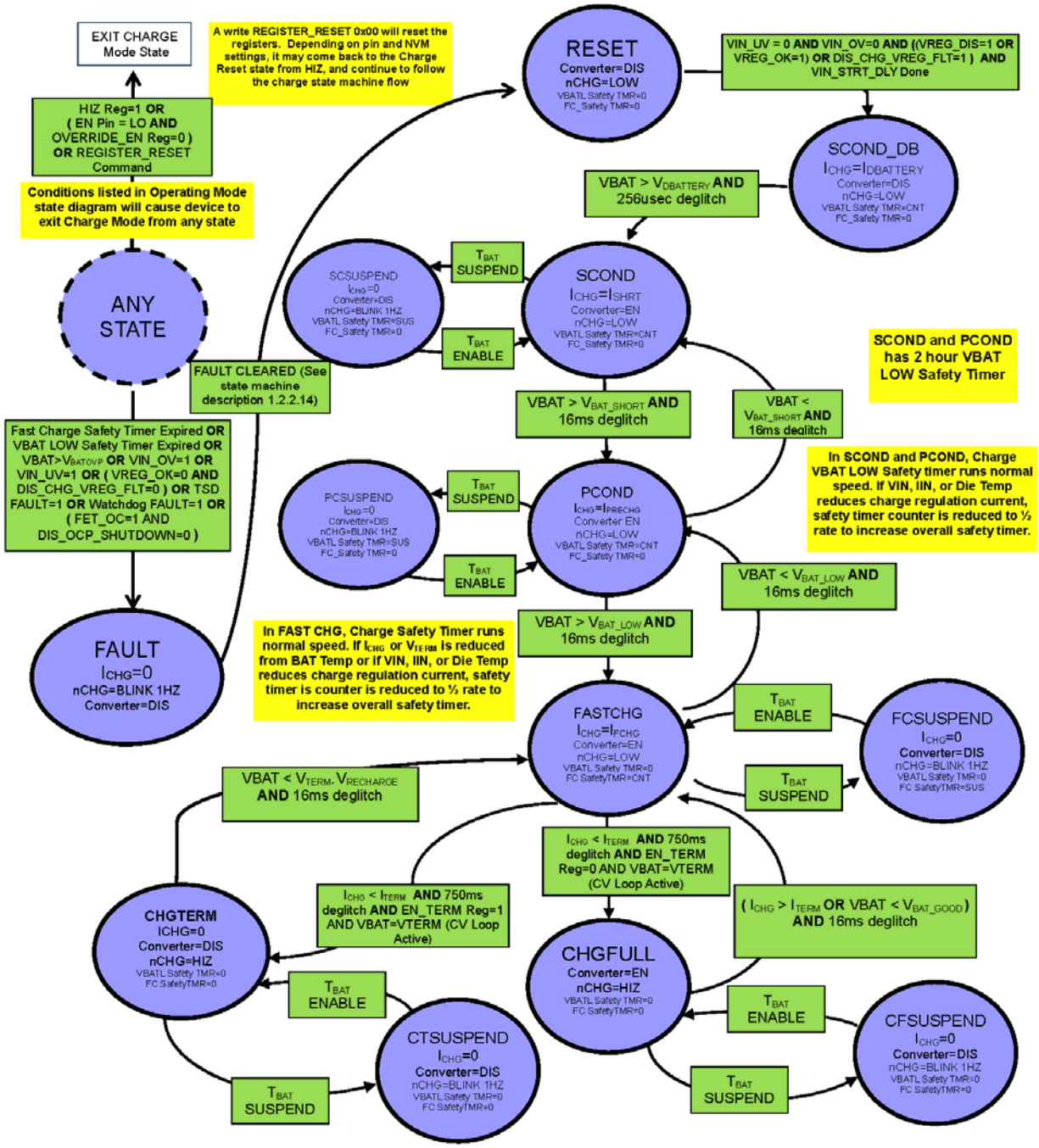


Figure 4: Charger State Machine

A Battery Temp or Battery OV fault during this state causes the charger to move to the Fault state and disable charging. An input UV or OV condition also moves the state machine into the Fault state. Finally, a fault on the VREG LDO, which is not masked with the DIS_CHG_VREG_FLT register moves the state machine into the Fault state.

The nCHG pin is HIZ to indicate the charging has completed and the Fast Charge Safety Timer is reset and held at 0.

Charge Termination Suspend (CTSUSPEND)

This state prevents charging when the battery temperature measured by the TH pin exceeds the JEITA or Battery Temp registers settings for Hot or Cold. The state machine only enters CTSUSPEND from the CHGTERM state. The charger transitions back to the CHGTERM state and resumes charging when the temperature returns to allowable levels. The system can force the IC out of the CTSUSPEND state by disabling the TH input via I²C.

In this state, the Fast Charge Safety Timer is still held at 0.

During this state the nCHG output blinks at 1HZ to indicate a fault condition.

Fault Mode (FAULT)

This state protects the battery against all system level faults by disabling the charger and preventing any additional current to go to the battery.

The charger enters the FAULT state if any of the following occurs:

1. Fast Charge Safety Timer Timeout – If the timer exceeds the setting in the FC_SAFETY_TIMER[4:0] register 0x1Bh, then the charger enters the FAULT state. It stays in the FAULT state until this timer is reset with the I²C bit DIS_SAFETY_TIMER in register 0x1Bh. Any condition that clears the Fast Charge Safety timer makes the charger exit the FAULT state and returns the charger to the RESET state to start charging again. The Fast Charge Safety timer can be reset by setting the I²C bit DIS_SAFETY_TIMER = 1. The charger also exits the FAULT state if the IC is enters HIZ or SHIPMODE. Refer to the Operating Modes State Machine Diagram for more details.

2. Low Battery Safety Timer Timeout – If the timer exceeds 120 minutes for the states when VBAT is less than VBAT LOW, then the charger enters the FAULT state. It stays in the FAULT state until this timer is reset with the I²C bit DIS_SAFETY_TIMER in register 0x1Bh. Any condition that clears the Low Battery Safety Timer makes the charger exit the FAULT state and returns the charger to the RESET state to start charging again. The Low Battery Safety Timer can be reset by setting the I²C bit DIS_SAFETY_TIMER = 1. The charger also exits the FAULT state if the IC is enters HIZ or SHIPMODE. Refer to the Operating Modes State Machine Diagram for more details.

3. VBAT OV Fault – This fault can be latching or non-latching depending on the I²C bit DIS_VBAT_OVP in register 0x01h setting. If DIS_VBAT_OVP=0, then a battery overvoltage fault is latching. This requires the IC to exit the Charge state to exit the charger FAULT state. Exit the Charge state with the EN_CHG pin or any other method shown in the Operating Modes State Machine Diagram

If DIS_VBAT_OVP=1, then a battery overvoltage fault is not latching. The charger exits the FAULT state and returns to the RESET state when the overvoltage fault clears.

A 40msec deglitch timer is available to prevent false OV fault detection due to noise or short battery voltage transients The I²C bit VBAT_OV_DEGLITCH_EN in register 0x0Bh sets the deglitch time. Setting this bit = 1 gives a 40ms deglitch time. Setting it = 0 gives a 5us deglitch time.

4. VIN OV or VIN UV Fault – If the VIN voltage exceeds the UVLO or OVLO thresholds, the charger stops charging and enters the FAULT state. Once the input voltage returns to an acceptable level, the IC returns to the RESET state to restart the charging process.

5. VREG LDO Fault – If the VREG LDO is not within regulation or in an overcurrent condition, the charger enters the FAULT state. Once the fault condition has been removed from the LDO, the charger returns to the RESET state to restart the charging process. This fault can be ignored, if I²C bit DIS_CHG_VREG_FLT in register 0x0Dh = 1. If this bit = 1, the charger does NOT go to the FAULT state with a VREG LDO fault.

6. Die Thermal Shutdown (TSD) – If the die temperature exceeds TSHUT (160°C) the charger moves into the FAULT state until it cools down by the thermal hysteresis, TSHUT_HYST (30°C). This fault cannot be cleared or masked. The IC must cool down before exiting the FAULT state. Once the IC cools down, it automatically clears this fault, exits the FAULT state, and returns to the RESET state to resume charging.

7. Watchdog Fault – If the watchdog timer is enabled and the timer ties out, the Watchdog fault holds the charger in the FAULT state until the watchdog timer is reset or cleared. It can be reset by writing a 1 to the I²C bit WATCHDOG_RESET or by disabling the Watchdog timer with I²C bit WATCHDOG[1:0]=00.

8. FET_OC – If any of the FET currents reach the over-current limit threshold for 16 cycles in a row, the IC enters FET_OC fault. The fault latches and the IC must EXIT the Charge state to clear the latch. Exit the Charge state with the EN_CHG pin or any other method shown in the Operating Modes State Machine Diagram

When the IC is in the FAULT state, the switching charger is disabled and the charge current to the battery is 0A.

When in the FAULT state, the nCHG pin blinks at a 1HZ rate to indicate a fault condition.

OTG STATE MACHINE

The ACT2861 has a dedicated OTG state machine. This state machine handles the startup, normal operation and fault conditions in OTG mode.

OTG Reset State (OTG_RST)

The OTG state machine always starts from the OTG_RST state. All OTG operation starts from this state. In this state, the switcher is disabled and the state machine is waiting for all the required conditions to move to the OTG_SS state.

After all the following fault conditions are cleared, the IC starts the OTG Enable Delay Timer. This timer is controlled by I²C bit OTG_EN_DLY[1:0] in register 0x0Fh. Once the timer has expired, the state machine moves to the OTG_SS state.

OTG Reset Faults:

OTG_VBAT_CUTOFF voltage: This fault is active when the battery voltage is lower than the programmed OTG battery cutoff voltage. The cutoff voltage is set by I²C bit OTG_VBAT_CUTOFF in register 0x0Fh. This fault self-clears when VBAT is higher than the OTG battery cutoff voltage.

VREG LDO OK – This fault is set when an LDO fault is detected. This includes the 100msec timeout period. This fault automatically clears when the VREG LDO has exited the faulted condition. Note: This fault can be masked to allow the state machine to exit OTG_RST while there is a fault on the VREG LDO by using the I²C bit DIS_OTG_VREG_FLT in register 0x10 Bit 1.

OTG HOT or OTG COLD: This fault is active if the battery temperature as detected on the TH pin is above or below the programmed temperature thresholds. This fault self-clears when the battery temperature goes back into the allowable range.

Watchdog Timer Fault: This fault is active if the watchdog timer is enabled and the timer times out. This fault clears when the watchdog timer is reset or cleared. It can be reset by writing a 1 into the I²C bit WATCHDOG_RESET in register 0x00h. It can be cleared by disabling the watchdog timer by setting I²C bits WATCHDOG[1:0] = 0x00h.

During this state, the Fast Charge Safety and Low Battery Safety Timer timers are suspended and held at their current value.

FET Overcurrent Fault: This fault is set if a switching FET exceeds the cycle-by-cycle current limit for 8 (or 16) consecutive cycles. The FET_OC fault is latched. To clear this latch, the IC must exit the OTG mode and enter HIZ mode. This is typically accomplished by toggling the nOTG pin or setting the HIZ register to 1.

VBAT Overvoltage: This fault is set if VBAT exceeds the $V_{OTG\_BAT\_OV}$ voltage. The OV fault self-clears when VBAT drops below $V_{OTG\_BAT\_OV}$ and the IC exits the OTG_RST state.

Die Thermal Shutdown (TSD): This fault is active when die temperature exceeds the T_{SHUT} (160°C) temperature. This fault self-clears when the die temperature cools down by the temperature hysteresis, T_{SHUT_HYST} (30°C). This fault cannot be cleared or masked. The IC must cool down before exiting the OST_RST state.

OTG Softstart State (OTG_SS)

In this state, the IC enables the converter and softstarts the OTG output voltage.

The state machine enters OTG_SS from the OTG_RST state when all faults are cleared. The state machine transitions to the OTG_REG state after the OTG output is softstarted an in regulation.

The softstart time is controllable by the I²C bit OTG_SS in register 0x0Eh. If a fault occurs during the softstart, the state machine jumps back to the OTG_RST state and disables the converter. Once the soft start is done, the IC jumps to the OTG_REG state.

OTG Regulation State (OTG_REG)

The normal regulation occurs in the OTG_REG state. If a major fault occurs during operation the IC will jump back to the reset state and disable the converter. During this state, the converter can be disabled with a light load condition. Additionally, if the output drops below V_{OTG_UVP} (3.0V), the IC will go into a hiccup mode to protect the output in a shorted condition.