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23V Buck-Boost Converter with Integrated MOSFETs

BENEFITS and FEATURES

- **Buck-Boost Converter with 4 Integrated Switches**
- **Wide VIN Range: 3.9V to 23V (No Dead Zone)**
- **Wide VOUT Range: 3.0V to 23V**
- **Supports QC3.0 / USB PD + PPS output levels and transition times**
- **Programmable Frequency: 125KHz, 250KHz, 500kHz, and 1MHz**
- **2V ~ 5V/100mA Programmable Output LDO**
- **Precision 0.5% Voltage Reference**
- **+/-4% Output Constant Current Regulation**
- **Programmable Output Voltage and Currents via both IC pins and I²C**
- **Programmable Soft-Start**
- **Programmable Safety Timer**
- **Cycle-by-Cycle Current Limit**
- **Built in ADC for Temperature, Input and Output Voltage and Current monitoring**
- **Thermal Regulation and Protection**
- **25mΩ FET from VIN to SW1**
- **25mΩ FET from SW2 to VOUT**
- **35mΩ FET from SW1 to PGND**
- **35mΩ FET from SW2 to PGND**
- **Thermally Enhanced 32-Lead 4mx4mm QFN**

APPLICATIONS

- Car Charger
- Power Bank
- 24V Industrial Applications
- Automotive Power Systems
- Multiple Power Source Supplies
- DC UPS
- Solar Powered Devices
- Solid-State Lighting

GENERAL DESCRIPTION

The ACT510x is a buck-boost converter with 4 integrated MOSFETs. It offers a high efficiency, low component count, compact solution for a wide input voltage: 3.9V to 23V

The 4 internal low resistance NMOS switches minimize the size of the application circuit and reduce power losses to maximize efficiency. Internal high side gate drivers, which require only the addition of two small external capacitors, further simplify the design process. An advanced switch control algorithm allows the buck-boost converter to maintain output voltage regulation with input voltages that are above, below or equal to the output voltage. Transitions between these operating modes are seamless and free of transients and subharmonic switching.

The ACT510x has been optimized to reduce input current in shipping, shutdown, and standby for applications which are sensitive to quiescent current draw, such as battery-powered devices.

The ACT510x output voltage can be set between 3V ~ 23V which can be configured by either I²C (ACT5101) or an external resistor divider (ACT5102). The output constant current limit and cord compensation makes it flexible for any kinds of protocols such as USB PD, QC 3.0/4.0 etc. The system can be monitored and configured by I²C as well. The build-in ADC can be read for the information of input/output voltages and currents, and the die temperature.

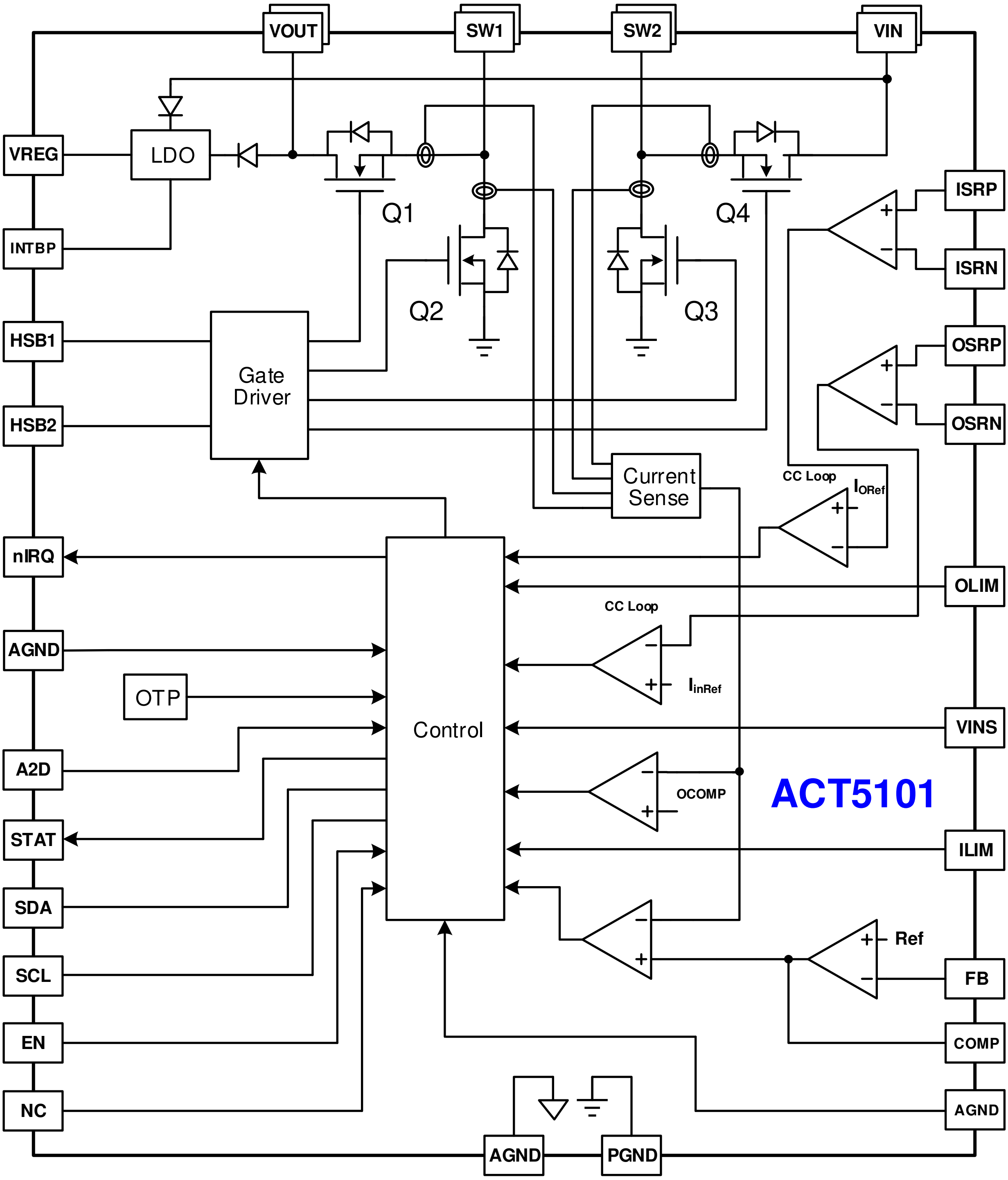
ACT510x integrates a 100mA LDO with OCP/UVLO protection to provide power for the MCU and other peripheral components inside the system.

The ACT510x operation frequency can be configured from 125 kHz to 1MHz, making the system design flexible for components size and efficiency optimization.

The ACT510x has been optimized to reduce input current for applications which are sensitive to quiescent current draw, such as battery-powered devices.

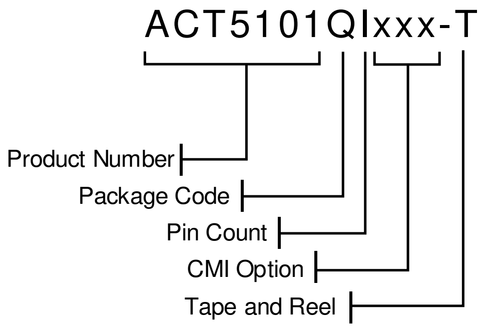
The AC510x is available in 32-pin, 4 x 4 mm FCOL QFN package.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	Feedback	Default Output Voltage	Default LDO Voltage	Fsw	ADC Converter	PACKAGE
ACT5101QI102-T	Internal	5.1V	5.0V	500kHz	Yes	FCQFN4x4-32
ACT5102QI102-T	External	n/a	5.0V	500kHz	No	FCQFN4x4-32



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

Note 3: Package Code designator “Q” represents QFN

Note 4: Pin Count designator “I” represents 32 pins

Note 5: See the CMI Options section at the back of the datasheet for more information on each CMI’s settings.

PIN CONFIGURATION

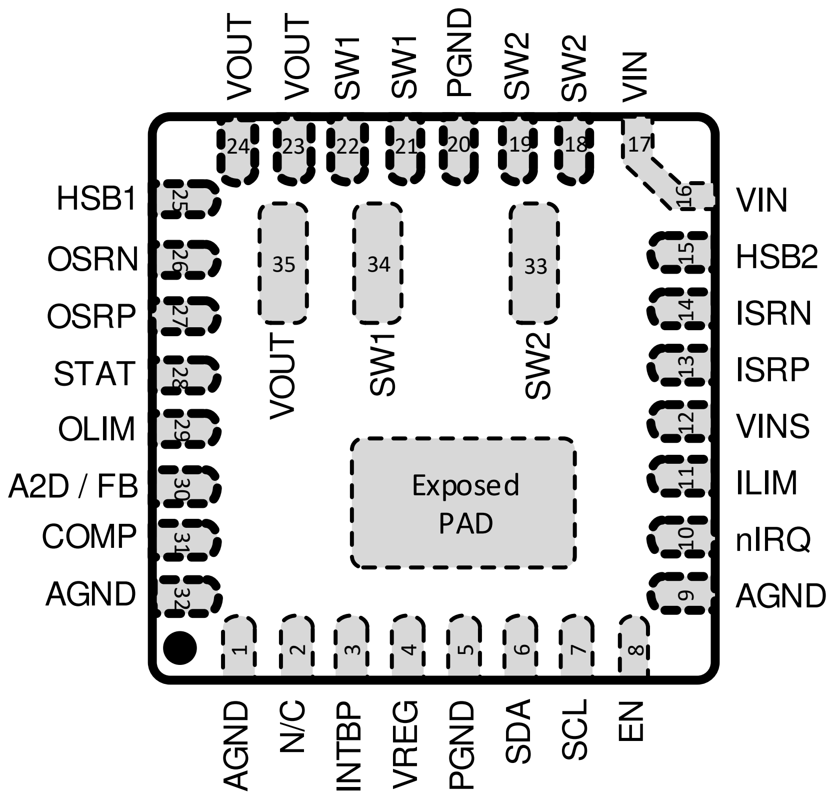


Figure 1: Pin Configuration – Top View – QFN4x4-32

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1, 9, 32	AGND	Analog Ground. Kelvin connect AGND to the PGND plane.
2	NC	No Connect. Connect this pin to AGND.
3	INTBP	Internal Voltage Bypass - Connect a 100nF ceramic capacitor between INTBP and AGND
4	VREG	Internal VREG LDO output. The output voltage is programmable from 2V to 5V. Connect a 1.0uF between VREG and AGND. The maximum current capability for this pin is 100mA.
5, 20	PGND	Power Ground. Connect to large ground plane on PCB with thermal vias.
6	SDA	I^2C Data Input and Output. Needs an external pull up resistor.
7	SCL	I^2C Clock Input. Needs an external pull up resistor.
8	EN	Enable Input. The converter is enabled when EN is pulled high and disabled when EN is pulled low.
10	nIRQ	Interrupt Open-Drain Output. nIRQ goes low to indicate a fault condition. nIRQ is referenced to AGND.
11	ILIM	Input current limit setting pin. Connect a resistor from ILIM to AGND to program the maximum input current.
12	VINS	Input Voltage Sense Input – Kelvin connect to the input voltage input capacitors.
13	ISRP	Input current sense resistor positive input.
14	ISRN	Input current sense resistor negative input.
15	HSB2	High Side Bias Boot-strap pin. This provides power to the internal high-side MOSFET gate driver circuitry. Connect a 47nF capacitor from HSB2 to SW2 pin
16, 17	VIN	Power Input pins. Connect these pins to 22uF-100uF ceramic capacitors placed as close to the IC as possible.
18, 19	SW2	Power switching output to external inductor.
21, 22	SW1	Power switching output to external inductor.
23, 24	VOUT	Output voltage pins. Place 22uF to 44uF decoupling capacitors between VOUT and PGND.
25	HSB1	High Side Bias Boot-strap pin. This provides power to the internal high-side MOSFET gate driver circuitry. Connect a 47nF capacitor from HSB1 to SW1 pin
26	OSRN	Output current sense resistor negative input
27	OSRP	Output current sense resistor positive input.
28	STAT	Open drain status output to indicate various IC operating conditions. A LOW indicates the converter is enabled and has a valid output. A HIZ indicates the converter is disabled for any reason
29	OLIM	Output constant current limit setting pin. Connect a resistor from OLIM to AGND to program the output current.
30 (ACT5101)	A2D	A2D input pin
30 (ACT5102)	FB	Output voltage feedback pin.
31	COMP	Error Amplifier Output. This pin is used to compensate the converter.
Exposed Pad	PGND	Power Ground. Connect to large ground plane on PCB with thermal vias.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE	UNIT
VOUT	-0.3 to +24	V
OSRP, OSRN	-0.3 to VOUT + 0.3	V
VIN	-0.3 to +23	V
ISRP, ISRN	-0.3 to VIN + 0.3	V
VINS	-0.3 to ISRN + 0.3	V
SW1	-0.3 to VOUT + 0.3	V
SW2	-0.3 to VIN + 0.3	V
HSB1	V_{SW1} - 0.3 to V_{SW1} + 5.5	V
HSB2	V_{SW2} - 0.3 to V_{SW2} + 5.5	V
VREG	-0.3 to +6	V
SCL, SDA, VREG, STAT, EN, nIRQ, FB, COMP, ILIM, OLIM, A2D	-0.3 to +6	V
AGND to PGND	-0.3 to +0.3	V
Junction to Ambient Thermal Resistance (θ_{JA})	35	°C/W
Operating Junction Temperature (T_J)	-40 to 150	°C
Operating Ambient Temperature Range (T_A)	-40 to 85	°C
Store Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

Note1: Measured on Active-Semi Evaluation Kit

Note2: Do not exceed these limits to prevent damage to the IC. Exposure to absolute maximum rating conditions for long periods may affect IC reliability.

SYSTEM CHARACTERISTICS

(VIN = 5V, T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Inputs						
Input voltage Range	V_{IN}		4		23	V
Input Over Voltage Threshold	V_{IN_OV}	Rising Measured at VINS Pin	22.75	23.5	24.25	V
Input Over Voltage Hysteresis	$V_{IN\_OV\_HYST}$	VIN Falling Measured at VINS Pin		300		mV
VIN UVLO Threshold	V_{IN_UV}	VIN Rising Measured at VINS Pin	-3.0	V_{IN_UV}	3.0	%
VIN UVLO Hysteresis	$V_{IN\_UVLO\_HYST}$	VIN Falling Measured at VINS Pin	3	4	5	%
Input Current	I_{IN}	VIN=8.4V, V_{OUT}=5V		1		mA
Converter Operation						
Output Voltage	$V_{OUT\_REG\_ACC}$	Internal Feedback Mode VOUT_I2C Register = 1 Converter output in PWM mode Measured at VOUT Pin	-1		1	%
FB Reference Voltage	$V_{OUT\_REF\_ACC}$	ACT5102 IC only	1.99	2	2.01	V
Output Current Range	I_{OUT_RANGE}	With I_{OUT}=100% register setting	0.5		5	A
Output Constant Current (measured at OSRN and OSRP pins)	I_{OUT_OCP}	I_{OUT_OCP} = 0.5A to 1A	-20	I_{OUT}	+20	%
		I_{OUT_OCP} = 1A to 2A	-15	I_{OUT}	+15	%
		I_{OUT_OCP} > 2A	-10	I_{OUT}	+10	%
Output Constant Current Undervoltage Protection Threshold	V_{OUT_UVP}	VOUT Falling, Enters Hiccup Mode Measured at VOUT pin	2.62	2.72	2.82	V
Output Constant Current Undervoltage Protection Deglitch Time	t_{OUT_UVP}	V_{OUT} Falling		7		us
Hiccup Mode Off Time	t_{OUT_HICCUP}	Off time after V_{OUT} falls below V_{OUT_UVP}		3		s
Over-Voltage Threshold	$V_{OUT\_OVP\_EXT}$	I^2C Feedback (ACT5101) Relative to the VOUT Register Setting	105	108	111	%
		External Feedback (ACT5102) Voltage at FB Pin	2.18	2.24	2.30	V
Over-Voltage Threshold Hysteresis	$V_{OUT\_OVP\_HYS}$	Falling Threshold		2		%
Soft Start Time	t_{OUT_SS}	Relative to the factory default SOFT_START Register Setting. From 0 to 100%	-30	SOFT START Setting	30	%
Pulldown Current Source	I_{OUT_PD}	V_{OUT} Output > 2.0V	30	65	120	mA

Off Delay Current Timer	$t_{OUT\_OFF\_DLY}$	EN_DLY Enabled	-10	OFF_DLY Setting	+10	%
Off Delay Current	$I_{OUT\_OFF\_LOAD}$	OFF_LOAD=1 Converter in Buck Mode Only $V_{IN} > V_{OUT} + 0.5V$	4	5	6	mA
Cord Compensation Accuracy	V_{OUT_CC}	CORD_COMP: 00: Disabled 01: 100mV 10: 200mV 11: 300mV Measured at VOUT Pin	-15	CORD_COMP Setting	+15	%
Output Slew Accuracy	t_{OUT_SLEW}	OUTPUT_SLEW 00: 1.0V/ms 01: 0.5V/ms 10: 0.3V/ms 11: 0.1V/ms Internal Feedback Only VOUT_I2C Register = 1	-20	OUTPUT_SLEW Setting	+20	%
Input Current ILIM	I_{ILIM}	I_{ILIM} = 0.5A to 1A	-20	I_{ILIM}	+20	%
		I_{ILIM} = 1A to 2A	-15	I_{ILIM}	+15	%
		I_{ILIM} > 2A	-10	I_{ILIM}	+10	%
PWM OPERATION						
Frequency Range	f_{SW}		125		1000	kHz
Operation Frequency Accuracy	f_{SW}		-10%		+10%	kHz
Maximum PWM Duty Cycle	D_{MAX}			97		%
INPUT QUIESCENT CURRENTS						
Input Current in HIZ	I_{IN_HIZ2}	VIN=12V, Converter off, I²C on, VREG on		35		µA
	I_{IN_HIZ3}	VBAT=12V, Converter off, I²C on, VREG on, A2D Enabled, Fault Monitor Enabled		1100		µA
INTERNAL MOSFETS						
VOUT to SW1 FET Resistance	R_{DSONQ1}	T_J = 25C		25		mΩ
SW1 to PGND FET Resistance	R_{DSONQ2}	T_J = 25C		35		mΩ
SW2 to PGND FET Resistance	R_{DSONQ3}	T_J = 25C		35		mΩ
VIN to SW2 FET Resistance	R_{DSONQ4}	T_J = 25C		25		mΩ
Cycle By Cycle Current Limit	I_{FET_ILIM}	FET_ILIM=0 Q1, Q2, Q3, or Q4 in any mode	6.5	8.5	10.5	A
		FET_ILIM=1 Q1, Q2, Q3, or Q4 in any mode	7.75	10	12.25	A

LDO

(VIN = 12V, VOUT = 7.6V, T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VREG Regulation Voltage	VREG		2		5.1	V
VREG Regulation Accuracy	$VREG_{ACC}$	At Default Factory Setting	-2		2	%
VREG Dropout	$VREG_{DROPOUT}$	I_{OUT} = 100mA			300	mV
VREG UVLO Threshold	$VREG_{UVLO}$	VREG Falling	84	88	93	%
VREG UVLO Hysteresis	$VREG_{UVLO\_HYST}$			2		%
VREG Current Limit	$VREG_{ILIM}$	V_{VIN} = 12V, VREG = 5V	100	175	250	mA
VREG Current Limit Deglitch	$VREG_{ILIM\_DG}$	In current limit		50		us
VREG Current Limit Off Time	$VREG_{ILIM\_OFF}$	After Deglitch Time		100		ms
VREG Soft Start	$VREG_{SS}$			250		us

THERMAL PROTECTION

(VIN = 12V, VOUT = 7.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Thermal Regulation and Shutdown						
Charger Mode Junction Temperature Regulation Accuracy	T_{REG}	00: Disabled 01: 80 °C 10: 100 °C 11: 120 °C	-20	T_{REG}	+20	°C
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature Increasing		160		°C
Thermal Shutdown Hysteresis	T_{SHUT_HYS}			30		°C

ADC CONVERTER

(VIN = 12V, VOUT = 7.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Total Error	$A2D_{ERROR}$	12 Bit Range			0.5	LSB
Conversion Time	$A2D_{tCONV}$	All 6 Channels			100	ms
Conversion Time	$A2D_{tCONV}$	1 Channel			15	ms
Input Capacitance	$A2D_{CIN}$			5		pF
A2D Full Scale Input EXT_IN	$A2D_{FS}$			2.5		V
A2D Full Scale OUT	$A2D_{VOUT}$	Measurement input at VOUT pin	0		32.5	V
A2D Full Scale VIN	$A2D_{VIN}$	Measurement input at VIN Pin	1.5		25	V
A2D Full Scale OLIM, ILIM	$A2D_{OLIM}$, $A2D_{ILIM}$			2.5		V

LOGIC PIN CHARACTERISTICS – EN, STAT, NIRQ

(VIN = 12V, VOUT = 7.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
EN Input low threshold	V_{ILO}				0.4	V
EN Input high threshold	V_{IHI}		1.25			V
STAT, nIRQ Output Low Voltage	V_{OL}	Sink Current = 5 mA			0.4	V
STAT, nIRQ High Level Leakage Current	I_{OH}	Output = 5V			1	uA

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(VIN = 12V, VOUT = 7.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{ILO}	V_{IO} = 1.8V			0.4	V
SCL, SDA Input High	V_{IHI}	V_{IO} = 1.8V	1.25			V
SDA Leakage Current	I_{OH}	SDA = 5V			1	µA
SDA Output Low	V_{OL}	I_{OL} = 5mA			0.4	V
SCL Clock Frequency	f_{SCL}		0		1000	kHz
SCL Low Period	t_{SCL_LOW}		0.5			us
SCL High Period	t_{SCL_HI}		0.26			us
SDA Data Setup Time	t_{SU}		50			ns
SDA Data Hold Time	t_{HD}		0			ns
Start Setup Time	t_{ST}		260			ns
Stop Setup Time	t_{SP}		260			ns
Capacitance on SCL or SDA PIN	C_{IN}				10	pF
Noise suppression on SCL and SDA	$t_{DEGLITCH}$				50	ns
I²C Timeout Function	t_{out}	Total time required for I²C communication to cause I²C state machine to reset		100		ms

Note1: Comply with I²C timings for 1MHz operation - "Fast Mode Plus".
Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering UV/POR State.
Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the IC.
Note4: IC Address is factory configurable to 7'h24, 7'h66.

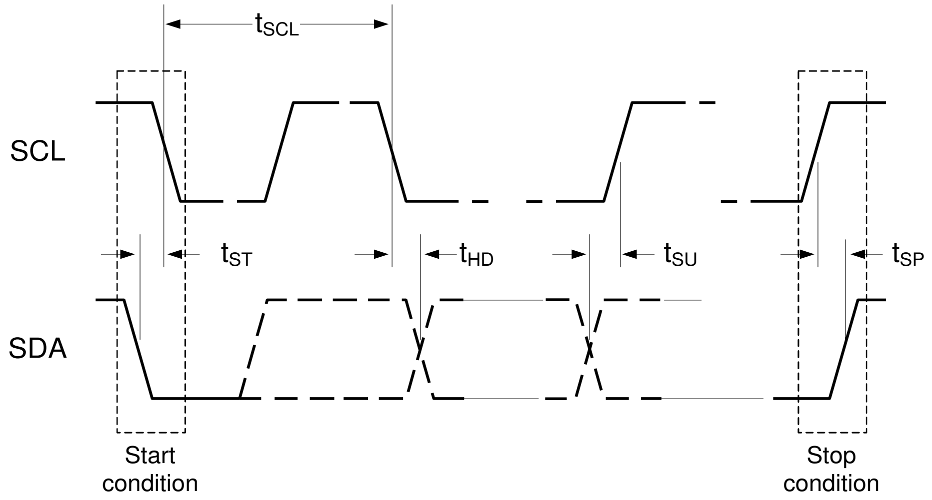


Figure 2: I²C Data Transfer

FUNCTIONAL DESCRIPTION

General

ACT510x is a buck-boost converter with integrated MOSFETs. It provides a high efficiency, low external component count, minimal size buck-boost power solution. Its wide input operating range of 3.9V to 23V allows operation from many input sources. The ACT5101 output voltage is set by internal registers. It has a built in A/D converter. The ACT5102 output voltage is set by an external resistor divider and does not have an A/D converter.

The ACT510x autonomously switches between buck, buck-boost, and boost modes depending on the input and output voltages. It is optimized for minimum quiescent current in shutdown and standby modes. This makes it ideal for battery powered applications.

The ACT510x can be operated in both stand-alone and host-controlled applications. External resistors set the input and output current limit. Using host controlled I²C operation, the user has full control over voltage, current, and fault settings.

I²C operation gives the host full control of operating parameters as well as full knowledge of the operating parameters and fault conditions. A built in ADC provides input voltage, output voltage, input current, output current, and die temperature. The ADC also has one general purpose input to measure an external analog signal.

The ACT510x is highly flexible and contains many I²C configurable functions. The IC's default functionality is defined by its default CMI (Code Matrix Index), but much of this functionality can be changed via I²C. I²C functionality includes OV and UV fault thresholds, switching frequencies, current limits, output voltage, slew rates, softstart time, and more. The CMI Options section shows the default settings for each available CMI option. Contact sales@active-semi.com for additional information about other configurations.

I²C Serial Interface

To ensure compatibility with a wide range of systems, the ACT510x uses standard I²C commands. It supports clock speeds up to 1MHz. The ACT510x always operates as a slave device, and can be factory configured to one of two 7-bit slave addresses. The 7-bit slave address is followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC's slave address

Table 1: ACT510x I²C Addresses

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x24h	010 0100b	0x48h	0x49h
0x66h	110 0110b	0xCCh	0xCDh

The I²C packet processing state machine has a 100ms timeout function for each I²C command. If there is greater than 100ms between a start bit and a stop bit, the ACT510x resets the I²C packet processing and sets the I²C_FAULT bit in register 0x06h. Any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet. The I²C functionality is operational in all states except RESET.

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pull-up resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics. For more information regarding the I²C 2-wire serial interface, refer to the NXP website: http://www.nxp.com.

I²C Registers

The ACT510x has an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, switching frequency, fault thresholds, fault masks, etc. These registers give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult sales@active-semi.com for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected IC behavior.

STATE MACHINE

ACT510x contains an internal state machine with three internal states: RESET, HIZ, and POWER ON.

RESET State

The IC enters the RESET state when power is applied. All registers are reset to their default values. I^2C is not functional in RESET. The IC transitions to the HIZ state when VIN goes above 3.9V

HIZ State

HIZ mode is a low power state with the switching converter disabled. In this mode, I^2C is active and the IC configuration can be changed. The IC enters HIZ from RESET and then either stays in HIZ or transitions to the POWER ON state. Note that the HIZ Register overrides the EN pin settings and may hold the IC in HIZ mode. See the HIZ section for more details.

POWER ON State

In the POWER ON state, the ACT510x transfers power from VIN to VOUT to provide a regulated output voltage. The IC enters this state with the EN pin or the EN_OVERRIDE register. Once in POWER ON, the IC follows the separate POWER ON State Machine. See the POWER ON State machine for more details.

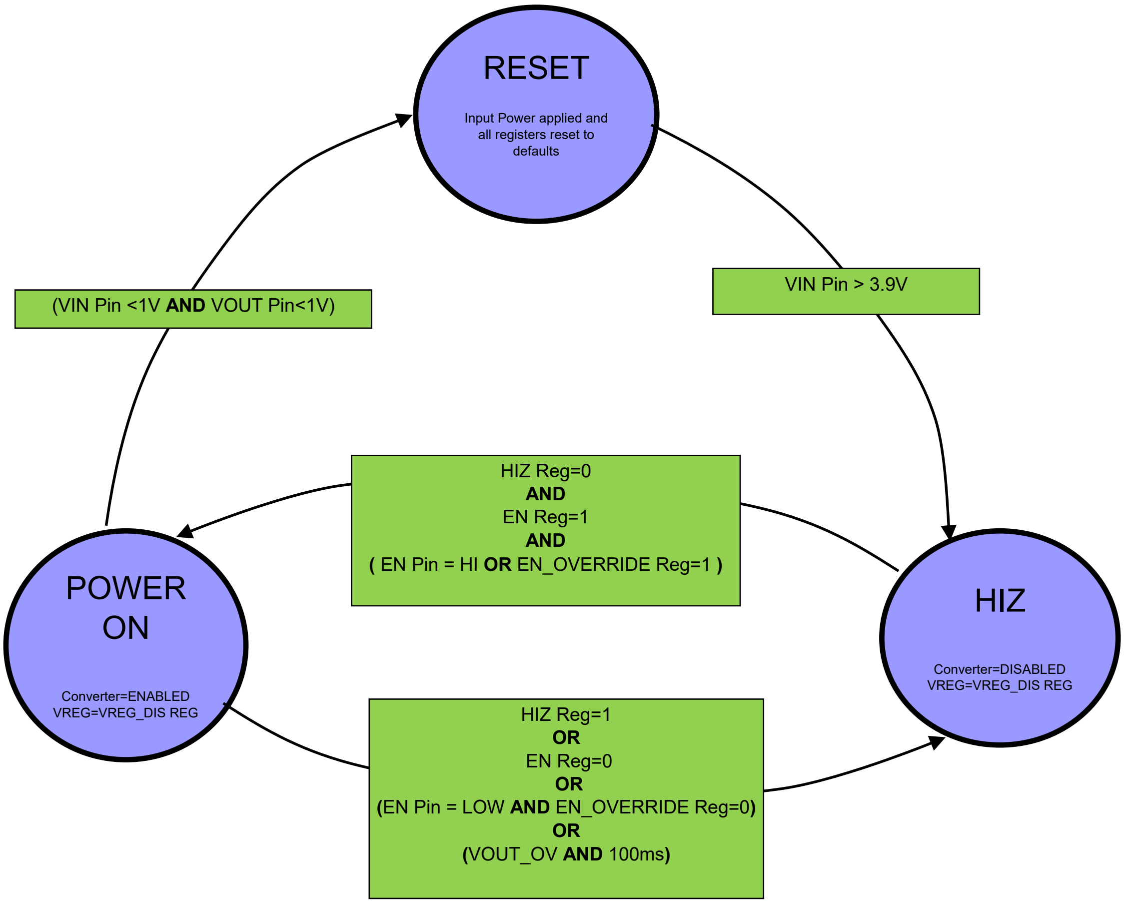


Figure 3: Operating Modes State Machine

POWER ON STATE MACHINE

The ACT510x has a dedicated POWER ON state machine. This state machine handles the startup, normal operation and fault conditions.

Reset State (RST)

The POWER ON state machine always starts from the RST state. All converter operation starts from this state. In this state, the switcher is disabled and the state machine is waiting for all the required conditions to move to the SS state.

After all the following fault conditions are cleared, the IC starts the Enable Delay Timer. This timer is controlled by I²C bit EN_DLY[1:0] in register 0x0Fh. Once the timer has expired, the state machine moves to the SS state.

Reset Faults:

VIN UV Shutdown voltage: This fault is active when the input voltage is lower than the programmed VIN UV Shutdown voltage. This shutdown voltage is set by two I²C registers: VIN_UV in register 0x0Fh and VIN_UV_OFFSET in register 0x1Ah. The actual shutdown voltage is equal to the programmed VIN_UV_OFFSET voltage minus the programmed VIN_UV voltage. This fault self-clears when VIN is higher than the UV Shutdown voltage.

VREG LDO OK – This fault is set when an LDO fault is detected. This includes the 100msec timeout period. This fault automatically clears when the VREG LDO has exited the faulted condition. Note: This fault can be masked to allow the state machine to exit RST while there is a fault on the VREG LDO by using the I²C bit DIS_VREG_FLT in register 0x10 Bit 1.

Watchdog Timer Fault: This fault is active if the watchdog timer is enabled and the timer times out. This fault clears when the watchdog timer is reset or cleared. It can be reset by writing a 1 into the I²C bit WATCHDOG_RESET in register 0x00h. It can be cleared by disabling the watchdog timer by setting I²C bits WATCHDOG[1:0] = 0x00h.

FET Overcurrent Fault: This fault is set if a switching FET exceeds the cycle-by-cycle current limit for 8 (or 16) consecutive cycles. The FET_OC fault is latched. To clear this latch, the IC must exit the POWER ON state and enter HIZ mode. This is typically accomplished by toggling the EN pin or setting the HIZ register to 1.

VIN Overvoltage: This fault is set if VIN exceeds the V_{VIN_OV} voltage, 23.5V. The OV fault self-clears when VIN drops below V_{VIN_OV} and the IC exits the RST state.

Die Thermal Shutdown (TSD): This fault is active when die temperature exceeds the T_{SHUT} (160°C) temperature. This fault self-clears when the die temperature cools down by the temperature hysteresis, T_{SHUT_HYST} (30°C). This fault cannot be cleared or masked. The IC must cool down before exiting the RST state.

Softstart State (SS)

In this state, the IC enables the converter and softstarts the output voltage.

The state machine enters the SS state from the RST state when all faults are cleared. The state machine transitions to the REG state after the output is softstarted an in regulation.

The softstart time is controllable by the I²C bit SS in register 0x0Eh. If a fault occurs during the softstart, the state machine jumps back to the RST state and disables the converter. Once the soft start is done, the IC jumps to the REG state.

Regulation State (REG)

The normal regulation occurs in the REG state. If a major fault occurs during operation the IC will jump back to the reset state and disable the converter. During this state, the converter can be disabled with a light load condition. Additionally, if the output drops below V_{OUT_UVP} (3.0V), the IC will go into a hiccup mode to protect the output in a shorted condition.

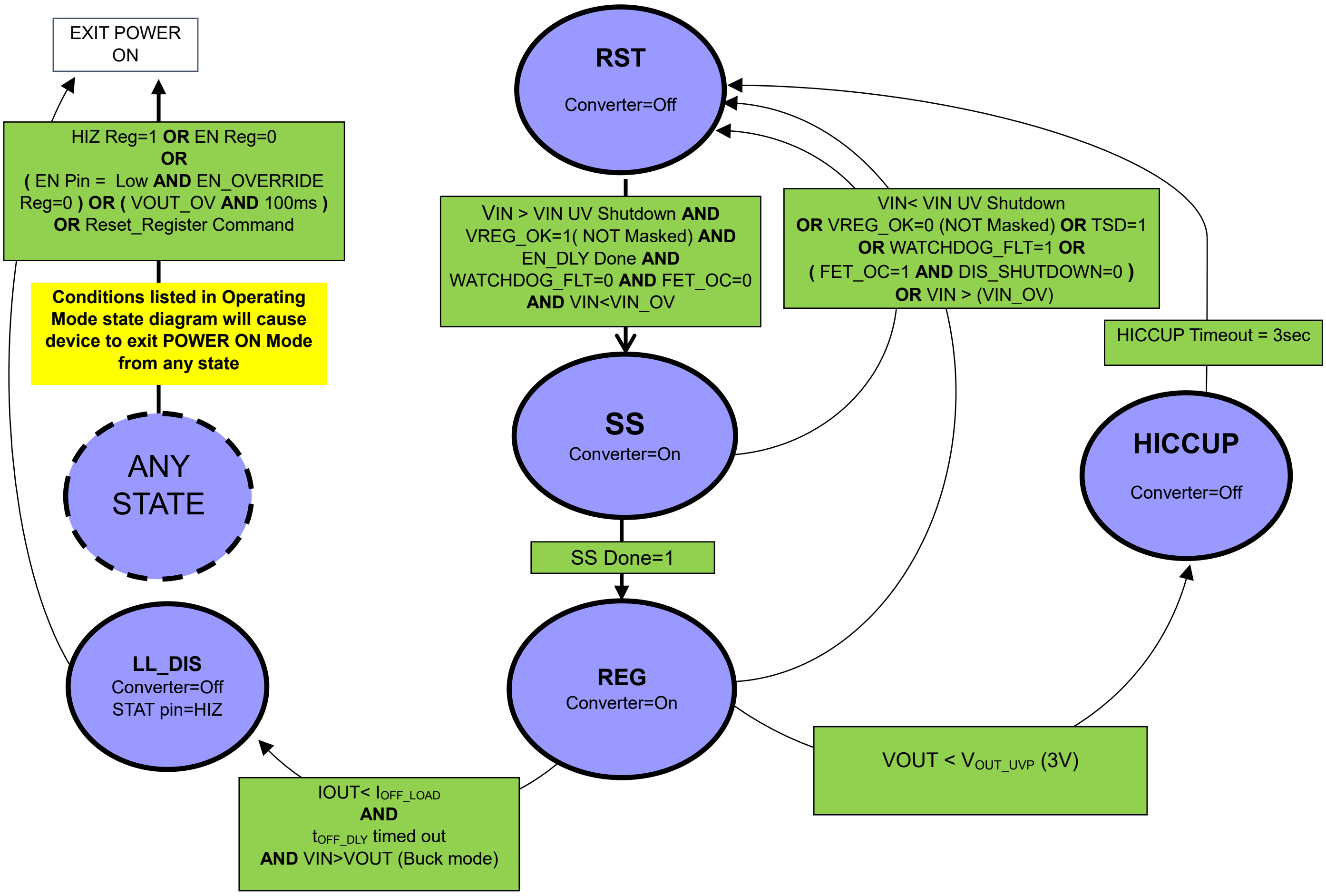


Figure 4: POWER ON State Machine Diagram

Light Load Disable State (LL_DIS)

In the state, the converter is disabled to minimize load on the input supply. This is especially useful in battery applications. It prevents the converter from switching with no load.

The state machine enters LL_DIS when it senses a light load for longer than the light load time out time. This time is set by I^{2}C bit OFF_DLY[1:0] in register 0x0Eh. Note that the converter only enters LL_DIS when operating in buck mode. It does not enter LL_DIS when in boost or buck-boost mode.

The state machine can only exit LL_DIS when the IC exits the POWER ON state with the EN pin or HIZ register.

Hiccup / Vout Fault State (HICCUP)

This state is a fault state that minimizes overall IC power dissipation in extreme output overload conditions.

The state machine enters this state when the output cannot support the load. When the output reaches the maximum programmed output current, it clamps the current and the voltage starts to drop. If the load increases, the output voltage drops even further. If it drops below V_{OUT_UVP} (3.0V), the converter is disabled for 3s. After 3s, it automatically moves to RST and restarts. If there is a fault on the output, this cycle continues until the fault is removed.

PIN FUNCTIONS

VIN

VIN is the ACT510x input power pin. Input voltage sensing is measured at the VIN pin. Connect input bypass capacitors directly between VIN and PGND.

ISRP

ISRP is the positive sense pin for input current sensing. ISRP requires an input RC filter. Refer to the **Input Current Regulation** section for more details. ISRP must be Kelvin connected to the input current sense resistor. Connect the input current sense resistor between ISRP and ISRN.

ISRN

ISRN is the negative sense pin for input current sensing. ISRN requires an input RC filter. Refer to the **Input Current Regulation** section for more details. ISRN must be Kelvin connected to the input current sense resistor. Connect the input current sense resistor between ISRP and ISRN.

SW1, SW2

SW1 and SW2 are the switch nodes for the internal buck-boost converter. SW1 switches between VOUT and PGND when the IC operates in buck-boost and boost modes. SW2 switches between VIN and PGND when the IC operates in buck and buck-boost modes. Connect the inductor between the SW1 and SW2 pins.

HSB1, HSB2

HSB1 and HSB2 provide power to the internal high-side MOSFET gate driver circuitry. Connect a 47nF capacitor from HSB1 to SW1. Connect a 47nF capacitor from HSB2 to SW2.

VOUT

VOUT is the ACT510x output power pin. Connect output bypass capacitors directly between VOUT and PGND.

VINS

VINS is the input voltage sense pin. Kelvin connect input VINS to the input bypass capacitors.

OSRP

OSRP is the positive sense pin for the output current. OSRP requires an input RC filter. Refer to the **Setting Maximum Output Current** section for more details. OSRP must be Kelvin connected to the output current sense resistor. Connect the output current sense resistor between OSRP and OSRN.

OSRN

OSRN is the negative sense pin for the output current. OSRN requires an input RC filter. Refer to the **Setting Maximum Output Current** section for more details. OSRN must be Kelvin connected to the output current sense resistor. Connect the output current sense resistor between OSRP and OSRN.

ILIM

ILIM sets the maximum input current. Connect a resistor between ILIM and AGND to set the current limits. The ILIM current limit can be scaled using I^2C. In some operating conditions, ILIM requires additional RC compensation. Refer to the **Input Current Regulation** section for more details.

OLIM

OLIM sets the maximum output current. Connect a resistor between OLIM and AGND to set the output current limit. The OLIM current limit can be scaled using I^2C. In some operating conditions, OLIM requires additional RC compensation. Refer to the **Setting Maximum Output Current** section for more details.

INTBP

INTBP is the internal bias voltage output pin. INTBP is supplied by an internal linear regulator. Do not power external circuity from the INTBP pin. Connect a 100nF ceramic capacitor between INTBP and AGND.

VREG

VREG is the internal LDO output pin. The internal LDO is programmable between 2V and 5V. Its maximum output current capability 100mA. Connect a 1uF ceramic capacitor between VREG and AGND

EN

EN is the active high enable input. Pulling EN high enables the converter. The EN polarity is configurable via NVM to make it active low or active high. Active high is the default. EN is 5V compliant.

STAT

STAT is an open drain status pin. It indicates the state of the converter. It goes low to indicate the converter is enabled and has a valid output voltage. It goes HIZ to indicate the converter is disabled or that the converter is enabled but in a fault condition.

Table 2: STAT Pin State

State	STAT Output Pin

Output Enabled and Output Valid	LOW
Output Disabled	HIZ
Output Enabled In Fault, Hic-cup, or Light Load states	HIZ

COMP

COMP is the converter compensation pin. Connect the compensation components between COMP and AGND. See the Compensation section for details.

A2D/FB

This is a dual function pin. It is an A2D input for the ACT510x. Connect this pin directly to the voltage to be measured. Note that the ADC full scale input voltage is 2.5V. It is the output voltage feedback pin for the ACT5102.

nIRQ

ACT510x has an interrupt pin to inform the host of any fault conditions. In general, any IC function with a status bit asserts nIRQ pin low if the status changes. The status changes can be masked by setting their corresponding register bits. If nIRQ is asserted low, the fault must be read before the IC deasserts nIRQ. If the fault remains after reading the status bits, nIRQ remains asserted. Refer to the **nIRQ Interrupt Pin (nIRQ)** section for more details.

nIRQ is an open-drain output and should be pulled up to an appropriate supply voltage with a 10kΩ or greater pull-up resistor. nIRQ is 5V compliant

SCL, SDA

SCL and SDA are the I^2C clock and data pins to the IC They have standard I^2C functionality. They are open-drain outputs and each require a pull-up resistor. The pull-up resistor is typically tied to the system's uP IO pins. The pullup voltage can range from 1.8V to 5.0V. SCL and SDA are open drain and are 5V compliant.

NC

This pin is not used and should be connected directly to AGND

PGND

The PGND pin is the buck-boost converters' power ground. The internal FETs connect directly to the PGND pins. The power supply input and output capacitors must connect to the PGND pins.

AGND

The AGND pin is the IC's analog ground pin. It is a "quiet" ground pin that is separate and isolated from the high power, high current carrying PGND ground plane. Connect the non-power components to AGND. AGND must be Kelvin connected to the PGND pin in a single location.

Exposed PAD

The Exposed pad is connected directly to the PGND pins and must be soldered to the top side ground plane. Place thermal vias under the Exposed PAD to improve the IC's thermal performance.

BUCK-BOOST OPERATION

The ACT510x is a monolithic buck-boost converter. Four internal, low resistance, NMOS switches minimize the application circuit size and reduce power losses to maximize efficiency. Internal high side gate drivers, which require only two small external capacitors, further simplify the design process. An advanced switch control algorithm allows the buck-boost converter to maintain constant output voltage regulation with input voltages that are above, equal to, or below the regulated output voltage. The ACT510x automatically transitions between these three operating modes, depending on the input to output voltage ratios.

Power Stage

Figure 5 shows the 4-switch, buck-boost power stage. The converter operates with current mode control. The internal control algorithm reconfigures the IC between a buck, a boost, and a buck-boost topology as needed. This reduces power dissipation and maximizes efficiency because only two FETs switch when in it operates in buck or boost mode. Table 3 shows the switch configuration in each topology. The voltage transition between buck to buck-boost and from buck-boost to boost modes is set by I²C bits XOVER_ADJ_BUCK and XOVER_ADJ_BOOST. With a fixed output voltage and a decreasing input voltage, the IC switches from buck mode to buck-boost mode when VIN – VOUT < XOVER_AJD_BUCK, which is typically 1V. It switches from buck-boost to boost mode when VOUT – VIN > XOVER_ADJ_BOOST, which is typically 2V. These values are set at the factory to optimize efficiency and performance for each CMI.

Q1-Q4 are all internal, N-ch MOSFETs to minimize size and maximize efficiency.

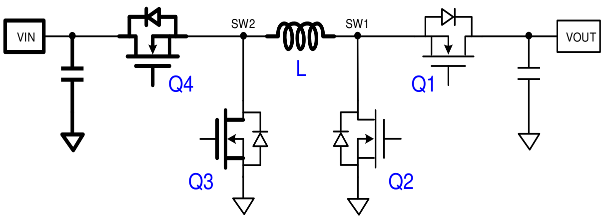


Figure 5: 4-Switch Buck-Boost Power Stage

Table 3: Buck-Boost Switch Configuration

	BUCK	BUCK-BOOST	BOOST
Q1	ON	SWITCHING	SWITCHING
Q2	OFF	SWITCHING	SWITCHING
Q3	SWITCHING	SWITCHING	OFF
Q4	SWITCHING	SWITCHING	ON

Figure 6 shows the power stage operating modes. A typical example of how the converter switches between modes can be explained with an example using a car charger cigarette lighter adapter (CLA) with a 12V input voltage and USB-PD3.0 + PPS compatible output voltages. When the CLA is first plugged in, the ACT510x operates in buck mode to generate 5V out (point A). If the downstream device requests a 9V (point B), the ACT510x still operates in buck mode. If the downstream device requests 12V (point C), the ACT510x operates in buck-boost mode. If the downstream device requests 15V or 20V (points D and E), the ACT510x operates in boost mode.

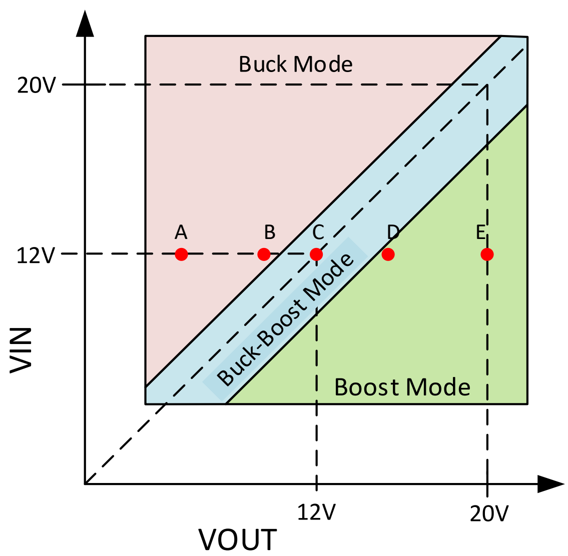


Figure 6: ACT510x Operating Modes

PFM/PWM Operation

At light loads, the ACT510x operates in the PFM (pulse skipping) mode to reduce switching losses. PFM mode can be disabled by the I²C bit DIS_PFM in register 0x10h. Setting this bit to 0 enables PFM mode. Setting this bit to 1 forces PWM mode.

Out-of-Audio Mode

When the IC operates in PFM mode, it reduces the switching frequency. At very light loads, the IC can switch in the audio range. The ACT510x features an Out-of-Audio mode that prevents switching below 31.25kHz. Set the I^2C bit AudioFreqLimit = 1 to enable this feature.

GENERAL DESCRIPTION

Startup

When power is first applied, the ACT510x starts up in HIZ mode and all registers are reset to their default values. The internal LDO, VREG, is enabled and the IC can communicate via I^2C. The ADC can be used at this time. If the EN pin is pulled high, the IC transitions to the POWER ON mode.

VREG LDO

The ACT510x contains a 100mA internal linear regulator that can be used to power other circuity in the system. VREG is enabled when the IC enters HIZ mode and input voltage stays above 3.9V.

I^2C bit VREG_DIS in register 0x01h = 0. This register bit can be programmed Hi or Low from the factory to match system level requirements.

The VREG output voltage is programmable between 2.0V and 5.1V in 100mV steps via I^2C bits VREG[4:0] in register 0x11h.

V_{VREG} = 2.0V + 0.1V * VREG[4:0].

Where VREG[4:0] is the decimal equivalent of the value in this register. For example, if VREG[4:0] = 01101b (13 decimal), the output voltage = 2.0V + 0.1V * 13 = 3.3V.

The VREG input can come from either the VIN pin or the VOUT pin. The ACT510x contains a Smart Diode Selector input that minimizes power dissipation by selecting the lower of these two input sources. The IC powers VREG from the lower of the VIN or VOUT pins. However, if the lower voltage pin cannot provide the headroom needed to regulate VREG, it selects the higher voltage pin.

The Smart Diode Selector can be overridden and manual control can be selected using the I^2C bits VREG_OVERRIDE and VREG_SELECT in register 0x0Bh. When VREG_OVERRIDE = 0, the Smart Diode Selector is active. When VREG_OVERRIDE = 1, the VREG input is determined by VREG_SELECT. When VREG_SELECT = 0, the input is VOUT. When VREG_SELECT = 1, the input is VIN.

If VREG LDO is overloaded or not within spec, the buck-boost converter shuts down, and I^2C fault bit VREG_OC_UVLO in register 0x05h is set to 1.

Additionally, if VREG is held in current limit for more than 90us, it shuts down for 100ms to prevent damage. It tries to restart after 100ms. It continues this cycle until the current limit condition is removed. VREG also contains UVLO detection, which is set to 88% of the programmed output voltage.

If the VREG output is in current limit for 90usec, or the VREG voltage is below the UVLO threshold, the state machine moves to the RST state and the buck-boost converter stops switching. The buck-boost converter can be programmed to ignore an overvoltage or undervoltage fault with I^2C bits DIS_VREG_FLT in register 0x10h. If this bit is set to 1, the IC continues to operate through the fault condition.

VREG requires a high quality, low-ESR, ceramic output capacitor. A 1uF is typically suitable, but this value can be increased without limit. The output capacitor should be a X5R, X7R, or similar dielectric. The effective output capacitance must be greater than 0.7uF to ensure LDO stability.

VREG contains a fixed 250us soft-start to reduce inrush current.

Interrupt Output Pin (nIRQ)

The nIRQ output pin can be used to signal a fault or other system effects. The conditions below can assert the nIRQ pin. All fault conditions can be individually masked using the I^2C nIRQ Control Registers 0x1Eh, 0x1Fh, and 0x20h. To clear the interrupt and de-assert the nIRQ pin, write a 1 into I^2C bit nIRQ_CLEAR in register 0x05h. nIRQ_CLEAR is a self-clearing register bit. nIRQ_CLEAR always returns a 0 when read, even after it is set to 1.

General nIRQ Fault Conditions

1. **Watchdog Expired** - If the watchdog timer expires at any time, it asserts nIRQ. This is a level sensitive function. The watchdog timer must be reset or disabled and a 1 must be written into nIRQ_CLEAR to de-asserted nIRQ.
2. **VREG LDO Overcurrent or Under-voltage Lockout** - Any time the VREG LDO is in overcurrent or under-voltage lockout, nIRQ is asserted. This is a level sensitive function. VREG must be in regulation AND a 1 must be written into nIRQ_CLEAR to deassert nIRQ. If the VREG LDO is in the 100ms shutdown wait period, it will not clear the nIRQ output. This fault is detected in HIZ and POWER ON Modes.

3. **Over Temperature Shut Down** - Any time the die temperature exceeds the T_{SHUT} (160°C) threshold, nIRQ is asserted. This is a level sensitive function. The die temperature must be below the T_{SHUT_HYST} AND a 1 must be written into nIRQ_CLEAR to deassert nIRQ. Die TSD is active in all modes.

4. **FET Overcurrent Fault** – If the IC is disabled from switching because of a FET overcurrent fault, nIRQ is asserted. This is a level sensitive function. This fault is latched, so the latch must cleared by manually going into HIZ Mode AND a 1 must be written into nIRQ_CLEAR to deassert nIRQ.

5. **ADC Data Ready** – If the ADC is enabled, and a conversion is completed, nIRQ is asserted. This is an edge triggered event. A 1 must be written into nIRQ_CLEAR to deassert nIRQ. This is active in all modes when the ADC is enabled.

6. **HIZ Enter** – The ACT510x asserts nIRQ when it enters HIZ mode. This is an edge triggered event. 1 must be written into nIRQ_CLEAR to deassert nIRQ. The IC asserts nIRQ when entering HIZ mode to signal a fault or other condition that might have caused the IC to jump out POWER ON mode un-expectantly.

7. **I²C Fault** – If an I²C command takes more than 100ms between the start bit and the stop bit, nIRQ is asserted. This is an edge triggered event. The I²C state machine clears out any partial data, resets, and waits for another start bit for another I²C command. The state machine clears and restarts the 100ms timer when it receives the next start bit.

8. **VIN Above V_{VIN_OV} (23.5V) -** If VIN is above V_{VIN_OV} (23.5V), nIRQ is asserted. This is a level triggered event. 1 must be written into nIRQ_CLEAR to deassert nIRQ. This fault is detected in both the HIZ state and the POWER ON state.

9. **VIN UV Fault** – If the input voltage at the VINS pin is below the VIN_UV_OFFSET threshold, nIRQ is asserted. This is a level triggered event. VIN must be in the valid range AND 1 must be written into nIRQ_CLEAR to deassert nIRQ.

10. **Light Load Disable State** - Any time the IC enters the LL_DIS state, nIRQ is asserted. This is an edge triggered event. A 1 must be written into nIRQ_CLEAR to deassert nIRQ. The IC does not need to exit the LL_DIS state to de-assert nIRQ.

11. **Hiccup Mode / Vout Fault State** - Any time the IC enters the HICCUP state, nIRQ is asserted. This is an edge triggered event. A 1 must be written into nIRQ_CLEAR to deassert nIRQ.

Die Thermal Regulation

The ACT510x monitors the internal junction temperature, T_J, to avoid overheating When T_J exceeds the maximum thermal regulation limit set by I²C bits TREG [1:0], the IC reduces the output current to lower the die temperature. It effectively reduces the output current limit value. If the load current is not reduced, the output voltage will drop and generate an undervoltage fault. The maximum operating junction temperature is programmable to 80ºC, 100ºC, or 120ºC to allow the user to optimize their system thermal performance. This function can be disabled by setting TREG[1:0] = 00.

HIZ Mode

The ACT510x HIZ mode is a low power state where the buck-boost converter is disabled. The LDO can be enabled or disabled by I²C bit VREG_EN in register 0x01h. The IC always starts up in HIZ mode before going to POWER ON mode. If the IC is not enabled, it stays in the HIZ state indefinitely.

The IC enters HIZ mode from POWER ON mode when the converter is disabled or if a 1 is written into I²C bit HIZ in register 0x00h.

Thermal Shutdown

The ACT510x has thermal shutdown protection that disables the buck-boost converter when IC junction temperature exceeds T_{SHUT} (160°C). The fault register TSD is set to 1 and latched when a TSD fault is detected. The converter restarts automatically after the junction temperature falls below T_{SHUT} - T_{SHUT_HYST}, or approximately 160°C - 30°C = 130°C. After the system restarts, the TSD bit is latched until it is read by I²C.

FET Over Current Protection

The ACT510x closely monitors the HSFETs and LSFETs currents for safe operation. If any FET exceeds the maximum cycle-by-cycle current limit threshold set by I²C bit FET_ILIMIT in register 0x01h, the FET is immediately turned off for that switching cycle. Three thresholds of 5.7A, 8.5A, and 10A are available. If a FET detects the current limit for eight continuous cycles, the buck-boost converter is latched off.

After FET Overcurrent protection is triggered, there are two ways to clear the fault to let the converter resume normal operation. First is to set I²C bit

DIS_OCP_SHUTDOWN = 1 in register 0x01h. It can also be cleared by putting the IC into HIZ mode. Simply toggle the EN pin low and back high.

Overcurrent protection can be disabled by setting the I²C bit DIS_OCP_SHUTDOWN = 1.

Watchdog Timer

The ACT510x contains a watchdog timer to detect system level communication failures. The watchdog timer requires the host to periodically write a 1 into I²C bit WATCHDOG_RESET in register 0x00h. If the host latches up or is unable to perform the write command before the watchdog timer times out, the IC enters FAULT mode and disables the switching converter. The timer resets after each write to WATCHDOG_RESET. WATCHDOG_RESET is an auto-clearing register. It automatically resets back to 0 after it is set to 1.

The timeout value is controlled by I²C bit WATCHDOG[1:0] in register 0x01h. It can be set between 80s and 320s. If the IC is used in stand-alone operation, the watchdog timer can be disabled by setting WATCHDOG[1:0] = 00.

WATCHDOG is always disabled in HIZ Mode and cannot be enabled in HIZ. In addition, the timer is reset to 0 when entering HIZ mode and automatically starts counting when exiting HIZ mode.

CONVERTER OPERATION

Enable / Disable

The ACT510x is enabled and disabled from HIZ mode. When enabled, the converter operates in the POWER ON mode. When disabled, the IC operates in the HIZ mode. The EN pin is the typical method to enable and disable the IC. If I²C on/off control is required, the system microprocessor can enable and disable the IC via the EN and EN_OVERRIDE bits in register 0x0Eh. Set EN_OVERRIDE = 1 to override the EN pin input. Then set EN = 1 to enable the converter and set EN = 0 to disable the converter. Figure 7 shows both the hardware and I²C conditions required to enter turn the converter on.

Note that in all cases, the I²C bit HIZ in register 0x00h must be = 0 to enter enable the converter. When HIZ = 1, the IC is forced into HIZ mode.

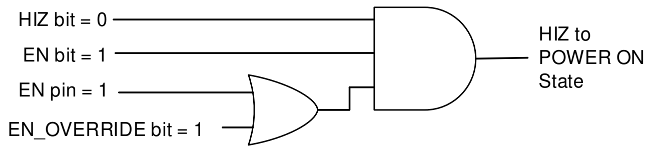


Figure 7: Conditions to Enter the POWER ON State from the HIZ State

After the IC is enabled and in the POWER ON mode, the conditions to exit POWER ON mode (disable the converter) change. When the converter is disabled, the IC state machine must go to HIZ mode. There are several ways to transition from POWER ON mode to HIZ mode.

1. Set the I²C HIZ bit = 1
2. Set the I²C EN bit = 0
3. Pull the EN pin LOW and set the I²C EN_OVERRIDE bit = 0.
4. The IC also exits POWER ON mode if there is an overvoltage condition for longer than 100ms.

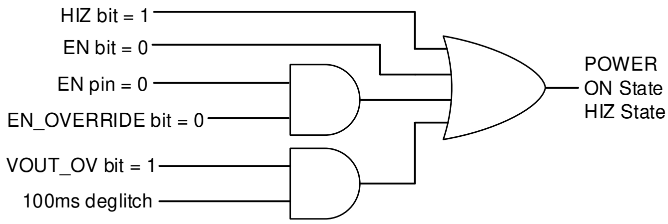


Figure 8: Conditions to Enter HIZ State from POWER ON State

Output Voltage Setting

The output voltage is programmable between 2.96V and 23.42V in 20mV steps via by I²C bits VOUT[9:0] in registers 0x13h and 0x14h.

$$V_{OUT} = 2.96V + 20mV * VOUT[9:0]$$

Where VOUT[9:0] is the decimal equivalent of the value in this register. For example, if VOUT[9:0] = 0111000100b (452 decimal), the output voltage = 2.96V + 0.02V * 452 = 12.00V.

When changing from one output voltage to another, the slew rate is programmable between 1V/ms and 0.1V/ms by I²C bits OUTPUT_SLEW[1:0] in register 0x10h. This allows the output to conform to QC2.0/QC3.0/USB PD/USB PD + PPS functions for higher output voltages.

The input voltage must always stay above the minimum allowable input voltage. This voltage is defined by registers VIN_UV_OFFSET in register 0x1Ah and VIN_UV in register 0x0Fh. The minimum allowable input voltage is the VIN_UV_OFFSET voltage minus the VIN_UV voltage. If the input voltage drops below this value, the IC turns off the output and goes to the RST state.

Active Discharge

When changing the output voltage to a higher level, the switcher ramps the output voltage by the programmed slew rate. When the output voltage is programmed from a higher to a lower voltage, the voltage drops at a rate determined by the output capacitance and the load current. To minimize the fall time in no-load conditions, the ACT510x can provide a 70mA sink when the output is transitioning to a lower output voltage. Enable this feature by writing 1 into I²C bit PULLDOWN_RAMP. The 70mA load turns on until the output voltage goes into regulation.

Enable Delay

Once the IC has the valid conditions for startup, the Enable Delay timer is enabled. The timer options allow a 0ms to 1s delay. The startup delay is controlled by the I²C bits EN_DLY[1:0]

Soft Start

After the Enable Delay has completed, the IC starts the output using a soft start function programmable by the I²C bits SOFT_START in register 0x0Eh. The softstart time is independent of the output voltage setting.

Setting Maximum Output Current

The maximum output current, I_{OUT_MAX}, is set by a combination of a current sense resistor, an OLIM resistor, and a scaling factor defined by I²C bits CC[6:0] in register 0x17h. The maximum allowable output current is 5A. Figure 9 shows the hardware circuitry that sets I_{OLIM}. I_{OLIM} is the maximum output current set by hardware. The actual output current limit, I_{OUT}, can be scaled from 1% to 100% of I_{OLIM} in 1% steps. The following equation defines the final maximum output current.

$$I_{OUT\_MAX} = I_{OLIM} * CC[6:0]$$

Where I_{OLIM} is the hardware programmed output current limit and CC[6:0] is the scaling factor. CC[6:0] is the decimal equivalent value in this register. For example, if I_{OLIM}, is programmed to 4A and CC[6:0] = 1001011b (75% decimal), the final maximum output current = 4A * 0.75 = 3A.

Note that CC[6:0] is a 7 bit register and can be programmed between 0x00h and 0x7Fh (0% and 127%). If a value of 0x00h is written to the register, the register retains 0x00h, but the IC sets the maximum output current to 1%. If a value above 0x64h (100%) is written to the register, the IC retains the written value, but sets the maximum output current to 100%.

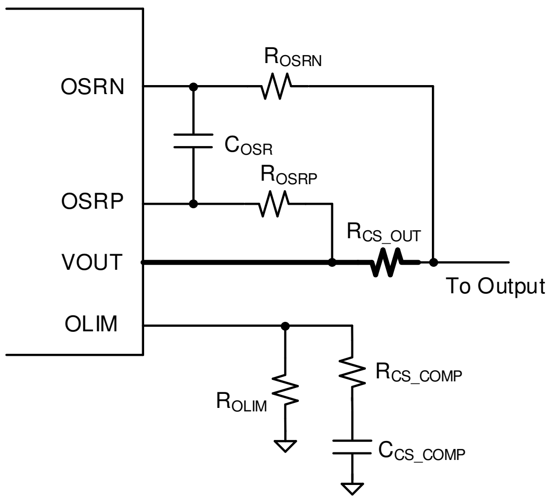


Figure 9: Output Current Limit Circuitry

The current sense resistor and OLIM resistor set the I_{OLIM} current.

$$I_{OLIM} = \frac{1000\frac{V^2}{A}}{R_{OLIM} * R_{CS\_OUT}}$$

Where R_{OLIM} is the resistor from the OLIM pin to AGND in ohms and R_{CS_OUT} is the current sense resistor value in ohms. The term 1000V^2/A is a constant with the units volts^2/Ampere.

The current sense resistor, R_{CS_OUT}, value should be chosen to give a maximum current sense voltage between 20mV and 50mV. 50mV is the absolute maximum allowable voltage. Using lower voltages reduces the resistor's power dissipation, but decreases accuracy. At lower output currents, additional RC compensation must be placed in parallel with R_{OLIM}. Table 4 gives recommended resistor values for different values of I_{OLIM} current. Contact sales@active-semi.com for compensation information if other configurations are required.

Table 4: Output Current Component Selection

Switching Frequency = 125kHz				
I_{OLIM} (A)	R_{CS} (mΩ)	R_{OLIM} (kΩ)	R_{CS_COMP} (kΩ)	C_{CS_COMP} (nF)
5	10	20	NA	NA
4	10	25	NA	NA
3	10	33	10	330
2	10	50	10	330
1.5	20	33	10	330
1	20	50	10	330
Switching Frequency = 250kHz, 500kHz, 1MHz				
I_{OLIM} (A)	R_{CS} (mΩ)	R_{OLIM} (kΩ)	R_{CS_COMP} (kΩ)	C_{CS_COMP} (nF)
5	10	20	NA	NA
4	10	25	NA	NA
3	10	33	NA	NA
2	10	50	15	56
1.5	20	33	10	100
1	20	50	10	100

To eliminate noise in the current measurement circuit, the current sense voltage must be filtered. The recommended values are R_{OSRP} = R_{OSRN} = 30.1ohm and C_{OSR} = 100nF. These values can be scaled up or down, but R_{OSRP} must be between 20ohm and 50ohm, and the resulting filter cutoff frequency must be between 20kHz and 30kHz.

The actual output current can be measured with the OLIM pin. The OLIM voltage is directly proportional to the output current. The following equation calculates the actual output current.

$$I_{OUT} = I_{OLIM}\frac{V_{OLIM}}{2V}$$

Where I_{OLIM} is the hardware programmed 100% output current limit in amps and V_{OLIM} is the voltage measured at the OLIM pin.

Constant Output Current Regulation

When the output current tries to increase above I_{OUT_MAX}, the converter transitions from constant output voltage regulation to constant output current regulation. The output voltage will drop to maintain a constant output current.

I²C bit OUTPUT_CC in register 0x20h indicates if the converter is operating in constant voltage or current regulation. When this bit = 0, the IC is regulating in constant voltage mode. When this bit = 1, the IC is regulating in constant current mode. If the output drops below 3V, the IC assumes an output fault has occurred and disables the output for 3s. This is the HICCUP state. After 3s, the state machine goes to RST and restarts. If a short or high current fault is present after the restart, the IC cycles back to HICCUP and RST. This cycle continues indefinitely until the converter is disabled or the fault is removed.

Input Current Regulation

At all times during operation, the IC monitors the current across the input current sense resistor (ISRP and ISRN) to provide input current protection. This provides compatibility with USB input current limitations and avoids over loading weak input voltage sources.

Figure 10 shows that the input current limiting circuitry is identical to the output current setting circuitry. When the input current reaches current limit, the ACT510x control circuitry starts regulating the maximum input current. This can cause the output voltage to drop if the load resistance continues to decrease. The maximum allowable input current is 5A. The actual input current limit, I_{IN_LIM} can be scaled to 150% or 200% of I_{ILIM}. The following equation defines the final input current limit.

$$I_{IN\_LIM} = I_{ILIM} * INPUT\_ILIM[1:0]$$

Where I_{ILIM} is the hardware programmed current limit and INPUT_ILIM[1:0] is the scaling factor. INPUT_ILIM can be 150% or 200% of I_{ILIM}. When INPUT_ILIM is programmed to 00, input current limiting is disabled.

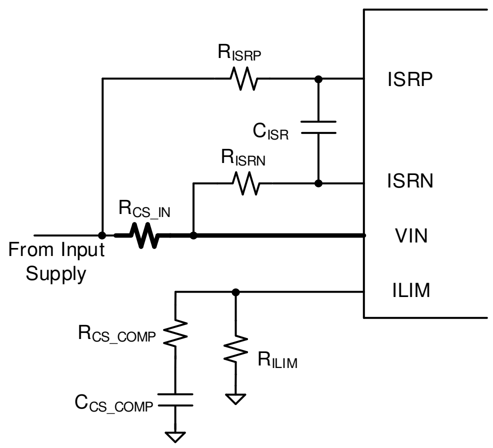


Figure 10: Input Current Circuitry

The current sense resistor and ILIM resistor set the I_{ILIM} current.

$$I_{ILIM} = \frac{1000\frac{V^2}{A}}{R_{ILIM} * R_{CS\_IN}}$$

Where R_{ILIM} is the resistor from the ILIM pin to AGND and R_{CS_IN} is the current sense resistor value in ohms. The term 1000V^2/A is a constant with the units volts^2/Ampere.

The current sense resistor, R_{CS_IN}, has the same limitations as R_{CS_OUT}. At lower maximum input currents, additional RC compensation must be placed in parallel with R_{ILIM}. Table 4 is also valid for the input current limit circuitry.

The input current limit circuitry, $R_{ISRP} = R_{ISRN} = 30.1$ohm and C_{ISR} also have the same input filter requirements as the output current circuitry.

The actual input current can also be externally measured with the ILIM pin. The ILIM voltage is directly proportional to the input current. The following equation calculates the actual input current.

$$I_{IN} = I_{ILIM}\frac{V_{ILIM}}{2V}$$

Table 5: I²C Input Current Limit Setting

INPUT_ILIM[1:0] Register Setting	Input Current Scaling Factor
00	Disabled
01	150% of I_{ILIM}
10	200% of I_{ILIM}
11	150% of I_{ILIM}

VOUT Over-Voltage Protection

To detect a possible plug in of a higher voltage supply on VOUT, the IC detects an overvoltage condition on VOUT and immediately stops switching. The output overvoltage threshold is fixed at 108% of the programmed output voltage. If the OV condition lasts for more than 100ms, the IC exits POWER ON Mode and enters HIZ Mode.

Cord Compensation

ACT510x provides cord compensation at the output. This feature compensates for system level voltage drops due to PCB, connector, and wiring resistances. These resistances reduce the output voltage at the load.

The ACT510x features Cord Compensation which allows the user to compensate for these system level resistances by increasing the voltage regulation set point proportional to the output current. The output voltage increases linearly with increasing load current. The I²C CORD_COMP[1:0] bits in register 0x0F set the Cord Comp value.

The Cord Compensation value is normalized to R_{CS_OUT} = 10mΩ and a 2.4A load current. It scales linearly with changes in current sense resistance or load current.

$$V_{Cord\_Comp} = V_{CORD\_COMP} * \frac{I_{OUT}}{2.4A} * \frac{R_{CS\_OUT}}{0.01\Omega}$$

Where V_{CORD_COMP} is the I²C Cord Compensation value of 100mV, 200mV, or 300mV per Table 6, I_{OUT} is the actual output current in Amperes, and R_{CS_OUT} is the current sense value in Ohms.

Table 6: Cord Comp Setting

CORD_COMP[1:0] Setting	Cord Comp Value	Equivalent System Resistance
00	0 (Disabled)	0mΩ
01	100mV	41.7mΩ
10	200mV	83.3mΩ
11	300mV	125.0mΩ

Light Load Disable

The ACT510x includes a Light Load Disable function. This function maximizes battery life when the IC is powered from a battery. It turns off the output and puts the IC into HIZ mode when the load drops very low. This condition typically happens when the ACT510x output supplies power to a charging portable device. When the portable device is fully charged, the output current drops to 0A. Light Load Disable minimizes battery current (the input to the ACT510x) consumption and extends battery life when the output is not needed.

Light Load Disable is available when the IC is operating in buck mode, VIN is higher than VOUT by a minimum of 0.5V, and the Output Voltage is less than 6V. Enable Light Load Disable by setting I²C bit OFF_LOAD_EN in register 0x0Eh = 1. Setting this bit = 0 disables the feature. The minimum current is set to 5mA typical. The current must be low for longer than the time set in I²C bit OFF_DLY[1:0]. This time can programmed to 10s, 20s, or 30s.

Once the state machine has detected a light load condition, it enters the LL_DIS state. The IC must exit POWER ON mode and re-enter POWER ON mode to restart the converter. This is typically accomplished by toggling the EN pin, but can also be accomplished via I²C.

Output Voltage DVS (ACT5101 only)

The ACT5101 is ideally suited for many industry standard charging protocols such as USB PD3.0, QC2.0, QC3.0, etc. This includes USB PD3.0 + PPD. To achieve this compatibility, the output voltage can be dynamically changed. VOUT in can be dynamically changed by writing to the VOUT[10:0] register. The OUTPUT_SLEW[1:0] register controls the slew rate between settings when the VOUT[10:0] is changed. When the voltage is increased, the internal ramp and regulator can compensate and increase the voltage. However, when the voltage is decreased, and there is no external load on the output, the output voltage may not decrease fast enough to the meet the requirements. To speed up the transition time from higher to lower output voltages, set PULLDOWN_RAMP=1. This turns on an internal 70mA load when the output voltage is stepped to a lower voltage using the VOUT[10:0] register. The 70mA load turns off when the voltage goes into regulation.

The ACT5101 also has a pulldown current that goes active during any output overvoltage condition. Enable this feature by setting the I^2C bit PULLDOWN_OV = 1.

POWER ON State Machine Status

The I^2C bits STATUS[2:0] in register 0x20h provide the user with real time status of the POWER ON state machine. These bits are always 000 when the IC is not in POWER ON mode.

Table 7: POWER ON State Machine Status

STATUS[2:0]	State Machine State
000	RST
001	SS
010	REG
011	HICCUP
100	LL_DIS
101-111	Not Valid

Frequency

The ACT510x can operate at 125kHz, 250kHz, 500kHz, or 1MHz. The switching frequency is set by the factory and is not user programmable. The default frequency is 500kHz to give the best tradeoff between size and efficiency, but can be programmed to the other options with a custom CMI. Note that the external component value requirements change with different switching frequencies. Contact sales@active-semi.com for additional information about other configurations.

Input Capacitor Selection

The input is connected directly to the VIN pins. The capacitor should be dedicated high quality, low-ESR, ceramic capacitor that is optimally placed to minimize the power routing. 22uF to 47uF capacitors are typically acceptable, but the final value is application dependent. Choose the input capacitor value to keep the input voltage ripple less than ~50mV. The C_{IN} input capacitor can be increased without limit.

$$C_{IN} = I_{OUT} * \frac{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{F_{SW} * V_{ripple}} \quad \text{Equation 6}$$

Where C_{IN} is the input capacitance in uF, I_{OUT} is the output current in Amperes, V_{OUT} is the output voltage in volts, V_{IN} is the input voltage in volts, F_{SW} is the switching frequency in Hz, and V_{ripple} is the maximum allowable input voltage ripple in volts.

If the input source is a battery, no additional capacitance is needed. If the input source is a power supply rail, adding an additional 100uF bulk electrolytic capacitor is recommended.

The ceramic capacitor PCB placement is critical. Refer to the Layout Guidelines selection and to the EVK layout for details.

Be sure to consider the input capacitor's DC bias effects. A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics is not recommended. Input capacitor placement is critical for proper operation. The input capacitor must be placed as close to the IC as possible. The traces from VBAT to the capacitor and from the capacitor to PGND should as short and wide as possible.

Output Capacitor Selection

The output capacitors are connected directly to VOUT. The output capacitance must be a combination of ceramic and bulk capacitance.

Table 8 gives the required capacitor values for stability. Note that the table has two output capacitor options: Standard Capacitance and Minimum Capacitance. The Standard Capacitance design requires more overall capacitance, but places no restriction on the bulk capacitor ESR. The Minimum Capacitance design results in an overall smaller design, but places restrictions on the ESR. The capacitor values can be increased without limit.

Note that the Ceramic and Bulk capacitor values are recommended "Capacitor Values". When choosing the ceramic capacitors, use X5R or X7R dielectrics and be sure to consider the capacitor's tolerance and DC bias