
Chipsmall
深圳市津利帝科技有限公司
Geelead Technology Limited
Chipsmall
采购部

ACT522

Rev 1, 26-Feb-16

ActiveQR™ Quasi-Resonant PWM Controller

FEATURES

- **DCM and Quasi-Resonant Operation**
- **QC2.0 Output Current Foldback Control at 5V, 9V and 12V**
- **High VDD Sustain Voltage for QC2.0 Wide Output Range Operation**
- **Adjustable up to 90kHz Switching Frequency**
- **Integrated Patented Line Compensation**
- **Built-in Soft-Start Circuit**
- **Line Under-Voltage, Thermal, Output Over-voltage, Output Short Protections**
- **Current Sense Resistor Short Protection**
- **Transformer Short Winding Protection**
- **30mW Standby Power**
- **Complies with Global Energy Efficiency and CEC Average Efficiency Standards**
- **Sop-8 Packages**

APPLICATIONS

- **AC/DC Adaptors/Chargers for Cell Phones, Cordless Phone, PDAs, E-books**
- **Adaptors for Portable Media Player, DSCs, Set-top boxes, DVD players, records**
- **Linear Adapter Replacements**

GENERAL DESCRIPTION

The ACT522 is a high performance peak current mode PWM controller. ACT522 applies *ActiveQR™* and frequency foldback technique to reduce EMI and improve efficiency. ACT522's maximum design switching frequency is set at 100kHz. Very low standby power, good dynamic response and accurate voltage regulation is achieved with an opto-coupler and the secondary side control circuit.

The idle mode operation enables low standby power of 30mW with small output voltage ripple. By applying frequency foldback and *ActiveQR™* technology, ACT522 increases the average system efficiency compared to conventional solutions and exceeds the latest ES2.0 efficiency standard with good margin.

ACT522 integrates comprehensive protection. In case of over temperature, over voltage, short winding, short current sense resistor, open loop and overload conditions, it would enter into auto restart mode including Cycle-by-Cycle current limiting.

ACT522 is to achieve no overshoot and very short rise time even with big capacitive load with the built-in fast and soft start process.

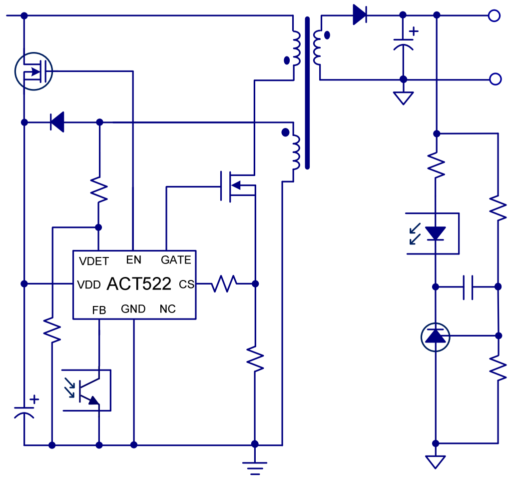
In low line full load condition, ACT522 is able to be designed to work in first valley turn on DCM mode to meet different types of applications. Quasi-Resonant (QR) operation mode can effectively improve efficiency during DCM operation, and reduce the EMI noise and further reduce the components in input filter.

ACT522 uses an opto-coupler feedback architecture to provide accurate constant voltage even at low loads, constant current (CV/CC) regulation. Integrated line and primary inductance compensation circuitry provides accurate constant current operation despite wide variations in line voltage and primary inductance.

ACT522 is idea for QC2.0 12V/1.25A;9V/1.67A; 5V/2A application.

Figure 1:

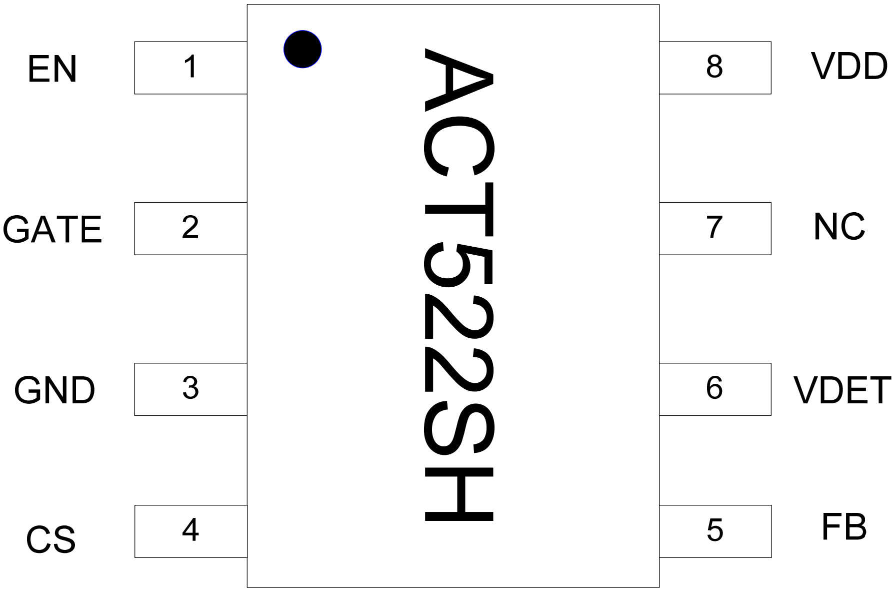
Simplified Application Circuit



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING METHOD	TOP MARK
ACT522SH-T	-40°C to 85°C	SOP-8	8	TUBE & REEL	ACT522SH

PIN CONFIGURATION



SOP-8
ACT522SH

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	EN	Connect this to the gate of the N-depletion FET.
2	GATE	Gate Drive. Gate driver for the external MOSFET transistor.
3	GND	Ground.
4	CS	Current Sense Pin. Connect an external resistor (R_{CS}) between this pin and ground to set peak current limit for the primary switch.
5	FB	Feedback Pin. Connect this pin to optocouplers's collector for output regulation.
6	VDET	Valley Detector Pin. Connect this pin to a resistor divider network from the auxiliary winding to detect zero-crossing points for valley turn on operation.
7	NC	Not Connect.
8	VDD	Power Supply. This pin provides bias power for the IC during startup and steady state operation.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
FB, CS, VDET to GND	-0.3 to + 6	V
VDD, GATE to GND	-0.3 to + 45	V
Maximum Power Dissipation (SOP-8)	0.625	W
Maximum Continuous VDD Current	100	mA
Operating Junction Temperature	-40 to 150	˚C
Junction to Ambient Thermal Resistance (θ_{JA})	160	˚C/W
Storage Temperature	-55 to 150	˚C
Lead Temperature (Soldering, 10 sec)	300	˚C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 32V, L_M = 0.47mH, R_{CS} = 0.91Ω, V_{OUT} = 12V, N_P = 40, N_S =6, N_A =15, T_A = 25°C, unless otherwise specified.)

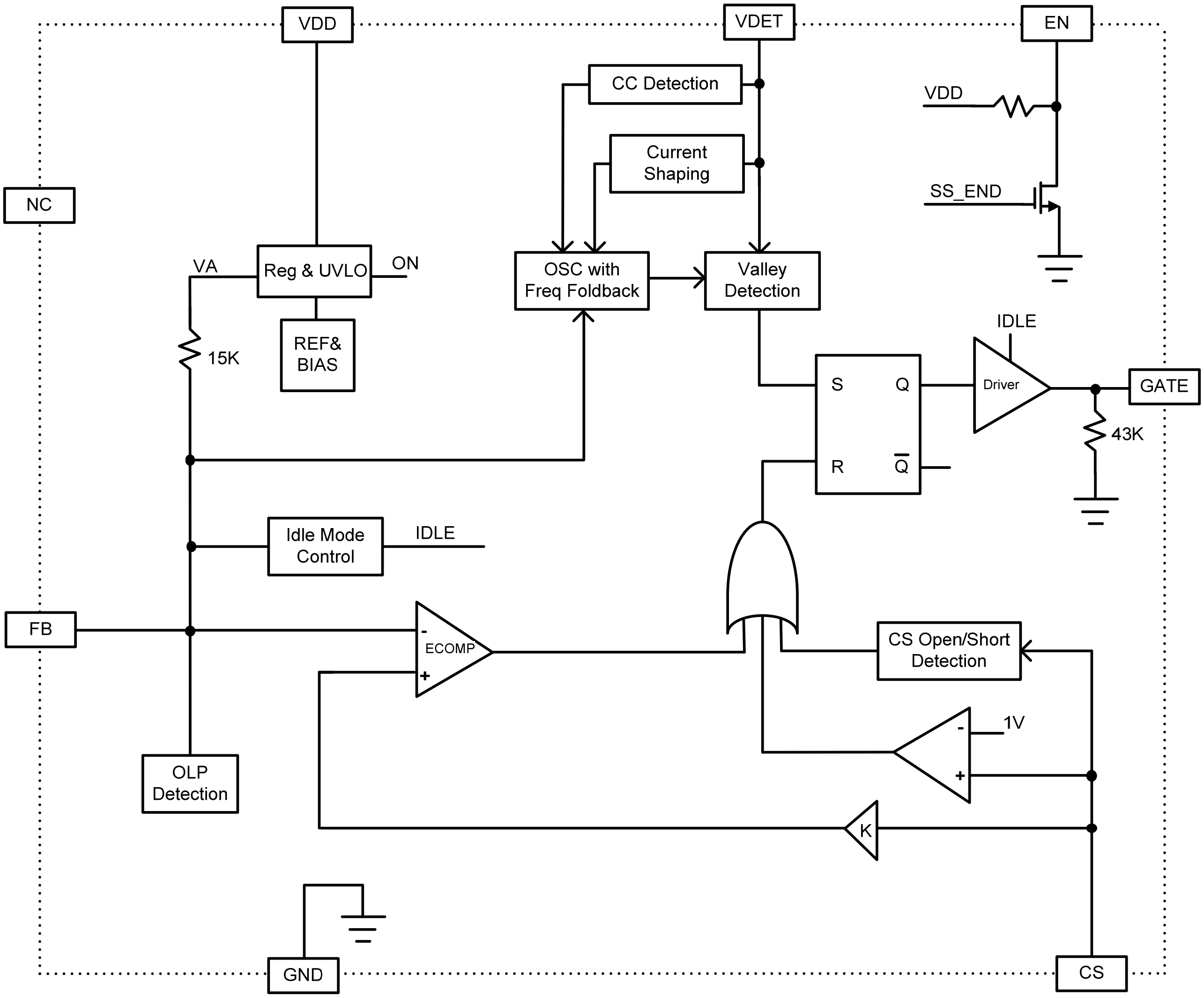
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
VDD Turn-On Voltage	V_{DDON}	V_{DD} Rising from 0V	16	18	20	V
VDD Turn-Off Voltage	V_{DDOFF}	V_{DD} Falling after Turn-on	6.5	7.0	7.5	V
VDD Over Voltage Protection	V_{DDOVP}	V_{DD} Rising from 0V	43	44	45	V
Start Up Supply Current	I_{DDST}	VDD=16V, before VDD Turn-on (with N-depletion FET)			10	µA
IDD Supply Current	I_{DD}	V_{DD} = 18V, after VDD Turn-on ,FB floating		0.5	0.8	mA
IDD Supply Current at Standby	I_{DDSTBY}	FB = 1.9V		0.2	0.3	mA
IDD Supply Current at Fault	$I_{DDFAULT}$	Fault mode, FB Floating		250		µA
Feedback						
FB Pull up Resistor	R_{FB}			15		kΩ
CS to FB Gain	A_{CS}			2		V/V
VFB at Max Peak Current	V_{FBPEAK}			3 + V_{BE}		V
FB Threshold to Stop Switching	V_{FBBM1}			1.9		V
FB Threshold to Start Switching	V_{FBBM2}			1.95		V
Output Overload Threshold	V_{FBOLP}			3.75		V
OverLoad/Over Voltage Blanking Time	$T_{OVBLANK}$			400		ms

ELECTRICAL CHARACTERISTICS CONT'D

(V_{DD} = = 32V, L_M = 0.47mH, R_{CS} = 0.91Ω, V_{OUT} = 12V, N_P = 40, N_S =6, N_A =15, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Limit						
CS Current Limit Threshold	V_{CSLIM}		0.936	0.955	0.974	V
Leading Edge Blanking Time	$T_{CSBLANK}$		240	300	360	ns
GATE DRIVE						
Gate High Level current source	I_{OG_ON}	V_{GATE} = 5V		23		mA
Gate Rise Time	T_{RISE}	VDD = 10V, CL = 1nF		250	350	ns
Gate Falling Time	T_{FALL}	VDD = 10V, CL = 1nF		50	100	ns
Gate High Level ON-Resistance	R_{ONHI}	I_{SOURCE} = 30mA		20		Ω
Gate Voltage	V_{GATE}	VDD = 10V, CL = 1nF		11		V
Max Gate Voltage	$V_{G.MAX}$	VDD = 45V, Switching			14	V
Gate Leakage Current		GATE = 25V, before VDD turn-on			1	µA
Oscillator						
Maximum Switching Frequency	f_{MAX}	V_{DET} = 2.2V		90		kHz
Switching Frequency Foldback	f_{MIN}	FB = 2.3V+V_{BE}		$f_{MAX}/3$		kHz
Maximum Duty Cycle	D_{MAX}		65	75		%
Frequency Transform Point1	f_{SW1}	$1.2 < V_{DET} \leq 2V$		90		kHz
Frequency Transform Point2	f_{SW2}	$V_{DET} \leq 1.2V$		75		kHz
Valley Detection						
ZCD Threshold Voltage	$VDET_{TH}$			100		mV
Valley Detection Time Window		No valley detected, force turn-on main switch		2.5		µs
VDET Leakage Current				1		µA
Protection						
CS Short Waiting Time				2.5		µs
CS Short Detection Threshold				0.1	0.15	V
CS Open Threshold Voltage				2.5		V
Abnormal OCP Blanking Time				150		ns
Line UVLO	$I_{VDETUVLO}$			60		µA
Line OVP	$I_{VDETOVP}$			2.4		mA
VDET Over Voltage Protection	$V_{DETVOOVP}$			2.75		V
VDET Vo Short Threshold	$V_{DETVOshort}$			0.45		V

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

ACT522 is a high performance peak current mode low-voltage PWM controller IC. The controller includes the most advance features that are required in the adaptor applications up to 30 Watt. Unique fast startup, frequency foldback, QR switching technique, accurate peak current line compensation, idle mode, short winding protection, OCP, OTP, OVP and UVLO are included in the controller.

Startup

VDD is the power supply terminal for the ACT522. During startup, the N-depletion FET will be turned ON. Once VDD reaches VDDON voltage, the ACT522 will start switching and the N-depletion FET is turned OFF. To startup with a big capacitive load, a fast startup sequence is implemented in ACT522. To eliminate the initial current stress on the MOSFET, a soft startup sequence is implemented in ACT522.

During startup period, the IC begins to operate with minimum Ippk to minimize the switching stresses for the main switch, output diode and transformers. And then, the IC operates at maximum power output to achieve fast rise time. After this, V_{OUT} reaches about 90% V_{OUT}, the IC operates with a 'soft-landing' mode(decrease Ippk) to avoid output overshoot.

Constant Voltage (CV) Mode Operation

In constant voltage operation, the ACT522 regulates its output voltage through secondary side control circuit . The output voltage information is sensed at FB pin through OPTO coupling. The error signal at FB pin is amplified through TL431 and OPTO circuit. When the secondary output voltage is above regulation, the error amplifier output voltage decreases to reduce the switch current. When the secondary output voltage is below regulation, the error amplifier output voltage increases to ramp up the switch current to bring the secondary output back to regulation. The output regulation voltage is determined by the following relationship:

$$V_{OUTCV} = V_{REF\_TL431} \times \left(1 + \frac{R_{F1}}{R_{F2}}\right) \qquad (1)$$

where R_{F1} (R15) and R_{F2} (R16) are top and bottom feedback resistor of the TL431.

Staged Constant Current (CC) Mode Operation

When the secondary output current reaches a level set by the internal current limiting circuit, the ACT522 enters current limit condition and causes the secondary output voltage to drop. As the output voltage decreases, so does the flyback voltage in a proportional manner. An internal current shaping circuitry adjusts the switching frequency based on the flyback voltage so that the transferred power remains proportional to the output voltage, resulting in a constant secondary side output current profile. The energy transferred to the output during each switching cycle is ½(LP × ILIM^2) × η, where LP is the transformer primary inductance, ILIM is the primary peak current, and η is the conversion efficiency. From this formula, the constant output current can be derived:

$$I_{OUTCC} = \frac{1}{2} \times L_p \times \left(\frac{V_{CS}}{R_{CS}}\right)^2 \times \left(\frac{\eta \times f_{SW}}{V_{OUTCV}}\right) \qquad (2)$$

where f_{SW} is the switching frequency and V_{OUTCV} is the nominal secondary output voltage. The constant current operation typically extends down to lower than 75% of nominal output voltage regulation.

When VDET detect V_{OUT} is lower than 75% of nominal output voltage regulation, the switching frequency will jump to 90KHz in order to increase output current, and then will drop vs output voltage base on equation (2) for constant current operation. And then when VDET detect V_{OUT} is lower than 44% of nominal output voltage regulation, the switching frequency will jump to 75KHz in order to increase output current, and then will drop vs output voltage base on equation (2) for constant current operation.

There is an external resistor, Rline, connected in series between CS pin and RCS. This resistor is used to compensate for the line voltage.

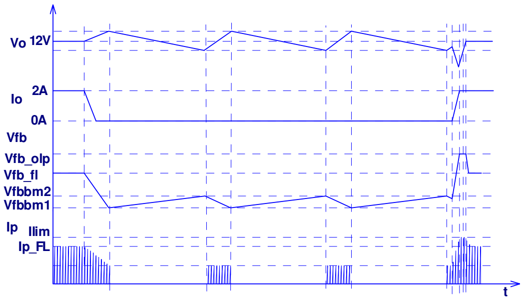
No Load Idle Mode

In no load standby mode, the feedback voltage falls below V_{FBBM2} and reaches V_{FBBM1}, ACT522 stop switching. After it stops, as a result of a feedback reaction, the feedback voltage increases. When the feedback voltage reaches V_{FBBM2}, ACT522 start switching again. Feedback voltage drops again and output voltage starts to bounds back and forward with very small output ripple. ACT522 leaves idle mode when load is added strong enough to pull feedback voltage exceed $V_{FBBM2.}$

FUNCTIONAL DESCRIPTION CONT'D

Figure 2:

Idle Mode



Primary Inductor Current Limit Compensation

The ACT522 integrates a primary inductor peak current limit compensation circuit to achieve constant current over wide line and wide inductance.

Frequency Foldback

When the load drops to 75% of full load level, ACT522 starts to reduce the switching frequency, which is proportional to the load current ,to improve the efficiency of the converter.

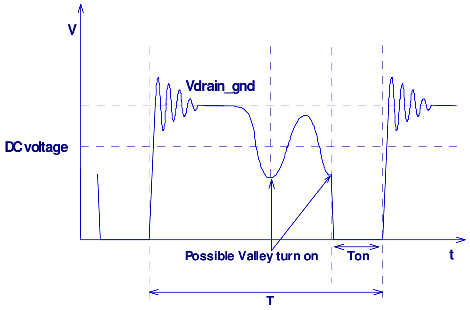
ACT522's load adaptive switching frequency enables applications to meet all latest green energy standards. The actual minimum average switching frequency is programmable with output capacitance, feedback circuit and dummy load (while still meeting standby power).

Valley Switching

ACT522 employed valley switching from no load to heavy load to reduce switching loss and EMI. In discontinuous mode operation, the resonant voltage between inductance and parasitic capacitance on MOSFET source pin is coupled by auxiliary winding and reflected on VDET pin through feedback network R5, R6. Internally, the VDET pin is connected to an zero-crossing detector to generate the switch turn on signal when the conditions are meet.

Figure 3:

Valley Switching



Protection Features

The ACT522 provides full protection functions. The following table summarizes all protection functions.

PROTECTION FUNCTIONS	FAILURE CONDITION	PROTECTION MODE
V_{DD} Over Voltage	$V_{DD} > 44V$ (4 duty cycle)	Auto Restart
V_{VDET} Over Voltage/No Voltage	$V_{VD} > 2.75V$ or No switching for 4 cycles	Auto Restart
Short Winding/ Short Diode	$V_{CS} > 2.5V$	Auto Restart
Over Load/Open Loop (No CC)	$IPK = I_{LIMIT}$ or $V_{FB} = 4V$ for 400ms	Auto Restart
Output Short Circuit	$V_{DET} < 0.45V$	Auto Restart
V_{DD} Under Voltage	$V_{DD} < 7V$	Auto Restart
Line Brown Out	$I_{VDETUVLO} < 60\mu A$	Auto Restart

Auto-Restart Operation

ACT522 will enter into auto-restart mode when a fault is identified. There is a startup phase in the auto-restart mode. After this startup phase the conditions are checked whether the failure is still present. Normal operation proceeds once the failure mode is removed. Otherwise, new startup phase will be initiated again.

To reduce the power loss during fault mode, the startup delay control is implemented. The startup delay time increases over lines.

TYPICAL APPLICATION

Design Example

The design example below gives the procedure for rapid charger flyback converter using ACT522. Refer to application circuit Figure 4, the design for an adapter application starts with the following specification:

Input Voltage Range	90VAC - 265VAC, 50/60Hz
Output Power, P_O	15W
Output Voltage, V_{OUTCV}	12/9/5V
Full Load Current, I_{OUTFL}	1.25/1.67/2.1A
System Efficiency CV, η	0.85

The operation for the circuit shown in Figure 4 is as follows: the rectifier bridge D1−D4 and the capacitor C1/C2 convert the AC line voltage to DC bus voltage. This voltage supplies the primary winding of the transformer T1 and the startup circuit of Q2 and C4 to VDD pin of ACT522. The primary power current path is formed by the transformer's primary winding, Q1, and the current sense resistor R9. The resistors R3, R2, diode D5 and capacitor C3 create a snubber clamping network that protects Q1 from damage due to high voltage spike during Q1's turn off. The network consisting of capacitor C4, diode D6 and resistor R4 provides a VDD supply voltage for ACT522 from the auxiliary winding of the transformer. The resistor R4 is optional, which filters out spikes and noise to makes VDD more stable. C4 is the decoupling capacitor of the supply voltage and energy storage component for startup. During power startup, the current charges C4 through startup mosfet Q2 from the rectified bus voltage. The diode D8 and the capacitor C5/L2/C6 rectify filter the output voltage. The resistor divider consists of R15 and R16 programs the output voltage. Since a bridge rectifier and bulk input capacitors are used, the resulting minimum and maximum DC input voltages can be calculated:

$$V_{INDC\_MIN} = \sqrt{2V_{INAC\_MIN}^{2} \quad \frac{2P_{OUT}(\frac{1}{2f_L} - t_C)}{\eta \times C_{IN}}}$$
$$= \sqrt{2\times 90^{2} - \frac{2\times 15\times(\frac{1}{2\times 47} - 3.5ms)}{0.85\times 24\mu F}} \approx 80V \qquad (3)$$

$$V_{IN(MAX)DC} = \sqrt{2}\times V_{IN(MAX)AC}$$
$$= \sqrt{2}\times(265\,V_{AC}) = 375\,V \qquad (4)$$

Where η is the estimated circuit efficiency, f_L is the line frequency, t_C is the estimated rectifier conduction time, C_{IN} is empirically selected to two 12μF electrolytic capacitors.

The maximum duty cycle is set to be 48% at low line voltage 90VAC and the circuit efficiency is estimated to be 85%. Then the maximum average input current is:

$$I_{IN\_MAX} = \frac{V_{OUT}\times I_{OUT}}{V_{INDC\_MIN}\times\eta}$$
$$= \frac{12\times 1.25}{80\times 0.85} = 221\ mA \qquad (5)$$

The maximum input primary peak current:

$$I_{PPK} = \frac{2\times L_{IN}}{D_{MAX}} = \frac{2\times 181}{0.5} = 921\,mA \qquad (6)$$

The primary inductance of the transformer:

$$L_p = \frac{V_{INDC\_MIN}D_{max}}{I_{LIM}\times f_s}$$
$$= \frac{80\times 0.48}{921\ mA\times 90\ k} \approx 0.47\ mH \qquad (7)$$

The maximum primary turns on time:

$$T_{ON\_MAX} = L_p\frac{I_{LIM}}{V_{INDC\_MIN}}$$
$$= \frac{0.47\,mH\times 921\,mA}{80} = 5.41\,\mu s \qquad (8)$$

The ringing periods from primary inductance with mosfet Drain-Source capacitor:

$$T_{RINGING\_MAX} = 2\pi\sqrt{L_{p\_MAX}C_{DS\_MAX}}$$
$$= 2\times 3.14\times\sqrt{0.47mH\times(1+7\%)\times 100PF} = 1.41\mu s \qquad (9)$$

Design only an half ringing cycle at maximum load in minimum low line, so secondly reset time:

$$T_{RST} = T_{SW} - T_{ON\_MAX} - 0.5T_{RINGING\_MAX}$$
$$= 1/90kHz - 5.41\mu s - 0.5\times 1.41\mu s = 5\mu s \qquad (10)$$

Base on conservation of energy and transformer transform identity, the primary to secondary turns ratio N_P/N_S:

$$\frac{N_P}{N_S} = \frac{T_{ON}}{T_{RST}}\times\frac{V_{IN\_MIN}}{V_{OUT}+V_D}$$
$$= \frac{5.41}{5}\times\frac{80}{12+0.35} = 7 \qquad (11)$$

The auxiliary to secondary turns ratio N_A/N_S:

$$\frac{N_A}{N_S} = \frac{V_{DD}+V_D'}{V_{OUT}+V_D} = \frac{31+0.45}{12+0.35} = 2.55 \qquad (12)$$

TYPICAL APPLICATION CONT'D

An EI16+ core is selected for the transformer. From the manufacture's catalogue recommendation, the gapped core with an effective inductance A_{LE} of 0.294 µH/T^2 is selected. The turn of the primary winding is:

$$N_P = \sqrt{\frac{L_P}{A_{LE}}} = \sqrt{\frac{0.47\,mH}{0.294\,\mu H / T^2}} = 40T \quad (13)$$

The turns of secondary and auxiliary winding can be derived accordingly:

$$N_S = \frac{N_s}{N_p} \times N_p = \frac{1}{7} \times 40 \approx 6T \quad (14)$$

$$N_A = \frac{N_A}{N_S} \times N_s = 2.55 \times 6 \approx 15T \quad (15)$$

Determining the value of the current sense resistor (R9) uses the peak current in the design. Since the ACT522 internal current limit is set to 0.96V, the design of the current sense resistor is given by:

$$R_{CS} = \frac{V_{CS}}{\sqrt{\frac{2 \times I_{OUT\_MAX} \times V_{OUT}}{L_P \times F_{SW} \times \eta_{system}}}} = \frac{0.96}{\sqrt{\frac{2 \times 1.45 \times 12}{0.47\,mH \times 90\,kHz \times 0.85}}} \approx 0.91\,\Omega \quad (16)$$

The voltage feedback resistors are selected according to the Ioccmax and Vo. The design Io_cc max is given by:

$$f_s = \frac{N_p}{N_s} \times \frac{R_{fb1} \times R_{fb2}}{R_{fb1} + R_{fb2}} \times \frac{V_O + V_D}{L_p \times \frac{V_{cs}}{R_{cs}} \times K_{f\_sw}} \quad (17)$$

The design Vo is given by:

$$V_o = (1 + \frac{R_{fb1}}{R_{fb2}}) \times \frac{N_s}{N_a} \times V_{FB} - V_D \quad (18)$$

Where k is IC constant and K=17120, then we can get the value:

$$R_{fb1} = 115K, R_{fb2} = 9.09K \quad (19)$$

When selecting the output capacitor, a low ESR electrolytic capacitor is recommended to minimize ripple from the current ripple. The approximate equation for the output capacitance value is given by:

$$C_{OUT} = \frac{I_{OUT}}{f_{sw} \times V_{RIPPLE}} = \frac{2.4}{75k \times 50mV} = 640\,\mu F \quad (20)$$

Two 330µF electrolytic capacitors are used to keep the ripple small.

PCB Layout Guideline

Good PCB layout is critical to have optimal performance. Decoupling capacitor (C4) and feedback resistor (R5/R6) should be placed close to VDD and FB pin respectively. There are two main power path loops. One is formed by C1/C2, primary winding, mosfet transistor and current sense resistor (R9). The other is secondary winding, rectifier D8 and output capacitors (C5/C6). Keep these loop areas as small as possible. Connecting high current ground returns, the input capacitor ground lead, and the ACT522 GND pin to a single point (star ground configuration).

Figure 4:
Universal VAC Input, 12/9/5V 1.25/1.67/2.1A rapid Charger

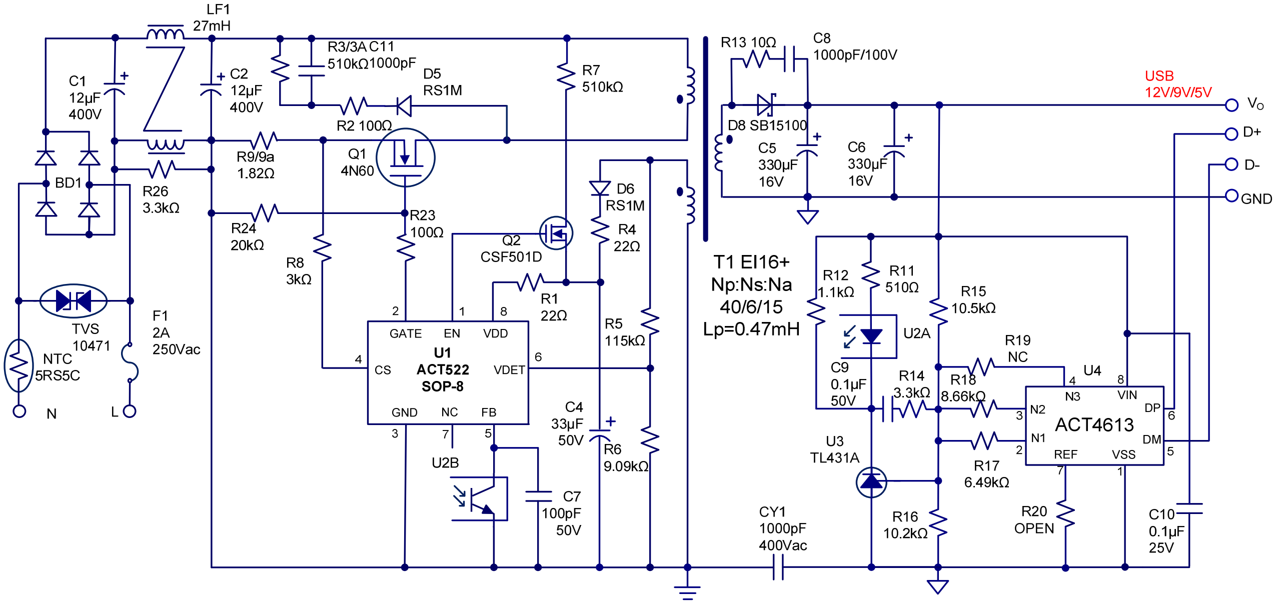


Figure 5:
Output CCCV curve

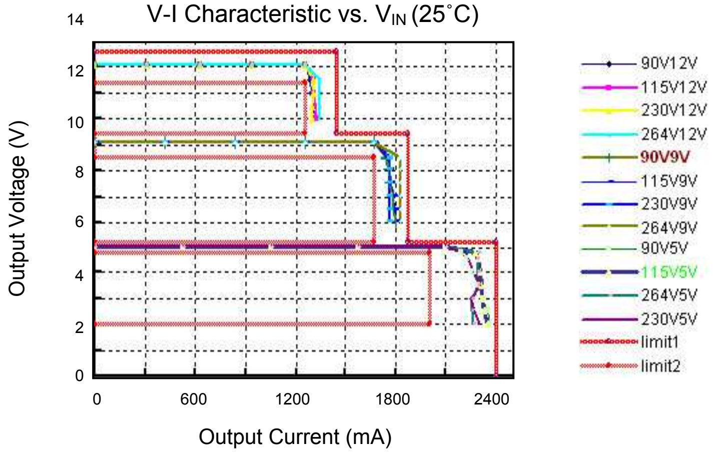


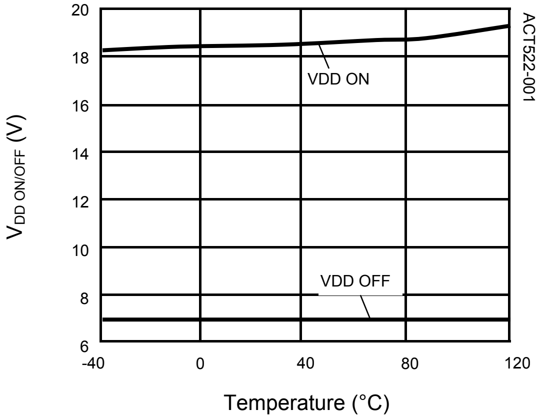
Table 1:

ACT522 5V12W Bill of Materials

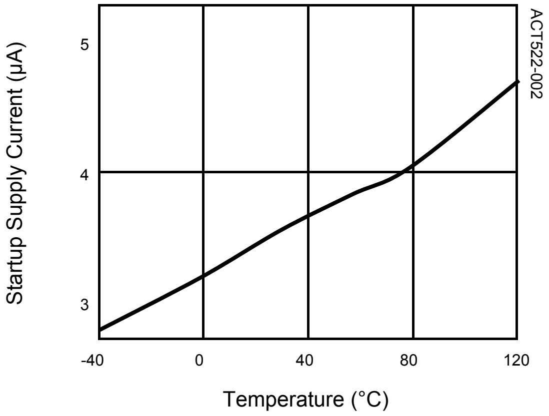
ITEM	REFERENCE	DESCRIPTION	QTY	MANUFACTURER
1	U1	IC, ACT522SH,SOP-8	1	Active-Semi.
2	U2	OPTO,EL3H7D,CTR:300-600%,4PIN SMD	1	EVERLIGHT
3	U3	TL431A, Ref=2.5V,1%,SOT23-3	1	TI
4	U4	IC, ACT4613SH201-T,SOP-8	1	Active-Semi.
5	C1,2	Capacitor, Electrolytic,12uF/400V, 8x14mm	2	RUBYCON
6	C11,C8	Capacitor, Ceramic, 1000pF/500V, 0805,SMD	2	POE
7	C4	Capacitor, Ceramic,33uF/50V, 1206	1	POE
8	C5,C6	Capacitor, Solid, 330uF/16V, 8x12mm	2	KSC
9	C9,10	Capacitor, Ceramic, 0.1uF/50V, 0805,SMD	2	POE
10	C7	Capacitor, Ceramic, 100pF/25V, 0805,SMD	1	POE
11	CY1	Safety Y1,Capacitor,1000pF/400V,Dip	1	UXT
12	BD1	BP06,1000V/1.0A,SDIP	1	PANJIT
13	D5,D6	Fast Recovery Rectifier, RS1M,1000V/1.0A, RMA	2	PANJIT
14	D8	Diode, Schottky, 100V/15A, TO-247AB	1	Diodes
15	LF1	CM Inductor, 27mH, EE8.3,D=0.2mm,90T	1	APY(安品源科技)
16	Q1	N-Mosfet Transistor, 4N60,TO-220	1	AUK
17	Q2	N-Mosfet, Depletion mode,CSF501D,20mA/600V,SOT23	1	HuiJing
18	PCB1	PCB, L*W*T=39x39x1.0mm,FR-4,Rev:A	1	Jintong
19	F1	Fuse,2A/250V	1	TY-OHM
20	R1,4	Chip Resistor, 22 ohm, 0805, 5%	2	TY-OHM
21	R2,23	Chip Resistor, 100 ohm, 0805, 5%	2	TY-OHM
22	R3,3A,7	Carbon Resistor, 510K ohm, 1206, 5%	3	TY-OHM
23	R5	Chip Resistor, 115K ohm, 0805,1%	1	TY-OHM
24	R6	Chip Resistor, 9.09K ohm, 0805, 1%	1	TY-OHM
25	R8	Chip Resistor, 3K ohm, 0805, 5%	1	TY-OHM
26	R9,R9a	Chip Resistor, 1.82 ohm,1206 , 1%	2	TY-OHM
27	R11	Chip Resistor, 510 ohm, 0805, 5%	1	TY-OHM
28	R12	Chip Resistor, 1.1k ohm, 0805,5%	1	TY-OHM
29	R14,26	Chip Resistor, 3.3k ohm, 0805, 5%	2	TY-OHM
30	R15	Chip Resistor, 10.5K ohm, 0805, 1%	1	TY-OHM
31	R16	Chip Resistor, 10.2K ohm, 0805, 1%	1	TY-OHM
32	R17	Chip Resistor, 6.49K ohm, 0805, 1%	1	TY-OHM
33	R18	Chip Resistor, 8.66K ohm, 0805, 1%	1	TY-OHM
34	R24	Chip Resistor, 20k ohm, 0805, 5%	1	TY-OHM
35	T1	Transformer, Lp=0.47mH, EI16+	1	APY(安品源科技)
36	NR1	Thermal resistor, SC053	1	TY-OHM
37	VR1	10D471	1	TY-OHM
38	USB1	Small standard USB connector.	1	TY-OHM
39	R19,20	NC		

TYPICAL PERFORMANCE CHARACTERISTICS

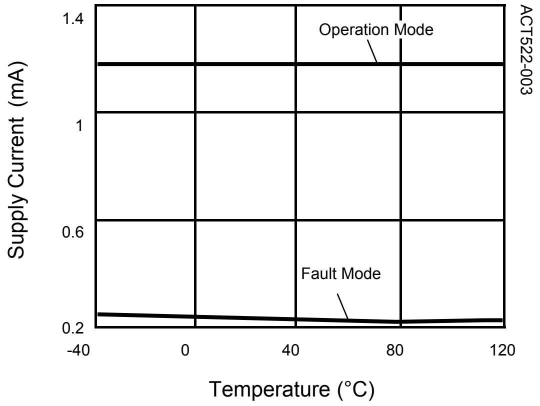
VDD ON/OFF Voltage vs. Temperature



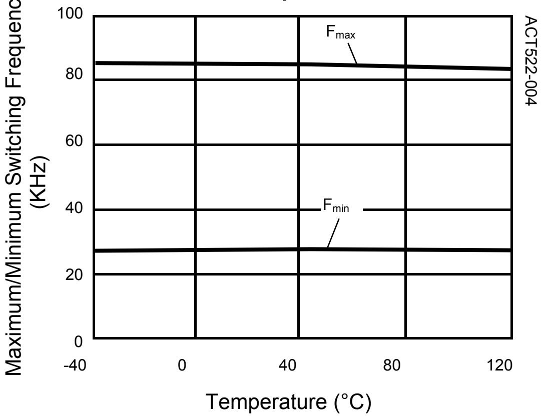
Startup Supply Current vs. Temperature



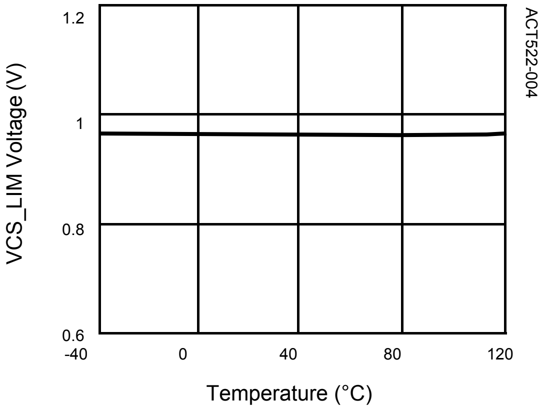
Supply Current at Operation/Fault Mode vs. Temperature



Maximum/Minimum Switching Frequency vs. Temperature

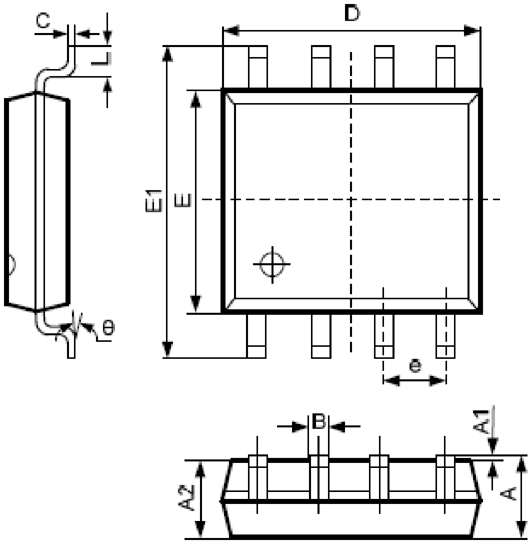


VCS_LIM Voltage vs. Temperature



PACKAGE OUTLINE

SOP-8 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Note: Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per end. Dimension E1 does not include flash or protrusion.