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ACT8600

Rev 4, 10-Sep-14

Advanced PMU for Ingenic JZ4760/60B/70 Processors

FEATURES

- Optimized for Ingenic JZ4760, JZ4760B, and JZ4770 Processors
- Three Step-Down DC/DC Converters
- One Step-Up DC/DC Converter
- USB OTG Switch with 600mA Current Limit
- Four Low-Noise LDOs
- Two Low IQ Keep-Alive LDOs
- Backup Battery Charger
- Single-Cell Li+*ActivePath*™ Battery Charger
- I²C™ Serial Interface
- Interrupt Controller
- Power On Reset Interface and Sequencing Controller
- Minimum External Components
- 5×5mm TQFN55-40 Package
  - 0.75mm Package Height
  - Pb-Free and RoHS Compliant

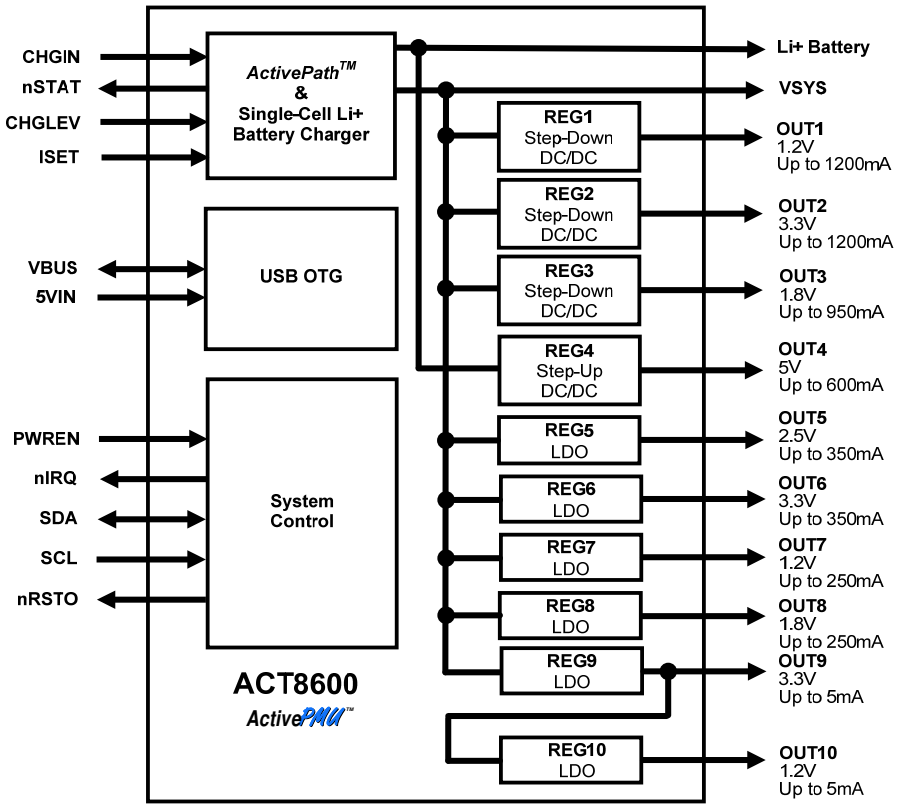
GENERAL DESCRIPTION

The ACT8600 is a complete, cost effective, highly-efficient *ActivePMU*™ power management solution, optimized for the unique power, voltage-sequencing, and control requirements of the Ingenic JZ4760, JZ4760B and JZ4770 processors.

This device features three highly efficient step-down DC/DC converters, one step-up DC/DC converter, four low-noise, low-dropout linear regulators, and two Low IQ always on Keep-Alive linear regulators, a current limit switch for USB OTG, along with a complete battery charging solution featuring the advanced *ActivePath*™ system-power selection function.

The ACT8600 is available in a compact, Pb-Free and RoHS-compliant TQFN55-40 package.

SYSTEM BLOCK DIAGRAM



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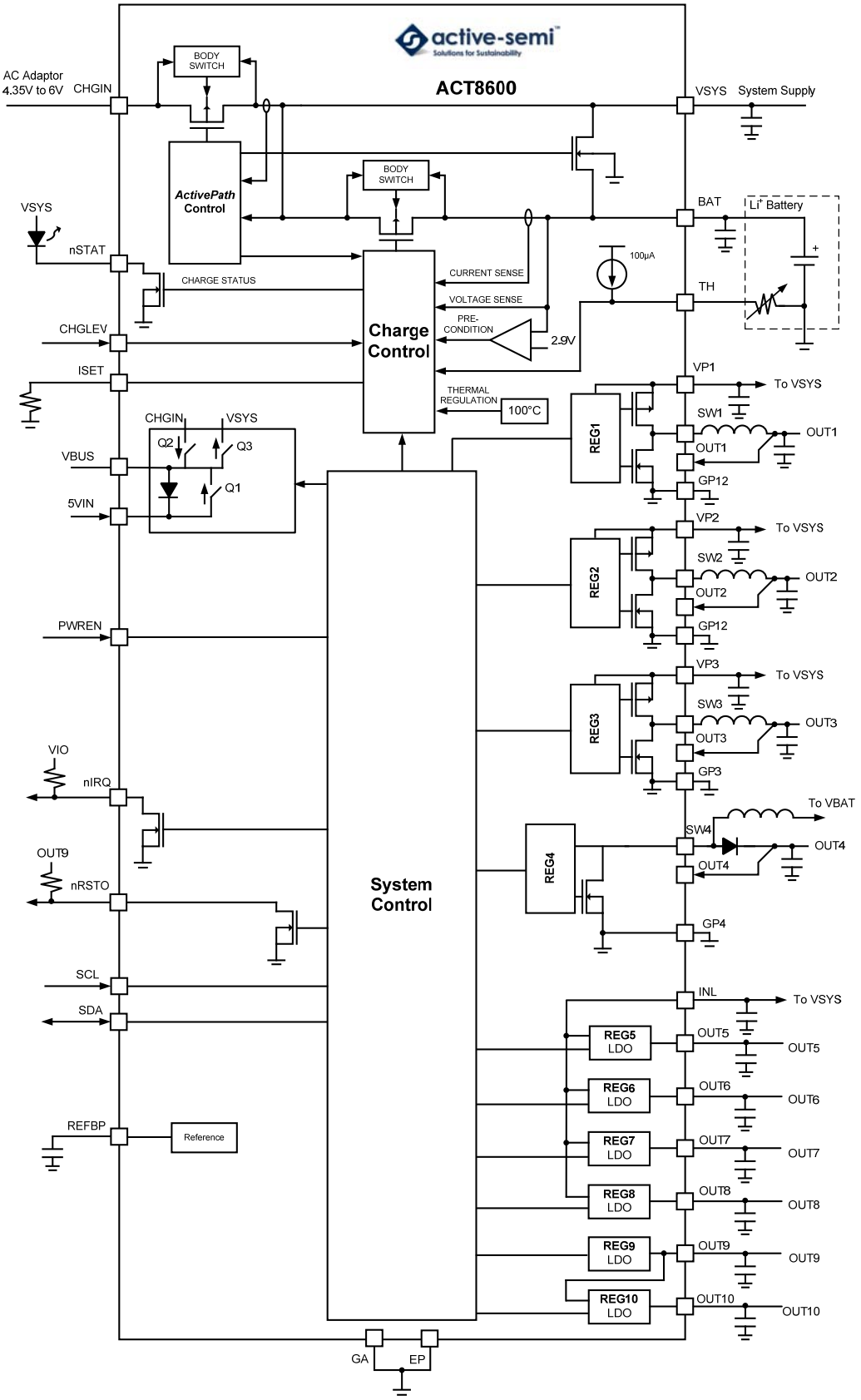
FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION①

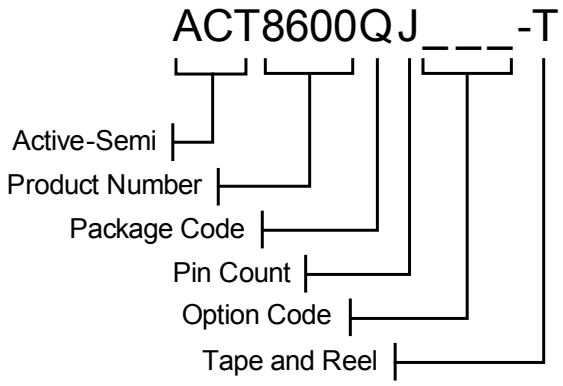
PART NUMBER	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{OUT4}	V_{OUT5}	V_{OUT6}	V_{OUT7}	V_{OUT8}	V_{OUT9}	V_{OUT10}	PACKAGE	PINS	TEMPERATURE RANGE
ACT8600QJ162-T	1.2V	3.3V	1.8V	5V	2.5V	3.3V	1.2V	1.8V	3.3V	1.2V	TQFN55-40	40	-40°C to +85°C
ACT8600QJ601-T	3.3V	1.8V	1.2V	5V	2.5V	3.3V	1.2V	1.8V	3.3V	1.2V	TQFN55-40	40	-40°C to +85°C

①: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

②: Standard product options are identified in this table. Contact factory for custom options. Minimum order quantity is 12,000 units.

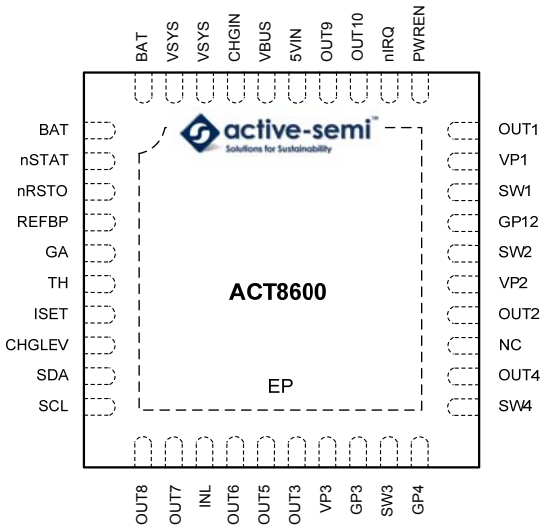
③: ACT8600QJ162-T is dedicated to Ingenic's application.

④: ACT8600QJ601-T is dedicated to Bloomberg's application.



PIN CONFIGURATION

TOP VIEW



Thin - QFN (TQFN55-40)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1, 40	BAT	Battery charger output. Connect this pin directly to the battery anode (+ terminal).
2	nSTAT	Active-Low Open-Drain Charger Status Output. nSTAT has a 8mA (typ.) current limit, allowing it to directly drive an indicator LED without additional external components.
3	nRSTO	Active low open-drain Reset Output.
4	REFBP	Reference Bypass. Connect a 0.047µF ceramic capacitor from REFBP to GA.
5	GA	Ground.
6	TH	Temperature Sensing Input.
7	ISET	Charge Current Set. Program the maximum charge current by connecting a resistor (R_{ISET}) between ISET and GA.
8	CHGLEV	Charge Current Selection Input.
9	SDA	Data Input for I^2C Serial Interface. Data is read on the rising edge of SCL.
10	SCL	Clock Input for I^2C Serial Interface.
11	OUT8	REG8 Output. Bypass it to ground with a 2.2µF capacitor.
12	OUT7	REG7 Output. Bypass it to ground with a 2.2µF capacitor.
13	INL	Power Input for the LDOs. Bypass to GA with a high quality ceramic capacitor placed as close to the IC as possible.
14	OUT6	REG6 Output. Bypass it to ground with a 2.2µF capacitor.
15	OUT5	REG5 Output. Bypass it to ground with a 2.2µF capacitor.
16	OUT3	Output voltage sense for REG3.
17	VP3	Power input for REG3. Bypass to GP3 with a high quality ceramic capacitor placed as close to the IC as possible.
18	GP3	Power Ground for REG3. Connect GA, GP12, GP3 and GP4 together at a single point as close to the IC as possible.
19	SW3	Switch Node for REG3.
20	GP4	Power Ground for REG4. Connect GA, GP12 and GP3 together at a single point as close to the IC as possible.

PIN DESCRIPTIONS CONT'D

PIN	NAME	DESCRIPTION
21	SW4	Switch Node for REG4.
22	OUT4	REG4 Output.
23	NC	No Connect.
24	OUT2	Output Voltage Sense for REG2.
25	VP2	Power Input for REG2. Bypass to GP12 with a high quality ceramic capacitor placed to the IC as close as possible.
26	SW2	Switch Node for REG2.
27	GP12	Power Ground for REG1 and REG2. Connect GA, GP12 and GP3 together at a single point as close to the IC as possible.
28	SW1	Switch Node for REG1.
29	VP1	Power Input for REG1. Bypass to GP12 with a high quality ceramic capacitor placed to the IC as close as possible.
30	OUT1	Output Voltage Sense for REG1.
31	PWREN	Master enable pin.
32	nIRQ	Open-Drain Interrupt Output.
33	OUT10	REG10 Output. Bypass it to GA with a 0.47µF capacitor.
34	OUT9	REG9 Output. Bypass it to GA with a 1µF capacitor.
35	5VIN	5V Input pin for OTG switch (optionally from OUT4 or external 5V source).
36	VBUS	USB VBUS.
37	CHGIN	Power Input for the Battery Charger. Bypass CHGIN to GA with a capacitor placed as close to the IC as possible. The battery charger is automatically enabled when a valid voltage is present on CHGIN .
38, 39	VSYS	System Output Pins. Bypass to GA with a 10µF or larger ceramic capacitor.
EP	EP	Exposed Pad. Must be soldered to ground on PCB.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
VP1, VP2 to GP12 VP3 to GP3	-0.3 to + 6	V
BAT, VSYS, INL, VBUS, 5VIN to GA	-0.3 to + 6	V
CHGIN to GA	-0.3 to + 14	V
SW1, OUT1 to GP12	-0.3 to (V_{VP1} + 0.3)	V
SW2, OUT2 to GP12	-0.3 to (V_{VP2} + 0.3)	V
SW3, OUT3 to GP3	-0.3 to (V_{VP3} + 0.3)	V
SW4, OUT4 to GP4	-0.3 to + 42	V
nIRQ, nRSTO, nSTAT to GA	-0.3 to + 6	V
PWREN, SCL, SDA, CHGLEV, TH, ISET, REFBP to GA	-0.3 to (V_{VSYS} + 0.3)	V
OUT5, OUT6, OUT7, OUT8, OUT9, OUT10 to GA	-0.3 to (V_{INL} + 0.3)	V
GP12, GP3, GP4 to GA	-0.3 to + 0.3	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Junction Temperature	125	°C
Maximum Power Dissipation TQFN55-40 (Thermal Resistance=30°C/W)	3.2	W
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

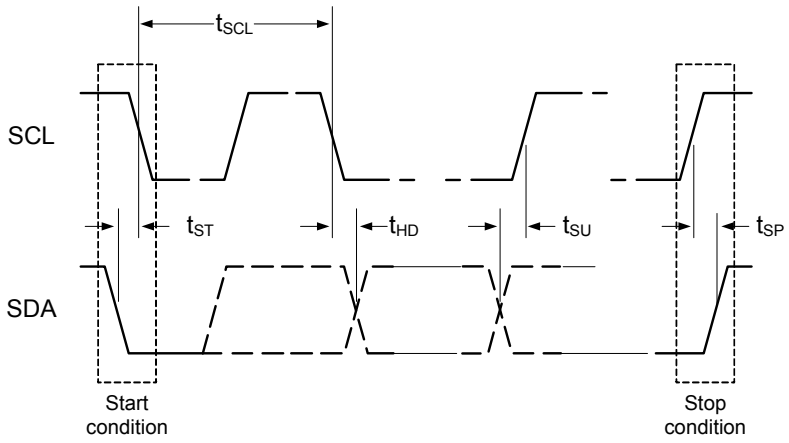
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{VSYS} = 3.1V to 5.5V, T_A = -40ºC to 85ºC			0.35	V
SCL, SDA Input High	V_{VSYS} = 3.1V to 5.5V, T_A = -40ºC to 85ºC	1.55			V
SDA Leakage Current			0	1	µA
SCL Leakage Current			0	1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Period, t_{SCL}		1.5			µs
SDA Data Setup Time, t_{SU}		100			ns
SDA Data Hold Time, t_{HD}		300			ns
Start Setup Time, t_{ST}	For Start Condition	100			ns
Stop Setup Time, t_{SP}	For Stop Condition	100			ns

Figure 1:
I²C Compatible Serial Bus Timing



GLOBAL REGISTER MAP

OUTPUT	ADDRESS		BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
SYS	0x00	NAME	nSYSLEVMSK	nSYSSTAT	VSYSDAT	*Reserved*	SYSLEV[3]	SYSLEV[2]	SYSLEV[1]	SYSLEV[0]
		DEFAULT①	0	R	R	0	0	0	0	0
SYS	0x01	NAME	nTMSK	TSTAT	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT①	0	R	0	0	0	0	0	0
REG1	0x10	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG1	0x12	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	0	0	0	0	0	0	R
REG2	0x20	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG2	0x22	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	0	0	0	0	1	0	R
REG3	0x30	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	0	0	1	0	0
REG3	0x32	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	0	0	0	0	0	0	R
REG4	0x40	NAME	VSET[7]	VSET[6]	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	0	1	0	1	0	0
REG4	0x41	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	OK
		DEFAULT①	0	0	0	0	0	0	0	R
REG5	0x50	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	1	0	0	0	1
REG5	0x51	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	0	0	0	0	1	0	R
REG6	0x60	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG6	0x61	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	0	0	0	0	0	1	0	R
REG7	0x70	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG7	0x71	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	0	0	0	0	0	1	0	R
REG8	0x80	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	0	0	1	0	0
REG8	0x81	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	0	0	0	0	0	1	0	R
REG910	0x91	NAME	ON9	ON10	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT①	1	0	0	0	0	0	0	0
APCH	0xA1	NAME	SUSCHG	*Reserved*	TOTTIMO[1]	TOTTIMO[0]	PRETIMO[1]	PRETIMO[0]	CHGLEV	OVPSET[0]
		DEFAULT①	0	0	1	0	1	0	0	0
APCH	0xA8	NAME	TIMRSTAT	TEMPSTAT	INSTAT	CHGSTAT	TIMRDAT	TEMPDAT	INDAT	CHGDAT
		DEFAULT①	R	R	R	R	R	R	R	R
APCH	0xA9	NAME	TIMRTOT	TEMPIN	INCON	CHGEOCIN	TIMRPRE	TEMPOUT	INDIS	CHGEOCOUT
		DEFAULT①	0	0	0	0	0	0	0	0
APCH	0xAA	NAME	CHG_ACIN	CHG_USB	CSTATE[0]	CSTATE[1]	*Reserved*	*Reserved*	*Reserved*	CHGLEVSTAT
		DEFAULT①	R	R	R	R	R	R	R	R
OTG	0xB0	NAME	ONQ1	ONQ2	ONQ3	Q1OK	Q2OK	VBUSSTAT	DBILIMQ3	VBUSDAT
		DEFAULT①	0	0	1	R	R	R	0	R
OTG	0xB2	NAME	INVBUSR	INVBUSF	*Reserved*	*Reserved*	nFLTMSKQ1	nFLTMSKQ2	*nVBUSMSK*	*Reserved*
		DEFAULT	0	0	0	0	0	0	0	0
INT	0xC1	NAME	INTADR7	INTADR6	INTADR5	INTADR4	INTADR3	INTADR2	INTADR1	INTADR0
		DEFAULT	R	R	R	R	R	R	R	R

①: Default values of ACT8600QJ162-T.

Note: Every Reserved bit should be kept as Default Value

REGISTER AND BIT DESCRIPTIONS

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
SYS	0x00	[7]	nSYSLEVMSK	R/W	VSYS Voltage Level Interrupt Mask. Set this bit to 1 to unmask the interrupt. See the *Programmable System Voltage Monitor* section for more information
SYS	0x00	[6]	nSYSSTAT	R	System Voltage Status. Value is 1 when SYSLEV interrupt is generated, value is 0 otherwise.
SYS	0x00	[5]	VSYSDAT	R	VSYS Voltage Monitor real time status. Value is 1 when V_{VSYS} < SYSLEV, value is 0 otherwise.
SYS	0x00	[4]	-	R	Reserved.
SYS	0x00	[3:0]	SYSLEV	R/W	System Voltage Detect Threshold. Defines the SYSLEV voltage threshold. See the *Programmable System Voltage Monitor* section for more information.
SYS	0x01	[7]	nTMSK	R/W	Thermal Interrupt Mask. Set this bit to 1 to unmask the interrupt.
SYS	0x01	[6]	TSTAT	R	Thermal Interrupt Status. Value is 1 when a thermal interrupt is generated, value is 0 otherwise.
SYS	0x01	[5:0]	-	R	Reserved.
REG1	0x10	[7:6]	-	R	Reserved.
REG1	0x10	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG1	0x12	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG1	0x12	[6:3]	-	R	Reserved.
REG1	0x12	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG1	0x12	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG1	0x12	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG2	0x20	[7:6]	-	R	Reserved.
REG2	0x20	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG2	0x22	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG2	0x22	[6:3]	-	R	Reserved.
REG2	0x22	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG2	0x22	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG2	0x22	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.

REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG3	0x30	[7:6]	-	R	Reserved.
REG3	0x30	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG3	0x32	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG3	0x32	[6:3]	-	R	Reserved.
REG3	0x32	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG3	0x32	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG3	0x32	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG4	0x40	[7:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG4	0x41	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG4	0x41	[6:1]	-	R	Reserved.
REG4	0x41	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG5	0x50	[7:6]	-	R	Reserved.
REG5	0x50	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG5	0x51	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG5	0x51	[6:3]	-	R	Reserved.
REG5	0x51	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG5	0x51	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG5	0x51	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG6	0x60	[7:6]	-	R	Reserved.
REG6	0x60	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG6	0x61	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG6	0x61	[6:3]	-	R	Reserved.
REG6	0x61	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG6	0x61	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG6	0x61	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.

REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG7	0x70	[7:6]	-	R	Reserved.
REG7	0x70	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG7	0x71	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG7	0x71	[6:3]	-	R	Reserved.
REG7	0x71	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG7	0x71	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG7	0x71	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG8	0x80	[7:6]	-	R	Reserved.
REG8	0x80	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG8	0x81	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG8	0x81	[6:3]	-	R	Reserved.
REG8	0x81	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG8	0x81	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG8	0x81	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG910	0x91	[7]	ON9	R/W	REG9 Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG910	0x91	[6]	ON10	R/W	REG10 Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG910	0x91	[5:0]	-	R	Reserved.
APCH	0xA1	[7]	SUSCHG	R/W	Charge Suspend Control Input. Set bit to 1 to suspend charging, clear bit to 0 to allow charging to resume.
APCH	0xA1	[6]	-	R	Reserved.
APCH	0xA1	[5:4]	TOTTIMO	R/W	Total Charge Time-out Selection. See the *Charge Safety Timers* section for more information.
APCH	0xA1	[3:2]	PRETIMO	R/W	Precondition Charge Time-out Selection. See the *Charge Safety Timers* section for more information.
APCH	0xA1	[1]	CHGLEV	R/W	Charge Current Selection Input. See *Charge Current Programming* Section.
APCH	0xA1	[0]	OVPSET	R/W	Input Over-Voltage Protection Threshold Selection. See the *Input Over-Voltage Protection* section for more information.
APCH	0xA8	[7]	TIMRSTAT①	R/W	Charge Time-out Interrupt Status. Set this bit with TIMRPRE[ ] and/or TIMRTOT[ ] to 1 to generate an interrupt when charge safety timers expire, read this bit to get charge time-out interrupt status. See the *Charge Safety Timers* section for more information.

①: Valid only when CHGIN UVLO Threshold<V_{CHGIN}<CHGIN OVP Threshold.

REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
APCH	0xA8	[6]	TEMPSTAT①	R/W	Battery Temperature Interrupt Status. Set this bit with TEMPIN[ ] and/or TEMPOUT[ ] to 1 to generate an interrupt when a battery temperature event occurs, read this bit to get the battery temperature interrupt status. See the *Battery Temperature Monitoring* section for more information.
APCH	0xA8	[5]	INSTAT	R/W	Input Voltage Interrupt Status. Set this bit with INCON[ ] and/or INDIS[ ] to generate an interrupt when UVLO or OVP condition occurs, read this bit to get the input voltage interrupt status. See the *Charge Current Programming* section for more information.
APCH	0xA8	[4]	CHGSTAT①	R/W	Charge State Interrupt Status. Set this bit with CHGEOCIN[ ] and/or CHGEOCOUT[ ] to 1 to generate an interrupt when the state machine gets in or out of EOC state, read this bit to get the charger state interrupt status. See the *State Machine Interrupts* section for more information.
APCH	0xA8	[3]	TIMRDAT①	R	Charge Timer Status. Value is 1 when precondition time-out or total charge time-out occurs. Value is 0 in other case.
APCH	0xA8	[2]	TEMPDAT①	R	Temperature Status. Value is 0 when battery temperature is outside of valid range. Value is 1 when battery temperature is inside of valid range.
APCH	0xA8	[1]	INDAT	R	Input Voltage Status. Value is 1 when a valid input at CHGIN is present. Value is 0 when a valid input at CHGIN is not present.
APCH	0xA8	[0]	CHGDAT①	R	Charge State Machine Status. Value is 1 indicates the charger state machine is in EOC state, value is 0 indicates the charger state machine is in other states.
APCH	0xA9	[7]	TIMRTOT	R/W	Total Charge Time-out Interrupt Control. Set both this bit and TIMRSTAT[ ] to 1 to generate an interrupt when a total charge time-out occurs. See the *Charge Safety Timers* section for more information.
APCH	0xA9	[6]	TEMPIN	R/W	Battery Temperature Interrupt Control. Set both this bit and TEMPSTAT[ ] to 1 to generate an interrupt when the battery temperature goes into the valid range. See the *Battery Temperature Monitoring* section for more information.
APCH	0xA9	[5]	INCON	R/W	Input Voltage Interrupt Control. Set both this bit and INSTAT[ ] to 1 to generate an interrupt when CHGIN input voltage goes into the valid range. See the *Charge Current Programming* section for more information.
APCH	0xA9	[4]	CHGEOCIN	R/W	Charge State Interrupt Control. Set both this bit and CHGSTAT[ ] to 1 to generate an interrupt when the state machine goes into the EOC state. See the *State Machine Interrupts* section for more information.
APCH	0xA9	[3]	TIMRPRE	R/W	PRECHARGE Time-out Interrupt Control. Set both this bit and TIMRSTAT[ ] to 1 to generate an interrupt when a PRECHARGE time-out occurs. See the *Charge Safety Timers* section for more information.
APCH	0xA9	[2]	TEMPOUT	R/W	Battery Temperature Interrupt Control. Set both this bit and TEMPSTAT[ ] to 1 to generate an interrupt when the battery temperature goes out of the valid range. See the *Battery Temperature Monitoring* section for more information.

①: Valid only when CHGIN UVLO Threshold<V_{CHGIN}<CHGIN OVP Threshold.

REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
APCH	0xA9	[1]	INDIS	R/W	Input Voltage Interrupt Control. Set both this bit and INSTAT[ ] to 1 to generate an interrupt when CHGIN input voltage goes out of the valid range. See the *Charge Current Programming* section for more information.
APCH	0xA9	[0]	CHGEOCOUT	R/W	Charge State Interrupt Control. Set both this bit and CHGSTAT[ ] to 1 to generate an interrupt when the state machines jumps out of the EOC state. See the *State Machine Interrupts* section for more information.
APCH	0xAA	[7]	CHG_ACIN	R	Charge source indicator. Value is 1 when charging from AC source and value is 0 when charging from other source.
APCH	0xAA	[6]	CHG_USB	R	Charge source indicator. Value is 1 when charging from USB source and value is 0 when charging from other source.
APCH	0xAA	[5:4]	CSTATE	R	Charge State. Values indicate the current charging state. See the *State Machine Interrupts* section for more information.
APCH	0xAA	[3:1]	-	R	Reserved.
APCH	0xAA	[0]	CHGLEVSTAT	R	CHGLEV pin status. Value is 0 if CHGLEVSTAT is logic low; value is 1 otherwise.
OTG	0xB0	[7]	ONQ1	R/W	OTG Q1 Enable Bit. Set bit to 1 to turn on Q1; clear bit to 0 to turn off Q1.
OTG	0xB0	[6]	ONQ2	R/W	OTG Q2 Enable Bit. Set bit to 1 to turn on Q2; clear bit to 0 to turn off Q2.
OTG	0xB0	[5]	ONQ3	R/W	OTG Q3 Enable Bit. Set bit to 1 to turn on Q3; clear bit to 0 to turn off Q3.
OTG	0xB0	[4]	Q1OK	R	OTG Q1 Status. Value is 0 if Q1 can not start up successfully, or in current limit status.
OTG	0xB0	[3]	Q2OK	R	OTG Q2 Status. Value is 0 if Q2 can not start up successfully, or in current limit status.
OTG	0xB0	[2]	VBUSSTAT	R	VBUS Interrupt Status. Value is 1 if an interrupt is generated by either INVBUSR or INVBUSF.
OTG	0xB0	[1]	DBILIMQ3	R/W	Set to 1 to double the current limit of Q3.
OTG	0xB0	[0]	VBUSDAT	R	VBUS status. Value is 1 if a valid charging source is present at VBUS. Value is 0 otherwise.
OTG	0xB2	[7]	INVBUSR	R/W	VBUS Interrupt control. Set this bit to 1 to generate an interrupt when connecting a charger to VBUS (rising edge of VBUS).
OTG	0xB2	[6]	INVBUSF	R/W	VBUS Interrupt control. Set this bit to 1 to generate an interrupt when disconnecting a charger to VBUS (falling edge of VBUS).
OTG	0xB2	[5:4]	-	R	Reserved.
OTG	0xB2	[3]	nFLTMSKQ1	R/W	Q1 Interrupt Mask. Set this bit to 1 to generate an interrupt when the over-current threshold for Q1 is triggered.
OTG	0xB2	[2]	nFLTMSKQ2	R/W	Q2 Interrupt Mask. Set this bit to 1 to generate an interrupt when the over-current threshold for Q2 is triggered.
OTG	0xB2	[1]	nVBUSMSK	R/W	VBUS Interrupt Mask. Set this bit to 1 unmask to VBUS connection and/or disconnection interrupt.
OTG	0xB2	[0]	-	R	Reserved.
INT	0xC1	[7:0]	INTADR	R	Global Interrupt Address. See the *Interrupt Service Routine Section* for more information.

①: Valid only when CHGIN UVLO Threshold<V_{CHGIN}<CHGIN OVP Threshold.

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		2.3		5.5	V
UVLO Threshold Voltage	V_{VSYS} Rising		3.45		V
UVLO Hysteresis	V_{VSYS} Falling		200		mV
Supply Current	All Regulators Enabled		420		µA
Shutdown Supply Current	All Regulators Disabled except REG9, V_{VSYS} =3.6V		30		µA
Oscillator Frequency		2.060	2.220	2.380	MHz
Logic High Input Voltage		1.4			V
Logic Low Input Voltage				0.4	V
nRSTO Delay			40		ms
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis			20		°C

STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = V_{VP3} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
UVLO_VP Threshold	Input Voltage Rising	2.5	2.6	2.7	V
UVLO_VP Hysteresis	Input Voltage Falling		100		mV
Standby Supply Current	Regulator Enabled, V_{VSYS} = 3.6V		68	95	µA
Shutdown Current	V_{VP} = 5.5V, Regulator Disabled		0	1	µA
Output Voltage Accuracy	V_{OUT} ≥ 1.2V, I_{OUT} = 10mA	-1.5%	V_{NOM}①	1.5%	V
Line Regulation	V_{VP} = Max (V_{NOM}① + 1, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT} = 10mA to IMAX②		0.0017		%/mA
Power Good Threshold	V_{OUT} Rising		93		%V_{NOM}
Power Good Hysteresis	V_{OUT} Falling		2.5		%V_{NOM}
Switching Frequency	V_{OUT} ≥ 20% of V_{NOM}	2.06	2.22	2.38	MHz
	V_{OUT} = 0V		520		kHz
Soft-Start Period	V_{OUT} = 3.3V		500		µs
Minimum On-Time			75	90	ns
REG1					
Maximum Output Current		1.2			A
Current Limit		1.70	2.00	2.75	A
PMOS On-Resistance	I_{SW1} = -100mA, V_{VSYS} = 3.6V		0.150		Ω
NMOS On-Resistance	I_{SW1} = 100mA, V_{VSYS} = 3.6V		0.120		Ω
SW1 Leakage Current	V_{VP1} = 5.5V, V_{SW1} = 0 or 5.5V		0	1	µA
REG2					
Maximum Output Current		1.2			A
Current Limit		1.70	2.00	2.75	A
PMOS On-Resistance	I_{SW2} = -100mA, V_{VSYS} = 3.6V		0.150		Ω
NMOS On-Resistance	I_{SW2} = 100mA, V_{VSYS} = 3.6V		0.120		Ω
SW2 Leakage Current	V_{VP2} = 5.5V, V_{SW2} = 0 or 5.5V		0	1	µA
REG3					
Maximum Output Current		0.95			A
Current Limit		1.10	1.45	1.85	A
PMOS On-Resistance	I_{SW3} = -100mA		0.150		Ω
NMOS On-Resistance	I_{SW3} = 100mA		0.120		Ω
SW3 Leakage Current	V_{VP3} = 5.5V, V_{SW3} = 0 or 5.5V		0	1	µA

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

STEP-UP DC/DC ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = V_{VP3} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		6	V
Operating Supply Current			0.8	1.7	mA
Standby Supply Current	No switching		80	150	μA
Shutdown Current	V_{VP} = 5.5V, Regulator Disabled		0.1	1	μA
Output Voltage Accuracy	V_{OUT} = 5V, I_{OUT} = 10mA	-3%	V_{NOM}①	3%	V
Line Regulation			0.019		%/V
Load Regulation			0.17		%/mA
Power Good Threshold	V_{OUT} Rising		93		$\%V_{NOM}$
Power Good Hysteresis	V_{OUT} Falling		7.5		$\%V_{NOM}$
Switching Frequency		1.032	1.110	1.188	MHz
Minimum On-Time			80		ns
Minimum Off-Time			40		ns
Maximum Output Current	V_{OUT} = 5V	0.6			A
Current Limit			1.35		A
Switch On-Resistance	I_{SW4} = 100mA		0.48		Ω
SW4 Leakage Current	V_{BAT} = 3.6V, V_{SW4} = 5V, REG4 disabled			10	μA

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

LOW-NOISE LDO ELECTRICAL CHARACTERISTICS

(V_{INL} = 3.6V, C_{OUT5} = C_{OUT6} = C_{OUT7} = C_{OUT8} = 2.2μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.4		5.5	V
Output Voltage Accuracy	V_{OUT} ≥ 1.2V, T_A = 25°C, I_{OUT} = 10mA	-1.5%	V_{NOM}①	1.5%	V
Line Regulation	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V, LOWIQ[ ] = [0]		0.5		mV/V
Load Regulation	I_{OUT} = 1mA to IMAX②		0.08		V/A
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 20mA, V_{OUT} =1.2V		80		dB
	f = 10kHz, I_{OUT} = 20mA, V_{OUT} =1.2V		70		
Supply Current per Output	Regulator Enabled		24	60	μA
	Regulator Disabled		0		
Soft-Start Period	V_{OUT} = 3.0V		100		μs
Power Good Threshold	V_{OUT} Rising		92		%
Power Good Hysteresis	V_{OUT} Falling		4		%
Output Noise	I_{OUT} = 20mA, f = 10Hz to 100kHz, V_{OUT} = 1.2V		30		$μV_{RMS}$
Discharge Resistance	LDO Disabled, DIS[ ] = 1		1.5		kΩ
REG5					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		130	200	mV
Maximum Output Current			350		mA
Current Limit④	V_{OUT} = 95% of regulation voltage	385	550		mA
Stable C_{OUT5} Range		2.2		20	μF
REG6					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		130	200	mV
Maximum Output Current			350		mA
Current Limit④	V_{OUT} = 95% of regulation voltage	385	550		mA
Stable C_{OUT6} Range		2.2		20	μF
REG7					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		160	300	mV
Maximum Output Current			250		mA
Current Limit④	V_{OUT} = 95% of regulation voltage	275	400		mA
Stable C_{OUT7} Range		2.2		20	μF
REG8					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		160	300	mV
Maximum Output Current			250		mA
Current Limit④	V_{OUT} = 95% of regulation voltage	275	400		mA
Stable C_{OUT8} Range		2.2		20	μF

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher).

④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 50% (typ)

LOW-IQ LDO ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, C_{OUT9} = C_{OUT10} = 1µF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REG9 (VDDRTC18) — V_{NOM} = 3.3V					
Operating Voltage Range	V_{OUT} =1.8V	2.5		5.5	V
Output Voltage Accuracy	I_{OUT} = 1mA	-2.5	V_{NOM} ①	3.5	%
Line Regulation	V_{VSYS} = V_{OUT} + 1.2V to V_{VSYS} = 5.5V		0.2		%/V
Supply Current from VSYS	V_{VSYS} = V_{OUT} + 1.2V		2		µA
	V_{VSYS} < V_{OUT} + 0.7V		10		
Maximum Output current		5			mA
Stable C_{OUT} Range		0.47			µF
REG10 (VDDRTC12) — V_{NOM} = 1.2V					
Operating Voltage Range		1.7		5.5	V
Output Voltage Accuracy	I_{OUT} = 1mA	-3.5	V_{NOM} ①	2.5	%
Line Regulation	V_{IN} = V_{OUT} + 0.5V to V_{IN} = 5.5V		0.2		%/V
Supply Current from V_{OUT9}			2		µA
Maximum Output current		5			mA
Stable C_{OUT} Range		0.22			µF

OTG SUBSYSTEM ELECTRICAL CHARACTERISTICS

(V_{INL} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
5VIN to VBUS (Q1)					
Switch on resistance	5VIN = 5V, I_{LOAD} = 100mA		0.23		Ω
Current Limit Threshold		500	700		mA
Current Limit Delay			256		ms
CHGIN to VBUS (Q2)					
Switch on resistance	CHGIN = 5V, I_{LOAD} = 100mA		0.34		Ω
Current Limit Threshold		500	700		mA
Current Limit Delay			256		ms

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

ActivePath™ CHARGER ELECTRICAL CHARACTERISTICS

(V_{CHGIN} = 5.0V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ActivePath					
CHGIN Operating Voltage Range		4.35		6.0	V
CHGIN UVLO Threshold	CHGIN Voltage Rising	3.1	3.5	3.9	V
CHGIN UVLO Hysteresis	CHGIN Voltage Falling		0.5		V
CHGIN OVP Threshold	CHGIN Voltage Rising	6.0	6.6	7.2	V
CHGIN OVP Hysteresis	CHGIN Voltage Falling		0.4		V
VBUS_UVLO Threshold	VBUS Voltage Rising	3.3	4.0	4.8	V
VBUS_UVLO Hysteresis	VBUS Voltage Falling		400		mV
CHGIN Supply Current	V_{CHGIN} < V_{UVLO}		35	70	µA
	V_{CHGIN} < V_{BAT} + 50mV, V_{CHGIN} > V_{UVLO}		100	200	µA
	V_{CHGIN} > V_{BAT} + 150mV, V_{CHGIN} > V_{UVLO} Charger disabled, I_{VSYS} = 0mA		1.2	2.0	mA
CHGIN to VSYS On-Resistance	I_{VSYS} = 100mA		0.25		Ω
CHGIN to VSYS Current Limit		1.5	2.25		A
VBUS Input Current Limit	CHGLEV = GA, V_{VSYS} =3.6V		75	110	mA
	CHGLEV = V_{VSYS}, DBILIMQ3[ ] = 0, V_{VSYS} =3.6V	400	450	500	
	CHGLEV = V_{VSYS}, DBILIMQ3[ ] = 1.		900		
VSYS REGULATION					
CHGIN to VSYS Regulated Voltage	I_{VSYS} = 10mA	4.45	4.6	4.8	V
nSTAT OUTPUT					
nSTAT Sink current	V_{nSTAT} = 2V	4	8	12	mA
nSTAT Leakage Current	V_{nSTAT} = 4.2V			1	µA
CHGLEV INPUTS					
CHGLEV Logic High Input Voltage		1.4			V
CHGLEV Logic Low Input Voltage				0.4	V
CHGLEV Leakage Current	V_{CHGLEV} = 4.2V			1	µA
TH INPUT					
TH Pull-Up Current	V_{CHGIN} > V_{BAT} + 100mV, Hysteresis = 50mV	91	100	109	µA
V_{TH} Upper Temperature Voltage Threshold (V_{THH})	Hot Detect NTC Thermistor	2.45	2.50	2.54	V
V_{TH} Lower Temperature Voltage Threshold (V_{THL})	Cold Detect NTC Thermistor	0.482	0.50	0.518	V
V_{TH} Hysteresis	Upper and Lower Thresholds		40		mV

ActivePath™ CHARGER ELECTRICAL CHARACTERISTICS CONT'D

(V_{CHGIN} = 5.0V, T_A = 25°C, unless otherwise specified.)

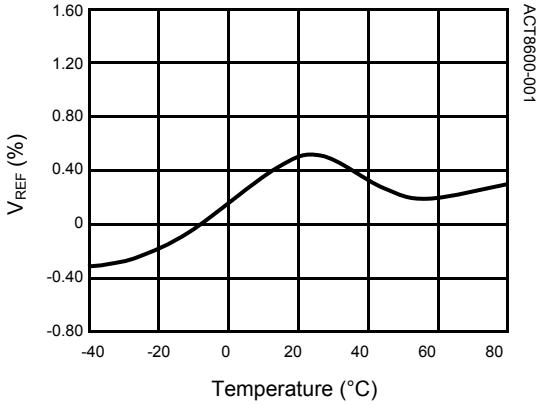
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CHARGER						
BAT Reverse Leakage Current	V_{CHGIN} = 0V, V_{BAT} = 4.2V, I_{VSYS} = 0mA, All REGs are OFF.			15		µA
BAT to VSYS On-Resistance				70		mΩ
ISET Pin Voltage	Fast Charge			1.2		V
	Precondition			0.13		
Charge Termination Voltage	T_A = -20°C to 70°C		4.179	4.200	4.221	V
	T_A = -40°C to 85°C		4.170	4.200	4.230	
Charge Current	V_{BAT} = 3.8V	AC-Mode	-10%	I_{CHG} ①	+10%	mA
		USB-Mode, CHGLEV = GA		Min (75mA, I_{CHG})		
		USB-Mode, CHGLEV = V_{VSYS}, DBILIMQ3[ ] = 0.		Min (450mA, I_{CHG})		
		USB-Mode, CHGLEV = V_{VSYS}, DBILIMQ3[ ] = 1.		Min (900mA, I_{CHG})		
Precondition Charge Current	V_{BAT} = 2.7V	AC-Mode		10% I_{CHG}		mA
		USB-Mode, CHGLEV = GA		Min (75mA, 10% × I_{CHG})		
		USB-Mode, CHGLEV = V_{VSYS}, DBILIMQ3[ ] = 0.		10% I_{CHG}		
		USB-Mode, CHGLEV = V_{VSYS}, DBILIMQ3[ ] = 1.		10% I_{CHG}		
Precondition Threshold Voltage	V_{BAT} Voltage Rising		2.7	2.9	3.1	V
Precondition Threshold Hysteresis	V_{BAT} Voltage Falling			150		mV
END-OF-CHARGE Current Threshold	V_{BAT} = 4.15V	AC-Mode, CHGLEV = V_{VSYS}		10% I_{CHG}		mA
		AC-Mode, CHGLEV = GA		10% I_{CHG}		
		USB-Mode, CHGLEV = V_{VSYS}		45		
		USB-Mode, CHGLEV = GA		45		
Charge Restart Threshold	V_{VSYS} - V_{BAT}, V_{BAT} Falling		170	200	230	mV
Precondition Safety Timer	PRETIMO[ ] = 10			80		min
Total Safety Timer	TOTTIMO[ ] = 10			6.5		hr
Thermal Regulation Threshold				100		°C

①: R_{ISET} (kΩ) = 2336 × (1V/I_{CHG} (mA)) - 0.205

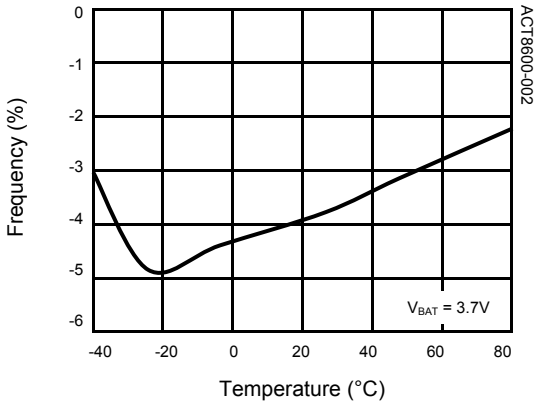
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

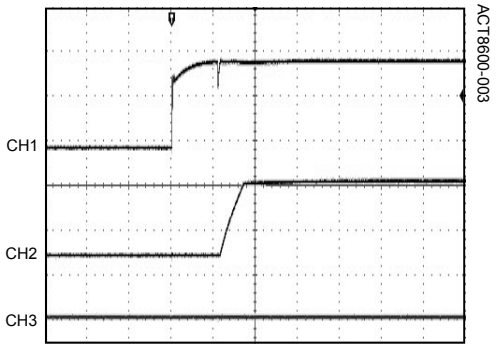
V_{REF} vs. Temperature



Frequency vs. Temperature

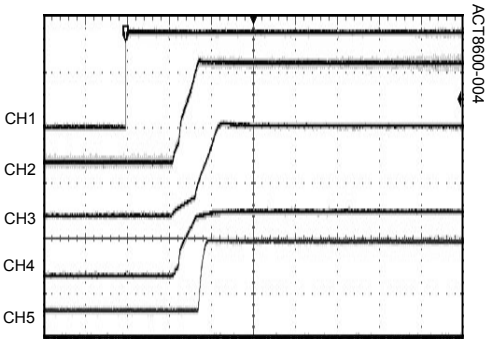


VBAT Connect



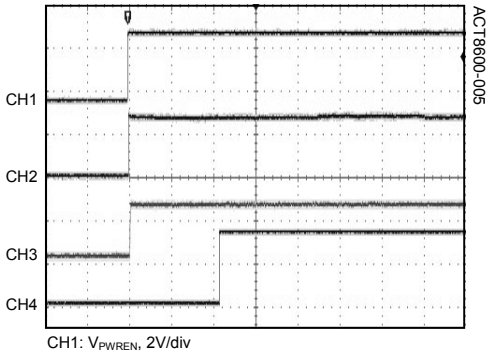
CH1: V_{BAT}, 2V/div
CH2: V_{OUT9}, 2V/div
CH3: V_{OUT10}, 1V/div
TIME: 400µs/div

PWREN Sequence



CH1: V_{PWREN}, 2V/div
CH2: V_{OUT3}, 1V/div
CH3: V_{OUT2}, 2V/div
CH4: V_{OUT1}, 1V/div
CH5: V_{OUT5}, 2V/div
TIME: 400µs/div

nRSTO Startup Sequence

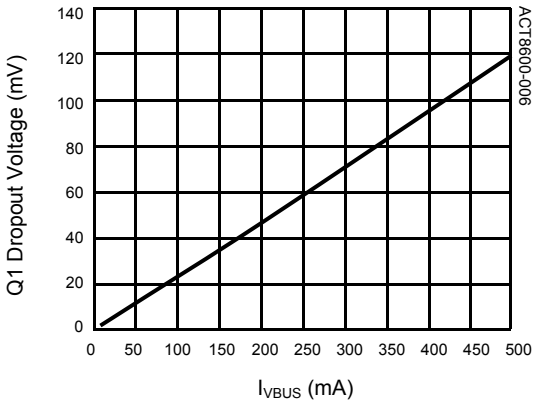


CH1: V_{PWREN}, 2V/div
CH2: V_{OUT3}, 1V/div
CH3: V_{OUT1}, 1V/div
CH4: V_{nRSTO}, 2V/div
TIME: 20ms/div

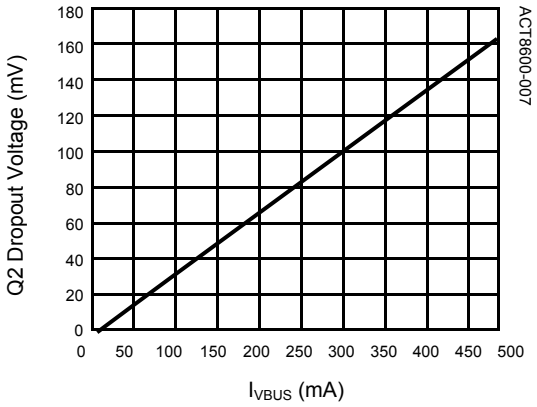
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

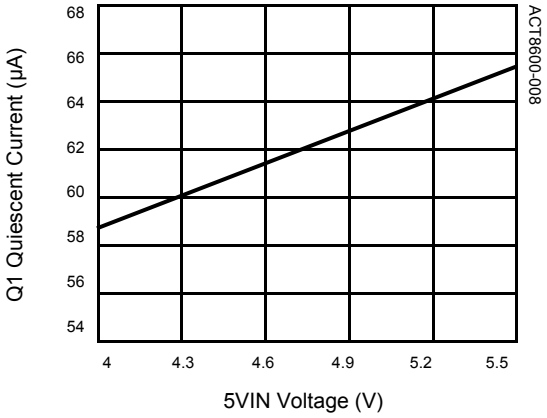
Q1 Dropout Voltage vs. I_{VBUS}



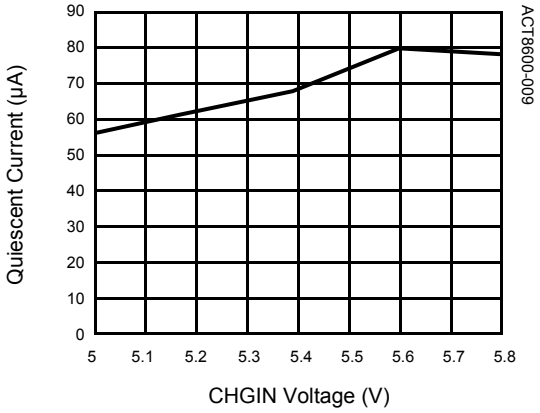
Q2 Dropout Voltage vs. I_{VBUS}



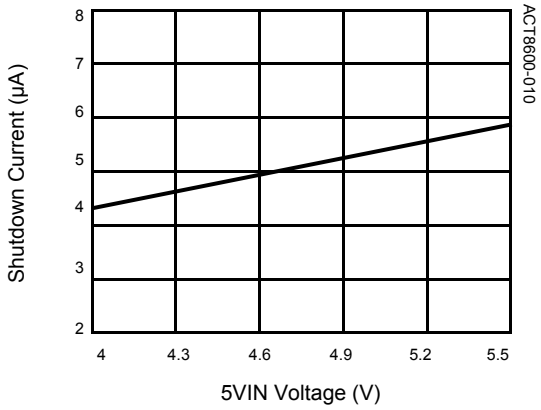
Q1 Quiescent Current vs. 5VIN Voltage



Q2 Quiescent Current vs. CHGIN Voltage



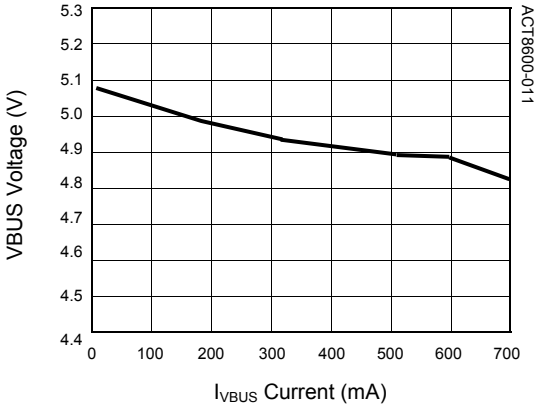
Q1 Shutdown Current vs. 5VIN Voltage



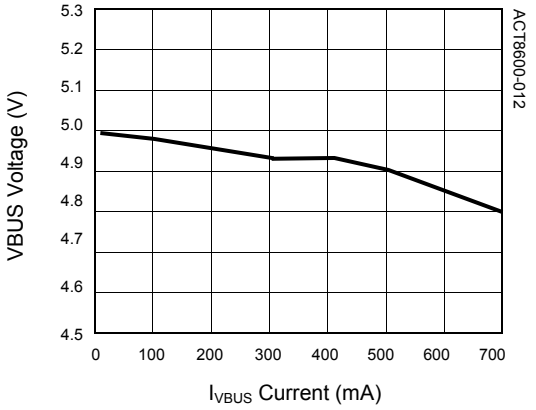
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

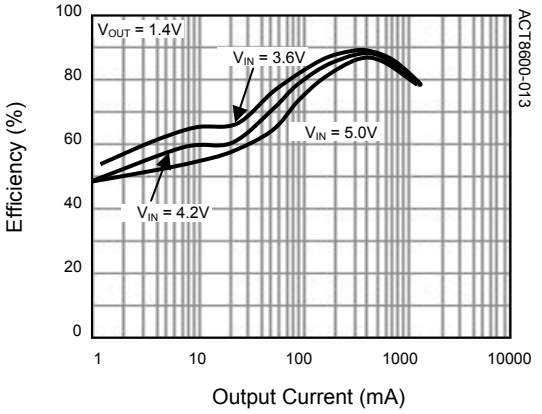
VBUS Voltage vs. I_{VBUS} Current (Supplied from 5VIN)



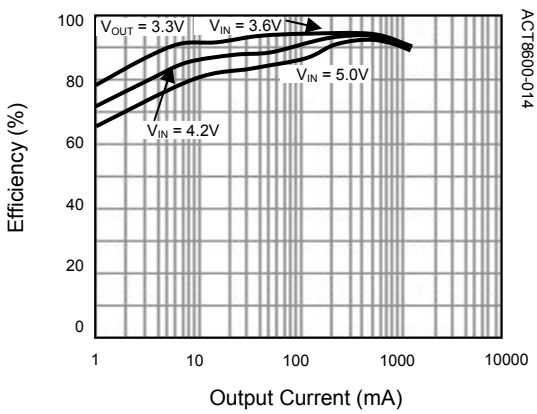
VBUS Voltage vs. I_{VBUS} (CHGIN Supply)



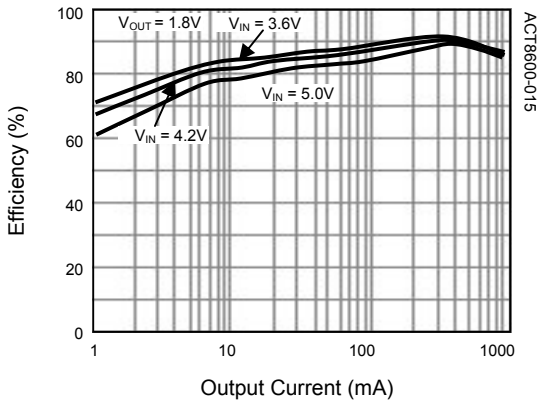
REG1 Efficiency vs. Output Current



REG2 Efficiency vs. Output Current



REG3 Efficiency vs. Output Current



REG4 Efficiency vs. Output Current