Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ACT8810

Rev 9, 15-Nov-12

Eight Channel *ActivePath*™ Power Management IC

FEATURES

- ***ActivePath***™ **Li+ Charger with System Power Selection**
- **Six Integrated Regulators**
  - **1.3A High Efficiency Step-Down DC/DC**
  - **1.0A High Efficiency Step-Down DC/DC**
  - **0.55A High Efficiency Step-Down DC/DC**
  - **2×360mA Low Noise, High PSRR LDOs**
  - **30mA RTC LDO / Backup Battery Charger**
- **I²C™ Serial Interface**
- **Minimal External Components**
- **Compatible with USB or AC-Adapter Charging**
- **5mm × 5mm, Thin-QFN (TQFN55-40) Package**
  - **Only 0.75mm Height**
  - **RoHS Compliant**

APPLICATIONS

- **Personal Navigation Devices**
- **Portable Media Players**
- **Smart Phones**

GENERAL DESCRIPTION

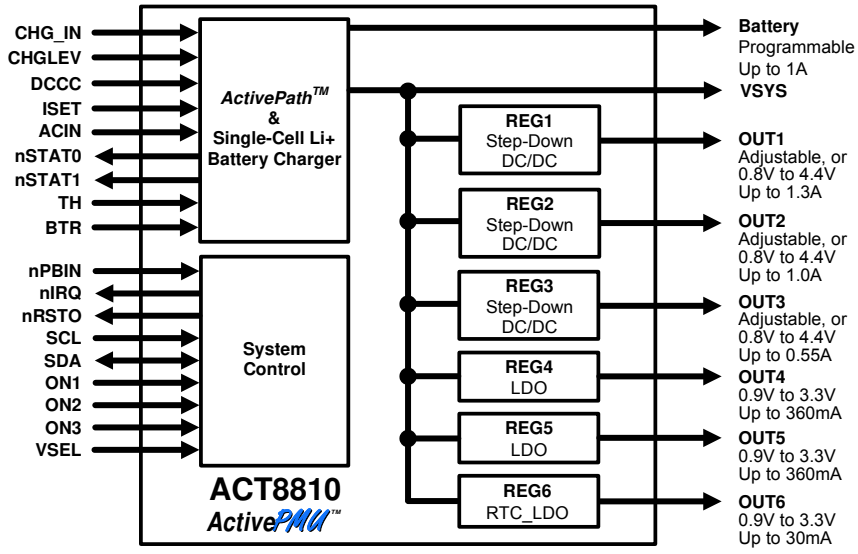
The patent-pending ACT8810 is a complete, cost effective, highly-efficient *ActivePMU*™ power management solution that is ideal for a wide range of high performance portable handheld applications such as personal navigation devices (PNDs). This device integrates the *ActivePath*™ complete battery charging and management system with six power supply channels.

The *ActivePath* architecture automatically selects the best available input supply for the system. If the external input source is not present or the system load current is more than the input source can provide, the *ActivePath* supplies additional current from the battery to the system. The charger is a complete, thermally-regulated, stand-alone single-cell linear Li+ charger that incorporates an internal power MOSFET.

REG1, REG2, and REG3 are three independent, fixed-frequency, current-mode step-down DC/DC converters that output 1.3A, 1.0A, and 0.55A, respectively. REG4 and REG5 are high performance, low-noise, low-dropout linear regulators that output up to 360mA each. REG6 is a RTC LDO that outputs up to 30mA for a real time clock. Finally, an I²C serial interface provides programmability for the DC/DC converters and LDOs.

The ACT8810 is available in a tiny 5mm x 5mm 40-pin Thin-QFN package that is just 0.75mm thin.

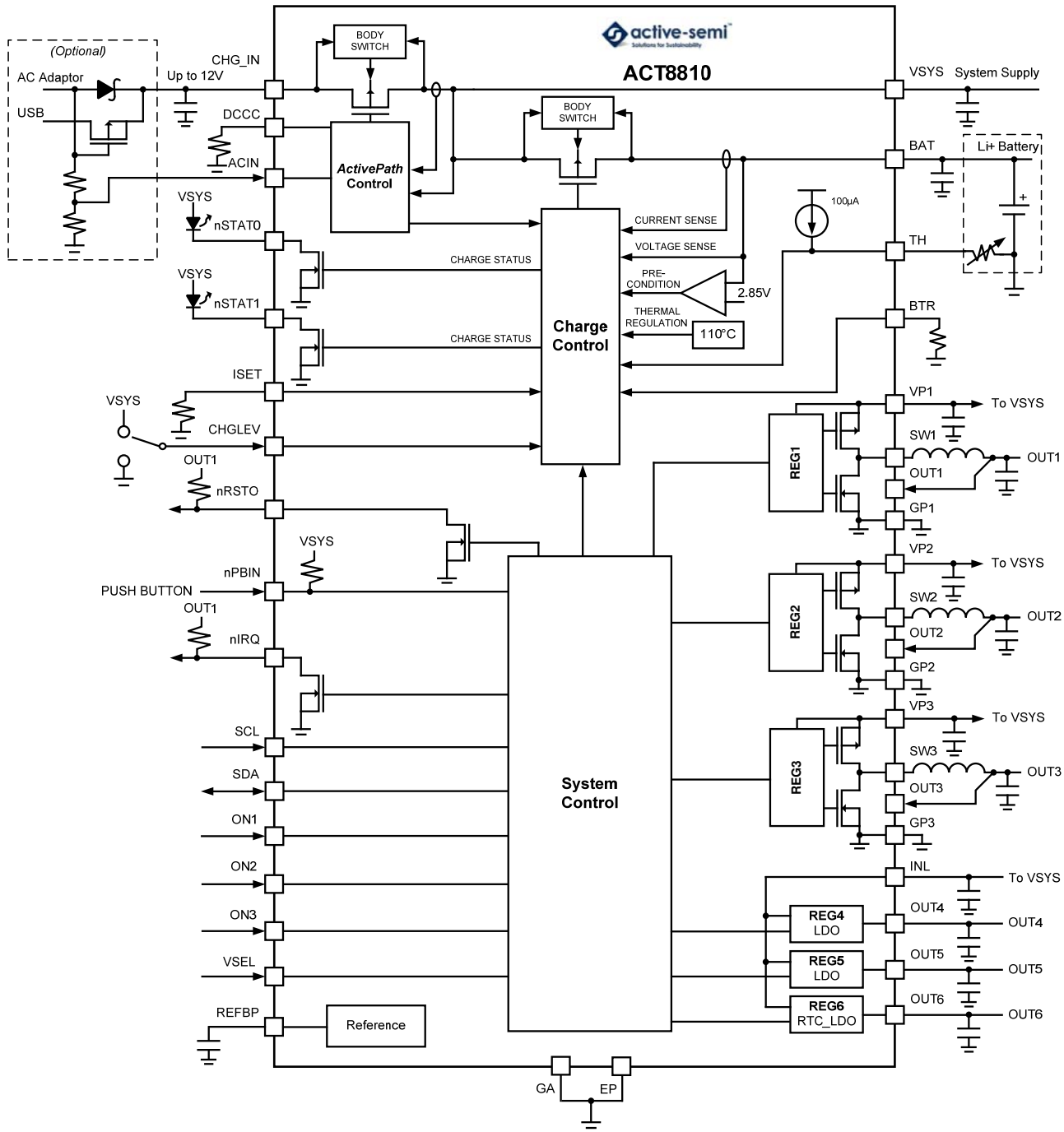
SYSTEM BLOCK DIAGRAM



Pb-free

TABLE OF CONTENTS

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION①

PART NUMBER	V_{OUT1}/V_{STBY1}②	V_{OUT2}/V_{STBY2}	V_{OUT3}/V_{STBY3}	V_{OUT4}	V_{OUT5}	V_{OUT6}	CONTROL SEQUENCE③
ACT8810QJ1C1-T	3.3V/3.3V	1.1V/1.2V	1.2V/1.2V	1.2V	2.8V	3.3V	Sequence A
ACT8810QJ213-T	1.2V/1.2V	1.8V/1.8V	1.0V/1.0V	3.3V	1.2V	3.0V	Sequence B
ACT8810QJ3EB-T	3.3V/3.3V	1.2V/1.2V	1.8V/1.8V	1.5V	2.8V	3.3V	Sequence C
ACT8810QJ420-T	3.3V/3.3V	1.8V/1.8V	1.1V/1.2V	1.2V	3.3V	2.5V	Sequence D
ACT8810QJ50F-T	1.2V/1.2V	3.3V/3.3V	1.8V/1.8V	3.3V	1.8V	3.0V	Sequence E

PACKAGING DETAILS	PACKAGE	PINS	TEMPERATURE RANGE	PACKING
ACT8810QJ###-T	TQFN55-40	40	-40°C to +85°C	TAPE & REEL

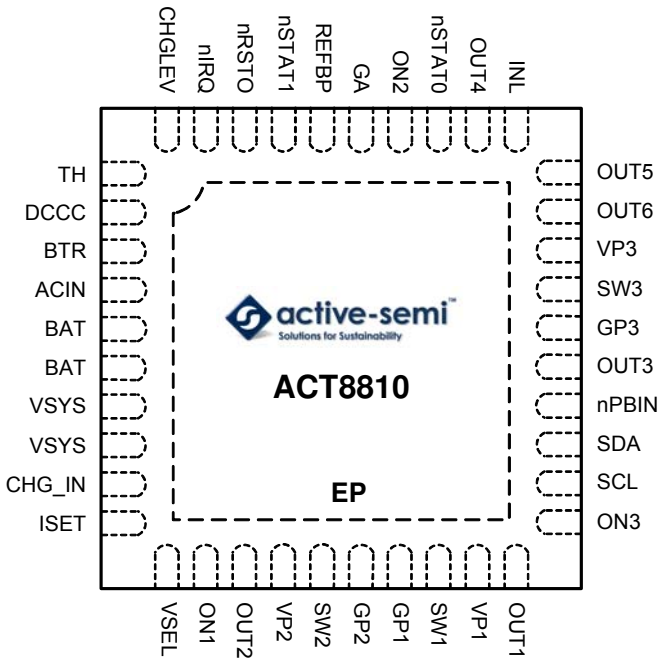
①: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

②: To select V_{STBYx} as a output regulation voltage of REGx, tie VSEL to VSYS or a logic high.

③: Refer to the Control Sequence section for more information.

PIN CONFIGURATION

TOP VIEW



Thin - QFN (TQFN55-40)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	TH	Temperature Sensing Input. Connect to battery thermistor. TH is pulled up with a 100µA current internally. See the *Battery Temperature Monitoring* section for more information.
2	DCCC	Dynamic Charging Current Control. Connect a resistor to set the dynamic charging current control point. A internal 100µA current source sets up a voltage that is used to compare with VSYS and dynamically scale the charging current to maintain VSYS regulation. See the *Dynamic Charge Current Control* section for more information.
3	BTR	Safety Timer Program Pin. The resistance between this pin and GA determines the timers timeout values. See the *Charging Safety Timers* section for more information.
4	ACIN	AC Adaptor Detect. Detects presence of a wall adaptor and automatically adjusts the charge current to the maximum charge current level. Do not leave ACIN floating.
5, 6	BAT	Battery Charger Output. Connect this pin directly to the battery anode (+ terminal)
7, 8	VSYS	System Output Pin. Bypass to GA with a 10µF or larger ceramic capacitor.
9	CHG_IN	Power Input for the Battery Charger. Bypass CHG_IN to GA with a capacitor placed as close to the IC as possible. The battery charger are automatically enabled when a valid voltage is present on CHG_IN. See the *CHG_IN Bypass Capacitor Selection* section for more information.
10	ISET	Charge Current Set. Program the maximum charge current by connecting a resistor (R_{ISET}) between ISET and GA. See the *Charger Current Programming* section for more information.
11	VSEL	Step-Down DC/DCs Output Voltage Selection. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage. See the *Output Voltage Selection Pin* section for more information.
12	ON1	Independent Enable Control Input for REG1. Drive ON1 to VSYS or to a logic high for normal operation, drive to GA or a logic low to disable REG1. Do not leave ON1 floating.
13	OUT2	Output Feedback Sense for REG2. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
14	VP2	Power Input for REG2. Bypass to GP2 with a high quality ceramic capacitor placed as close as possible to the IC.
15	SW2	Switching Node Output for REG2. Connect this pin to the switching end of the inductor.
16	GP2	Power Ground for REG2. Connect GA, GP1, GP2 and GP3 together at a single point as close to the IC as possible.
17	GP1	Power Ground for REG1. Connect GA, GP1, GP2 and GP3 together at a single point as close to the IC as possible.
18	SW1	Switching Node Output for REG1. Connect this pin to the switching end of the inductor.
19	VP1	Power Input for REG1. Bypass to GP1 with a high quality ceramic capacitor placed as close as possible to the IC.
20	OUT1	Output Feedback Sense for REG1. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
21	ON3	Enable Control Input for REG3. Drive ON3 to a logic high for normal operation, drive to GA or a logic low to disable REG3. Do not leave ON3 floating.
22	SCL	Clock Input for I^2C Serial Interface.
23	SDA	Data Input for I^2C Serial Interface. Data is read on the rising edge of SCL.

PIN DESCRIPTIONS CONT'D

PIN	NAME	DESCRIPTION
24	nPBIN	Master Enable Input. Drive nPBIN to GA through a 100kΩ resistor to enable the IC, drive nPBIN directly to GA to assert a Hard-Reset condition. Refer to the *System Startup & Shutdown* and *Control Sequence* sections for more information. nPBIN is internally pulled up to VSYS through a 50kΩ resistor.
25	OUT3	Output Feedback Sense for REG3. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
26	GP3	Power Ground for REG3. Connect GA, GP1, GP2, and GP3 together at a single point as close to the IC as possible.
27	SW3	Switching Node Output for REG3. Connect this pin to the switching end of the inductor.
28	VP3	Power Input for REG3. Bypass to GP3 with a high quality ceramic capacitor placed as close as possible to the IC.
29	OUT6	RTC LDO Output Voltage. Capable of delivering up to 30mA of output current.
30	OUT5	Output Voltage for REG5. Capable of delivering up to 360mA of output current. The output is discharged to GA with 1kΩ when disabled.
31	INL	Power Input for REG4, REG5, and REG6. Bypass to GA with a high quality ceramic capacitor placed as close as possible to the IC.
32	OUT4	Output Voltage for REG4. Capable of delivering up to 360mA of output current. The output is discharged to GA with 1kΩ when disabled.
33	nSTAT0	Active-Low Open-Drain Charger Status Output. nSTAT0 has a 5mA (typ) current limit, allowing it to directly drive an indicator LED without additional external components. To generate a logic-level output, connect nSTAT0 to an appropriate supply voltage (typically VSYS) through a 10kΩ or greater pull-up resistor. See the *Charge Status Indication* section for more information.
34	ON2	Independent Enable Control Input for REG2. Drive ON2 to a logic high for normal operation, drive to GA or a logic low to disable REG2. Do not leave ON2 floating.
35	GA	Analog Ground. Connect GA directly to a quiet ground node. Connect GA, GP1, GP2, and GP3 together at a single point as close to the IC as possible.
36	REFBP	Reference Noise Bypass. Connect a 0.01µF ceramic capacitor from REFBP to GA. This pin is discharged to GA in shutdown.
37	nSTAT1	Active-Low Open-Drain Charger Status Output. nSTAT1 has a 5mA (typ) current limit, allowing it to directly drive an indicator LED without additional external components. To generate a logic-level output, connect nSTAT1 to an appropriate supply voltage (typically VSYS) through a 10kΩ or greater pull-up resistor. See the *Charge Status Indication* section for more information.
38	nRSTO	Open-Drain Reset Output. nRSTO asserts low whenever REG1 is out of regulation, and remains low for 260ms (typ) after REG1 reaches regulation.
39	nIRQ	Open-Drain Interrupt Output. nIRQ asserts any time nPBIN is asserted or an unmasked fault condition exists. See the *nIRQ Output* section for more information.
40	CHGLEV	Charging State Select Input. When ACIN = 0 charge current is internally set; Drive CHGLEV to a logic-high for high-current USB charging mode (maximum charge current is 500mA), drive CHGLEV to a logic-low for low-current USB charging mode (maximum charge current is 100mA). When ACIN = 1 charge current is externally set by R_{ISET}; Drive CHGLEV to a logic-high to for high-current charging mode (ISET (mA) = K_{ISET} × 1V/(R_{ISET} (kΩ) +0.031) where K_{ISET} = 628), drive CHGLEV to a logic-low for low-current charging mode (ISET (mA) = K_{ISET} × 1V/(R_{ISET} (kΩ) + 0.031) where K_{ISET} = 314). Do not leave CHGLEV floating.
EP	EP	Exposed Pad. Must be soldered to ground on the PCB.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
CHG_IN to GA t < 1ms and duty cycle <1% Steady State	 -0.3 to +18 -0.3 to +14	 V V
VP1 to GP1, VP2 to GP2, VP3 to GP3	-0.3 to +6	V
BAT, VSYS, INL to GA	-0.3 to +6	V
SW1, OUT1 to GP1	-0.3 to (V_{VP1} +0.3)	V
SW2, OUT2 to GP2	-0.3 to (V_{VP2} +0.3)	V
SW3, OUT3 to GP3	-0.3 to (V_{VP3} +0.3)	V
ON1, ON2, ON3, ISET, ACIN, VSEL, DCCC, CHGLEV, TH, SCL, SDA, REFBP, nIRQ, nRSTO, nSTAT0, nSTAT1, BTR, nPBIN to GA	-0.3 to +6	V
OUT4, OUT5, OUT6 to GA	-0.3 to (V_{INL} +0.3)	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Junction Temperature	125	°C
Maximum Power Dissipation TQFN55-40 (Thermal Resistance θ_{JA} = 30°C/W)	2.7	W
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

REGISTER DESCRIPTIONS

Table 1:

Global Register Map

OUTPUT	ADDRESS									DATA (DEFAULT VALUE)							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
SYS	06h	0	0	0	0	0	1	1	0	R	R	R	0	R	R	1	R
REG1	10h	0	0	0	1	0	0	0	0	R	R	V	V	V	V	V	V
REG1	11h	0	0	0	1	0	0	0	1	R	R	R	R	R	R	R	R
REG1	12h	0	0	0	1	0	0	1	0	R	R	R	R	R	0	R	1
REG1	13h	0	0	0	1	0	0	1	1	R	V	V	V	V	V	V	V
REG2	20h	0	0	1	0	0	0	0	0	R	R	V	V	V	V	V	V
REG2	21h	0	0	1	0	0	0	0	1	R	R	R	R	R	R	R	R
REG2	22h	0	0	1	0	0	0	1	0	R	R	R	R	R	0	R	1
REG2	23h	0	0	1	0	0	0	1	1	R	V	V	V	V	V	V	V
REG3	30h	0	0	1	1	0	0	0	0	R	R	V	V	V	V	V	V
REG3	31h	0	0	1	1	0	0	0	1	R	R	R	R	R	R	R	R
REG3	32h	0	0	1	1	0	0	1	0	R	R	R	R	R	0	R	1
REG3	33h	0	0	1	1	0	0	1	1	R	V	V	V	V	V	V	V
REG4	40h	0	1	0	0	0	0	0	0	1	R	1	V	V	V	V	V
REG4	43h	0	1	0	0	0	0	1	1	R	R	R	R	R	R	0	R
REG5	41h	0	1	0	0	0	0	0	1	1	R	1	V	V	V	V	V
REG6	42h	0	1	0	0	0	0	1	0	R	R	R	V	V	V	V	V

KEY:

R: Read-Only bits. No Default Assigned.

V: Default Values Depend on Voltage Option. Default Values May Vary.

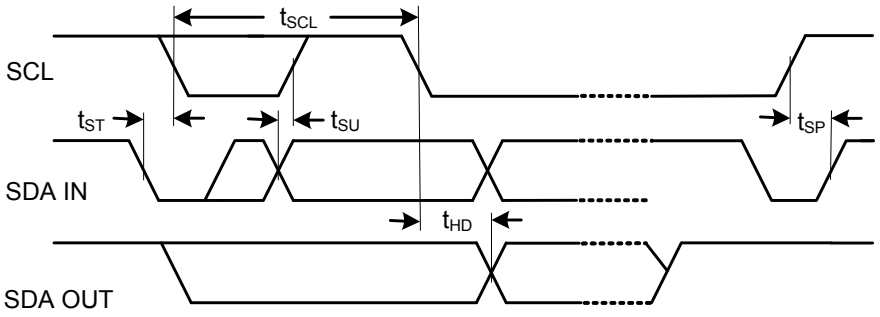
Note: Addresses other than those specified in Table 1 may be used for factory settings. Do not access any registers other than those specified in Table 1.

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Low Input Voltage	V_{VSYS} = 2.6V to 5.5V, T_A = -40ºC to 85ºC			0.35	V
SCL, SDA High Input Voltage	V_{VSYS} = 2.6V to 5.5V, T_A = -40ºC to 85ºC	1.55			V
SCL, SDA Leakage Current				1	µA
SDA Low Output Voltage	I_{OL} = 5mA			0.3	V
SCL Clock Period, t_{SCL}		2.5			µs
SDA Data In Setup Time to SCL High, t_{SU}		100			ns
SDA Data Out Hold Time after SCL Low, t_{HD}		300			ns
SDA Data Low Setup Time to SCL Low, t_{ST}	Start Condition	100			ns
SDA Data High Hold Time after Clock High, t_{SP}	Stop Condition	100			ns

Figure 1:
I²C Serial Bus Timing



ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		2.6		5.5	V
UVLO Threshold Voltage	VSYS Rising	2.35	2.5	2.6	V
UVLO Hysteresis	VSYS Falling		100		mV
VSYS Supply Current	ONx = VSYS		70		µA
VSYS Shutdown Current	ONx = GA, Not Charging		30		µA
Voltage Reference		1.24	1.25	1.26	V
Oscillator Frequency		1.35	1.6	1.85	MHz
Logic High Input Voltage	ON1, ON2, ON3, VSEL	1.4			V
Logic Low Input Voltage	ON1, ON2, ON3, VSEL			0.4	V
Leakage Current	V_{ON1} = V_{ON2} = V_{ON3} = V_{VSEL} = V_{nIRQ} = V_{nRSTO} = 4V			1	µA
nPBIN Internal Pull-up Resistance			50		kΩ
Low Level Output Voltage	nIRQ, nRSTO. Sinking 10mA		0.3		V
nRSTO Delay			260		ms
Thermal Shutdown Temperature	Temperature Rising		160		°C
Thermal Shutdown Hysteresis	Temperature Decreasing		20		°C

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 2:

Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
06h	R	R	R	W/E	R	R	nPBMASK	PBSTAT

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1.

Table 3:

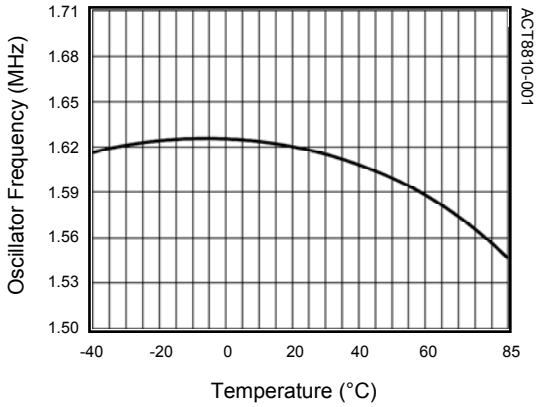
Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
06h	PBSTAT	[0]	R/W	Push Button Status	0	De-assert
					1	Asserted
06h	nPBMASK	[1]	R/W	Push Button Interrupt Mask Option	0	Masked
					1	Not Mask
06h		[3:2]	R		READ ONLY	
06h		[4]	W/E		WRITE-EXACT	
06h		[7:5]	R		READ ONLY	

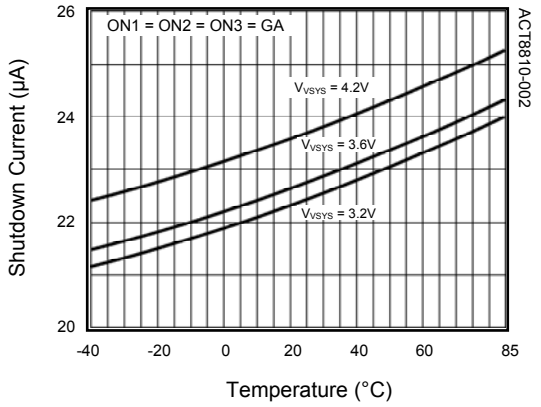
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

Oscillator Frequency vs. Temperature



Shutdown Current vs. Temperature



FUNCTIONAL DESCRIPTION

General Description

The ACT8810 offers a wide array of system management functions that allow it to be configured for optimal performance in a wide range of applications.

I²C Serial Interface

At the core of the ACT8810's flexible architecture is an I²C interface that permits optional programming capability to enhance overall system performance.

To ensure compatibility with a wide range of system processors, the ACT8810 uses standard I²C commands; I²C write-byte commands are used to program the ACT8810, and I²C read-byte commands are used to read the ACT8810's internal registers. The ACT8810 always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation, [1011010x].

SDA is a bi-directional data line and SCL is a clock input. The master initiates a transaction by issuing a START condition, defined by SDA transitioning from high to low while SCL is high. Data is transferred in 8-bit packets, beginning with the MSB, and is clocked-in on the rising edge of SCL. Each packet of data is followed by an "Acknowledge" (ACK) bit, used to confirm that the data was transmitted successfully.

For more information regarding the I²C 2-wire serial interface, go to the NXP website: http://www.nxp.com

System Startup and Shutdown

Startup Sequence

The ACT8810 features a flexible enable architecture that allows it to support a variety of push-button enable/disable schemes. Although other startup routines are possible, ACT8810 provides three typical startup and shutdown processes proceed as shown in *Control Sequence* section.

Shutdown Sequence

Once a successful power-up routine is completed, a shutdown process may be initiated by asserting nPBIN a second time, typically as the result of pressing the push-button. Although the shutdown process is completely software-controlled, a typical shutdown sequence proceeds as follows: The second assertion of nPBIN asserts nPBIN and interrupts the microprocessor, which then initiates an interrupt service routine to reveal that nPBIN has been asserted. If there is no input to the charger, then the microprocessor disables each regulator according to the sequencing requirements of the system, then the system will finally be disabled when each of ON1, ON2, and ON3 have been de-asserted.

nPBIN Input

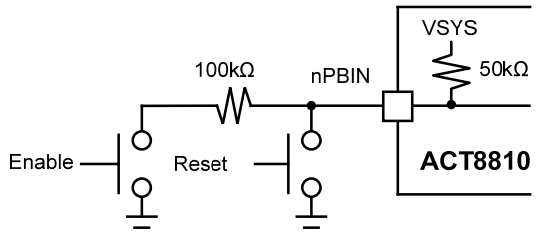
ACT8810's nPBIN pin is a dual-function pin, combining system enable/disable control with a hardware reset function. Refering to Figure 2, the two pin functions are obtained by asserting this pin low, either through a direct connection or through a 100kΩ resistor, as described below.

In most applications, nPBIN will be driven through a 100kΩ resistor. When driven in this way, nPBIN initiates system startup or shutdown, as described in the System Startup and Shutdown section.

When a hardware-reset function is desired, nPBIN may also be driven directly to GA. In this case, nRSTO is immediately asserted low and remains low until nPBIN is de-asserted and the reset timeout period expires. This provides a hardware-reset function, allowing the system to be manually reset if the system processor locks up.

Although a typical application will use momentary switches to drive nPBIN, as shown in Figure 2, nPBIN may also be driven by other sources, such as a GPIO or other logic output.

Figure 2:
nPBIN Input



Enable/Disable Inputs (ON1, ON2 and ON3)

The ACT8810 provides three manual enable/disable inputs, ON1, ON2 and ON3, which

FUNCTIONAL DESCRIPTION CONT'D

enable and disable REG1, REG2, and REG3, respectively. Once the system is enabled, the system will remain enabled until all of ON1, ON2, and ON3 have been de-asserted. See the *Control Sequence* section for more information.

Power-On Reset Output

nRSTO is an open-drain output which asserts low upon startup or when nPBIN is driven directly to GA, and remains asserted low until the 260ms (default) power-on reset timer has expired. Connect a 10kΩ or greater pull-up resistor from nRSTO to an appropriate voltage supply.

nIRQ Output

nIRQ is an open-drain output that asserts low any time startup or an unmasked fault condition exists. When asserted, nIRQ remains low until the microprocessor polls the ACT8810's I^2C interface. The ACT8810 supports a variety of other fault conditions, which may each be optionally unmasked via the I^2C interface. For more information about the available fault conditions, refer to the appropriate sections of this datasheet.

Connect a pull-up resistor from nIRQ to an appropriate voltage supply. nIRQ is typically used to drive the interrupt input of the system processor, and is useful in a variety of software-controlled enable/disable control routines.

Thermal Shutdown

The ACT8810 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions. This circuitry disables all regulators if the ACT8810 die temperature exceeds 160°C, and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ).

Control Sequence

Sequence A

The ACT8810QJ1## which is set with "sequence A", has a system startup is initiated whenever the following conditions occurs:

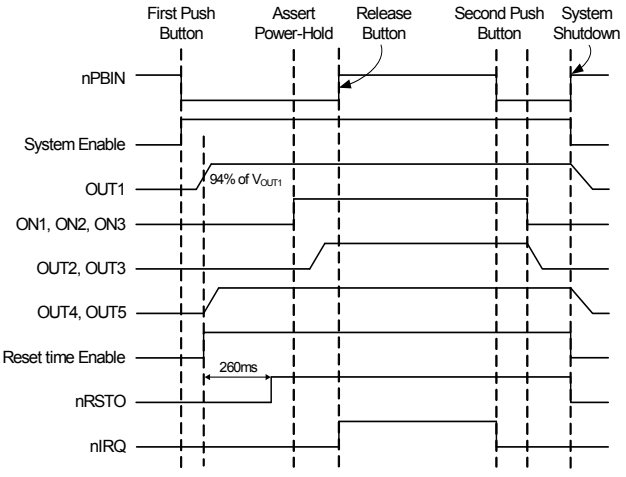
1) nPBIN is pushed low via 100kΩ resistance,

When ever this condition exists, the ACT8810QJ1## begins its system startup procedure by enabling REG1. When REG1 reaches 94% of its final regulation voltage, ACT8810QJ1## automatically turns on REG4 and REG5 and nRSTO is asserted low, holding the microprocessor in reset for a user-selectable reset period of 260ms. If V_{OUT1} is within 6% of its regulation voltage when the reset timer expires, the nRSTO is de-asserted, and the microprocessor can begin its power-up sequence. Once the power-up routine is successfully completed, the system remains enabled after the push-button is released as long as the microprocessor asserts any one of ON1, ON2 or ON3, and REG4, REG5 may be enabled or disabled via the I^2C interface.

This start-up procedure requires that the pushbutton be held until the microprocessor assumes control (by asserting any one of ON1, ON2, and ON3), providing protection against inadvertent momentary assertions of the pushbutton. If desired, longer "push-and-hold" times can be easily implemented by simply adding an additional time delay before asserting ON1, ON2, or ON3. If the microprocessor is unable to complete its power-up routine successfully before the user lets go of the push-button, the ACT8810QJ1## automatically shuts itself down.

Figure 3:

Sequence A



Sequence B

The ACT8810QJ2## which is set with "sequence B", has a system startup is initiated whenever the following conditions occurs:

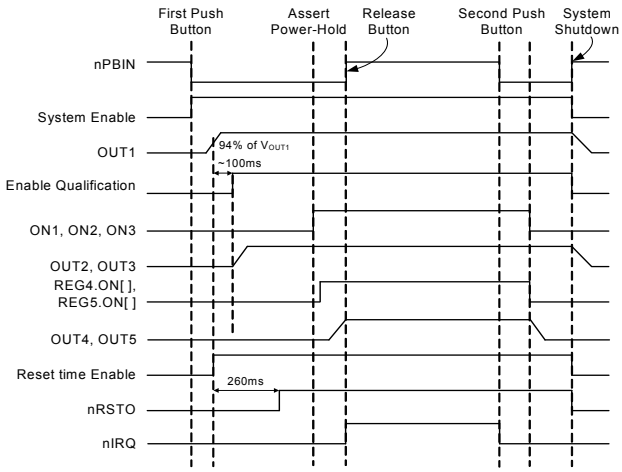
1) nPBIN is pushed low via 100kΩ resistance,

When ever this condition exists, the ACT8810QJ2## begins its system startup procedure by enabling REG1. When REG1 reaches 94% of its final regulation voltage, ACT8810QJ2## automatically turns on REG2 and REG3 and nRSTO is asserted low, holding the microprocessor in reset for a user-selectable reset period of 260ms. If V_{OUT1} is within 6% of its regulation voltage when the reset timer expires, the nRSTO is de-asserted, and the microprocessor can begin its power-up sequence. Once the power-up routine is successfully completed, the system remains enabled after the push-button is released as long as the microprocessor asserts any one of ON1, ON2 or ON3. REG4 and REG5 may be enabled if the microprocessor sets REG4.ON[ ] and REG5.ON[ ] to 1 via the I^2C interface. In other case, REG4 and REG5 are disable.

This start-up procedure requires that the pushbutton be held until the microprocessor assumes control (by asserting any one of ON1, ON2, and ON3), providing protection against inadvertent momentary assertions of the pushbutton. If desired, longer "push-and-hold" times can be easily implemented by simply adding an additional time delay before asserting ON1, ON2, or ON3. If the microprocessor is unable to complete its power-up routine successfully before the user lets go of the push-button, the ACT8810QJ2## automatically shuts itself down.

Figure 4:

Sequence B



Sequence C

The ACT8810QJ3## which is set with "sequence C", has a system startup is initiated whenever the following conditions occurs:

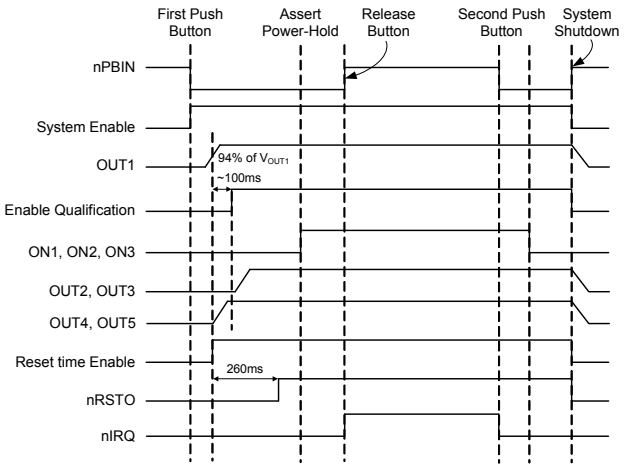
1) nPBIN is pushed low via 100kΩ resistance,

When ever this condition exists, the ACT8810QJ3## begins its system startup procedure by enabling REG1. When REG1 reaches 94% of its final regulation voltage, ACT8810QJ3## automatically turns on REG2, REG3, REG4, REG5 and nRSTO is asserted low, holding the microprocessor in reset for a user-selectable reset period of 260ms. If V_{OUT1} is within 6% of its regulation voltage when the reset timer expires, the nRSTO is de-asserted, and the microprocessor can begin its power-up sequence. Once the power-up routine is successfully completed, the system remains enabled after the push-button is released as long as the microprocessor asserts any one of ON1, ON2 or ON3, and REG4, REG5 may be enabled or disabled via the I^2C interface.

This start-up procedure requires that the pushbutton be held until the microprocessor assumes control (by asserting any one of ON1, ON2, and ON3), providing protection against inadvertent momentary assertions of the pushbutton. If desired, longer "push-and-hold" times can be easily implemented by simply adding an additional time delay before asserting ON1, ON2, or ON3. If the microprocessor is unable to complete its power-up routine successfully before the user lets go of the push-button, the ACT8810QJ3## automatically shuts itself down.

Figure 5:

Sequence C



Sequence D

The ACT8810QJ4## which is set with "sequence D", has a system startup is initiated whenever the following condition occurs:

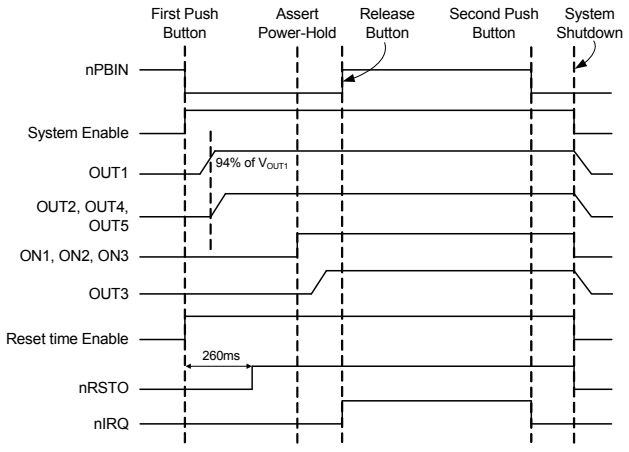
1) nPBIN is pushed low via 100kΩ resistance,

When ever this condition exists, the ACT8810QJ4## begins its system startup procedure by enabling REG1, When REG1 reaches 94% of its final regulation voltage, ACT8810QJ4## automatically turns on REG2, REG4, REG5 and nRSTO is asserted low, holding the microprocessor in reset for a user-selectable reset period of 260ms. when the reset timer expires, the nRSTO is de-asserted and the microprocessor can begin its power-up sequence. Once the power-up routine is successfully completed, the system remains enabled after the push-button is released as long as the microprocessor asserts any one of ON1, ON2 or ON3, holding REG1, REG2, REG4, REG5, and enabling REG3. And any regulators could be enabled or disabled via the I^2C interface.

This start-up procedure requires that the pushbutton be held until the microprocessor assumes control (by asserting any one of ON1, ON2, and ON3), providing protection against inadvertent momentary assertions of the pushbutton. If desired, longer "push-and-hold" times can be easily implemented by simply adding an additional time delay before asserting ON1, ON2, or ON3. If the microprocessor is unable to complete its power-up routine successfully before the user lets go of the push-button, the ACT8810QJ4## automatically shuts itself down.

Figure 6:

Sequence D



Sequence E

The ACT8810QJ5## which is set with "sequence E", has a system startup is initiated whenever the following conditions occurs:

1) A valid input voltage is present at VIN, or

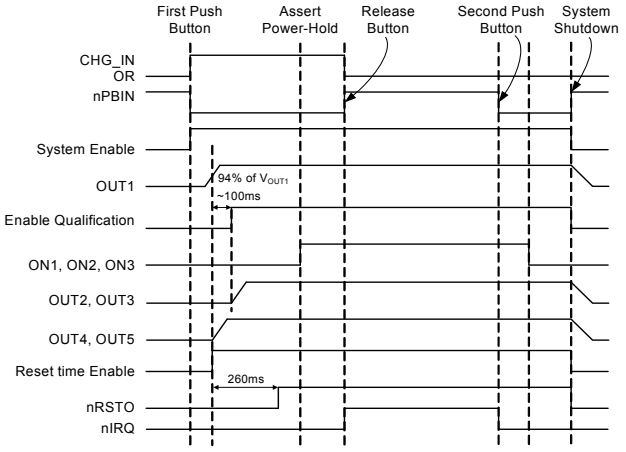
2) nPBIN is pushed low via 100kΩ resistance,

When ever this condition exists, the ACT8810QJ5## begins its system startup procedure by enabling REG1. When REG1 reaches 94% of its final regulation voltage, ACT8810QJ5## automatically turns on REG2, REG3, REG4, REG5 and nRSTO is asserted low, holding the microprocessor in reset for a user-selectable reset period of 260ms. If V_{OUT1} is within 6% of its regulation voltage when the reset timer expires, the nRSTO is de-asserted, and the microprocessor can begin its power-up sequence. Once the power-up routine is successfully completed, the system remains enabled after the push-button is released as long as the microprocessor asserts any one of ON1, ON2 or ON3, and REG4, REG5 may be enabled or disabled via the I^2C interface.

This start-up procedure requires that the pushbutton be held until the microprocessor assumes control (by asserting any one of ON1, ON2, and ON3), providing protection against inadvertent momentary assertions of the pushbutton. If desired, longer "push-and-hold" times can be easily implemented by simply adding an additional time delay before asserting ON1, ON2, or ON3. If the microprocessor is unable to complete its power-up routine successfully before the user lets go of the push-button or un-plug charger input, the ACT8810QJ5## automatically shuts itself down.

Figure 7:

Sequence E



ELECTRICAL CHARACTERISTICS (REG1)

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP1 Operating Voltage Range		2.9		5.5	V
VP1 UVLO Threshold	Input Voltage Rising	2.7	2.8	2.9	V
VP1 UVLO Hysteresis	Input Voltage Falling		85		mV
Quiescent Supply Current			130	200	μA
Shutdown Supply Current	REG1 is disabled, V_{VP1} = 4.2V		0.1	1	μA
Output Voltage Accuracy	V_{NOM1} < 1.5V, I_{OUT1} = 10mA	-2.1%	V_{NOM1}①	+2.1%	V
	V_{NOM1} ≥ 1.5V, I_{OUT1} = 10mA	-1.5%	V_{NOM1}	+1.5%	
Line Regulation	V_{VP1} = Max(V_{NOM1} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT1} = 10mA to 1.3A		0.0017		%/mA
Current Limit		1.4	1.8		A
Oscillator Frequency	V_{OUT1} ≥ 20% of V_{NOM1}	1.35	1.6	1.85	MHz
	V_{OUT1} = 0V		540		kHz
PMOS On-Resistance	I_{SW1} = -100mA		0.16	0.24	Ω
NMOS On-Resistance	I_{SW1} = 100mA		0.16	0.24	Ω
SW1 Leakage Current	V_{VP1} = 5.5V, V_{SW1} = 5.5V or 0V			1	μA
Power Good Threshold			94		%V_{NOM1}
Minimum On-Time			60		ns

①: V_{NOM1} refers to the nominal output voltage level for V_{OUT1} as defined by the *Ordering Information* section.

ELECTRICAL CHARACTERISTICS (REG2)

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP2 Operating Voltage Range		2.9		5.5	V
VP2 UVLO Threshold	Input Voltage Rising	2.7	2.8	2.9	V
VP2 UVLO Hysteresis	Input Voltage Falling		85		mV
Quiescent Supply Current			130	200	µA
Shutdown Supply Current	REG2 Disabled, V_{VP2} = 4.2V		0.1	1	µA
Output Voltage Regulation Accuracy	V_{NOM2} < 1.5V, I_{OUT2} = 10mA	-2.1%	V_{NOM2}①	+2.1%	V
	V_{NOM2} ≥ 1.5V, I_{OUT2} = 10mA	-1.5%	V_{NOM2}	+1.5%	
Line Regulation	V_{VP2} = Max(V_{NOM2} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT2} = 10mA to 1.0A		0.0017		%/mA
Current Limit		1.15	1.45		A
Oscillator Frequency	V_{OUT2} ≥ 20% of V_{NOM2}	1.35	1.6	1.85	MHz
	V_{OUT2} = 0V		540		kHz
PMOS On-Resistance	I_{SW2} = -100mA		0.25	0.38	Ω
NMOS On-Resistance	I_{SW2} = 100mA		0.17	0.26	Ω
SW2 Leakage Current	V_{VP2} = 5.5V, V_{SW2} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM2}
Minimum On-Time			60		ns

①: V_{NOM2} refers to the nominal output voltage level for V_{OUT2} as defined by the *Ordering Information* section.

ELECTRICAL CHARACTERISTICS (REG3)

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

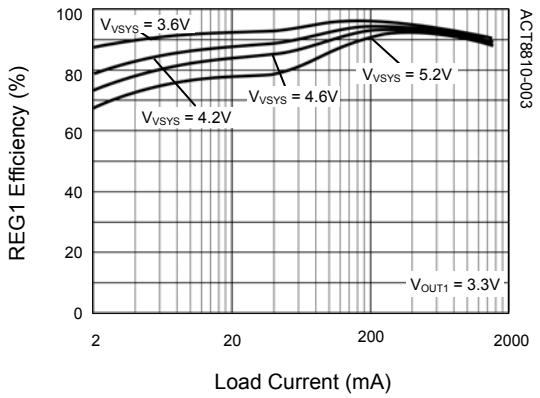
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP3 Operating Voltage Range		2.9		5.5	V
VP3 UVLO Threshold	Input Voltage Rising	2.7	2.8	2.9	V
VP3 UVLO Hysteresis	Input Voltage Falling		85		mV
Quiescent Supply Current			130	200	μA
Shutdown Supply Current	REG3 Disabled, V_{VP3} = 4.2V		0.1	1	μA
Output Voltage Regulation Accuracy	V_{NOM3} < 1.5V, I_{OUT3} = 10mA	-2.1%	V_{NOM3}①	+2.1%	V
	V_{NOM3} ≥ 1.5V, I_{OUT3} = 10mA	-1.5%	V_{NOM3}	+1.5%	
Line Regulation	V_{VP3} = Max(V_{NOM3} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT3} = 10mA to 550mA		0.0017		%/mA
Current Limit		0.55	0.7		A
Oscillator Frequency	V_{OUT3} ≥ 20% of V_{NOM3}	1.35	1.6	1.85	MHz
	V_{OUT3} = 0V		540		kHz
PMOS On-Resistance	I_{SW3} = -100mA		0.46	0.69	Ω
NMOS On-Resistance	I_{SW3} = 100mA		0.3	0.55	Ω
SW3 Leakage Current	V_{VP3} = 5.5V, V_{SW3} = 5.5V or 0V			1	μA
Power Good Threshold			94		%V_{NOM3}
Minimum On-Time			60		ns

①: V_{NOM3} refers to the nominal output voltage level for V_{OUT3} as defined by the *Ordering Information* section.

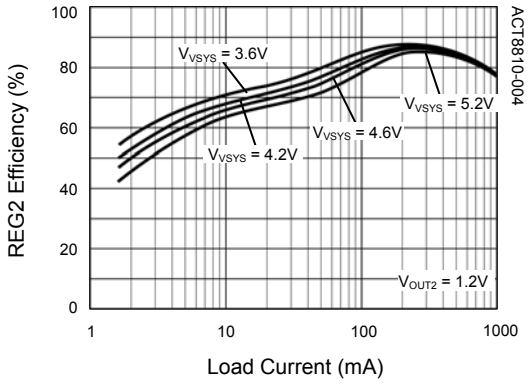
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8810QJ3EB, V_{VP1} = V_{VP2} = 3.6V, L = 3.3μH, C_{VP1} = C_{VP2} = 4.7μF, C_{OUT1} = 22μF, C_{OUT2} = 10μF, T_A = 25°C, unless otherwise specified.)

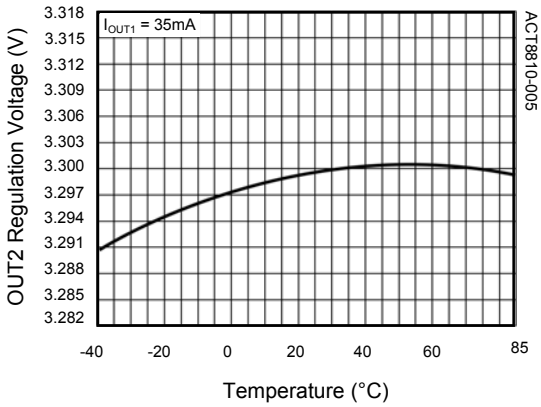
REG1 Efficiency vs. Load Current



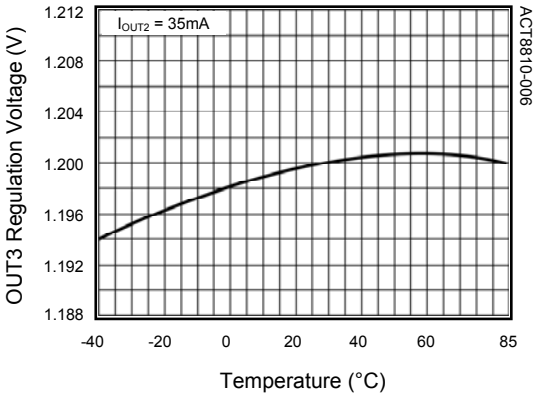
REG2 Efficiency vs. Load Current



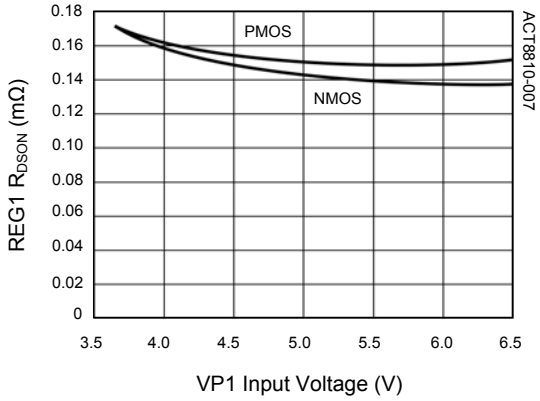
OUT1 Regulation Voltage vs. Temperature



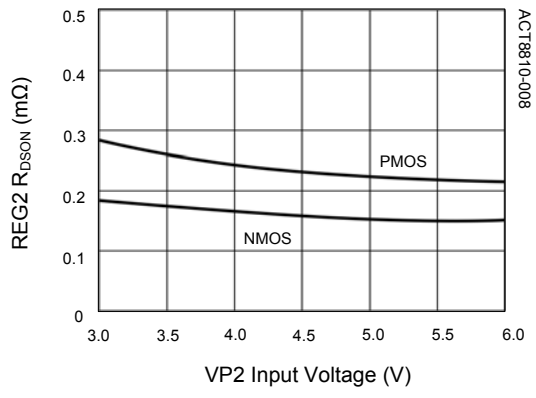
OUT2 Regulation Voltage vs. Temperature



REG1 R_{DSON} vs. VP1 Input Voltage



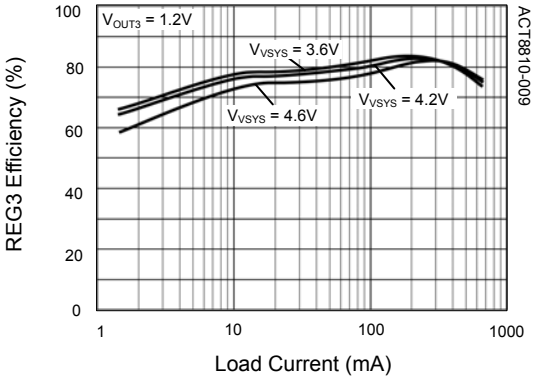
REG2 R_{DSON} vs. VP2 Input Voltage



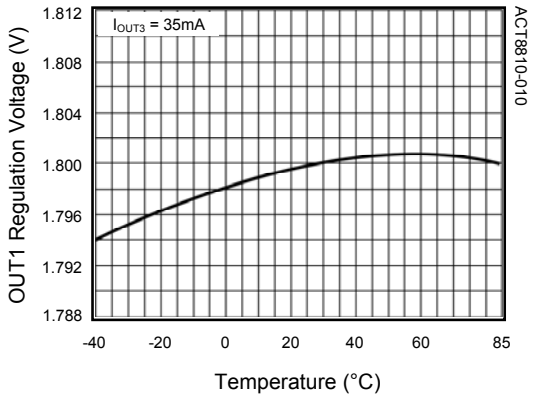
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(ACT8810QJ3EB, V_{VP3} = 3.6V, L = 3.3µH, C_{VP3} = 4.7µF, C_{OUT3} = 10µF, T_A = 25°C, unless otherwise specified.)

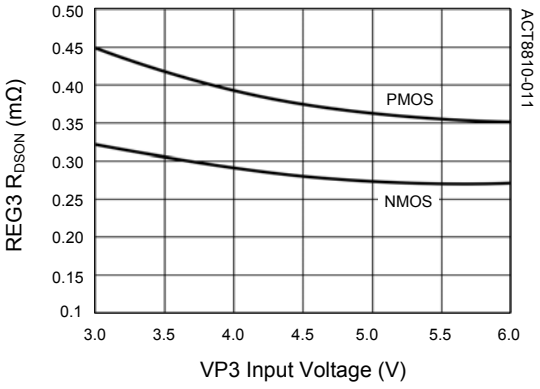
REG3 Efficiency vs. Load Current



OUT3 Regulation Voltage vs. Tempera-



REG3 R_{DSON} vs. VP3 Input Voltage



REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 4:

REG1 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
10h	R	R	VSET1					
11h	R	R	R	R	R	R	R	R
12h	R	R	R	R	R	nFLTMSK	OK	ON
13h	R	VRANGE	VSET0					

R: Read-Only bits. Default Values May Vary.

Table 5:

REG1 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
10h	VSET1	[5:0]	R/W	REG1 Standby Output Voltage Selection	See Table 4	
10h		[7:6]	R		READ ONLY	
11h		[7:0]	R		READ ONLY	
12h	ON	[0]	R/W	REG1 Enable	0	REG1 Disable
					1	REG1 Enable
12h	OK	[1]	R	REG1 Power-OK	0	Output is not OK
					1	Output is OK
12h	nFLTMSK	[2]	R/W	REG1 Output Voltage Fault Mask Option	0	Masked
					1	Not Mask
12h		[7:3]	R		READ ONLY	
13h	VSET0	[5:0]	R/W	REG1 Output Voltage Selection	See Table 4	
13h	VRANGE	[6]	R/W	REG1 Voltage Range	0	Min V_{OUT} = 0.8V
					1	Min V_{OUT} = 1.25V
13h		[7]	R		READ ONLY	

REGISTER DESCRIPTIONS CONT'D

Table 6:

REG1/VSETx[ ] Output Voltage Setting

REG1/VSETx[3:0]	REG1/VSETx[5:4]							
	REG1/VRANGE[ ] = [0]①				REG1/VRANGE[ ] = [1]			
	00	01	10	11	00	01	10	11
0000	Adjustable②	1.025	1.425	1.825	Adjustable	2.050	2.850	3.650
0001	0.800	1.050	1.450	1.850	1.300	2.100	2.900	3.700
0010	0.800	1.075	1.480	1.875	1.350	2.150	2.950	3.750
0011	0.800	1.100	1.500	1.900	1.400	2.200	3.000	3.800
0100	0.800	1.125	1.525	1.925	1.450	2.250	3.050	3.850
0101	0.800	1.150	1.550	1.950	1.500	2.300	3.100	3.900
0110	0.800	1.175	1.575	1.975	1.550	2.350	3.150	3.950
0111	0.800	1.200	1.600	2.000	1.600	2.400	3.200	4.000
1000	0.825	1.225	1.625	2.025	1.650	2.450	3.250	4.050
1001	0.850	1.250	1.650	2.050	1.700	2.500	3.300	4.100
1010	0.875	1.275	1.675	2.075	1.750	2.550	3.350	4.150
1011	0.900	1.300	1.700	2.100	1.800	2.600	3.400	4.200
1100	0.925	1.325	1.725	2.125	1.850	2.650	3.450	4.250
1101	0.950	1.350	1.750	2.150	1.900	2.700	3.500	4.300
1110	0.975	1.375	1.775	2.175	1.950	2.750	3.550	4.350
1111	1.000	1.400	1.800	2.200	2.000	2.800	3.600	4.400

①: Care must be taken when adjusting the VRANGE[ ] selection at address 13h bit-6 to avoid undesired output voltage selections. The VRANGE bit allows selection of the two output voltage ranges available for REG1, REG2 and REG3 (VRANGE = 0 – V_{OUT} range 0.8V to 2.2V, VRANGE = 1 – V_{OUT} range 1.3V to 4.4V). It is recommended that the user first establishes if the new V_{OUT} voltage is within the current selected voltage range (selected by VRANGE) prior to changing the value of the VRANGE bit.

②: Refer to the *Output Voltage Programming* section for more information.

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 7:

REG2 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
20h	R	R	VSET1					
21h	R	R	R	R	R	R	R	R
22h	R	R	R	R	R	nFLTMSK	OK	ON
23h	R	VRANGE	VSET0					

R: Read-Only bits. Default Values May Vary.

Table 8:

REG2 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
20h	VSET1	[5:0]	R/W	REG2 Standby Output Voltage Selection	See Table 7	
20h		[7:6]	R		READ ONLY	
21h		[7:0]	R		READ ONLY	
22h	ON	[0]	R/W	REG2 Enable	0	REG2 Disable
					1	REG2 Enable
22h	OK	[1]	R	REG2 Power-OK	0	Output is not OK
					1	Output is OK
22h	nFLTMSK	[2]	R/W	REG2 Output Voltage Fault Mask Option	0	Masked
					1	Not Mask
22h		[7:3]	R		READ ONLY	
23h	VSET0	[5:0]	R/W	REG2 Output Voltage Selection	See Table 7	
23h	VRANGE	[6]	R/W	REG2 Voltage Range	0	Min V_{OUT} = 0.8V
					1	Min V_{OUT} = 1.25V
23h		[7]	R		READ ONLY	

REGISTER DESCRIPTIONS CONT'D

Table 9:

REG2/VSETx[ ] Output Voltage Setting

REG2/VSETx[3:0]	REG2/VSETx[5:4]							
	REG2/VRANGE[ ] = [0]①				REG2/VRANGE[ ] = [1]			
	00	01	10	11	00	01	10	11
0000	Adjustable②	1.025	1.425	1.825	Adjustable	2.050	2.850	3.650
0001	0.800	1.050	1.450	1.850	1.300	2.100	2.900	3.700
0010	0.800	1.075	1.480	1.875	1.350	2.150	2.950	3.750
0011	0.800	1.100	1.500	1.900	1.400	2.200	3.000	3.800
0100	0.800	1.125	1.525	1.925	1.450	2.250	3.050	3.850
0101	0.800	1.150	1.550	1.950	1.500	2.300	3.100	3.900
0110	0.800	1.175	1.575	1.975	1.550	2.350	3.150	3.950
0111	0.800	1.200	1.600	2.000	1.600	2.400	3.200	4.000
1000	0.825	1.225	1.625	2.025	1.650	2.450	3.250	4.050
1001	0.850	1.250	1.650	2.050	1.700	2.500	3.300	4.100
1010	0.875	1.275	1.675	2.075	1.750	2.550	3.350	4.150
1011	0.900	1.300	1.700	2.100	1.800	2.600	3.400	4.200
1100	0.925	1.325	1.725	2.125	1.850	2.650	3.450	4.250
1101	0.950	1.350	1.750	2.150	1.900	2.700	3.500	4.300
1110	0.975	1.375	1.775	2.175	1.950	2.750	3.550	4.350
1111	1.000	1.400	1.800	2.200	2.000	2.800	3.600	4.400

①: Care must be taken when adjusting the VRANGE[ ] selection at address 23h bit-6 to avoid undesired output voltage selections. The VRANGE bit allows selection of the two output voltage ranges available for REG1, REG2 and REG3 (VRANGE = 0 – V_{OUT} range 0.8V to 2.2V, VRANGE = 1 – V_{OUT} range 1.3V to 4.4V). It is recommended that the user first establishes if the new V_{OUT} voltage is within the current selected voltage range (selected by VRANGE) prior to changing the value of the VRANGE bit.

②: Refer to the *Output Voltage Programming* section for more information.