Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Advanced PMU with Inrush Control and Bypass Switch

BENEFITS and FEATURES

- **Wide input voltage range**
  - **Vin = 2.7V to 5.5V**
  - **Blocking up to 20V**
- **Complete integrated power solution**
  - **One 4A DC/DC Step-Down with Bypass Mode**
  - **Two 2.5A DC/DC Step-Down Regulators**
  - **Two 200mA LDOs**
  - **High Power Load Switch Gate Driver with Slew Rate Control**
- **Space Savings**
  - **Fully integrated**
  - **High Fsw = 2.25MHz or 1.125MHz**
  - **Integrated sequencing**
- **Easy system level design**
  - **Configurable sequencing**
  - **Seamless sequencing with external supplies**
  - **Programmable Reset and Power Good GPIO's**
- **Buck 1 Bypass Mode for 3.3V system level compliance**
- **Highly configurable**
  - **uP interface for status reporting and con-trollability**
  - **Flexible Sequencing Options**
  - **I^{2}C Interface – 1MHz**
  - **Multiple Sleep Modes**
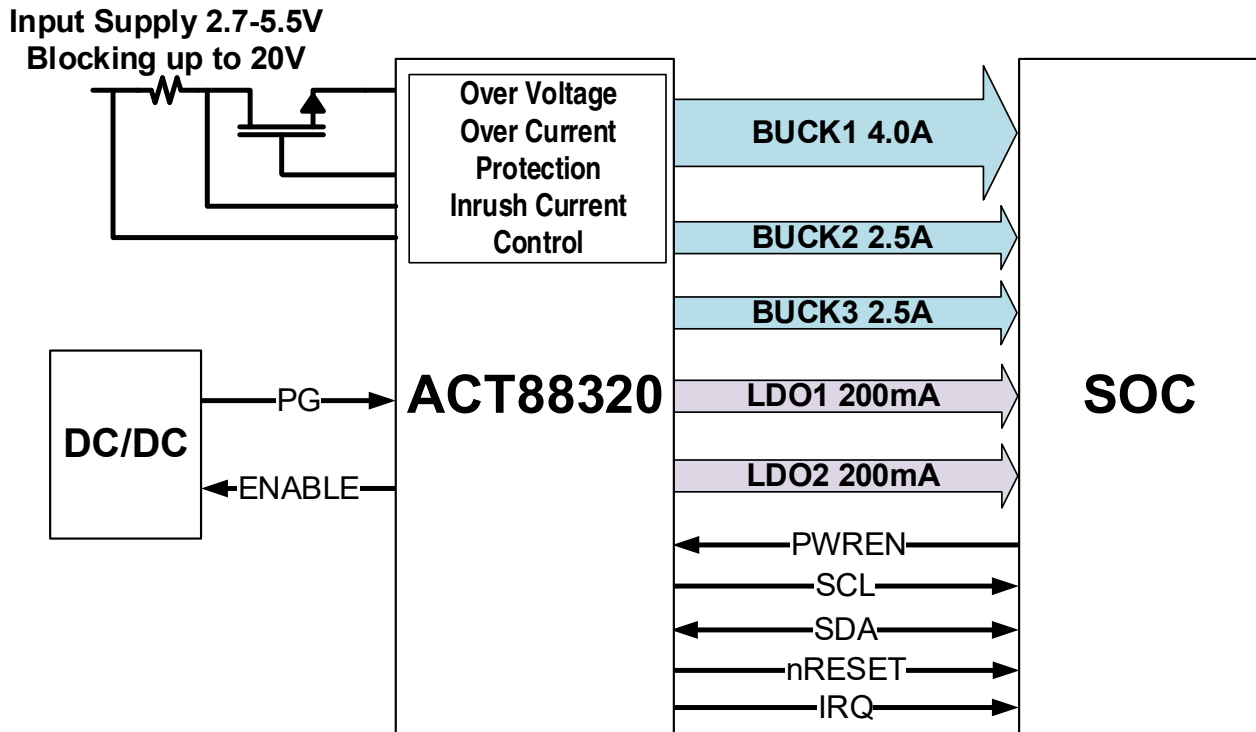 - **See ACT88321 for Pushbutton Startup**

GENERAL DESCRIPTION

The ACT88320 PMIC is an integrated ActivePMU power management unit. It is highly flexible and can be reconfigured via I^{2}C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speeds time to market. Examples of configurable options include output voltage, startup time, slew rate, system level sequencing, switching frequency, sleep modes, operating modes etc. The core of the device includes 3 DC/DC step down converters using integrated power FETs, and 2 low-dropout regulators (LDOs). Each regulator can be configured for a wide range of output voltages through the I^{2}C interface.

ACT88320 is programmed at the factory with a default configuration. The default settings can be optimized for a specific design through the I^{2}C interface. Contact the factory for specific default configurations.

The ACT88320 includes features that allow flexibility for all system level configurations. The buck converter can be reconfigured as a bypass switch. It also contains a high power load switch controller. It's external power supply enable and power good interface allows seamless sequencing with external power supplies.

The ACT88320 PMIC is available in a 4 x 4 mm 32 pin QFN package.

APPLICATIONS

- Solid-State Drives
- Microcontroller Applications
- FPGA
- Personal Navigation Devices

Typical Application Diagram

FUNCTIONAL BLOCK DIAGRAM
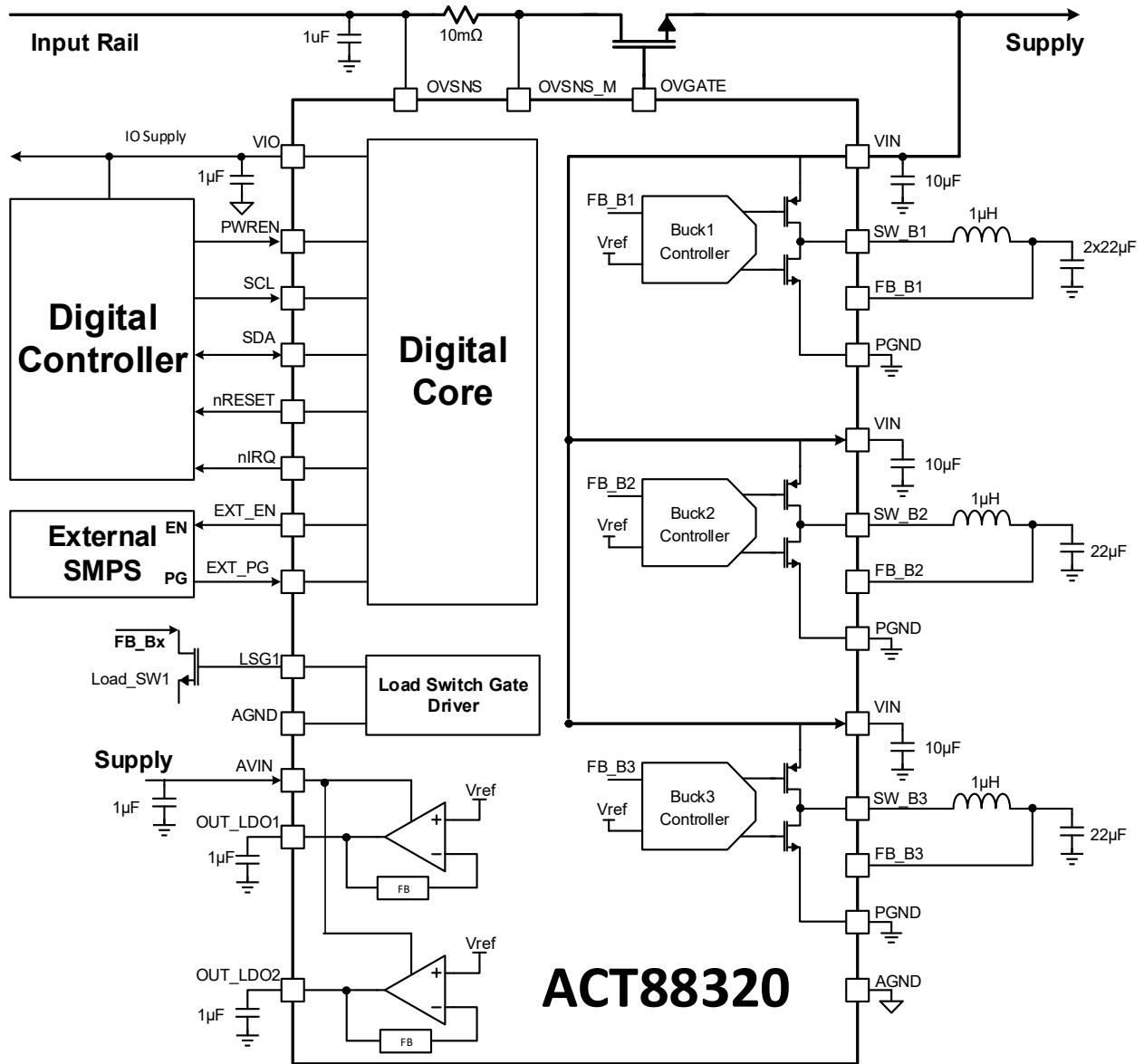
ORDERING INFORMATION

PART NUMBER	V_{BUCK1}	V_{BUCK2}	V_{BUCK3}	V_{LDO1}	V_{LDO2}	V_{LSWG1}	PACKAGE
ACT88320QI101-T	3.3V	1.8V	1.15/0.9V	3.3V	1.8V	OFF	TQFN 4mmx4mm
ACT88320QI103-T	1.2V	1.8V	3.3V	2.5V	3.3V	OFF	TQFN 4mmx4mm
ACT88320QI104-T	0.9V/0.75V	1.2V/1.8V	1.5V/1.35V	OFF	1.8V	ON	TQFN 4mmx4mm
ACT88320QI105-T	1.05V	1.8V	1.5V/1.35V	OFF	1.8V	OFF	TQFN 4mmx4mm
ACT88320QI106-T	0.9V	1.8V	1.2V	OFF	1.8V	OFF	TQFN 4mmx4mm
ACT88320QI108-T	3.3V	1.8V	1.15V	3.3V	1.8V	OFF	TQFN 4mmx4mm

ACT88320QIxxx-T

Product Number

Package Code

Pin Count

Option Code

Tape and Reel
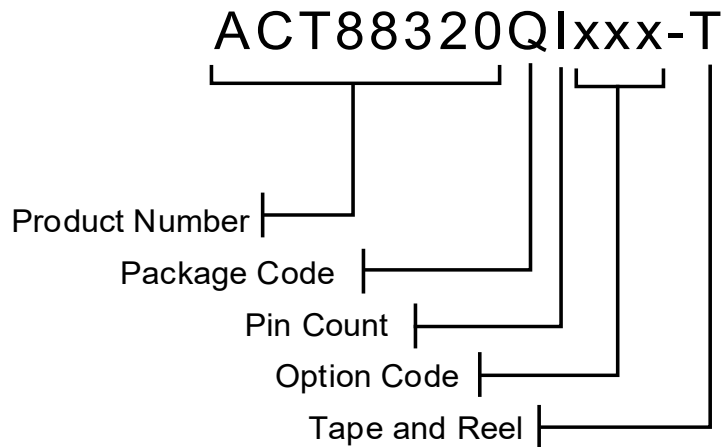
Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

Note 3: Package Code designator "Q" represents QFN

Note 4: Pin Count designator "I" represents 32 pins

Note 5: "xxx" represents the CMI (Code Matrix Index) option. The CMI identifies the IC's default register settings

Note 6: See the CMI Option section in the back of the datasheet for a more detailed description of each CMI's settings.
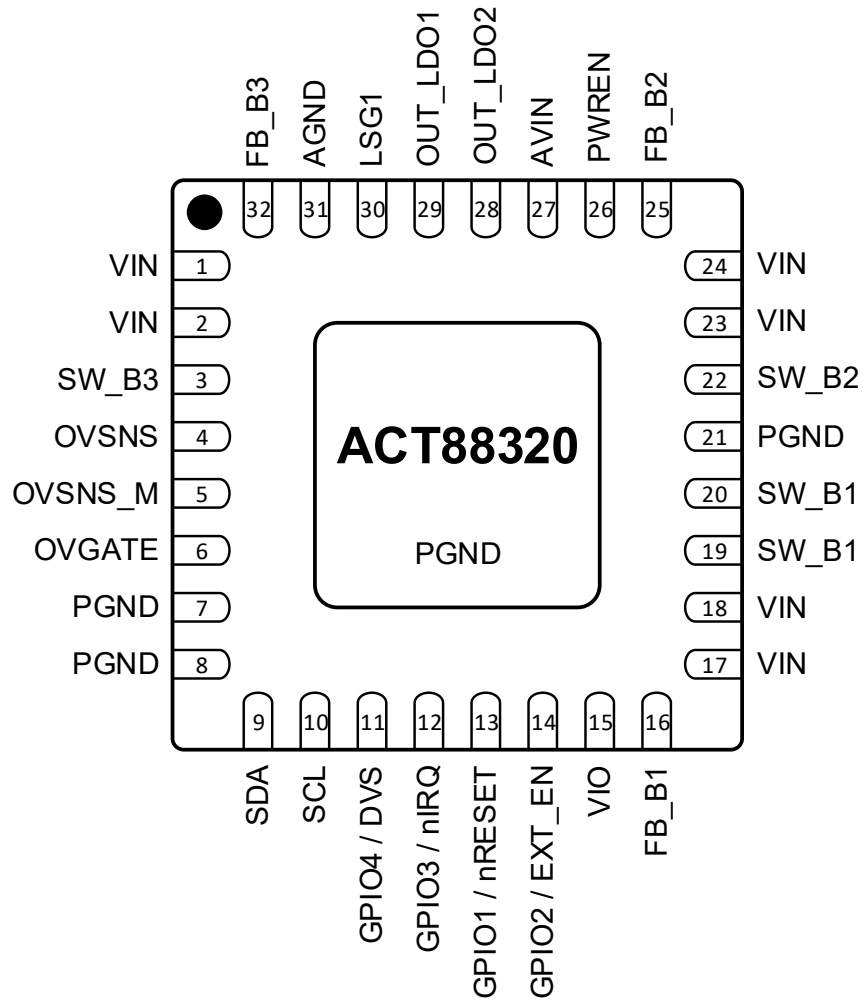
PIN CONFIGURATION

Figure 1: Pin Configuration – Top View – QFN44-32

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1,2	VIN	Dedicated VIN power input for BUCK3. Connect the BUCK3 input caps directly to these pins
3	SW_B3	Switch Pin for BUCK3 Regulator
4	OVSNS	Analog VIN+ Input. Used to monitor and start inrush control FET
5	OVSNS_M	Analog VIN- Input. Used to monitor current in external resistor (RSNS)
6	OVGATE	Gate drive for the inrush control FET. Voltage is typically 8V above VIN which requires a 12V n-ch FET.
7,8	PGND	Power Ground for Buck3. Connect the BUCK3 input caps directly to these pins.
9	SDA	I^{2}C Data Input and Output
10	SCL	I^{2}C Clock Input
11	GPIO4 / DVS	GPIO. Configured as a dynamic voltage scaling input.
12	GPIO3 / nIRQ	GPIO. Configured as an interrupt (IRQ) open drain output.
13	GPIO1 / nRESET	GPIO. Configured as an nRESET open drain output
14	GPIO2 / EXT_EN	GPIO. Configured as an open drain output to enable an external power supply
15	VIO	Digital input reference voltage. Connect a 1uF capacitor between VIO and AGND
16	FB_B1	Feedback for BUCK1 regulator. Connect directly to the Buck1 output capacitor.
17, 18	VIN	Dedicated VIN power input for BUCK1. Connect the Buck1 input caps directly to these pins.
19, 20	SW_B1	Switch pin for BUCK1 Regulator
21	PGND	Power Ground for BUCK1 and BUCK2. Connect BUCK1 and BUCK2 input caps directly to this pin.
22	SW_B2	Switch Pin for BUCK2 Regulator
23, 24	VIN	Dedicated VIN power input for BUCK2. Connect the BUCK2 input caps directly to these pins.
25	FB_B2	Feedback for BUCK2 Regulator
26	PWREN	Power Enable Digital Input
27	AVIN	Dedicated VIN power input for LDO1 & 2 Regulators and Analog VIN Input
28	OUT_LDO2	Output for LDO2 Regulator
29	OUT_LDO1	Output for LDO1 Regulator
30	LSG1	Output1 Load Switch Gate driver
31	AGND	Analog Ground
32	FB_B3	Feedback for BUCK3 Regulator
33	Exposed Pad	Must be soldered to the top layer ground plane.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE	UNIT
All Pins to AGND and PGND unless stated otherwise below	-0.3 to 6	V
OVSNS, OVSNS_M to PGND	-0.3 to 22	V
OVGATE to VIN	-0.3 to 13.2	V
VIN to PGND	-0.3 to 6	V
SW_Bx to PGND	-0.3 to VIN + 1	V
PWREN to AGND	-0.3 to AVIN + 0.3	V
GPIOx to AGND	-0.3V to VIO + 0.3	V
FB_Bx to PGND	-0.3 to VIN + 0.3	V
OUTx to PGND	-0.3 to VIN + 0.3	V
AGND to PGND	-0.3 to + 0.3	V
Junction to Ambient Thermal Resistance (Note 2)	26.5	°C/W
Junction to Case Thermal Resistance (Note 2)	13.1	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C

Note1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Note2: Measured on Active-Semi Evaluation Kit

DIGITAL I/O ELECTRICAL CHARACTERISTICS

(VIO = 1.8V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWREN Input Low	AVIN = 3.3V			1.6	V
PWREN Input High	AVIN = 3.3V	2.1			V
PWREN Input Low	AVIN = 5V			2.2	V
PWREN Input High	AVIN = 5V	2.7			V
nIRQ, EXT_PG Input Low	VIO = 1.8V			0.4	V
nIRQ, EXT_PG Input High	VIO = 1.8V	1.25			V
nIRQ, EXT_PG Input Low	VIO = 3.3V			1.0	V
nIRQ, EXT_PG Input High	VIO = 3.3V	2.3			V
nIRQ, nRESET, EXT_PG, EXT_EN Leakage Current	Output = 5V			1	µA
nIRQ, EXT_PG Output Low	I_{OL} = 5mA			0.35	V
EXT_EN, nRESET Output Low	I_{OL} = 1mA			0.35	V
nRESET Output High	I_{OH} = 1mA	VIO-0.35			V
EXT_EN Output High	I_{OH} = 1mA	VIO-0.35			V
PWREN, EXT_PG Deglitch Time (falling)			15		µs
PWREN, EXT_PG Deglitch Time (rising)			10		µs
VIO Operating Range		1.5		VIN	V

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(VIO = 1.8V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Voltage Range: AVIN referenced to AGND		2.7		5.5	V
UVLO Threshold Falling		2.5	2.6	2.7	V
UVLO Hysteresis		100			mV
System Monitor (SYSMON) Programmable Range		2.7		4.2	V
OV Threshold Rising		5.5	5.75	6.0	V
OV Hysteresis		100	200	300	mV
Operating Supply Current	All Regulators Disabled		10		µA
Operating Supply Current	All Regulators Enabled but no load		250		µA
Thermal Shutdown	Temperature rising	140	160	180	°C
Thermal Shutdown Hysteresis			30		°C
Power Up Delay after initial VIN	Time from VIN > UVLO threshold to Internal Power-On Clear (POR)		120	200	µs
Startup Delay after initial VIN	Time from VIN > UVLO threshold to start of first regulator turning On. (zero delay)		1500	2000	µs
Oscillator Frequency		2.13	2.25	2.37	MHz
VIN UV Interrupt Threshold Falling	Referenced to rising threshold		200		mV
VIN UV Threshold Rising Programming Range	Rising edge threshold can power up device. Configurable in 100mV steps.	2.7	3	4.2	V
VIN UV Shutdown Threshold Falling			2.6		V
VIN OV Shutdown Threshold Rising			5.75		V
VIN OV Shutdown Threshold Falling			5.5		V
VIN Deglitch Time UV		80	100	120	µs
VIN Deglitch Time OV		160	200	240	µs
Transition time from Deep Sleep (DPSLP) State to Active State	Time from PWREN pin low to high transition to time when the first regulator turns ON with minimum turn on delay configuration.			1	ms
Transition time from Sleep State (SLEEP) to Active State	Time from I2C command to clear sleep mode to time when the first regulator turns ON with minimum turn on delay configuration.		100		µs
Time to first power rail turn off	Time from turn Off event to when the first power rail turns off with minimum turn off delay configuration		120	200	µs
Startup Delay Programmable Range	ONDLY=00 ONDLY=01 ONDLY=10 ONDLY=11		0 0.25 0.5 1.0		ms
Turn Off Delay Programmable Range	Configurable in 0.25ms steps	0		7.75	ms
nRESET Programmable Range	Configurable to 20, 40, 60 or 100ms.	20		100	ms

Note 1: All Under-voltage Lockout, Overvoltage measurements are referenced to the AVIN Input and AGND Pins.
Note 2: All POK Under-voltage and Overvoltage measurements are referenced to the VIN Input and GND Pins.

OVP, INRUSH NMOS SWITCH, ELECTRICAL CHARACTERISITICS

(VIN = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage Range (VIN)		2.7		5.5	V
VIN Input Current	IC Disabled			1	µA
OVGATE Pull-up Current	OVGATE = 0V		10		µA
OVGATE Discharge Resistance			10		Ω
Overcurrent Shutdown Threshold	Voltage across current sense resistor	70	85	100	mV
Overcurrent Warning Threshold	Percent of shutdown voltage	72.5	80	87.5	%
Soft-Start Slew Rate	Start up from 0V to 5.0V on OVGATE. C_{Gate} = 1nF		500		µs
Over Current Deglitch Time	Steady state operation		40		µs
Over Current Blanking Time	Blanking time during power up		85		µs
Retry time after Over Current			42		ms
OVSNS POK Threshold (falling)			2.5		V
OVSNS POK Threshold (rising)			2.7		V
OVSNS POK Threshold Hysteresis		100	200		mV
OVSNS OV Threshold (rising)			6		V
OVSNS OV Threshold hysteresis		200		400	mV
Startup Delay	After OVSNS POK to OVGATE rising, C_{Gate} = 1nF		40		µs
Standby Current into OVSNS and OVSNS_M	After OVSNS POK, steady state mode		40	50	µA
VOVGATE Voltage (VOVGATE – VIN)	OVSNS = 3.3V		5.4		V
	OVSNS = 5V		8		

INTERNAL STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS REGULATOR: (BUCK1)

(VIN = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Operating Voltage Range		2.7		5.5	V
Output Voltage Programming Range	See CMI section for programming details	0.6		4.0	V
Standby Supply Current, Low Power Mode Enabled	V_{OUT_B1} = 103% setpoint, Enabled, V_{OUT_B1} setpoint = 1.0V, No Load		40	55	µA
Shutdown Current	Regulator Disabled			1	µA
Output Voltage Accuracy	V_{OUT_B1} = default CMI voltage, continuous PWM mode	-1	V_{NOM}	1	%
Output Voltage Accuracy	V_{OUT_B1} = default CMI voltage, PFM mode	-2	V_{NOM}	2	%
Line Regulation	V_{OUT_B1} = default CMI voltage, PWM Regulation		0.1		%/V
Load Regulation	V_{OUT_B1} = at default CM, PWM Regulation		0.1		%/A
Power Good Threshold	V_{OUT_B1} Rising	90	92.5	95	%V_{NOM}
Power Good Hysteresis	V_{OUT_B1} Falling		3		%V_{NOM}
Overvoltage Fault Threshold	V_{OUT_B1} Rising	107.5	110	112.5	%V_{NOM}
Overvoltage Fault Hysteresis	V_{OUT_B1} Falling		3		%V_{NOM}
Switching Frequency	V_{OUT_B1} ≥ 20% of V_{NOM}, Configurable	-5%	1.125 / 2.25	+5%	MHz
Soft-Start Period T_{set}	10% to 90% V_{NOM}		480	600	µs
Current Limit, Cycle-by-Cycle		4.14	4.6	5.06	A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	112.5	122.5	132.5	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	67.5	75	82.5	%
PMOS On-Resistance	I_{SW} = -1A, VIN = 5.0V		40	50	mΩ
NMOS On-Resistance	I_{SW} = 1A, VIN = 5.0V		16	25	mΩ
SW Leakage Current	VIN = 5.5V, V_{SW} = 0V			1	µA
	VIN = 5.5V, V_{SW} = 5.5V			1	µA
Dynamic Voltage Scaling Rate			3.50		mV/µs
Output Pull Down Resistance	Enabled when regulator disabled		4.4	8.75	Ohms

INTERNAL STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS REGULATOR: (BUCK1) – BYPASS MODE

(VIN = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage for By-Pass Mode		2.7	3.3	3.7	V
PMOS On-Resistance	I_{SW} = -1A, VIN = 3.3V, Max=125°C at $T_{Junction}$		0.04	0.06	Ω
Internal PMOS Current Detection	Triggers Interrupt on IRQ Pin	3.0	3.5	4.0	A
Internal PMOS Current Detection Deglitch Time			10		µs
Internal PMOS Current Shutdown	Shuts down after deglitch time and stays off for Off-Time	5.0	5.6	6.2	A
Internal PMOS Current Shutdown Deglitch Time			5		µs
Internal PMOS Current Shutdown Off-Time (Retry time)			14		ms
Internal PMOS Soft start	VIN = 3.3V Input, C_{out} = 47uF, Default setting ISS[1:0]=00		500		µs

INTERNAL STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS REGULATOR: (BUCK2-3)

(AVIN = VIN = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Operating Voltage Range		2.7		5.5	V
Output Voltage Programming Range	Configurable in 12.5mV steps.	0.8		3.9875	V
Standby Supply Current, Low Power Mode Enabled	V_{OUTx} = 103%, Regulator Enabled, No load, V_{OUTx} = default CMI voltage		35		μA
Shutdown Current	VIN = 5.0V, Regulator Disabled		0.1	1	μA
Output Voltage Accuracy	V_{OUTx} = default CMI voltage, I_{OUTx} = 1A (continuous PWM mode)	-1%	V_{NOM}	1%	V
Line Regulation	V_{OUTx} = default CMI voltage, PWM Regulation		0.1		%
Load Regulation	V_{OUTx} = default CMI voltage, PWM Regulation		0.1		%
Power Good Threshold	V_{OUTx} Rising	90	92.5	95	%V_{NOM}
Power Good Hysteresis	V_{OUTx} Falling		3		%V_{NOM}
Overvoltage Fault Threshold	V_{OUTx} Rising	107.5	110	112.5	%V_{NOM}
Overvoltage Fault Hysteresis	V_{OUTx} Falling		3		%V_{NOM}
Switching Frequency	V_{OUTx} ≥ 20% of VNOM	-5%	1.125 / 2.25	+5%	MHz
Soft-Start Period T_{set}	10% to 90% VNOM		480	600	μs
Startup Time	Time from Enable to PG		700		μs
Current Limit, Cycle-by-Cycle		2.7	3.0	3.3	A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	112.5	122.5	132.5	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	67.5	75	82.5	%
PMOS On-Resistance	I_{SW_Bx} = -500mA, V_{IN} = 5V		80		mΩ
NMOS On-Resistance	I_{SW_Bx} = 500mA, V_{IN} = 5V		50		mΩ
SW Leakage Current	V_{IN} = 5.5V, V_{SW_Bx} = 0 or 0V			1	μA
	V_{IN} = 5.5V, V_{SW_Bx} = 0 or 5.5V			1	μA
Dynamic Voltage Scaling Rate			3.50		mV/us
Output Pull Down Resistance	Enabled when regulator disabled		9.4	20	Ω

LDO1-2 ELECTRICAL CHARACTERISTICS

(AVIN = VIN = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range LDO1	AVIN (Input Voltage) to the LDO1	2.7		5.5	V
Output Voltage Range	Option 1 Configurable in 9.375mV steps	0.6		2.991	V
	Option 2 Configurable in 12.5mV steps	0.8		3.9875	V
Output Current		180	200		mA
Output Voltage Accuracy	AVIN - V_{LDOx_OUT} > 0.4V	-1	V_{NOM}	1	%
Line Regulation	AVIN - V_{LDOx_OUT} > 0.4V I_{LDOx_OUT} = 1mA		0.03	0.2	%
Load Regulation	I_{LDOx_OUT} = 1mA to 100mA, V_{LDOx_OUT} = default CMI			0.5	%
Power Supply Rejection Ratio	f = 1kHz, I_{LDOx_OUT} = 20mA, V_{LDOx_OUT} = 1.8V, Note 1		40.8		dB
	f = 10kHz, I_{LDOx_OUT} = 20mA, V_{LDOx_OUT} = 1.8V, Note 1		31.2		dB
	f = 2.25MHz, I_{LDOx_OUT} = 20mA, V_{LDOx_OUT} = 1.8V, Note 1		53.6		dB
Supply Current per Output	Regulator Disabled			1	µA
Supply Current	Regulator Enabled, No load		15	20	µA
Soft-Start Period	Time from soft start "ON" to PGOOD. V_{LDOx} = 1.8V	150	215	300	µs
	Time from soft start "ON" to PGOOD. V_{LDOx} = 3.3V	200	275	350	µs
Power Good Threshold	V_{LDOx_OUT} Rising	90	92.5	95	% V_{NOM}
Power Good Hysteresis	V_{LDOx_OUT} Falling		3		% V_{NOM}
Overvoltage Fault Threshold	V_{LDOx_OUT} Rising	106	110	114	% V_{NOM}
Overvoltage Fault Hysteresis	V_{LDOx_OUT} Falling		3		% V_{NOM}
Discharge Resistance			50	125	Ω
Dropout Voltage	I_{LDOx_OUT} = 220mA, V_{LDOx_OUT} = 2.7V			150	mV
Output Current Limit	ILIM [1:0] = 00 ILIM [1:0] = 01 ILIM [1:0] = 10 ILIM [1:0] = 11	-35%	110 150 210 315	+35%	mA
Startup Time	Time from Enable to PG		300	400	µs

Note 1: AVIN - V_{LDOx_OUT} > 0.4V

LOAD SWITCH GATE DRIVER ELECTRICAL CHARACTERISTICS

(VIN = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Maximum Output - Gate Voltage	Gate fully on			2*VIN	V
Soft-Start Slew Rate	Gate Node rising from 0 to 2V with 1nF output capacitor. (configurable via OVGATE current)		800 400 260 200		us
OVGATE Pin Pull-up Current (V_{OVGATE}=0V)	GATE1 SLEW = 00 GATE1 SLEW = 01 GATE1 SLEW = 10 GATE1 SLEW = 11		2.5 5 7.5 10		µA µA µA µA
Fault Deglitch Time			10		µs
Gate Discharge Resistance				75	Ω
Startup Delay				75	µs

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{IO} = 1.8V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	VIO = 1.8V			0.4	V
SCL, SDA Input High	VIO = 1.8V	1.25			V
SCL, SDA Input Low	VIO = 3.3V			1.0	V
SCL, SDA Input High	VIO = 3.3V	2.3			V
SDA Leakage Current	SDA=5V			1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Frequency, f_{SCL}		0		1000	kHz
SCL Low Period, t_{LOW}		0.5			µs
SCL High Period, t_{HIGH}		0.26			µs
SDA Data Setup Time, t_{SU}		50			ns
SDA Data Hold Time, t_{HD}	(Note1)	0			ns
Start Setup Time, t_{ST}	For Start Condition	260			ns
Stop Setup Time, t_{SP}	For Stop Condition	260			ns
Capacitance on SCL or SDA Pin				10	pF
SDA Fall Time SDA, T_{of}	Device requirement			120	ns
Pulse Width of spikes must be suppressed on SCL and SDA		0		50	ns

Note1: Comply with I²C timings for 1MHz operation - "Fast Mode Plus".

Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering Deep Sleep, Sleep, OVUVFLT, and THERMAL states to clear any transactions that may have been occurring when entering the above states.

Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the device.

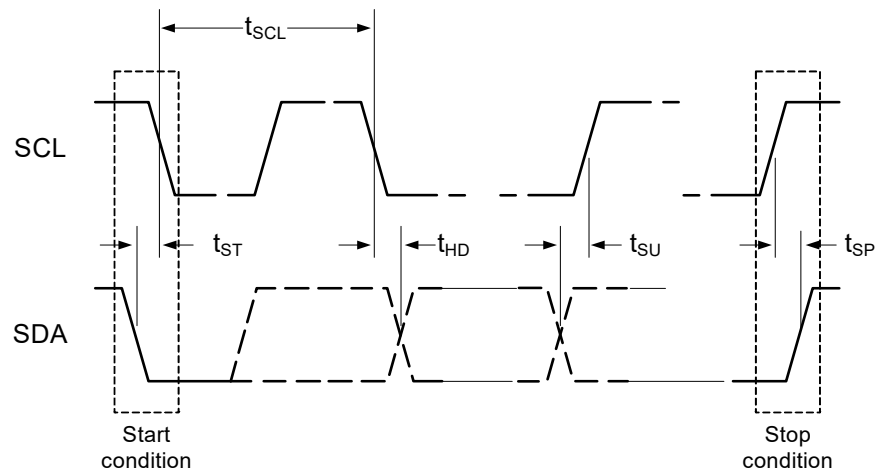Note4: Device Address is factory configurable to 7'h25, 7'h27, 7'h67, 7'h6B.

Figure 2: I²C Data Transfer

SYSTEM CONTROL INFORMATION

General

The ACT88320 is a single-chip integrated power management solution designed to power many processors such as the Silicon Motion SM2258 and SM2259 solid state drive controllers and the Atmel SAMA5D processors. It integrates three highly efficient buck regulators, two LDOs, an integrated load bypass switch, and a built in inrush and overvoltage controller. Its high integration and high switching frequency result in an extremely small footprint and low cost power solution. It contains a master controller that manages startup sequencing, timing, voltages, slew rates, sleep states, and fault conditions. I²C configurability allows system level changes without the need for costly PCB changes. The built-in load bypass switch enables full sequencing configurability in 3.3V systems.

The ACT88320 master controller monitors all outputs and reports faults via I²C and hardwired status signals. Faults can be masked and fault levels and responses are configurable via I²C.

Many of the ACT88320 pins and functions are configurable. The IC's default functionality is defined by the default CMI (Code Matrix Index), but much of this functionality can be changed via I²C. Several GPIOs can be configured as enable inputs, reset outputs, dynamic voltage (DVS) inputs, LED drivers, etc. The GPIO configuration is specifically defined for each ACT88320 orderable part number. The first part of the datasheet describes basic IC functionality and default pin functions. The end of the datasheet provides the configuration and functionality specific to each CMI version. Contact sales@active-semi.com for additional information about other configurations.

I²C Serial Interface

To ensure compatibility with a wide range of systems, the ACT88320 uses standard I²C commands. The ACT88320 operates as a slave device, and can be factory configured to one of four 7-bit slave addresses. The 7-bit slave address is followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC's slave address

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x25h	010 0101b	0x4Ah	0x4Bh
0x27h	010 0111b	0x4Eh	0x4Fh
0x67h	110 0111b	0xCEh	0xCFh
0x6Bh	110 1011b	0xD6h	0xD7h

There is no timeout function in the I²C packet processing state machine, however, any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet. The I²C functionality is operational in all states except RESET.

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pull-up resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics Table.

I²C Registers

The ACT88320 contains an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, sequencing, fault thresholds, fault masks, etc. These registers are what give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult sales@active-semi.com for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected device behavior.

State Machine

Figure 1 shows the ACT88320 internal state machine.

RESET State

In the RESET, or "cold" state, the ACT88320 is waiting for the input voltage on VIN to be within a valid range defined by the VIN_UV and VIN_OV thresholds. All regulators are off in RESET. All reset outputs are asserted low. All volatile registers are reset to defaults and Non-Volatile registers are reset to programmed defaults. The IC transitions from RESET to POWER SEQUENCE START when the input voltage enters the valid range. The IC transitions from any other state to RESET if the input voltage drops below the VIN_UV threshold voltage. It is important to note any transition to RESET returns all volatile and non-volatile registers to their default states.

POWER SEQUENCE START State

The POWER SEQUENCE START state is a transitional state while the regulators are starting. The IC does not operate in this state.

ACTIVE State

The ACTIVE state is the normal operating state when the input voltage is within the allowable range, all outputs are turned on, and no faults are present.

SLEEP State

The SLEEP state is a low power mode for the operating system. Each output can be programmed to be on or off in the SLEEP state. The outputs follow their programmed sequencing delay times when turning on or off as they enter or exit the SLEEP state. Buck1/2/3 can be programmed to regulate to their VSET0 voltage, VSET1 voltage, or be turned off in the SLEEP state. LDO1/2 can be programmed to regulate to their VSET0 voltage or can be programmed to be turned off. Note that LDO1/2 do not have a VSET1 voltage.

The IC can enter SLEEP state via I²C registers SLEEP and SLEEP EN. Table 1 shows the conditions to enter

SLEEP state. ACT88320 I²C stays enabled in SLEEP state. The IC exits the SLEEP state when the conditions to enter SLEEP state are no longer present.

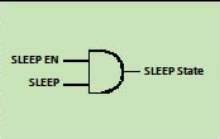| SLEEP Mode				
SLEEP MODE (Register)	PWREN Pin	SLEEP_EN (Register)	SLEEP (Register)	Enter SLEEP State
x	x	0	0	NO
x	x	0	1	NO
x	x	1	0	NO
x	x	1	1	YES
x	x	0	0	NO
x	x	0	1	NO
x	x	1	0	NO
x	x	1	1	YES

Table 1. SLEEP Mode Truth Table

DPSLP State

The DPSLP state is another low power operating mode for the operating system. It is intended to be used in a lower power configuration than the SLEEP mode. It is similar to the SLEEP state, but DPSLP uses slightly different configurations to enter and exit this mode. Each output can be programmed to be on or off in the DPSLP state. This programming can different from the SLEEP state. The outputs follow their programmed sequencing delay times when turning on or off as they enter or exit the DPSLP state.

The IC can enter DPSLP state via I²C registers DPSLP and DPSLP EN and/or a GPIO input pin. Table 2 shows the conditions to enter DPSLP state. ACT88320 I²C stays enabled in DPSLP state. The IC exits the DPSLP state when the conditions to enter DPSLP state are no longer present.

If OV, UV, or THERMAL faults occur when in DPSLP state, the IC resets to the POWER ON/Active state.
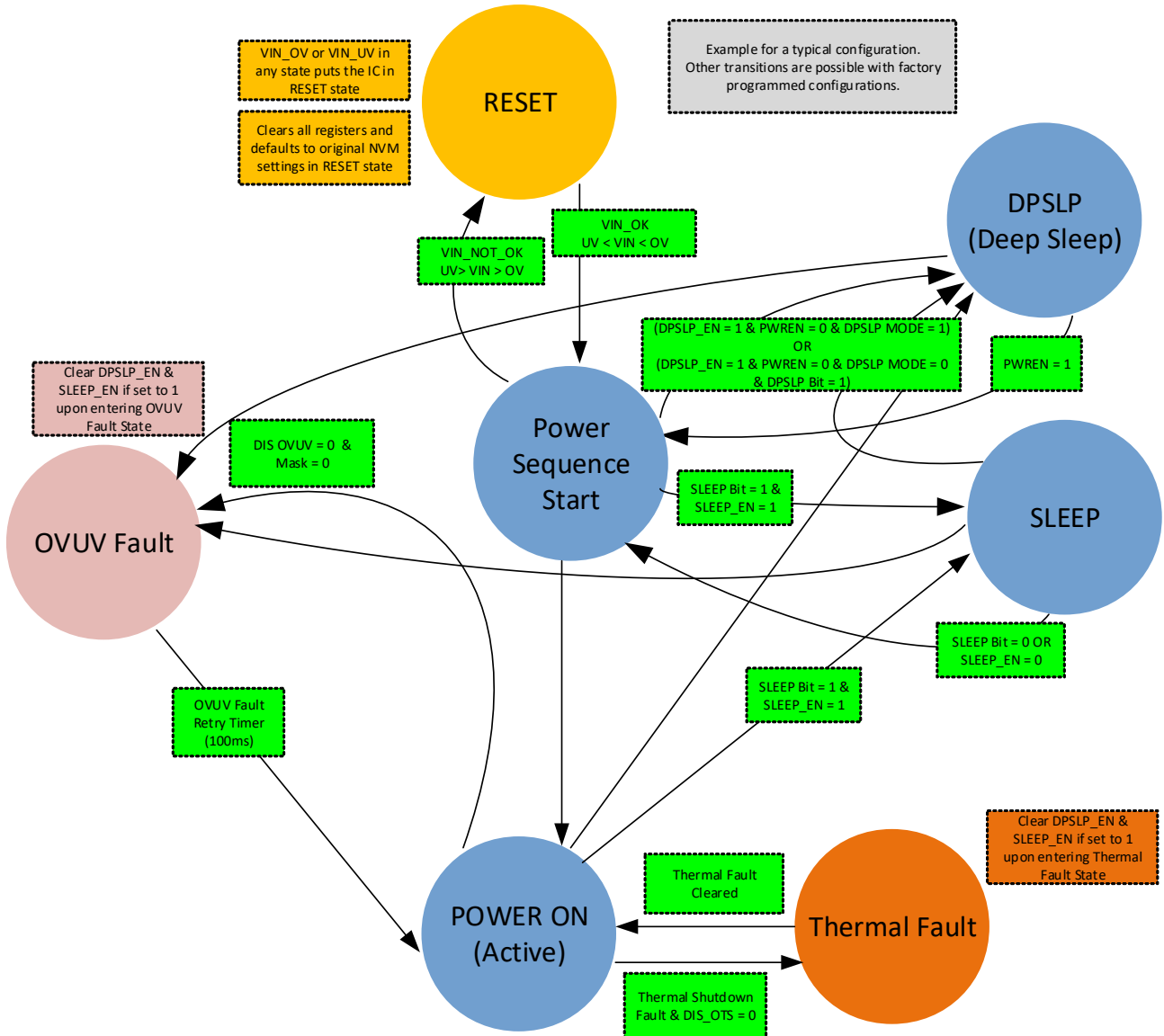
Figure 1 PWREN State Machine

Special consideration is needed for DPSLP state in with a non-I2C system. When PWREN is first toggled high after power up, the ACT88320 detects the first rising transition of PWREN from 0 to 1 and sets the DPSLP_EN register bit to 1. On the falling transition of PWREN from 1 to 0, DPSLP state is entered. In a condition when the system is powered up when PWREN = 1, PWREN must be toggled to 0 and back to 1 to set the DPSLP_EN bit. The next falling PWREN transition puts

the IC into the DPSLP state. While in DPSLP mode, if there is a fault condition such as system UV or OV or a thermal fault, the IC resets the DPSLP_EN bit back to 0 when it exits DPSLP mode. This requires PWREN to be toggled high to set the DPSLP_EN to 1 again and then toggled back low to enter DPSLP state again. The IC does not automatically go back into DPSLP state after exiting the DPSLP state due to fault conditions.

DPSLP MODE (Register)	PWREN pin	DPSLP_EN (Register)	DPSLP (Register)	Enter DPSLP State
0	0	0	0	No
0	0	0	1	No
0	0	1	0	No
0	0	1	1	Yes
0	1	0	0	No
0	1	0	1	No
0	1	1	0	No
0	1	1	1	No
1	0	0	0	No
1	0	0	1	No
1	0	1	0	Yes
1	0	1	1	Yes
1	1	0	0	No
1	1	0	1	No
1	1	1	0	No
1	1	1	1	No
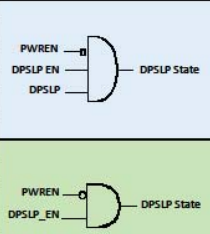
Table 2. DPSLP Mode with Truth Table

THERMAL State

In the THERMAL state the chip has exceeded the thermal shutdown temperature. To protect the device, all the regulators are shut down and the reset pins are asserted low. This state can be disabled by setting register 0x01h bit5 (TMSK) = 1. TMSK prevents the interrupt from going active, but does not prevent the IC from entering the THERMAL State.

OVUV FAULT State

In the OVUV FAULT state one of the regulators has exceed an OV level at any time or UV level after the soft start ramp has completed. All regulators shutdown and all three reset outputs are asserted low when the IC enters OVUVFLT state. The OVUVFLT state is timed to retry after 100ms and enter the ACTIVE state. If the OV or UV condition still exists in the ACTIVE state the IC returns back to the OVUVFLT state. The cycle continues until the OV or UV fault is removed or the input power is removed. This state can be disabled by setting the DIS_OVUV_SHUTDOWN bit high. The IC does not directly enter OVUVFLT in an overcurrent condition, but does enter this state due to the resulting UV condition.

Each regulator has an undervoltage fault mask and an overvoltage fault mask. If the UV or OV fault mask is active, nIRQ is not asserted in the fault condition. Even though the fault is masked, the system can still read each regulators UV and OV. Even though the fault is masked, the IC still enters the OVUV Fault state.

Startup/Shutdown

The IC automatically transitions from the RESET state to the POWER SEQUENCE START state when input power is applied. The IC then transitions to either the POWER ON, SLEEP, or DPSLP state depending on the status of the inputs in Tables 1 and 2. A typical startup profile is for the system to automatically transition from RESET to POWER ON when input power is applied. The typical shutdown sequence is for the system to pull PWREN low to enter DPSLP.

Sequencing

The ACT88320 provides the end user with extremely versatile sequencing capability that can be optimized for many different applications. Each of the five outputs has four basic sequencing parameters: input trigger, turn-on delay, turn-off delay, and output voltage. The buck converters also have softstart time control. Each of these parameters is controlled via the ICs internal registers. As an example, the ACT88320QI101-T sequencing and output voltages are optimized for the Silicon Motion SM2258 and SM2259 processors. The specifics for this IC as well as others are detailed at the end of the datasheet. Contact sales@active-semi.com for custom sequencing configurations. Refer to the Active-Semi Application Note AN-109, ACT88320Q101 Register Definitions, for full details on the I2C register map functionality and programming ranges.

Input trigger. The input trigger for a regulator is the event that turns that regulator on. Each output can have a separate input trigger. The input trigger can be the internal power ok (POK) signal from one of the other regulators, the internal VIN POK signal, or an external signal applied to an input pin such as EXT_PG or GPIO. This flexibility allows a wide range of sequencing possibilities, including having some of the outputs be sequenced with an external power supply or a control signal from the host. As an example, if the LDO1 input trigger is Buck1, LDO1 will not turn on until Buck1 is in regulation. Input triggers are defined at the factory and can only be changed with a custom CMI configuration. The GPIOx outputs can be connected to an internal power supply's POK signal and used to trigger external supplies in the overall sequencing scheme. The GPIOx inputs can also be connected to an external power supply's power good output and used as an input trigger for an ACT88320 supply.

Turn-on Delay. The turn-on delay is the time between an input trigger going active and the output starting to turn on. Each output's turn-on delay is configured via its I2C bit ON DELAY. Turn-on delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Turn-off Delay. The turn-off delay is the time between an input trigger going inactive and the output starting to

turn off. Each output's turn-off delay is configured via its I2C bit OFF_DELAY. Turn-off delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Softstart Time. The softstart time is the time it takes an output to ramp from 10% to 90% of its programmed voltage. All buck converter softstart times are controlled by a single I2C bit ALL_BUCKS_FASTER_SS. When set to 0, the softstart times are 600µs. When set to 1, the softstart times are 250µs. The default softstart time can be changed after the IC is powered on, but it is volatile and resets to the factory defaults when power is recycled.

Output Voltage. The output voltage is each regulator's desired voltage. Each buck's output voltage is programmed via its I2C bits VSET0 and VSET1. The output regulates to VSET0 in ACTIVE mode. They can be programmed to regulate to VSET1 in DVS, SLEEP, and DSPSLP modes. Each LDO has a single register, VSET, to set its output voltage. Each output's voltage can be changed after the IC is powered on, but the new setting is volatile and is reset to the factory defaults when power is recycled. Output voltages can be changed on the fly. If a large output voltage change is required, it is best to make multiple smaller changes. This prevents the IC from detecting an instantaneous over or under voltage condition because the fault thresholds are immediately changed, but the output takes time to respond.

Dynamic Voltage Scaling

On-the-fly dynamic voltage scaling (DVS) for the three buck converters is available via either the I2C interface or a GPIO. DVS allows systems to save power by quickly adjusting the microprocessor performance level when the workload changes. Note that DVS is not a different operating state. The IC operates in the ACTIVE state, but just regulates the outputs to a different voltage. Each buck converter operates at its VOUT0 voltage in normal operation and operates at its VOUT1 voltage when the DVS input trigger is active. DVS can be implemented three ways.

The first method is to individually put each buck converter in DVS by manually writing a new voltage regulation setpoint into its VOUT0 register.

DVS can also be implemented for all buck converters at one time via a single GPIO input. The IC's specific CMI determines the specific GPIO used for DVS. This setting can be modified with a custom CMI.

DVS can be implemented for all buck converters at one time via I2C. The user can select from two different configurations to enter DVS via I2C. Note that DVS is disabled when EN_DVS_I2C = 0.

1. **Enable DVS via a single I2C write to I2C_DVS_ON bit:** With EN_DVS_I2C = 1 and SEL_DVS_IN = 0, the IC enters DVS when I2C_DVS_ON = 1 and exits DVS when it equals 0.

2. **Enable DVS whenever the IC enters SLEEP state:** With EN_DVS_I2C = 1 and SEL_DVS_IN = 1, any condition that puts the IC into SLEEP state also puts the IC into DVS mode. Note that I2C_DVS_ON bit does not affect this configuration.

Note that the IC cannot be configured to enter DVS in DPSLP state. Table 3 summarizes I2C DVS functionality.

EN_DVS_I2C	SEL_DVS_IN	I2C_DVS_ON	DVS MODE
0	x	x	Off
1	0	0	Off
1	0	1	On
1	1	x	On in SLEEP state

Table 3. I2C DVS Control

For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

Input Voltage Monitoring (SYSMON)

The ACT88320 monitors the input voltage on the VIN pins to ensure it is within specified limits for system level operation. The IC "wakes up" and allows I2C communication when VIN rises above UVLO (~2.7V). However, the outputs do not turn on until VIN rises above the SYSMON threshold. SYSMON is programmable between 2.7V and 4.2V. The IC then asserts the nIRQ pin if VIN drops below SYSMON, but the outputs continue to operate normally. The IC turns off all outputs if the input

voltage drops below UVLO. I²C bit VSYSSTAT = 1 when VIN < SYSMON and 0 when VIN > SYSMON. This fault can be masked with I²C bit VSYSMSK.

Fault Protection

The ACT88320 contains several levels of fault protection, including the following:

Output Overvoltage

Output Undervoltage

Output Current Limit and short circuit

Thermal Warning

Thermal Shutdown

There are three types of I²C register bits associated with each fault condition: fault flag bits, fault bits, and mask bits. The fault flag bits display the real-time fault status. Their status is valid regardless of whether or not that fault is masked. The mask bits either block or allow the fault to affect the fault bit. Each potential fault condition can be masked via I²C if desired. Any unmasked fault condition results in the fault bit going high, which asserts the nIRQ pin. nIRQ is typically active low. The nIRQ pin only de-asserts after the fault condition is no longer present and the corresponding fault bit is read via I²C. Note that masked faults can still be read in the fault flag bit. Refer to Active-Semi Application Note describing the Register Map for full details on I²C functionality and programming ranges.

nIRQ (Interrupt)

The interrupt function is typically used to drive the interrupt input of the system processor. Many of the ACT88320's functions support interrupt-generation as a result of various conditions. These are typically masked by default, but may be unmasked via the I²C interface. For more information about the available fault conditions, refer to the appropriate sections of this datasheet. nIRQ can be triggered from:

1. Die temperature warning generated

2. Any buck regulator exceeding peak current limit for 16 cycles after soft start or a UV/OV condition.

3. Any LDO regulator exceeding current limit for more than 16uS after soft start or a UV/OV condition.

4. Input goes above OVP threshold or falls below the UV threshold.

If any of these faults occur the nIRQ output is asserted active low. After nIRQ pin is asserted, an I²C reading operation of the interrupt status registers clears the interrupt provided the interrupting condition is removed. If the interrupting condition is still present, nIRQ stays asserted and the interrupt status bit stays set. The interrupt status registers are 0x00h, 0x01h, 0x03h, 0x04h, 0x05h, 0xA0h, 0xA6h, and 0xE5h.

The ICs specific CMI determines which GPIOx is used for the nIRQ pin. nIRQ is an open-drain output and should be pulled up to an appropriate supply voltage with a 10kΩ or greater pull-up resistor.

nRESET

The ACT88320 provides a reset function to issue a master reset to the system CPU/controller. nRESET is immediately asserted low when either the VIN voltage is above or below the UV or OV thresholds or any power supply that is connected to the nRESET functionality goes below its Power Good threshold. The IC's specific CMI configures which power supplies are connected to the nRESET functionality. After startup, nRESET de-asserts after a programmable delay time when VIN and all connected power supply outputs are above their respective UVLO thresholds. The reset delay time, 20ms to 100ms, is controlled by the I²C TRST_DLY register bits. The IC's CMI programs the specific GPIOx pin used for the reset functionality. The CMI also programs which regulators outputs are monitored for the reset functionality.

EXT_EN

The ACT88320 provides an external power supply enable function, EXT_EN. EXT_EN is used to control an external regulator or to provide a control signal to other system components. It is used as part of the sequencing profile and can be programmed to have different input triggers as well as delay times. The IC's CMI programs the specific GPIOx pin used for the EXT_EN functionality.

EXT_PG

The ACT88320 provides an external input trigger, EXT_PG, for startup sequencing. EXT_PG can be used as the startup trigger for one or of the power supplies. EXT_EN and EXT_PG allow the IC to fully incorporate one or more external power supplies into the startup sequence. The IC's CMI programs the specific GPIOx pin used for the EXT_EN functionality.

Output Under/Over Voltage

The ACT88320 monitors the output voltages for under voltage and over voltage conditions. If an output enters an UV/OV fault condition, the IC shuts down all outputs for 100ms and restarts with the programmed power up

sequence. If an output is in current limit, it is possible that its voltage can drop below the UV threshold which also shuts down all outputs. If that behavior is not desired, mask the appropriate fault bit. Each output still provides its real-time UV/OV fault status via its fault flag, even if the fault is masked. Masking an OV/UV fault just prevents the fault from being reported via the IRQ pin. A UV/OV fault condition pulls the nRESET pin low. Note that the IC's specific CMI sets the defaults for which regulators mask the UV and OV fault conditions.

Output Current Limit

The ACT88320 incorporates a three level overcurrent protection scheme for the buck converters and a single level scheme for the LDOs. For the buck converters, the overcurrent current threshold refers to the peak switch current. The first protection level is when a buck converter's peak switch current reaches 75% of the Cycle-by-Cycle current limit threshold for greater than 16 switching cycles. Under this condition, the IC reports the fault via the appropriate fault flag bit. If the fault is unmasked, it asserts the nIRQ pin. The next level is when the current increases to the Cycle-by-Cycle threshold. The buck converter limits the peak switch current in each switching cycle. This reduces the effective duty cycle and causes the output voltage to drop, potentially creating an undervoltage condition. When the overcurrent condition results in an UV condition, and UV is not masked, the IC turns off all supplies for 100ms and restarts. The third level is when the peak switch current reaches 122% of the Cycle-by-Cycle current limit threshold. This immediately shuts down the regulator and waits 14ms before restarting.

For LDOs, the overcurrent thresholds are set by each LDO's Output Current Limit setting. When the output current reaches the Current Limit threshold, the LDO limits the output current. This reduces the output voltage, creating an undervoltage condition, causing all supplies to turn off for 100ms before restarting.

The overcurrent fault limits for the buck converters are adjustable via I2C. LDO current limit is fixed. Overcurrent fault reporting can be masked via I2C, but the overcurrent limits are always active and will shut down the IC when exceeded.

Thermal Warning and Thermal Shutdown

The ACT88320 monitors its internal die temperature and reports a warning via nIRQ when the temperature rises above the Thermal Interrupt Threshold of typically 135 deg C. It reports a fault when the temperature rises above the Thermal Shutdown Temperature of typically 160 deg C. A temperature fault shuts down all outputs unless the fault is masked. Both the fault and the warning can be masked via I2C. The temperature warning and fault flags still provide real-time status even if the faults are masked. Masking just prevents the faults from being reported via the nIRQ pin.

INRUSH CONTROL

When power is applied to the system, the OVSNS pin checks for under voltage and over voltage. If the input voltage is within spec, the IC turns on an external N-Channel MOSFET, which supplies power to the VIN and AVIN pins. VIN and AVIN power the IC, the buck converters, and the LDOs. The IC controls the voltage ramp on VIN to control the inrush current from the input voltage. The gate drive voltage is typically V, which requires a 12V gate drive FET.

OVP CONTROL

When over voltage is detected on the OVSNS pin, it generates a fault condition to shutdown the inrush controller. The overvoltage condition latches VIN output off until the overvoltage condition is removed. When the input voltage is within specified limits, the IC automatically restarts. An OVP condition is not reported via I2C.

Input Current Limit

An external sense resistor can be used between OVSNS and OVSNS_M to detect the input current to VIN. An overcurrent warning occurs when the voltage across the sense resistor reaches 72.5% of the current limit threshold. The current warning asserts nIRQ low. The current limit warning can be masked with I2C bit IN-RUSH_ILIM_MSK. An overcurrent condition occurs when the voltage across the sense resistor reaches the current limit threshold voltage of 85mV. OVGATE modulates the external MOSFET gate voltage to regulate the maximum current through the MOSFET and protect against an overcurrent condition. If the system attempts to pull more current, the VIN voltage starts to drop. If VIN drops below the programmed SYSMON setting, the IC asserts nIRQ.

Pin Descriptions

Many of the ACT88320 input and output pins are configurable via CMI configurations. The following descriptions are refer to basic pin functions and capabilities. Refer to the CMI Options section in the back of the datasheet for specific pin functionality for each CMI.

VIN

VIN pins are the dedicated input power to the buck converters. Buck1 uses pins 17 and 18. Buck2 uses pins 23 and 24. Buck 3 uses pins 1 and 2. Each buck converter must be bypassed directly to PGND on the top PCB layer with a 10uF capacitor.

AVIN

AVIN is the input power to the LDOs. It also powers the IC's analog circuitry. AVIN must be bypassed directly to AGND on the top PCB layer with a 1uF ceramic capacitor.

OVGATE

This pin drives the gate of an external N-ch FET. OVGATE slowly turns on the FET to provide softstart when power is applied. It quickly turns off the FET in an overvoltage condition. Connect to PGND if the input overvoltage FET is not used.

OVSNS, OVSNS_M

These are the positive and negative input current sense pins. They should be kelvin connected to the input current sense resistor. OVSNS is also the input voltage sense pin. Connect to PGND if the input overvoltage FET is not used.

VIO

This is the bias supply input to the IC's digital circuitry. It powers the GPIO pins. VIO is typically connected to the VIN pins, but can be powered from a different voltage rail if desired. VIO should be bypassed to PGND with a 1uF ceramic capacitor.

PWREN

PWREN is a digital input that helps determine if the IC operates in POWER ON mode or DPSLP mode. Refer to the DPSLP State section for details.

PWREN is referenced to the AVIN pin, and is 5.5V tolerant meaning that PWREN can go to 5.5V even if AVIN is less than 5.5V.   PWREN has a 10us bidirectional filter to prevent unwanted triggering from noise.

GPIOx

The ACT88320 has four GPIO pins. Each GPIO is programmed for a specific function by the IC's CMI. The available functions are input triggers for sequencing (EXT_PG), output triggers for sequencing (EXT_EN), nRESET, nIRQ, DVS, voltage select pins for the voltage regulators, LED drivers, and GPIO.

GPIO1 (pin 13).

GPIO1 can be programmed for any of the above functions except the LED drivers. It can be programmed for both open-drain and push-pull.

GPIO2 (pin 14).

GPIO2 is the same as GPIO1

GPIO3 (pin 12).

GPIO3 can be programmed for all the above functions including the LED drivers. It can be only be programmed for open-drain outputs.

GPIO4 (pin 11).

GPIO4 is the same as GPIO3

GPIOx pins can be programmed as an input or an output. They are 5.5V tolerant meaning they can go to 5.5V even if VIO is less than 5.5V.

SCL, SDA

These are the I²C clock and data pins to the IC. They have standard I²C functionality.

PGND

The PGND pins are the buck converter power ground pins. They connect directly to the buck converters' low side FETs. Buck1 and Buck2 use pin 21. Buck3 uses pins 7 and 8. All PGND pins must be connected directly to the IC's exposed pad under the IC.

SWx

SWx are the switch nodes for the buck converters. They connect directly to the buck inductor on the top layer.

FB_Bx

These are the feedback pins for the buck regulators. They should be kelvin connected to the buck output capacitors.

LSG1

LSG1 is the load switch FET gate drive pin.

OUT_LDOx

These are the LDO output pins. Each LDO output must be bypassed to AGND with a 1uF capacitor.

AGND

AGND is the ground pin for the IC's analog circuitry and LDOs. AGND must be connected to the IC's exposed pad. The connection between AGND and the exposed pad should not have high currents flowing through it.

EXPOSED PAD

The exposed pad is the ICs ground reference. All ground pins must connect to the exposed pad. It must be soldered to the PCB.

Step-down DC/DC Converters

General Description

The ACT88320 contains three fully integrated step-down converters. Buck1 is a 4A output, while Buck2 and Buck3 are 2.5A outputs. All buck converters are fixed frequency, current-mode controlled, synchronous PWM converters that achieve peak efficiencies of up to 95%. The buck converters switch at 1.125MHz or 2.25MHz and are internally compensated, requiring only three small external components (Cin, Cout, and L) for operation. The buck regulators minimize noise in sensitive applications with the use of a switching phase delay and offset. Additionally, all regulators are available with a variety of standard and custom output voltages, and may be software-controlled via the I2C interface for systems that require advanced power management functions.

The ACT88320 buck regulators are highly configurable and can be quickly and easily reconfigured via I2C. This allows them to support changes in hardware requirements without the need for PCB changes. Examples of I2C functionality are given below:

Real-time power good, OV, and current limit status

Ability to mask individual faults

Dynamically change output voltage

On/Off control

Softstart ramp

Slew rate control

Switching delay and phase control

Low power mode

Overcurrent thresholds

Refer to the Active-Semi Application Note describing the Register Map for full details on I2C functionality and programming ranges.

100% Duty Cycle Operation

All buck converters are capable of 100% duty cycle operation. During 100% duty cycle operation, the high-side power MOSFETs are held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

Operating Mode

By default, all buck converters operate in fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving mode at light loads in order to save power. Power-save mode reduces conduction losses by preventing the inductor current from going negative.

To further optimize efficiency, a low power mode, LPM, is available that provides even higher efficiency with very small load currents. LPM minimizes quiescent current at the expense of slightly larger transient response. LPM is user controllable and can be enabled and disabled dynamically to allow the customer to optimize the balance between power consumption and transient response. LPM is enabled when I2C bits DISLPM = 0 and LP_MODE = 1.

The buck converters can also be forced to operate in PWM mode at light load by setting I2C bit ForcePWM = 1. This results in slightly lower efficiency at light loads, but improves transient response.

Synchronous Rectification

Buck1/2/3 each feature integrated synchronous rectifiers (or LS FET drivers), maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Soft-Start

Buck1/2/3 include internal 600us soft-start ramps which limit the rate of change of the output voltage, minimizing input inrush current and ensuring that the output powers up in a monotonic manner that is independent of loading on the outputs. This circuitry is effective any time the regulator is enabled, as well as after responding to a short-circuit or other fault condition. A single I2C register, ALL_BUCKS_FASTER_SS, adjusts softstart between 600us when = 0 and 250us when = 1.

Output Voltage Setting

Buck1/2/3 regulate to the voltage defined by I2C register VSET0 in normal operation and by VSET1 in DVS mode. Buck1 can be programmed between 0.6V and 2.991V in 9.376mV steps.

$$V_{buck1} = 0.6 + VOUTx * 0.009376V$$

Where VOUTx is the decimal equivalent of the value in each regulator's I2C VOUTx register. The VOUTx registers contain an unsigned 8-bit binary value. As an example, if Buck 1's VOUT0 register contains 01000000b (128 decimal), the output voltage is 1.8V.