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ACT8848

Rev 2, 15-Nov-12

Advanced PMU for Multi-core Application Processors

FEATURES

INTEGRATED POWER SUPPLIES

- **Four DC/DC Step-Down (Buck) Regulators**
  - **2 x 2.8A, 2 x 1.5A**
- **Five Low-Noise LDOs (350mA)**
- **Three Low-Input Voltage LDOs (350mA)**
- **One Low IQ Keep-Alive LDO**
- **Backup Battery Charger**

SYSTEM CONTROL AND INTERFACE

- **Six General Purpose I/O with PWM Drivers**
- **I²C Serial Interface**
- **Interrupt Controller**

SYSTEM MANAGEMENT

- **Reset Interface and Sequencing Controller**
  - **Power on Reset**
  - **Soft / Hard Reset**
  - **Watchdog Supervision**
  - **Multiple Sleep Modes**
- **Thermal Management Subsystem**

APPLICATIONS

- **Tablet PC**
- **Mobile Internet Devices (MID)**
- **Ebooks**
- **Personal Navigation Devices**

GENERAL DESCRIPTION

The ACT8848 is a complete, cost effective, and highly-efficient *ActivePMU™* power management solution optimized for the power, voltage sequencing and control requirements of Telechips TCC88xx and Samsung S5PC210 application processors. (Please see the ORDERING INFORMATION section to get the Full Part Numbers.)

The ACT8848 features four fixed-frequency, current-mode, synchronous PWM step-down converters that achieve peak efficiencies of up to 97%. These regulators operate with a fixed frequency of 2.25MHz, minimizing noise in sensitive applications and allowing the use of small external components. These buck regulators supply up to 2.8A of output current and can fully satisfy the power and control requirements of the multi-core application processors. Dynamic Voltage Scaling (DVS) is supported either by dedicated control pins, or through I2C interface to optimize the energy-per-task performance for the processors. This device also includes eight low-noise LDOs (up to 350mA per LDO), one always-ON LDO and an integrated backup battery charger to provide the complete power system for the processors.

The power sequence and reset controller provides power-on reset, SW-initiated reset, and power cycle reset for the processor. It also features the watchdog supervisory function. Multiple sleep modes with autonomous sleep and wake-up sequence control are supported.

The thermal management and protection subsystem allows the host processor to manage the power dissipation of the PMU and the overall system dynamically. The PMU provides a thermal warning to the host processor when the temperature reaches a certain threshold such that the system can turn off some of the non-essential functions, reduce the clock frequency and etc to manage the system temperature.

The ACT8848 is available in a compact, Pb-Free and RoHS-compliant TQFN66-48 package.

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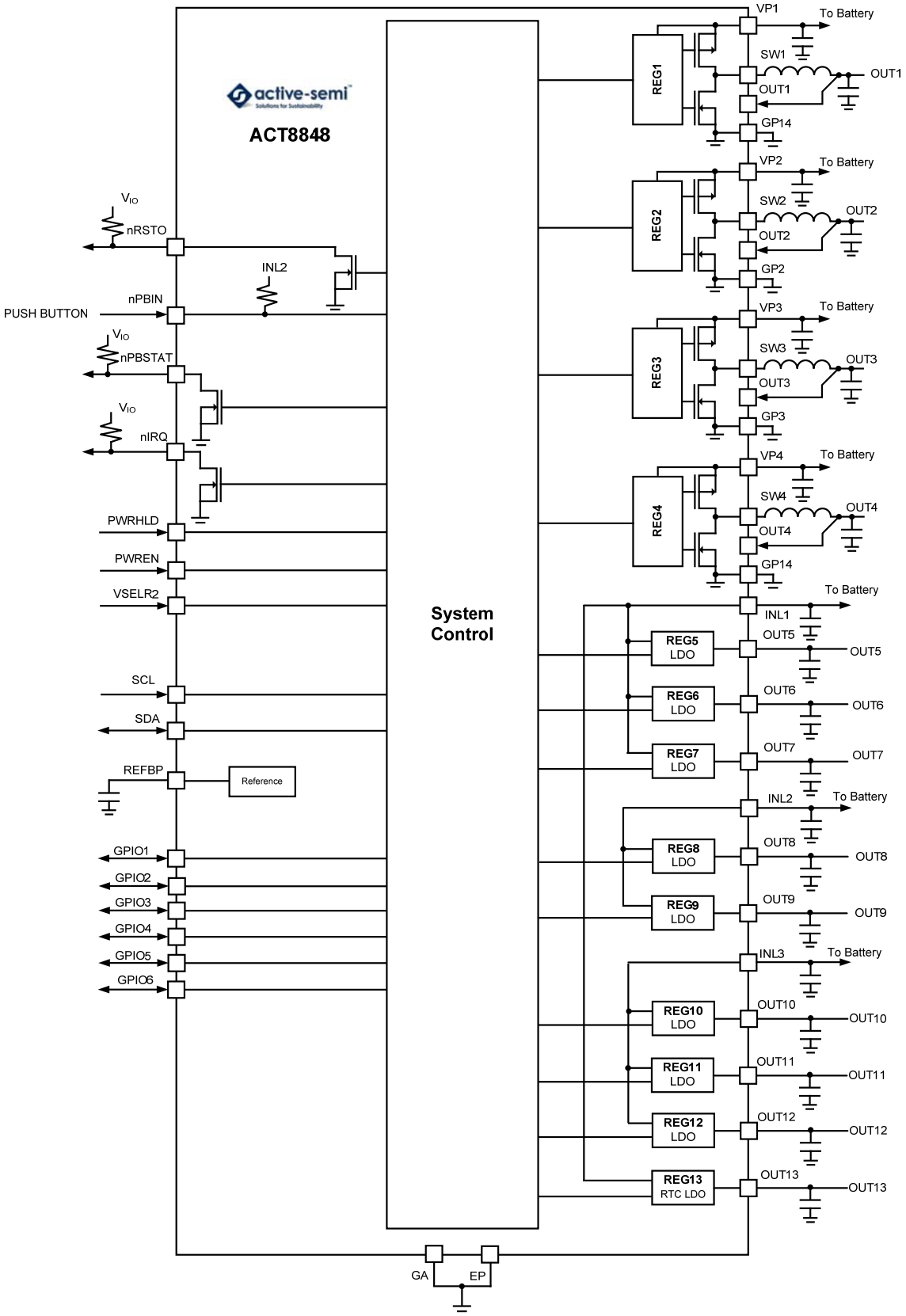
FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION①

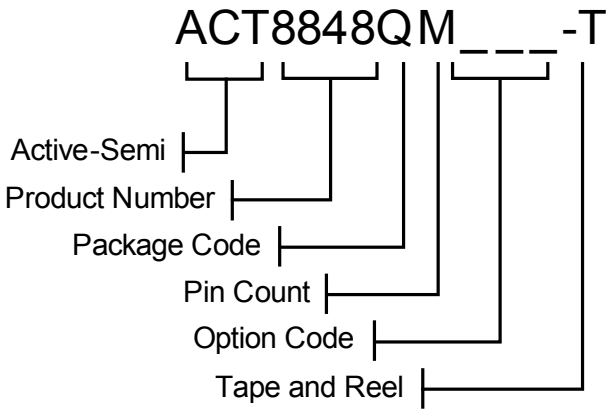
PART NUMBER	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{OUT4}	V_{OUT5}	V_{OUT6}	V_{OUT7}	V_{OUT8}	V_{OUT9}	V_{OUT10}	V_{OUT11}	V_{OUT12}	V_{OUT13}
ACT8848QM135-T	1.8V	1.45V	1.25V	3.3V	2.8V	3.3V	3.3V	1.8V	1.2V	1.2V	1.8V	1.8V	3.3V
ACT8848QM144-T	1.5V	1.45V	1.25V	3.3V	2.8V	3.3V	3.3V	1.8V	1.2V	1.2V	1.8V	1.8V	3.3V
ACT8848QM201-T	1.2V	1.2V	1.1V	1.1V	1.1V	1.1V	2.8V	1.8V	3.3V	1.2V	1.1V	1.8V	1.8V

PACKAGE	PINS	TEMPERATURE RANGE
TQFN66-48	48	-40°C to +85°C

①: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

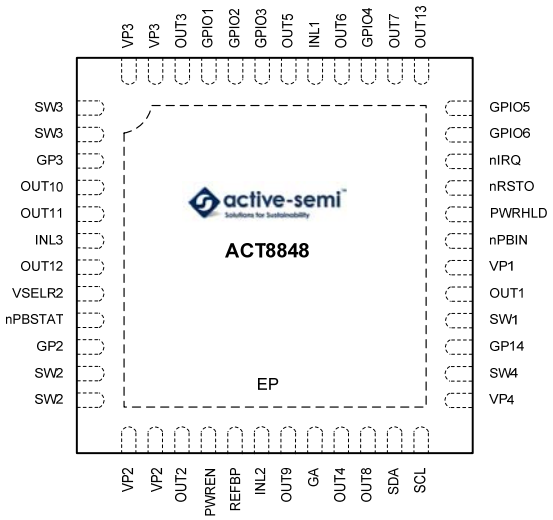
②: ACT8848QM144-T has the same specification as ACT8848QM135-T except V_{OUT1} which is set as 1.5V to support DDR III application.

③: ACT8848 Data Sheet is described according to ACT8848QM135-T application; please see the Appendix of ACT8848QM201-T for its specification.



PIN CONFIGURATION

TOP VIEW



Thin - QFN (TQFN66-48)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1, 2	SW3	Switch Node for REG3.
3	GP3	Power Ground for REG3. Connect GP14, GP2, GP3, and GA together at a single point as close to the IC as possible.
4	OUT10	REG10 output. Bypass it to ground with a 2.2µF capacitor.
5	OUT11	REG11 output. Bypass it to ground with a 2.2µF capacitor.
6	INL3	Power input for REG10, REG11 and REG12.
7	OUT12	REG12 output. Bypass it to ground with a 2.2µF capacitor.
8	VSELR2	Output Voltage Selection for REG2. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage.
9	nPBSTAT	Active-Low Open-Drain Push-Button Status Output. nPBSTAT is asserted low whenever the nPBIN is pushed, and is high-Z otherwise.
10	GP2	Power ground for REG2. Connect GP14, GP2, GP3, and GA together at a single point as close to the IC as possible.
11, 12	SW2	Switch Node for REG2.
13, 14	VP2	Power input for REG2. Bypass to GP2 with a high quality ceramic capacitor placed as close to the IC as possible.
15	OUT2	Output Voltage Sense for REG2.
16	PWREN	Power enable input.
17	REFBP	Reference Bypass. Connect a 0.047µF ceramic capacitor from REFBP to GA. This pin is discharged to GA in shutdown.
18	INL2	Power Input for REG8, REG9.
19	OUT9	REG9 output. Bypass it to ground with a 2.2µF capacitor.
20	GA	Analog Ground.
21	OUT4	Output voltage sense for REG4.
22	OUT8	REG8 output. Bypass it to ground with a 2.2µF capacitor.
23	SDA	Data Input for I^2C Serial Interface. Data is read on the rising edge of SCL.
24	SCL	Clock Input for I^2C Serial Interface.
25	VP4	Power input for REG4. Bypass to GP14 with a high quality ceramic capacitor placed as close to the IC as possible.

PIN DESCRIPTIONS CONT'D

PIN	NAME	DESCRIPTION
26	SW4	Switch Node for REG4.
27	GP14	Power Ground for REG1 and REG4. Connect GP14, GP2, GP3, and GA together at a single point as close to the IC as possible.
28	SW1	Switch Node for REG1.
29	OUT1	Output Voltage Sense for REG1.
30	VP1	Power Input for REG1. Bypass to GP14 with a high quality ceramic capacitor placed as close to the IC as possible.
31	nPBIN	Master Enable Input. Drive nPBIN to GA through a 50kΩ resistor to enable the IC, drive nPBIN directly to GA to assert a Manual-Reset condition.
32	PWRHLD	Power hold Input.
33	nRSTO	Open-Drain Reset Output.
34	nIRQ	Open-Drain Interrupt Output.
35	GPIO6	General Purpose I/O #6. Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the *PWM LED Drive* section for more information.
36	GPIO5	General Purpose I/O #5. Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the *PWM LED Driver* section for more information.
37	OUT13	REG13 output. Bypass it to ground with a 2.2µF capacitor.
38	OUT7	REG7 output. Bypass it to ground with a 2.2µF capacitor.
39	GPIO4	General Purpose I/O #4. Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the *PWM LED Driver* section for more information.
40	OUT6	REG6 output. Bypass it to ground with a 2.2µF capacitor.
41	INL1	Power Input for REG5, REG6, REG7.
42	OUT5	REG5 output. Bypass it to ground with a 2.2µF capacitor.
43	GPIO3	General Purpose I/O #3. Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the *PWM LED Drier* section for more information.
44	GPIO2	General Purpose I/O #2. Configured as VSELR4 for Voltage Selection of REG4. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage.
45	GPIO1	General Purpose I/O #1. Configured as VSELR3 for Voltage Selection of REG3. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage.
46	OUT3	Output Voltage Sense for REG3.
47,48	VP3	Power input for REG3. Bypass to GP3 with a high quality ceramic capacitor placed as close to the IC as possible.
EP	EP	Exposed Pad. Must be soldered to ground on PCB.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
INL1, INL2, INL3 to GA; VP1, SW1, OUT1 to GP14; VP2, SW2, OUT2 to GP2; VP3, SW3, OUT3 to GP3; VP4, SW4, OUT4 to GP14	-0.3 to 6	V
GP14, GP2, GP3 to GA	-0.3 to + 0.3	V
OUT5, OUT6, OUT7, OUT13 to GA	-0.3 to INL1 + 0.3	V
OUT8, OUT9, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, VSELR2, nPBIN, nRSTO, nIRQ, nPBSTAT, PWREN, PWRHLD, REFBP, SCL, SDA to GA	-0.3 to INL2 + 0.3	V
OUT10, OUT11, OUT12 to GA	-0.3 to INL3 + 0.3	V
Junction to Ambient Thermal Resistance	21	°C/W
Operating Ambient Temperature Range	-40 to 85	°C
Operating Junction Temperature	-40 to 125	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

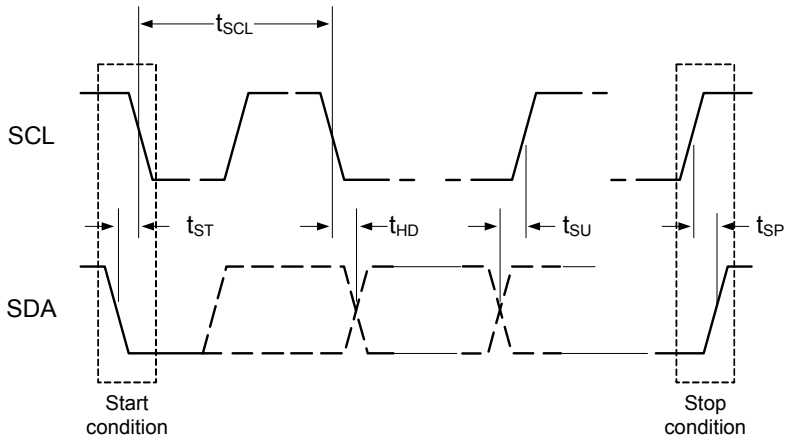
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{INL2} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{INL2} = 3.1V to 5.5V, T_A = -40ºC to 85ºC			0.35	V
SCL, SDA Input High	V_{INL2} = 3.1V to 5.5V, T_A = -40ºC to 85ºC	1.55			V
SDA Leakage Current				1	µA
SCL Leakage Current				1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Period, t_{SCL}		1.5			µs
SDA Data Setup Time, t_{SU}		100			ns
SDA Data Hold Time, t_{HD}		300			ns
Start Setup Time, t_{ST}	For Start Condition	100			ns
Stop Setup Time, t_{SP}	For Stop Condition	100			ns

Figure 1:
I²C Compatible Serial Bus Timing



GLOBAL REGISTER MAP

BLOCK	ADDRESS		BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
SYS	0x00	NAME	nBATLEVMSK	nBATSTAT	VBATDAT	*Reserved*	BATLEV[3]	BATLEV[2]	BATLEV[1]	BATLEV[0]
		DEFAULT①	0	R	R	0	0	0	0	0
SYS	0x01	NAME	nTMSK	TSTAT	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT①	0	R	0	0	0	0	0	0
REG1	0x10	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	0	0	1	0	0
REG1	0x12	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	0	0	R
REG2	0x20	NAME	*Reserved*	*Reserved*	VSET0[5]	VSET0[4]	VSET0[3]	VSET0[2]	VSET0[1]	VSET0[0]
		DEFAULT①	0	0	0	1	1	1	0	1
REG2	0x21	NAME	*Reserved*	*Reserved*	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	0	1	1	1	0	1
REG2	0x22	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	0	0	R
REG3	0x30	NAME	*Reserved*	*Reserved*	VSET0[5]	VSET0[4]	VSET0[3]	VSET0[2]	VSET0[1]	VSET0[0]
		DEFAULT①	0	0	0	1	1	0	0	1
REG3	0x31	NAME	*Reserved*	*Reserved*	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	0	1	1	0	0	1
REG3	0x32	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	1	0	R
REG4	0x40	NAME	*Reserved*	*Reserved*	VSET0[5]	VSET0[4]	VSET0[3]	VSET0[2]	VSET0[1]	VSET0[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG4	0x41	NAME	*Reserved*	*Reserved*	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG4	0x42	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	1	0	R
REG5	0x50	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	1	0	1	0	0
REG5	0x51	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	1	0	R
REG6	0x58	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	1	1	0	0	1
REG6	0x59	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	1	0	R
REG7	0x60	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG7	0x61	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	0	0	0	0	0	1	0	R
REG8	0x68	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	0	0	1	0	0
REG8	0x69	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	0	0	0	0	0	1	0	R

①: Default values of ACT8848QM135-T.

GLOBAL REGISTER MAP CONT'D

BLOCK	ADDRESS		BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
REG9	0x70	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG9	0x71	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	0	0	0	0	0	1	0	R
REG10	0x80	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	0	1	1	0	0	0
REG10	0x81	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	1	0	R
REG11	0x90	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	0	0	1	0	0
REG11	0x91	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	1	0	R
REG12	0xA0	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	0	0	1	0	0
REG12	0xA1	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	1	0	R
REG13	0xB1	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT①	1	0	0	0	0	0	0	0
PB	0xC0	NAME	PBAMSK	PBDMSK	*Reserved*	*Reserved*	*Reserved*	*Reserved*	WDSREN	WDPCEN
		DEFAULT①	0	0	0	0	0	0	0	0
PB	0xC1	NAME	INTADR [7]	INTADR [6]	INTADR [5]	INTADR [4]	INTADR [3]	INTADR [2]	INTADR [1]	INTADR [0]
		DEFAULT①	R	R	R	R	R	R	R	R
PB	0xC2	NAME	PBASTAT	PBDSTAT	PBDAT	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT①	R	R	R	R	R	R	R	R
PB	0xC3	NAME	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	SIPC
		DEFAULT①	0	0	0	0	0	0	0	0
PB	0xC5	NAME	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PCSTAT	SRSTAT
		DEFAULT①	0	0	0	0	0	0	R	R
GPIO6	0xE3	NAME	PWM6EN	FRE6[2]	FRE6[1]	FRE6[0]	DUTY6[3]	DUTY6[2]	DUTY6[1]	DUTY6[0]
		DEFAULT①	0	0	0	0	0	0	0	0
GPIO5	0xE4	NAME	PWM5EN	FRE5[2]	FRE5[1]	FRE5[0]	DUTY5[3]	DUTY5[2]	DUTY5[1]	DUTY5[0]
		DEFAULT①	0	0	0	0	0	0	0	0
GPIO3	0xF4	NAME	PWM3EN	FRE3[2]	FRE3[1]	FRE3[0]	DUTY3[3]	DUTY3[2]	DUTY3[1]	DUTY3[0]
		DEFAULT①	0	0	0	0	0	0	0	0
GPIO4	0xF5	NAME	PWM4EN	FRE4[2]	FRE4[1]	FRE4[0]	DUTY4[3]	DUTY4[2]	DUTY4[1]	DUTY4[0]
		DEFAULT①	0	0	0	0	0	0	0	0

①: Default values of ACT8848QM135-T.

REGISTER AND BIT DESCRIPTIONS

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
SYS	0x00	[7]	nBATLEVMSK	R/W	Battery Voltage Level Interrupt Mask. Set this bit to 1 to unmask the interrupt. See the *Programmable Battery Voltage Monitor* section for more information
SYS	0x00	[6]	nBATSTAT	R	Battery Voltage Status. Value is 1 when BATLEV interrupt is generated, value is 0 otherwise.
SYS	0x00	[5]	VBATDAT	R	Battery Voltage Monitor real time status. Value is 1 when VBAT < BATLEV, value is 0 otherwise.
SYS	0x00	[4]	-	R/W	Reserved.
SYS	0x00	[3:0]	BATLEV	R/W	Battery Voltage Detect Threshold. Defines the BATLEV voltage threshold. See the *Programmable Battary Voltage Monitor* section for more information.
SYS	0x01	[7]	nTMSK	R/W	Thermal Interrupt Mask. Set this bit to 1 to unmask the interrupt.
SYS	0x01	[6]	TSTAT	R	Thermal Interrupt Status. Value is 1 when a thermal interrupt is generated, value is 0 otherwise.
SYS	0x01	[5:0]	-	R/W	Reserved.
REG1	0x10	[7:6]	-	R	Reserved.
REG1	0x10	[5:0]	VSET0	R/W	Primary Output Voltage Selection. See the *Output Voltage Programming* section for more information
REG1	0x12	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG1	0x12	[6:3]	-	R	Reserved.
REG1	0x12	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG1	0x12	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG1	0x12	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG2	0x20	[7:6]	-	R	Reserved.
REG2	0x20	[5:0]	VSET0	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information
REG2	0x21	[7:6]	-	R	Reserved.
REG2	0x21	[5:0]	VSET1	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information.
REG2	0x22	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG2	0x22	[6:3]	-	R	Reserved.
REG2	0x22	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG2	0x22	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG2	0x22	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG3	0x30	[7:6]	-	R	Reserved.
REG3	0x30	[5:0]	VSET0	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information
REG3	0x31	[7:6]	-	R	Reserved.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG3	0x31	[5:0]	VSET1	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information.
REG3	0x32	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG3	0x32	[6:3]	-	R	Reserved.
REG3	0x32	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG3	0x32	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG3	0x32	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG4	0x40	[7:6]	-	R	Reserved.
REG4	0x40	[5:0]	VSET0	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information
REG4	0x41	[7:6]	-	R	Reserved.
REG4	0x41	[5:0]	VSET1	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information.
REG4	0x42	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG4	0x42	[6:3]	-	R	Reserved.
REG4	0x42	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG4	0x42	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG4	0x42	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG5	0x50	[7:6]	-	R	Reserved.
REG5	0x50	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG5	0x51	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG5	0x51	[6:3]	-	R	Reserved.
REG5	0x51	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG5	0x51	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG5	0x51	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG6	0x58	[7:6]	-	R	Reserved.
REG6	0x58	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG6	0x59	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG6	0x59	[6:3]	-	R	Reserved.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG6	0x59	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG6	0x59	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG6	0x59	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG7	0x60	[7:6]	-	R	Reserved.
REG7	0x60	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG7	0x61	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG7	0x61	[6:3]	-	R	Reserved.
REG7	0x61	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG7	0x61	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG7	0x61	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG8	0x68	[7:6]	-	R	Reserved.
REG8	0x68	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG8	0x69	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG8	0x69	[6:3]	-	R	Reserved.
REG8	0x69	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG8	0x69	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG8	0x69	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG9	0x70	[7:6]	-	R	Reserved.
REG9	0x70	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG9	0x71	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG9	0x71	[6:3]	-	R	Reserved.
REG9	0x71	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG9	0x71	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG9	0x71	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG10	0x80	[7:6]	-	R	Reserved.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG10	0x80	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG10	0x81	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG10	0x81	[6:3]	-	R	Reserved.
REG10	0x81	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG10	0x81	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG10	0x81	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG11	0x90	[7:6]	-	R	Reserved.
REG11	0x90	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG11	0x91	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG11	0x91	[6:3]	-	R	Reserved.
REG11	0x91	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG11	0x91	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG11	0x91	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG12	0xA0	[7:6]	-	R	Reserved.
REG12	0xA0	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG12	0xA1	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG12	0xA1	[6:3]	-	R	Reserved.
REG12	0xA1	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG12	0xA1	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG12	0xA1	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG13	0xB1	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG13	0xB1	[6:0]	-	R	Reserved.
PB	0xC0	7	nPBAMSK	R/W	nPBIN Assertion Interrupt Control. Set this bit to 1 to generate an interrupt when nPBIN is asserted.
PB	0xC0	6	nPBDMSK	R/W	nPBIN De-assertion Interrupt Control. Set this bit to 1 to generate an interrupt when nPBIN is de-asserted.
PB	0xC0	[5:2]	-	R	Reserved.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
PB	0xC0	1	WDSREN	R/W	Watchdog Soft-Reset Enable. Set this bit to 1 to enable watchdog function. When the watchdog timer expires, the PMU commences a soft-reset routine. This bit is automatically reset to 0 when entering sleep mode.
PB	0xC0	0	WDPCEN	R/W	Watchdog Power-Cycle Enable. Set this bit to 1 to enable watchdog function. When watchdog timer expires, the PMU commence a power cycle. This bit is automatically reset to 0 when entering sleep mode.
PB	0xC1	[7:0]	INTADR	R	Interrupt Address. It holds the address of the block that triggers the interrupt. This byte defaults to 0xFF and is automatically set to 0xFF after being read. Bit 7 is the MSB while Bit 0 is the LSB.
PB	0xC2	7	PBASTAT	R	nPBIN Assertion Interrupt Status. The value of this bit is 1 if the nPBIN Assertion Interrupt is triggered.
PB	0xC2	6	PBDSTAT	R	nPBIN De-assertion Interrupt Status. The value of this bit is 1 if the nPBIN De-assertion Interrupt is triggered.
PB	0xC2	5	PBASTAT	R	nPBIN Status bit. This bit contains the real-time status of the nPBIN pin. The value of this bit is 1 if nPBIN is asserted, and is 0 if nPBIN is de-asserted.
PB	0xC2	[4:0]	-	R	Reserved.
PB	0xC3	[7:1]	-	R	Reserved.
PB	0xC3	0	SIPC	R/W	Software Initiated Power Cycle. When this bit is set, the PMU commences a power cycle after 8ms delay.
PB	0xC5	[7:2]	-	R	Reserved.
PB	0xC5	1	PCSTAT	R/W	Power-cycle Flag. The value of this bit is 1 after a power cycle. This bit is automatically cleared to 0 after read.
PB	0xC5	0	SRSTAT	R/W	Soft-reset Flag. The value of this bit is 1 after a soft-reset. This bit is automatically cleared to 0 after read.
GPIO6	0xE3	[7]	PWM6EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO6.
GPIO6	0xE3	[6:4]	FRE6	R/W	PWM Frequency Selection Bits for GPIO6. See the Table 6 for code to frequency cross.
GPIO6	0xE3	[3:0]	DUTY6	R/W	Duty Cycle Selection Bits for GPIO6. See the Table 7 for code to duty cross.
GPIO5	0xE4	[7]	PWM5EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO5.
GPIO5	0xE4	[6:4]	FRE5	R/W	PWM Frequency Selection Bits for GPIO5. See the Table 6 for code to frequency cross.
GPIO5	0xE4	[3:0]	DUTY5	R/W	Duty Cycle Selection Bits for GPIO5. See the Table 7 for code to duty cross.
GPIO3	0xF4	[7]	PWM3EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO3.
GPIO3	0xF4	[6:4]	FRE3	R/W	PWM Frequency Selection Bits for GPIO3. See the Table 6 for code to frequency cross.
GPIO3	0xF4	[3:0]	DUTY3	R/W	Duty Cycle Selection Bits for GPIO3. See the Table 7 for code to duty cross.
GPIO4	0xF5	[7]	PWM4EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO4.
GPIO4	0xF5	[6:4]	FRE4	R/W	PWM Frequency Selection Bits for GPIO4. See the Table 6 for code to frequency cross.
GPIO4	0xF5	[3:0]	DUTY4	R/W	Duty Cycle Selection Bits for GPIO4. See the Table 7 for code to duty cross.

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(V_{INL2} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		3.0		5.5	V
UVLO Threshold Voltage	V_{INL2} Rising	2.6	2.8	3.0	V
UVLO Hysteresis	V_{INL2} Hysteresis		200		mV
Operating Supply Current	All Regulators Enabled but no load		0.6	1.2	mA
Shutdown Supply Current	All Regulators Disabled except REG13		10	20	µA
Oscillator Frequency		2.0	2.25	2.5	MHz
Logic High Input Voltage		1.4			V
Logic Low Input Voltage				0.4	V
Leakage Current	V[nIRQ] = V[nRSTO] = 4.2V			1	µA
Low Level Output Voltage	nIRQ, nRSTO, ISINK = 5mA			0.3	V
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis			20		°C

STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = V_{VP3} = V_{VP4} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
UVLO Threshold	Input Voltage Rising	2.5	2.6	2.7	V
UVLO Hysteresis	Input Voltage Falling		100		mV
Standby Supply Current	V_{OUT} = 103%, Regulator Enabled		72	100	μA
Shutdown Current	V_{VP} = 5.5V, Regulator Disabled		0	2	μA
Output Voltage Accuracy	V_{OUT} ≥ 1.0V, I_{OUT} = 10mA	-1%	V_{NOM}①	1%	V
	V_{OUT} < 1.0V, I_{OUT} = 10mA	-10		10	mV
Line Regulation	V_{VP} = Max (V_{NOM}① +1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation REG1/4	I_{OUT} = 10mA to IMAX②		1.70		%/A
Load Regulation REG2/3	I_{OUT} = 10mA to IMAX②		1.00		%/A
Power Good Threshold	V_{OUT} Rising		93		%V_{NOM}
Power Good Hysteresis	V_{OUT} Falling		2		%V_{NOM}
Switching Frequency	V_{OUT} ≥ 20% of V_{NOM}	2	2.25	2.5	MHz
	V_{OUT} = 0V		550		kHz
Soft-Start Period			400		μs
Minimum On-Time			75		ns
REG1 AND REG4					
Maximum Output Current		1.5			A
Current Limit		1.8	2.2	2.7	A
PMOS On-Resistance	I_{SW} = -100mA		0.11		Ω
NMOS On-Resistance	I_{SW} = 100mA		0.08		Ω
SW Leakage Current	V_{VP} = 5.5V, V_{SW} = 0 or 5.5V		0	2	μA
Input Capacitor			4.7		μF
Output Capacitor			33		μF
Power Inductor		1.0	2.2	3.3	μH
REG2 AND REG3					
Maximum Output Current		2.8			A
Current Limit		3.5	4.2		A
PMOS On-Resistance	I_{SW} = -100mA		0.07		Ω
NMOS On-Resistance	I_{SW} = 100mA		0.08		Ω
SW Leakage Current	V_{VP} = 5.5V, V_{SW} = 0 or 5.5V		0	2	μA
Input Capacitor			10		μF
Output Capacitor			44		μF
Power Inductor		0.5	1	2.2	μH

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

LOW-NOISE LDO ELECTRICAL CHARACTERISTICS

(V_{INL1} = V_{INL2} = 3.6V, C_{OUT5} = C_{OUT6} = C_{OUT7} = C_{OUT8} = C_{OUT9} = 2.2μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.5		5.5	V
Output Voltage Accuracy	V_{OUT} ≥ 1.0V, I_{OUT} = 10mA	-1	V_{NOM}①	1	%
	V_{OUT} < 1.0V, I_{OUT} = 10mA	-10		10	mV
Line Regulation	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V		0.5		mV
Load Regulation	I_{OUT} = 1mA to IMAX②		0.1		V/A
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		75		dB
	f = 10kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		65		
Supply Current per Output	Regulator Enabled		25		μA
	Regulator Disabled		0	2	
Soft-Start Period	V_{OUT} = 3.0V		140		μs
Power Good Threshold	V_{OUT} Rising		92		%
Power Good Hysteresis	V_{OUT} Falling		3.5		%
Output Noise	I_{OUT} = 20mA, f = 10Hz to 100kHz, V_{OUT} = 1.2V		30		$μV_{RMS}$
Discharge Resistance	LDO Disabled, DIS[ ] = 1		1.5		kΩ
LDO rated at 350mA (REG5, REG6, REG7, REG8 & REG9)					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		140	280	mV
Maximum Output Current		350			mA
Current Limit④	V_{OUT} = 95% of regulation voltage	400			mA
Recommend Output Capacitor			2.2		μF

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher).

④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 50% (typ.)

LOW-INPUT VOLTAGE LDO ELECTRICAL CHARACTERISTICS

(V_{INL3} = 3.6V, C_{OUT10} = C_{OUT11} = C_{OUT12} = 2.2μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		1.7		5.5	V
Output Voltage Accuracy	V_{OUT} ≥ 1.0V, I_{OUT} = 10mA	-1	V_{NOM}①	1	%
	V_{OUT} < 1.0V, I_{OUT} = 10mA	-10		10	mV
Line Regulation	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V		0.5		mV
Load Regulation	I_{OUT} = 1mA to IMAX②		0.1		V/A
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		50		dB
	f = 10kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		40		
Supply Current per Output	Regulator Enabled		22		μA
	Regulator Disabled		0	2	
Soft-Start Period	V_{OUT} = 3.0V		100		μs
Power Good Threshold	V_{OUT} Rising		92		%
Power Good Hysteresis	V_{OUT} Falling		3.5		%
Output Noise	I_{OUT} = 20mA, f = 10Hz to 100kHz, V_{OUT} = 1.2V		30		$μV_{RMS}$
Discharge Resistance	LDO Disabled, DIS[ ] = 1		1.5		kΩ
LDO rated at 350mA (REG10, REG11 & REG12)					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		100	200	mV
Maximum Output Current		350			mA
Current Limit④	V_{OUT} = 95% of regulation voltage	400			mA
Recommend Output Capacitor			2.2		μF

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher).

④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 50% (typ)

LOW-POWER(ALWAYS-ON) LDO ELECTRICAL CHARACTERISTICS

(V_{INL1} = 3.6V, C_{OUT13} = 1μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REG13					
Operating Voltage Range		2.5		5.5	V
Output Voltage Accuracy		-3	V_{NOM}①	3	%
Line Regulation	V_{INL1} = Max (V_{OUT} + 0.2V, 2.5V) to 5.5V		13		mV
Supply Current from V_{INL1}			5		μA
Maximum Output current		50			mA
Recommend Output Capacitor		0.47			μF

PWM LED DRIVER ELECTRICAL CHARACTERISTICS

(V_{INL2} = 3.6V, T_A = 25°C, unless otherwise specified.)

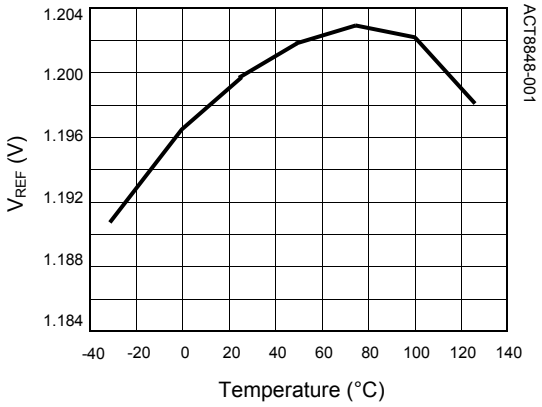
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Current	100% Duty Cycle	6	10	16	mA
Output Low Voltage	Feed in with 6mA			0.35	V
Leakage Current	Sinking from 5.5V source			1	μA
PWM Frequency	FRE[2:0] = 000		0.25		Hz
PWM Duty Adjustment	DUTY[3:0] = 0000 to 1111	6.25		100	%

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

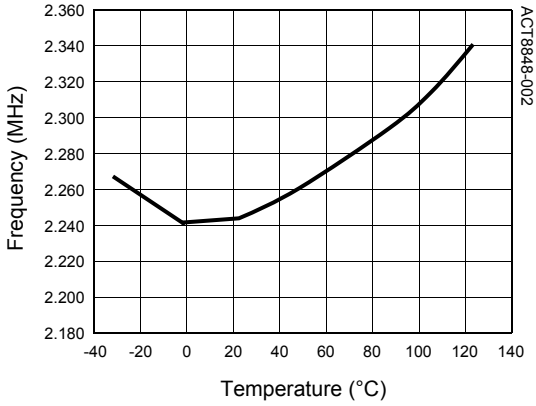
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, unless otherwise specified.)

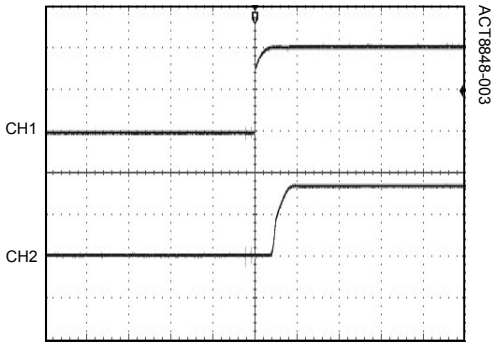
V_{REF} vs. Temperature



Frequency vs. Temperature

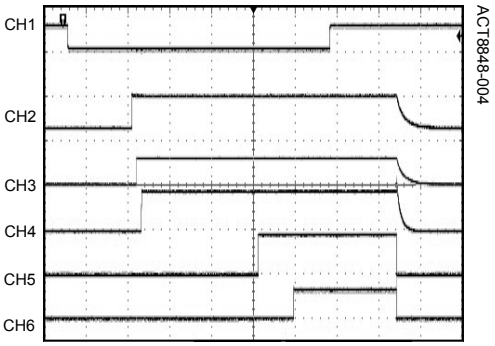


Startup of VIN/OUT13



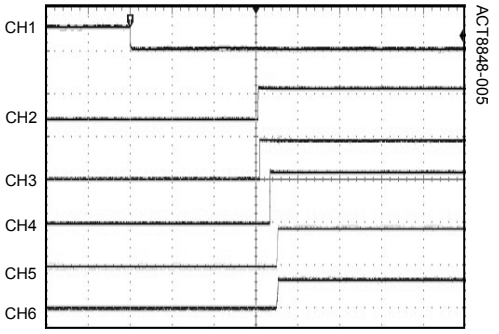
CH1: V_{in}, 2V/div
CH2: V_{OUT13}, 2V/div
TIME: 1ms/div

Startup Shutdown of nPBIN/OUT2/OUT3/ OUT1/nRSTO/PWRHLD



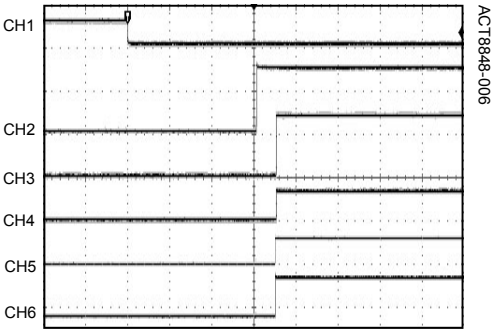
CH1: V_{nPBIN}, 2V/div
CH2: V_{OUT2}, 2V/div
CH3: V_{OUT3}, 2V/div
CH4: V_{OUT1}, 2V/div
CH5: V_{nRSTO}, 2V/div
CH6: V_{PWRHLD}, 5V/div
TIME: 20ms/div

Startup of nPBIN/OUT2/OUT11/OUT3/ OUT1/OUT4



CH1: V_{nPBIN}, 2V/div
CH2: V_{OUT2}, 2V/div
CH3: V_{OUT11}, 2V/div
CH4: V_{OUT3}, 1V/div
CH5: V_{OUT1}, 2V/div
CH6: V_{OUT4}, 5V/div
TIME: 10ms/div

Startup of nPBIN/OUT2/OUT5/OUT6/ OUT10/OUT12

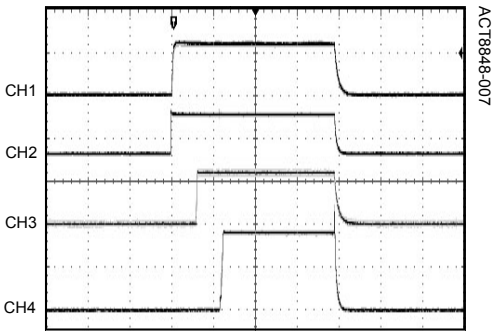


CH1: V_{nPBIN}, 2V/div
CH2: V_{OUT2}, 1V/div
CH3: V_{OUT5}, 2V/div
CH4: V_{OUT6}, 5V/div
CH5: V_{OUT10}, 2V/div
CH6: V_{OUT12}, 2V/div
TIME: 10ms/div

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

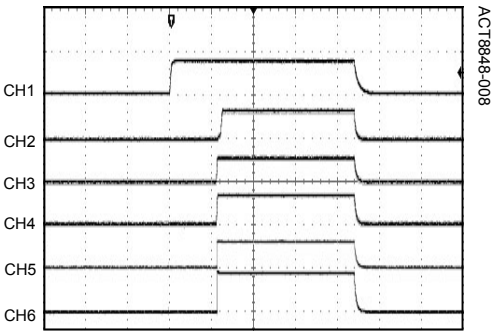
(T_A = 25°C, unless otherwise specified.)

Startup Shutdown of OUT2/OUT11/ OUT3/OUT1



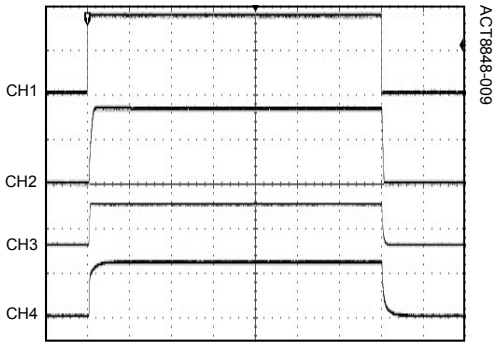
CH1: V_{OUT2}, 1V/div
CH2: V_{OUT11}, 2V/div
CH3: V_{OUT3}, 1V/div
CH4: V_{OUT1}, 1V/div
TIME: 4ms/div

Startup Shutdown of OUT2/OUT4/OUT5/ OUT6/OUT10/OUT12



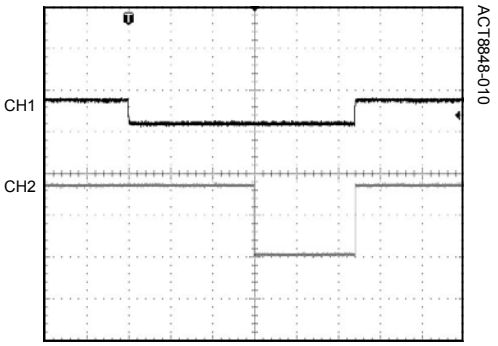
CH1: V_{OUT2}, 2V/div
CH2: V_{OUT4}, 5V/div
CH3: V_{OUT5}, 5V/div
CH4: V_{OUT6}, 5V/div
CH5: V_{OUT10}, 2V/div
CH6: V_{OUT12}, 2V/div
TIME: 4ms/div

Startup Shutdown of PWREN/OUT7/ OUT8/OUT9



CH1: V_{PWREN}, 2V/div
CH2: V_{OUT7}, 2V/div
CH3: V_{OUT8}, 2V/div
CH3: V_{OUT9}, 1V/div
TIME: 1ms/div

nPBIN and nPBSTAT

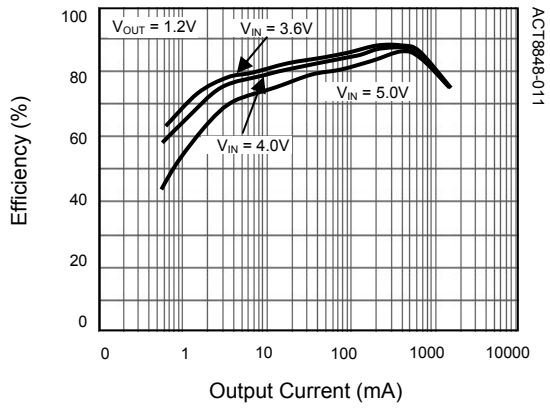


CH1: V_{nPBIN}, 2V/div
CH2: $V_{nPBSTAT}$, 2V/div
TIME: 10ms/div

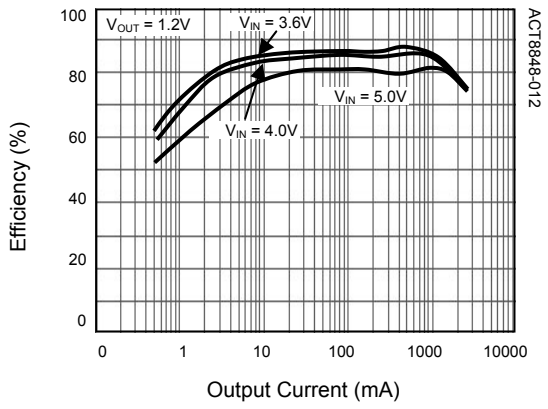
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

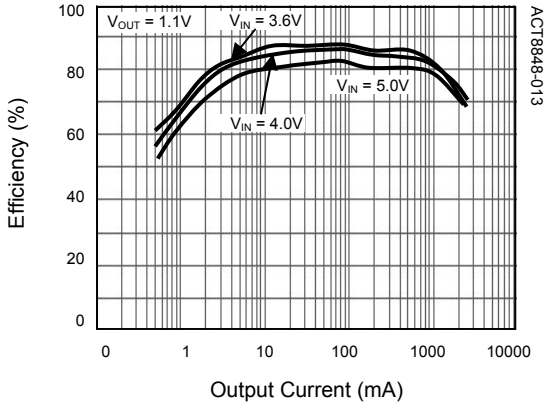
REG1 Efficiency vs. Output Current



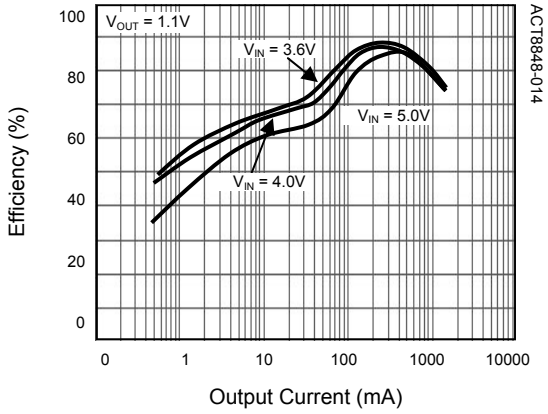
REG2 Efficiency vs. Output Current



REG3 Efficiency vs. Output Current



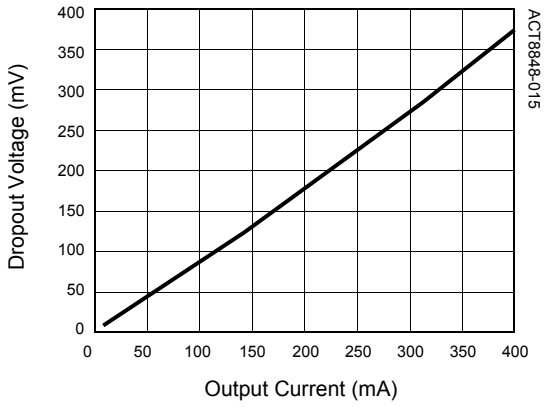
REG4 Efficiency vs. Output Current



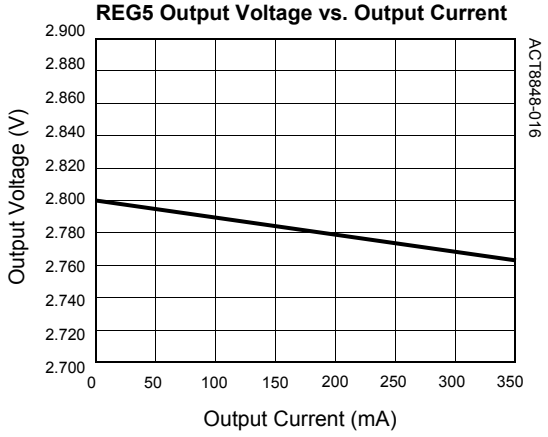
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

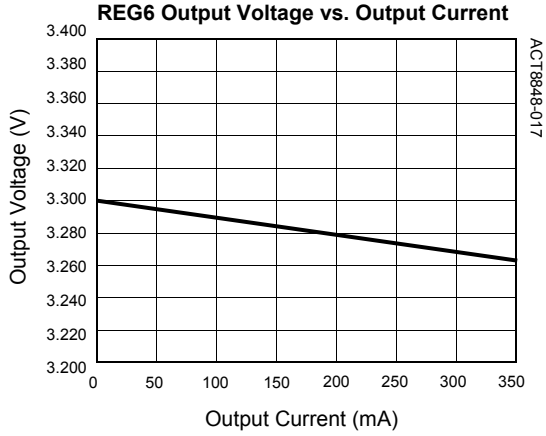
REG5/6/7/8 Dropout Voltage vs. Output Current



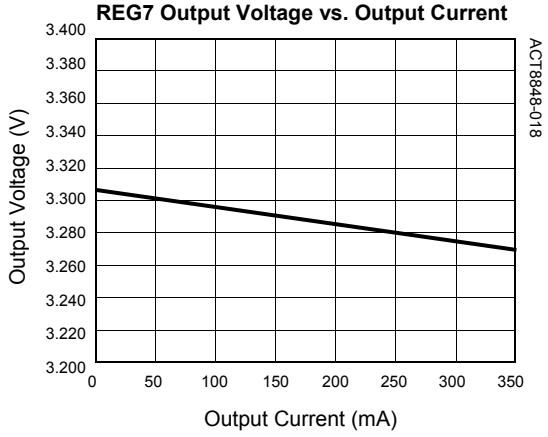
REG5 Output Voltage vs. Output Current



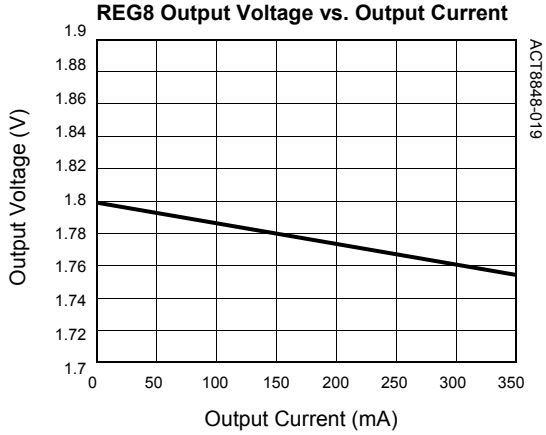
REG6 Output Voltage vs. Output Current



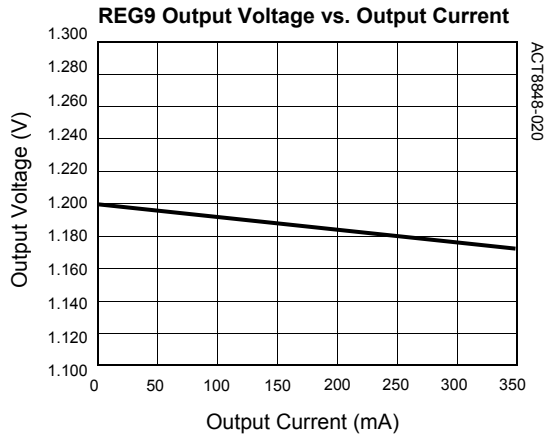
REG7 Output Voltage vs. Output Current



REG8 Output Voltage vs. Output Current



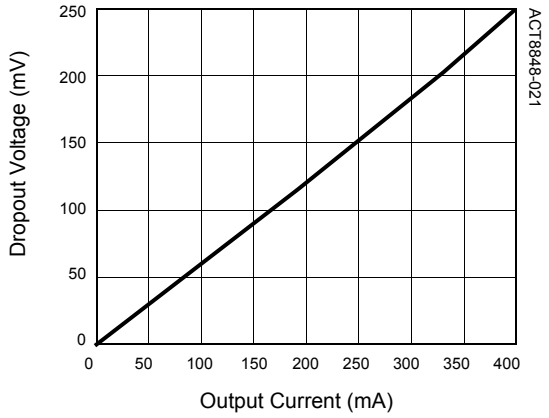
REG9 Output Voltage vs. Output Current



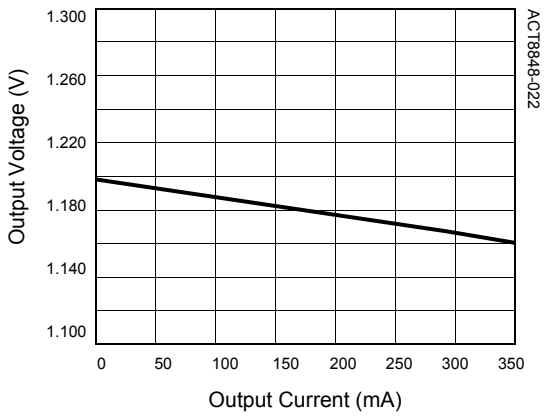
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

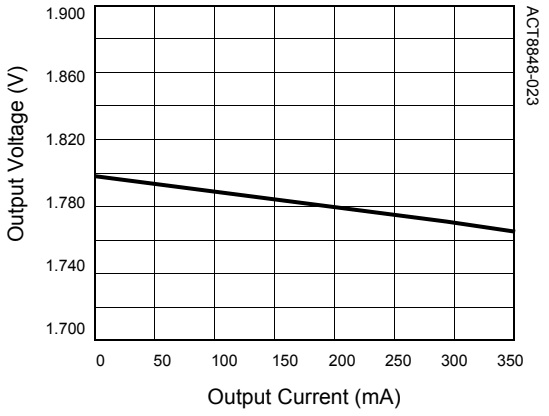
REG10/11/12 Dropout Voltage vs. Output Current



REG10 Output Voltage vs. Output Current



REG11 Output Voltage vs. Output Current



REG12 Output Voltage vs. Output Current