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**Advanced PMU for Microcontrollers and Solid State Drive Applications****BENEFITS and FEATURES**

- **Wide input voltage range**
  - **V<sub>in</sub> = 2.8V to 5.5V**
- **Complete integrated power solution**
  - **One 4A DC/DC Step-Down (Buck) Regulator**
  - **Three 2.5A DC/DC Step-Down (Buck) Regulators**
  - **One 800mA LDO**
  - **Two 200mA LDOs**
- **Space Savings**
  - **Fully integrated**
  - **High F<sub>sw</sub> = 2.25MHz or 1.125MHz**
  - **Integrated sequencing**
- **Easy system level design**
  - **Configurable sequencing**
  - **Seamless sequencing with external supplies**
- **Buck 1 Bypass Mode for 3.3V system level compliance**
- **Highly configurable**
  - **uP interface for status reporting and controllability**
  - **Programmable Reset and Power Good GPIO's**
  - **Flexible Sequencing Options**
- **I<sup>2</sup>C Interface – 1MHz**

**APPLICATIONS**

- Microcontroller Applications
- Solid-State Drives
- FPGA
- Video Processor

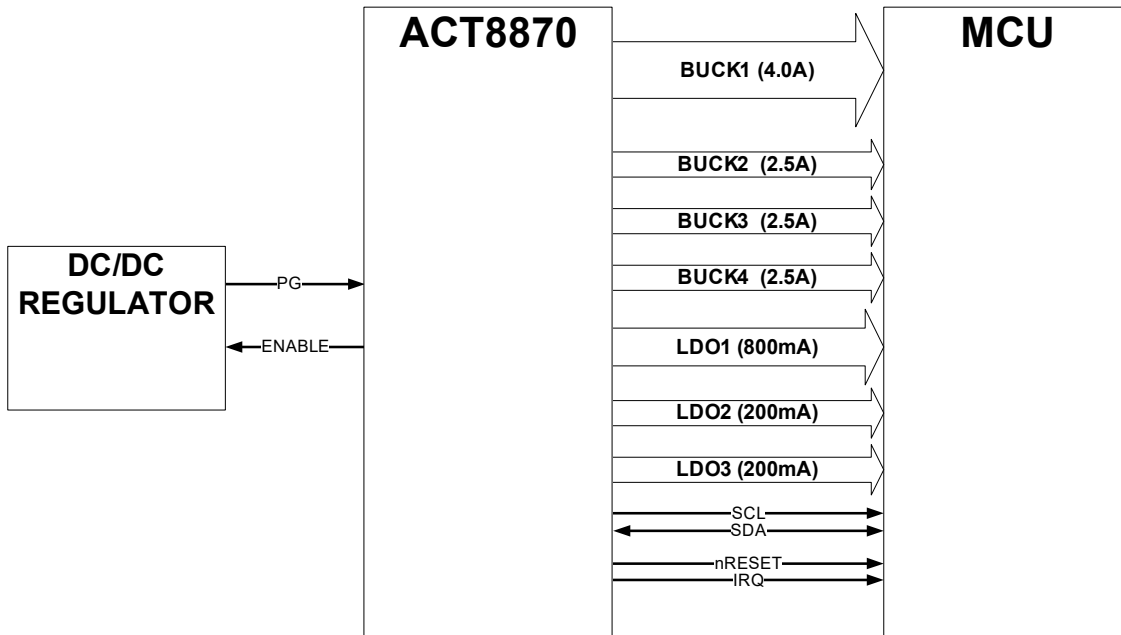
**GENERAL DESCRIPTION**

The ACT8870 PMIC is an integrated ActivePMU power management unit. It is designed to power a wide range of processors, including Atmel's SAMA5D2, FPGA's, peripherals, microcontrollers, and solid-state drive applications. It is highly flexible and can be reconfigured via I<sup>2</sup>C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speeds time to market. Examples of configurable options include output voltage, startup time, slew rate, system level sequencing, switching frequency, sleep modes, operating modes etc. ACT8870 is programmed at the factory with default configuration. These settings can be optimized for a specific design through the I<sup>2</sup>C interface. The ACT8870 comes in several default configuration. Contact the factory for specific default configurations.

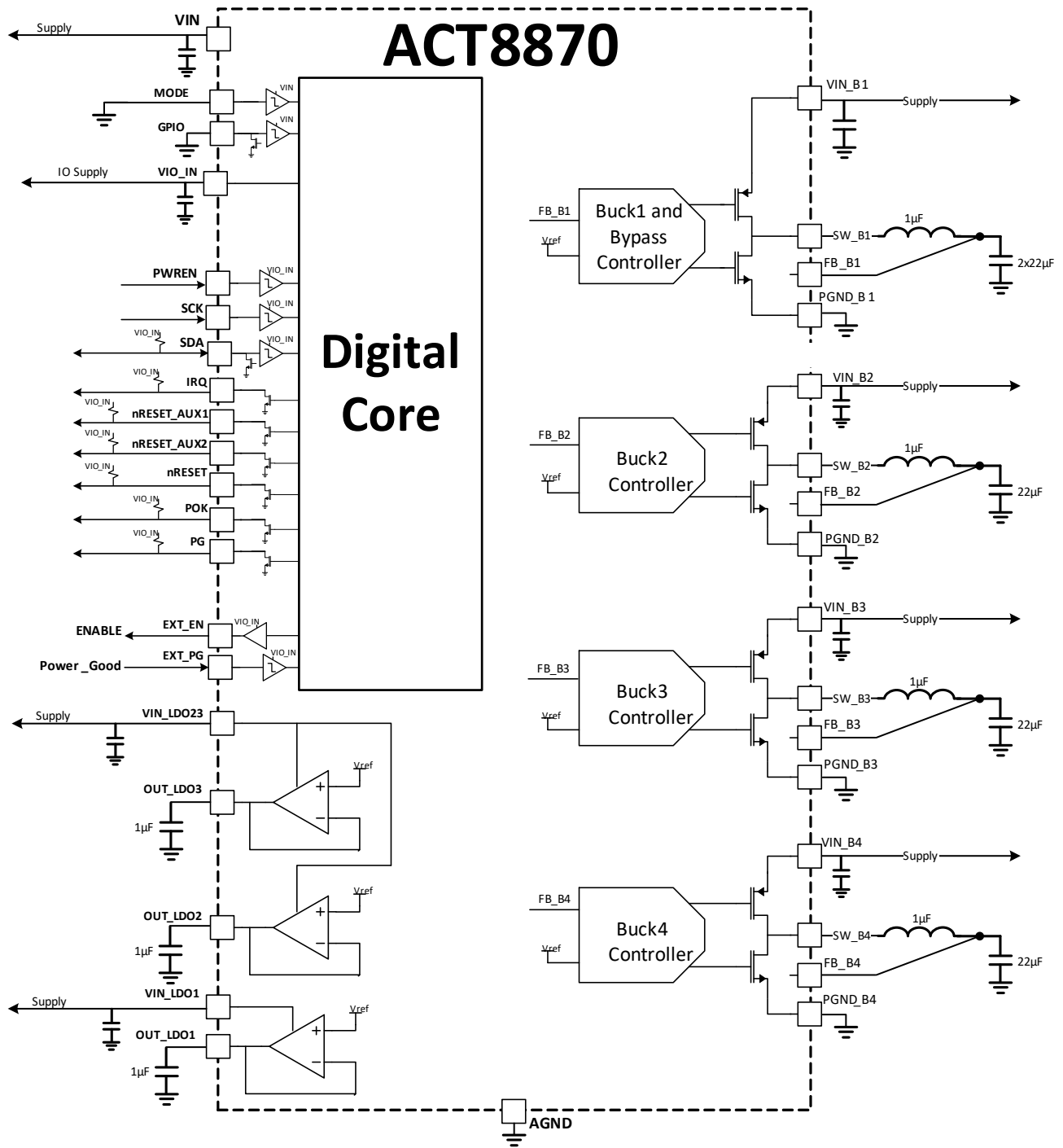
The core of the device includes four DC/DC step down converters using integrated power FETs, three low-dropout regulators (LDOs), and an optional load switch. Each DC/DC regulator switches at 2.25MHz, requiring only three small components for operation. The LDOs only require small ceramic capacitors. All are highly configurable via the I<sup>2</sup>C interface.

The ACT8870 PMIC is available in a 5 x 5 mm 40 pin QFN package or a 3.2x4.2 mm 0.5mm 48 ball wafer chip-scale package.

**Typical Application Diagram**

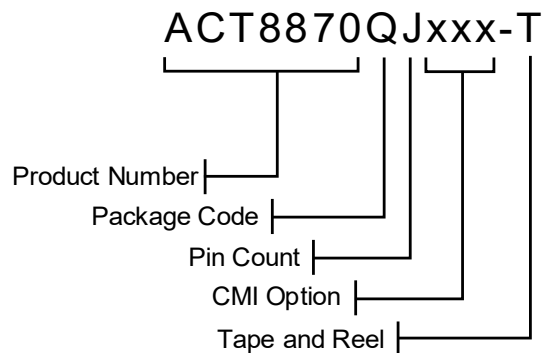


**FUNCTIONAL BLOCK DIAGRAM**



**ORDERING INFORMATION**

PART NUMBER	V <sub>OUT1</sub>	V <sub>OUT2</sub>	V <sub>OUT3</sub>	V <sub>OUT4</sub>	V <sub>LDO1</sub>	V <sub>LDO2</sub>	V <sub>LDO3</sub>	Device ID 0x7DFh	Package
ACT8870QJ101-T	Off	1.5V	1.25V	3.3V	3.3V	1.8V	2.5V	0x2Fh	5x5 40 pin
ACT8870QJ102-T	3.3V	1.5V/1.35V	1.2V/1.8V	1.15V	3.3V	1.8V	1.8V	0x0Bh	5x5 40 pin
ACT8870QJ104-T	3.3V	1.5V/1.35V	1.2V/1.8V	1.2V	3.3V	1.8V	1.8V	0x0Dh	5x5 40 pin



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

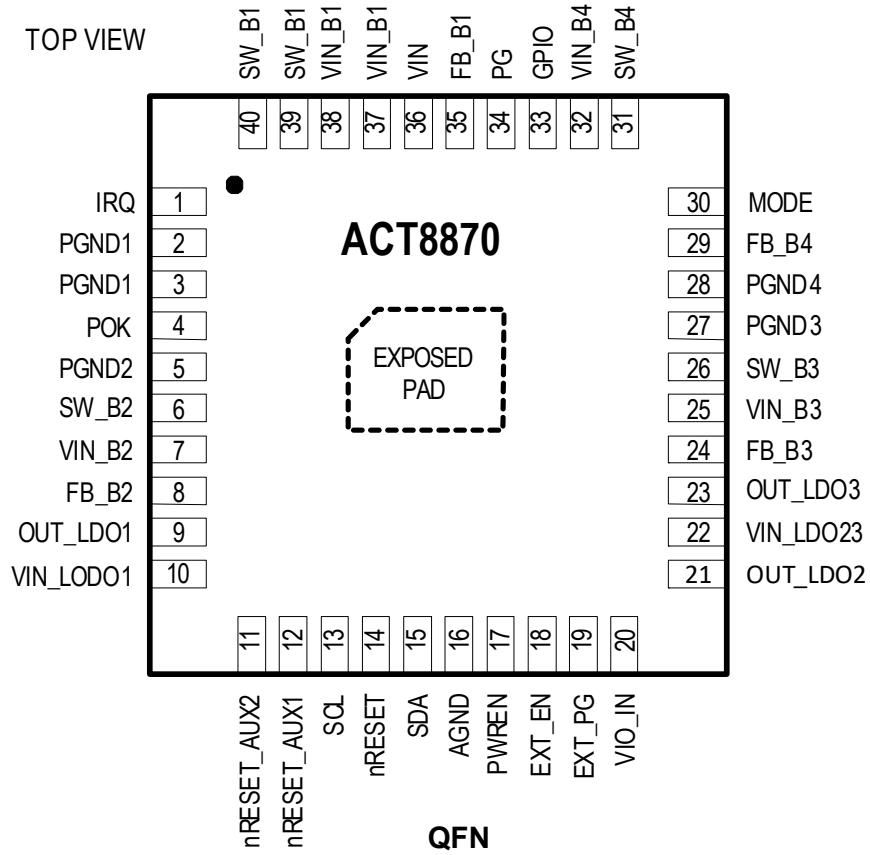
Note 2: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

Note 3: Package Code designator "Q" represents QFN

Note 4: Pin Count designator "J" represents 40 pins

Note 5: "xxx" represents the CMI (Code Matrix Index) option The CMI identifies the IC's default register settings.

**PIN CONFIGURATION - QFN**



**Figure 1: Pin Configuration – Top View – QFN55-40**

**PIN DESCRIPTIONS - QFN**

PIN	NAME	DESCRIPTION
1	IRQ	Interrupt IRQ Open Drain Output indicates a fault occurred.
2,3	PGND1	Dedicated Power Ground for BUCK1 Regulator.
4	POK	Power OK Open Drain Output, indicates Overvoltage or Undervoltage on VIN input supply.
5	PGND2	Dedicated Power Ground for Buck 2 Regulator.
6	SW_B2	Switch Pin for BUCK2 Regulator.
7	VIN_B2	Dedicated VIN power input for BUCK2 Regulator.
8	FB_B2	Feedback for BUCK2 Regulator. Connect to the BUCK2 output.
9	OUT_LDO1	Output for LDO1 Regulator (Leave unconnected if LDO1 is not used and disabled).
10	VIN_LDO1	Dedicated VIN power input for LDO1 Regulator.
11	nRESET_AUX2	Auxiliary nRESET configurable, Open Drain Output (configurable as an input).
12	nRESET_AUX1	Auxiliary nRESET configurable. Open Drain Output (configurable as an input).
13	SCL	I <sup>2</sup> C Clock Input.
14	nRESET	nRESET Open Drain Output. This pin is configurable.
15	SDA	I <sup>2</sup> C Data Input and Output.
16	AGND	Analog Ground.
17	PWREN	Power Enable Digital Input. This pin is configurable.
18	EXT_EN	External Regulator Enable Push-Pull Digital Output.
19	EXT_PG	External Power Good Digital Input. This pin is configurable.
20	VIO_IN	Digital Input Reference Voltage Input. Connect a 0.1uF ceramic capacitor between VIN_IN and AGND
21	OUT_LDO2	Output for LDO2 Regulator (Leave unconnected if LDO2 is not used and disabled).
22	VIN_LDO23	Dedicated VIN power input for LDO2 and LDO3 Regulator.
23	OUT_LDO3	Output for LDO3 Regulator (Leave unconnected if LDO3 is not used and disabled).
24	FB_B3	Feedback for BUCK3 Regulator. Connect to the BUCK3 output.
25	VIN_B3	Dedicated VIN power input for BUCK3 Regulator.
26	SW_B3	Switch Pin for BUCK3 Regulator.
27	PGND3	Dedicated Power Ground for BUCK3 Regulator.
28	PGND4	Dedicated Power Ground for BUCK4 Regulator.
29	FB_B4	Feedback for BUCK4 Regulator. Connect to the BUCK4 output.
30	MODE	Configuration input pin. This pin is read at power up to configure BUCK1.
31	SW_B4	Switch Pin for BUCK4 Regulator.
32	VIN_B4	Dedicated VIN power input for BUCK4 Regulator.
33	GPIO	Configurable General purpose input/open drain output.
34	PG	Power Good Output. This pin is configurable. Open Drain Output.
35	FB_B1	Feedback for BUCK1 Regulator. Connect to the BUCK1 output.
36	VIN	Analog Input supply monitored by POK thresholds.
37,38	VIN_B1	Dedicated VIN power input for BUCK1 Regulator.
39,40	SW_B1	Switch pin for BUCK1 Regulator.
Exposed Pad		Tie to Ground Plane for best performance

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	VALUE	UNIT
All I/O and Power pins except PGND_B1, PGND_B2, PGND_B3, PGND_B4, GND	-0.3 to 6	V
Grounds: Any PGND referenced to GND	-0.3 to +0.3	V
SW_Bx to PGNDx	-0.3 to VIN_Bx + 1	V
FB_Bx to PGNDx	-0.3 to VIN_Bx + 0.3	V
OUT_LDOx to PGNDx	-0.3 to VINx + 0.3	V
EXT_EN, nRESET_AUX1, nRESET_AUX2	-0.3 to VIO_IN + 0.3	V
Junction to Ambient Thermal Resistance, QFN (Note2)	26	°C/W
Junction to Ambient Thermal Resistance, WCSP (Note2)	31	°C/W
Operating Junction Temperature	-40 to 125	°C
Storage Temperature	-55 to 150	°C

Note1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Note2: Measured on Active-Semi Evaluation Kit

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN, VIN_B1, VIN_B2, VIN_B3, VIN_B4, VIN_LDO1, VIN_LDO23		2.8		5.5	V
VIO_IN		1.62		5.5	V
Average lifetime operating current. QFN. (Note 1)	SW_B2, SW_B3, SW_B4 SW_B1			1.6 3.2	A
Operating Junction Temperature		-40		105	°C

Note1: This temperature range is used for lifetime reliability testing.



**DIGITAL I/O ELECTRICAL CHARACTERISTICS**

 ( $V_{VIO\_IN} = 1.8V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWREN, EXT_PG Input Low	$V_{VIO\_IN} = 1.8V$			0.4	V
PWREN, EXT_PG Input High	$V_{VIO\_IN} = 1.8V$	1.25			V
PWREN, EXT_PG Input Low	$V_{VIO\_IN} = 3.3V$			1.0	V
PWREN, EXT_PG Input High	$V_{VIO\_IN} = 3.3V$	2.3			V
POK, IRQ, nRESET, nRESET_AUX1, nRESET_AUX2, GPIO, PG Leakage Current	Output = 5V			1	$\mu A$
POK, IRQ, nRESET, nRESET_AUX1, nRESET_AUX2, GPIO, PG Output Low	$I_{OL} = 5mA$			0.35	V
EXT_EN Output Low	$I_{OL} = 1mA$			0.35	V
EXT_EN Output High	$I_{OH} = 1mA$	$V_{VIO\_IN} - 0.35$			V
MODE, GPIO Input Low	$V_{AVIN} = 3.3V$			1.0	V
MODE, GPIO Input High	$V_{AVIN} = 3.3V$	2.3			V
MODE, GPIO Input Low	$V_{AVIN} = 5.0V$			1.5	V
MODE, GPIO Input High	$V_{AVIN} = 5.0V$	3.5			V
PWREN, EXT_PG, MODE Deglitch Time			10		$\mu s$
$V_{VIO\_IN}$ UVLO Threshold Falling				1.2	V

**SYSTEM CONTROL ELECTRICAL CHARACTERISTICS**

 (V<sub>VID\_IN</sub> = 1.8V, T<sub>A</sub> = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Inputs Voltage Range: VIN_B1 referenced to PGND_B1					
VIN_B2 referenced to PGND_B2		2.8		5.5	V
VIN_B3 referenced to PGND_B3					
VIN_B4 referenced to PGND_B4					
VIN_LDO1 referenced to GND		2.4		5.5	V
VIN_LDO23 referenced to GND		2.8		5.5	V
UVLO Threshold Falling (Note 1)	VIN_LVL=0	2.6	2.7	2.8	V
	VIN_LVL=1 UV_LVL=0	2.6	2.7	2.8	V
	VIN_LVL=1 UV_LVL=1	3.7	3.8	3.9	V
UVLO Hysteresis (Note 1)	VIN_LVL=0	50	100	150	mV
	VIN_LVL=1 UV_LVL=0	50	100	150	mV
	VIN_LVL=1 UV_LVL=1	200	300	400	mV
OV Threshold Rising (Note 1)	VIN_LVL = 0	3.6	3.7	3.8	V
	VIN_LVL = 1	5.55	5.75	5.95	V
OV Hysteresis (Note 1)	VIN_LVL = 0	50	100	150	mV
	VIN_LVL = 1	100	150	200	mV
Operating Supply Current	All Regulators Disabled		60		μA
	All Regulators Enabled but no load		300		μA
Thermal Shutdown Temperature TSD_SHUTDWN	Temperature rising	150	165	180	°C
Thermal Shutdown Hysteresis			20		°C
Startup Delay after initial VIN	start of first regulator output assuming start delay=100μsec minimum (Note 2)		435	485	μs
SLEEP Mode exit delay after de-asserting PWREN pin	Configuration dependent (Note 2)	30	38	50	μs
Thermal Interrupt Threshold TSD_ALERT	Temperature rising. Typically 30 degrees lower than TSD_SHUTDWN		135		°C

Thermal Interrupt Hysteresis		15	°C
POK UV Interrupt Threshold Falling (VIN_LVL=0) (Note 3) (Note 4)	POK_UV_SET=00 (88% of 3.3V) POK_UV_SET=01 (86% of 3.3V) POK_UV_SET=10 (84% of 3.3V) POK_UV_SET=11 (Disable)	2.80 2.90 3.00 2.74 2.84 2.94 2.67 2.77 2.87 N/A N/A N/A	V
POK UV Interrupt Threshold Falling (VIN_LVL=1) (Note 3) (Note 4)	POK_UV_SET=00 (88% of 3.3V) POK_UV_SET=01 (85% of 3.3V) POK_UV_SET=10 (85% of 5.0V) POK_UV_SET=11 (Disable)	2.80 2.90 3.00 2.70 2.80 2.90 4.08 4.25 4.42 N/A N/A N/A	V
POK OV Interrupt Threshold Rising (VIN_LVL=0) (Note 3) (Note 4)	POK_OV_SET=00 (107% of 3.3V) POK_OV_SET=01 (109% of 3.3V) POK_OV_SET=10 (110% of 3.3V) POK_OV_SET=11 (Disable)	3.43 3.53 3.63 3.50 3.60 3.70 3.53 3.63 3.73 N/A N/A N/A	V
POK OV Interrupt Threshold Rising (VIN_LVL=1, POK_LVL = 0) (Note 3) (Note 4)	POK_OV_SET=00 (133% of 3.3V) POK_OV_SET=01 (136% of 3.3V) POK_OV_SET=10 (136% of 3.3V) POK_OV_SET=11 (Disable)	4.23 4.40 4.57 4.33 4.50 4.67 4.33 4.50 4.67 N/A N/A N/A	V
POK OV Interrupt Threshold Rising (VIN_LVL=1, POK_LVL = 1) (Note 3) (Note 4)	POK_OV_SET=00 (110% of 5.0V) POK_OV_SET=01 (112% of 5.0V) POK_OV_SET=10 (114% of 5.0V) POK_OV_SET=11 (Disable)	5.33 5.50 5.67 5.43 5.60 5.77 5.53 5.70 5.87 N/A N/A N/A	V
POK Deglitch Time OV or UV		5	µs

Note 1: All Under-voltage Lockout, Overvoltage measurements are referenced to the AVIN Input and GND Pins.

Note 2: This delay can be affected by programming sequence and startup delays.

Note 3: All POK Under-voltage and Overvoltage measurements are referenced to the VIN Input and GND Pins.

Note 4: There is no hysteresis on OV and UV threshold for the POK interrupt.

**INTERNAL STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS REGULATOR: (BUCK1)**

(VIN\_B1 = 5V, TA = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Operating Voltage Range		2.8		5.5	V
Output Voltage Range	Configurable in 12.5mV steps	0.8		4.0	V
Standby Supply Current, Low Power Mode Enabled	V <sub>OUT_B1</sub> = 103%, Regulator Enabled, No Load		45		μA
Shutdown Current	Regulator Disabled			1	μA
Output Voltage Accuracy – Default Voltage - PWM Mode	V <sub>OUT_B1</sub> = 3.3V, I <sub>OUT</sub> = 2A	-1%	V <sub>NOM</sub>	1%	V
Output Voltage Accuracy – Default Voltage - PFM Mode	V <sub>OUT_B1</sub> = 3.3V, I <sub>OUT</sub> = 1mA	-1%	V <sub>NOM</sub>	1%	V
Line Regulation	V <sub>OUT_B1</sub> = 2.8V V <sub>IN_B1</sub> = 3.3V to 5.5V, PWM Regulation		0.02		%/V
Load Regulation	V <sub>OUT_B1</sub> = 3.3V PWM Regulation		0.04		%/A
Power Good Threshold	V <sub>OUT_B1</sub> Rising	92	93	94	%V <sub>NOM</sub>
Power Good Hysteresis	V <sub>OUT_B1</sub> Falling		3		%V <sub>NOM</sub>
Overvoltage Fault Threshold	V <sub>OUT_B1</sub> Rising	107.5	110	112.5	%V <sub>NOM</sub>
Overvoltage Fault Hysteresis	V <sub>OUT_B1</sub> Falling		3		%V <sub>NOM</sub>
Switching Frequency	V <sub>OUT_B1</sub> ≥ 20% of V <sub>NOM</sub>	1.075	1.125	1.180	MHz
Programmable Soft-Start Time, T <sub>SET</sub>	Configurable 10% to 90% V <sub>NOM</sub>	300		1000	μs
Soft-Start Time Tolerance	Tolerance from T <sub>SET</sub>	-25		+25	%
High Side FET Peak Current Limit (Cycle-by-Cycle) ILIMSET	B1_ILIMSET=11 B1_ILIMSET=10 B1_ILIMSET=01 B1_ILIMSET=00		3.0 3.8 4.6 5.3		A
High Side FET Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIMSET	-10	ILIMSET	+10	%
	At other set points	-15	ILIMSET	+15	%
High Side FET Peak Current Limit, IRQ Trigger Level	Below ILIMSET = 00, 01, 10	-30.0	-22.5	-15.0	%
	Below ILIMSET = 11	-32.5	-22.5	-12.5	%
High Side FET Peak Current Limit, Shutdown Level	Above ILIMSET = 00, 01, 10	+15.0	+22.5	+30	%
	Above ILIMSET = 11	+12.5	+22.5	+32.5	%
PMOS On-Resistance	I <sub>SW</sub> = -1A, VIN = 5.0V		0.025	0.04	Ω
NMOS On-Resistance	I <sub>SW</sub> = 1A, VIN = 5.0V		0.025		Ω
SW Leakage Current	V <sub>IN_B1</sub> = 5.5V, V <sub>SW</sub> = 0 or 5.5V			1	μA

Dynamic Voltage Scaling Rate	B1_SLEW=00 (not allowed) B1_SLEW=01 B1_SLEW=10 B1_SLEW=11	N/A 14.0 3.50 0.88	mV/us
Switching Rise / Fall Times	B1_DRVADJ=00 $V_{IN\_B1} = 5V$ B1_DRVADJ=01 B1_DRVADJ=10 B1_DRVADJ=11	6.3/9.0 4.5/7.4 3.1/5.9 3.0/5.0	ns
Discharge Resistance	Enabled when regulator disabled	2.75      4.4      8.75	$\Omega$

**INTERNAL STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS REGULATOR: (BUCK1) – BYPASS MODE**

(VIN\_B1 = 3.3V, TA = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Bypass Mode</b>					
Input Voltage for By-Pass Mode		2.7	3.3	3.7	V
PMOS On-Resistance	ISW = -1A, VIN = 3.3V Max=125°C at TJunction		0.025	0.04	Ω
Internal PMOS Current Detection	Triggers Interrupt on IRQ Pin	1.4	3	4.6	A
Internal PMOS Current Detection Deglitch Time			10		μs
Internal PMOS Current Shutdown	Shuts down after deglitch time and stays off for Off Time	5.4	6.0	6.6	A
Internal PMOS Current Shutdown Deglitch Time			10		μs
Internal PMOS Current Shutdown Off time			100		ms
Internal PMOS Softstart	Only used with 3.3V Input	5.94	6.6	7.26	mV/us

**INTERNAL STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS REGULATOR: (BUCK2-4)**

(VIN\_Bx = 5V, TA = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Operating Voltage Range		2.8		5.5	V
Output Voltage Range	Configurable in 12.5mV steps	0.8		4	V
Maximum Output Current		2			A
Standby Supply Current, Low Power Mode Enabled	V <sub>OUT_Bx</sub> = 103%, Regulator Enabled, No load		35		μA
Shutdown Current	V <sub>IN_Bx</sub> = 5.5V, Regulator Disabled		0.1	1	μA
B2 Voltage Accuracy – Default Voltage – PWM Mode	CMI101 V <sub>OUT_B2</sub> = 1.5V, I <sub>OUT</sub> = 1A	-1%	V <sub>NOM</sub>	1%	V
B3 Voltage Accuracy – Default Voltage – PWM Mode	CMI101 V <sub>OUT_B3</sub> = 1.25V, I <sub>OUT</sub> = 1A	-1%	V <sub>NOM</sub>	1%	V
B4 Voltage Accuracy – Default Voltage – PWM Mode	CMI101 V <sub>OUT_B4</sub> = 3.3V, I <sub>OUT</sub> = 1A	-1%	V <sub>NOM</sub>	1%	V
B2 Voltage Accuracy – Default Voltage – PFM Mode	CMI101 V <sub>OUT_B2</sub> = 1.5V, I <sub>OUT</sub> = 1A	-1%	V <sub>NOM</sub>	1%	V
B3 Voltage Accuracy – Default Voltage – PFM Mode	CMI101 V <sub>OUT_B3</sub> = 1.25V, I <sub>OUT</sub> = 1A	-1%	V <sub>NOM</sub>	1%	V
B4 Voltage Accuracy – Default Voltage – PFM Mode	CMI101 V <sub>OUT_B4</sub> = 3.3V, I <sub>OUT</sub> = 1A	-1%	V <sub>NOM</sub>	1%	V
Line Regulation	V <sub>OUT_Bx</sub> = 1.8V V <sub>IN_Bx</sub> = 2.8V to 5.5V PWM Regulation		0.02		%/V
Load Regulation	V <sub>OUT_Bx</sub> = 1.8V PWM Regulation		0.04		%/A
Power Good Threshold	V <sub>OUT_B2</sub> Rising	92	93	94	%V <sub>NOM</sub>
	V <sub>OUT_B3</sub> Rising	94	95	96	
	V <sub>OUT_B4</sub> Rising	94	95	96	
Power Good Hysteresis	V <sub>OUT_Bx</sub> Falling		3		%V <sub>NOM</sub>
Overvoltage Fault Threshold	V <sub>OUT_Bx</sub> Rising	107.5	110	112.5	%V <sub>NOM</sub>
Overvoltage Fault Hysteresis	V <sub>OUT_Bx</sub> Falling		3		%V <sub>NOM</sub>
Switching Frequency	V <sub>OUT_Bx</sub> ≥ 20% of V <sub>NOM</sub>	2.15	2.25	2.36	MHz
Programmable Soft-Start Time, T <sub>SET</sub>	Configurable 10% to 90% V <sub>NOM</sub>	300		1000	μs
Soft-Start Time Tolerance	Tolerance from T <sub>SET</sub>	-25		+25	%
High Side FET Current Limit (Cycle-by-Cycle) ILIMSET	Bx_ILIMSET=11 Bx_ILIMSET=10 Bx_ILIMSET=01 Bx_ILIMSET=00		2.0 2.5 3.0 3.5		A
High Side FET Current Limit (Cycle-by-Cycle) Tolerance	At default ILIMSET	-10	ILIMSET	+10	%
	At other setpoints	-15	ILIMSET	+15	%
High Side FET Peak Current Limit, IRQ	Below ILIMSET = 00, 01, 10	-27.5	-22.5	-17.5	%

Trigger Level	Below ILIMSET = 11	-30.0	-22.5	-15.0	%
High Side FET Peak Current Limit, Shutdown Level	Above ILIMSET = 00, 01, 10	+15.0	+22.5	+30	%
	Above ILIMSET = 11	+12.5	+22.5	+32.5	%
PMOS On-Resistance	I <sub>SW</sub> = -500mA		0.08		Ω
NMOS On-Resistance	I <sub>SW</sub> = 500mA		0.05		Ω
SW Leakage Current	V <sub>VIN_BX</sub> = 5.5V, V <sub>SW</sub> = 0 or 5.5V			1	μA
Dynamic Voltage Scaling Rate	BX_SLEW=00 BX_SLEW=01 BX_SLEW=10 BX_SLEW=11		Not Allowed 14.0 3.50 0.88		mV/us
Switching Rise / Fall Times	BX_DRVADJ=00 V <sub>IN_BX</sub> = 5V BX_DRVADJ=01 BX_DRVADJ=10 BX_DRVADJ=11		6.3/9.0 4.5/7.4 3.1/5.9 3.0/5.0		ns
Discharge Resistance	Enabled when regulator disabled	6.25	9.40	20	Ω



**LDO1 ELECTRICAL CHARACTERISTICS**

(VIN\_LDO1 = 5V, TA = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.4		5.5	V
Output Voltage Range–VSET	Configurable in 25mV steps	0.8		4.0	V
Output Current	VIN_LDO1 = 2.8V to 5.5V, LDO1_ILIM=11	0.75			A
Output Current	VIN_LDO1 = 2.4V to 2.8V, LDO1_ILIM=1x	0.4			A
Output Voltage Accuracy	VIN_LDO1 - VLDO1_OUT > 0.4V	-1	VSET	1	%
Line Regulation	VIN_LDO1 - VLDO1_OUT > 0.4V VIN_LDO1 = 2.8V to 5.5V ILDO1_OUT = 1mA		0.005		% / V
Load Regulation	ILDO1_OUT = 1mA to 750mA, LDO1_ILIM=11		0.15		% / A
Power Supply Rejection Ratio	f = 1kHz, ILDO1_OUT = 20mA, VLDO1_OUT = 2.5V		54		dB
	f = 10kHz, ILDO1_OUT = 20mA, VLDO1_OUT = 2.5V		53		
	f = 2.25MHz, ILDO1_OUT = 20mA, VLDO1_OUT = 2.5V		44		
Supply Current per Output	Regulator Enabled No Load		25	42	µA
	Regulator Disabled		0	1	
Soft-Start Period	VLDO1_OUT = 1.8V Setting (10% to 90%) LDO1_SS_RAMP=00 LDO1_SS_RAMP=01 LDO1_SS_RAMP=10 LDO1_SS_RAMP=11		240 330 450 575		µs
	VLDO1_OUT = 2.5V Setting (10% to 90%) LDO1_SS_RAMP=00 LDO1_SS_RAMP=01 LDO1_SS_RAMP=10 LDO1_SS_RAMP=11		Not allowed 385 465 600		
	VLDO1_OUT = 3.3V Setting (10% to 90%) LDO1_SS_RAMP=00 LDO1_SS_RAMP=01 LDO1_SS_RAMP=10 LDO1_SS_RAMP=11		Not allowed 450 525 660		
Power Good Threshold	VLDO1_OUT Rising	92	93	94	%VNOM
Power Good Hysteresis	VLDO1_OUT Falling		3		%VNOM
Overvoltage Fault Threshold	VLDO1_OUT Rising	105	110	114	%VNOM
Overvoltage Fault Hysteresis	VLDO1_OUT Falling		3		%VNOM
Discharge Resistance		10	25	75	Ω
Dropout Voltage	ILDO1_OUT = 200mA			200	mV
Dropout Voltage	ILDO1_OUT = 400mA, LDO1_ILIM=1x			300	mV
Dropout Voltage	ILDO1_OUT = 750mA VIN_LDO1 > 2.8 LDO_ILIM=11			400	mV
Output Current Limit	LDO1_ILIM=00 LDO1_ILIM=01 LDO1_ILIM=10 LDO1_ILIM=11 (800mA min)	-15%	350 500 630 1000	+15%	mA
Startup Delay	Additional startup delay required before soft start ramp LDO1_SS_RAMP=00	31	44	65	µs

**LDO2 AND LDO3 ELECTRICAL CHARACTERISTICS**

 (VIN\_LDO23 = 5V, T<sub>A</sub> = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.4		5.5	V
Output Voltage Range – VSET	Configurable in 25mV steps	0.8		4.0	V
Output Voltage Accuracy	V <sub>IN_LDO23</sub> - V <sub>LDOX_OUT</sub> > 0.4V	-1	V <sub>SET</sub>	1	%
Line Regulation	V <sub>IN_LDO23</sub> - V <sub>LDOX_OUT</sub> > 0.4V V <sub>IN_LDO23</sub> = 2.8V to 5.5V I <sub>LDOX_OUT</sub> = 1mA		0.007		% / V
Load Regulation	I <sub>LDOX_OUT</sub> = 1mA to 100mA, LDOX_ILIM=1X		-1		% / A
Power Supply Rejection Ratio	f = 1kHz, I <sub>LDOX_OUT</sub> = 20mA, V <sub>LDOX_OUT</sub> = 1.8V		56		dB
	f = 10kHz, I <sub>LDOX_OUT</sub> = 20mA, V <sub>LDOX_OUT</sub> = 1.8V		45		
	f = 2.25MHz, I <sub>LDOX_OUT</sub> = 20mA, V <sub>LDOX_OUT</sub> = 1.8V		55		
Supply Current per Output	Regulator Disabled		0.02	1	μA
Supply Current per Output	Regulator Enabled, No load		15		μA
Soft-Start Period	V <sub>LDOX_OUT</sub> = 1.8V Setting (10% to 90%) LDO23 SS_RAMP=00 LDO23 SS_RAMP=01 LDO23 SS_RAMP=10 LDO23 SS_RAMP=11		110 110 165 215		μs
	V <sub>LDOX_OUT</sub> = 2.5V Setting (10% to 90%) LDO23 SS_RAMP=00 LDO23 SS_RAMP=01 LDO23 SS_RAMP=10 LDO23 SS_RAMP=11		145 145 175 215		
	V <sub>LDOX_OUT</sub> = 3.3V Setting (10% to 90%) LDO23 SS_RAMP=00 LDO23 SS_RAMP=01 LDO23 SS_RAMP=10 LDO23 SS_RAMP=11		200 200 210 235		
Power Good Threshold	V <sub>LDOX_OUT</sub> Rising	91	93	95	%V <sub>NOM</sub>
Power Good Hysteresis	V <sub>LDOX_OUT</sub> Falling		3		%V <sub>NOM</sub>
Overvoltage Fault Threshold	V <sub>LDOX_OUT</sub> Rising	105	110	114	%V <sub>NOM</sub>
Overvoltage Fault Hysteresis	V <sub>LDOX_OUT</sub> Falling		3		%V <sub>NOM</sub>
Discharge Resistance		20	50	125	Ω
Dropout Voltage	I <sub>LDOX_OUT</sub> = 30mA		50	90	mV
Dropout Voltage	I <sub>LDOX_OUT</sub> = 50mA, LDOX_ILIM=01		90	150	mV
Dropout Voltage	I <sub>LDOX_OUT</sub> = 100mA, LDOX_ILIM=1X		180	310	mV
Dropout Voltage	I <sub>LDOX_OUT</sub> = 150mA V <sub>IN_LDO23</sub> > 2.8 LDOX_ILIM=11		285	500	mV

Output Current Limit	LDOx_ILIM=00 LDOx_ILIM=01 LDOx_ILIM=10 LDOx_ILIM=11	60 100 150 200	80 145 225 290	mA
Startup Delay	Additional startup delay required before soft start ramp LDOx_SS_RAMP=01	20	36    55	μs

**OVERALL SYSTEM TIMING REQUIREMENTS**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Regulator Programmable Startup Delay Timings between turn on events	ONDLY=000	32.6	34.5	51.5	μs
	ONDLY=001	101	106.5	127.5	
	ONDLY=010	196	206.5	132.5	
	ONDLY=011	291	306.5	337.5	
	ONDLY=100	386	406.5	442.5	
	ONDLY=101	481	506.5	547.5	
	ONDLY=110	576	606.5	652.5	
	ONDLY=111	671	706.5	757.5	
nRESET, nRESET_AUX2 Programmable Delay Range	Step Size = 114μs	199		996	μs
nRESET, nRESET_AUX2 Min Delay Timing	Setting nRST_DLY=000	160	199	240	μs
nRESET, nRESET_AUX2 Max Delay Timing	Setting nRST_DLY=111	920	996	1080	μs
nRESET_AUX1 Delay Timings Programmable Delay Range	Step Size = 228μs	398		1991	μs
nRESET_AUX1 Min Delay Timing	Setting nRST_AUX1_DLY=000	360	398	435	μs
nRESET_AUX1 Max Delay Timing	Setting nRST_AUX1_DLY=111	1876	1991	2114	μs
AUX TIMER Delay Timing	Setting AUX_DLY=00	3.7	4	4.3	ms
	Setting AUX_DLY=01	7.7	8	8.3	
	Setting AUX_DLY=10	15.7	16	16.3	
	Setting AUX_DLY=11	31.7	32	32.3	

## I<sup>2</sup>C INTERFACE ELECTRICAL CHARACTERISTICS

(V<sub>IO\_IN</sub> = 1.8V, T<sub>A</sub> = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V <sub>IO_IN</sub> = 1.8V			0.4	V
SCL, SDA Input High	V <sub>IO_IN</sub> = 1.8V	1.25			V
SCL, SDA Input Low	V <sub>IO_IN</sub> = 3.3V			1.0	V
SCL, SDA Input High	V <sub>IO_IN</sub> = 3.3V	2.3			V
SDA Leakage Current	SDA=5V			1	μA
SDA Output Low	I <sub>OL</sub> = 5mA			0.35	V
SCL Clock Frequency, f <sub>SCL</sub>		0		1000	kHz
SCL Low Period, t <sub>LOW</sub>		0.5			μs
SCL High Period, t <sub>HIGH</sub>		0.26			μs
SDA Data Setup Time, t <sub>SU</sub>		50			ns
SDA Data Hold Time, t <sub>HD</sub>	(Note1)	0			ns
Start Setup Time, t <sub>ST</sub>	For Start Condition	260			ns
Stop Setup Time, t <sub>SP</sub>	For Stop Condition	260			ns
Capacitance on SCL or SDA Pin				10	pF
SDA Fall Time SDA, T <sub>of</sub>	Device requirement			120	ns
Pulse Width of spikes must be suppressed on SCL and SDA		0		50	ns

Note1: Comply to I<sup>2</sup>C timings for 1MHz operation - "Fast Mode Plus".

Note2: No internal timeout for I<sup>2</sup>C operations, however, I<sup>2</sup>C communication state machine will be reset when entering RESET, IDLE, OVUVFLT, and THERMAL states to clear any transactions that may have been occurring when entering the above states.

Note3: This is an I<sup>2</sup>C system specification only. Rise and fall time of SCL & SDA not controlled by the device.

Note4: Device Address is 7'h5A

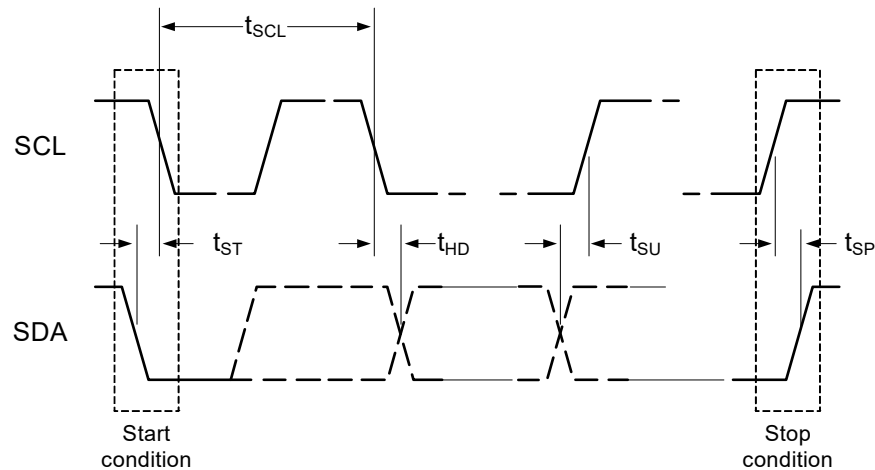


Figure 2: I<sup>2</sup>C Data Transfer

## SYSTEM CONTROL INFORMATION

### General

The ACT8870 is a single-chip integrated power management solution designed to power many processors such as the Atmel SAMA5D3. It integrates four highly efficient buck regulators, three LDOs, and an integrated load bypass switch. Its high integration and high switching frequency result in an extremely small footprint and lost power solution. It contains a master controller that manages startup sequencing, timing, voltages, slew rates, sleep states, and fault conditions. I<sup>2</sup>C configurability allows system level changes without the need for costly PCB changes. The built-in load bypass switch enables full sequencing configurability in 3.3V systems.

The ACT8870 master controller monitors all outputs and reports faults via I<sup>2</sup>C and hardwired status signals. Faults can be masked and fault levels and responses are configurable via I<sup>2</sup>C.

Many of the ACT8870 pins and functions are configurable. The IC's default functionality is defined by the default CMI (Code Matrix Index), but much of this functionality can be changed via I<sup>2</sup>C. The first part of the datasheet describes basic IC functionality and default pin functions. The end of the datasheet provides the configuration and functionality specific to each CMI version. Contact [sales@active-semi.com](mailto:sales@active-semi.com) for additional information about other configurations.

### I<sup>2</sup>C Serial Interface

To ensure compatibility with a wide range of systems, the ACT8870 uses standard I<sup>2</sup>C commands. The ACT8870 operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. As an example, the 7-bit slave address 0x5Ah follows the format 1011010x where "x" is a 0 for write operation and 1 for a read operation. This results in 0xB4h for write operations and 0xB5h for read operations.

There is no timeout function in the I<sup>2</sup>C packet processing state machine, however, any time the I<sup>2</sup>C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet.

The ACT8870 holds the I<sup>2</sup>C state machine in reset during the RESET, Idle, OVUVFLT, and THERMAL states to avoid a corruption of registers when the voltage regulators are out of spec.

I<sup>2</sup>C commands are communicated using the SCL and SDA pins. SCL is the I<sup>2</sup>C serial clock input. SDA is the data input and output. SDA is open drain and must have a pullup resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics Table.

### I<sup>2</sup>C Registers

The ACT8870 contains an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, sequencing, fault thresholds, fault masks, etc. These registers are what give the IC its operating flexibility. The two types of registers are described below.

**Basic Volatile** – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

**Basic Non-Volatile** – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult [sales@active-semi.com](mailto:sales@active-semi.com) for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected device behavior.

### State Machine

The ACT8870 contains an internal state machine with five internal states.

#### RESET State

In the RESET, or "cold" state, the ACT8870 is waiting for the input voltage on VIN to be within a valid range defined by I<sup>2</sup>C bits POK\_OV\_SET and POK\_UV\_SET. All regulators are off in RESET. nRESET, nRESET\_AUX1, and nRESET\_AUX2 are asserted low. All volatile registers are reset to defaults and Non-Volatile registers are reset to programmed defaults. The IC transitions from RESET to ACTIVE when the input voltage enters the valid range. The IC transitions from any other state to RESET if the input voltage drops below the UVLO threshold voltage.

#### ACTIVE State

The ACTIVE state is the normal operating state when the input voltage is within the allowable range, all outputs are turned on, and no faults are present. When en-

tering the ACTIVE state from the RESET state, all regulators are powered on following their programmed power up sequence. The regulators are not sequenced when entering ACTIVE from SLEEP.

### SLEEP State

The SLEEP state is a low power mode for the operating system. Each output can be programmed to be on or off in the SLEEP state. The outputs do not follow any sequencing when turning on or off as they enter or exit the SLEEP state. They do turn on with their programmed softstart time. Buck1/2/3/4 can be programmed to regulate to their VSET0 voltage, VSET1 voltage, or be turned off in the SLEEP state. LDO1/2/3 can be programmed to regulate to their VSET0 voltage or can be programmed to be turned off. Note that LDO1/2/3 do not have a VSET1 voltage.

The IC can enter SLEEP via a hardware input pin or an I<sup>2</sup>C command. The hardware input is typically the PWREN pin, but this can be reconfigured to other pins. To enable SLEEP via I<sup>2</sup>C, program the following:

Set register 0x08h bit1 (PWR\_DN\_MODE) = 1

Set register 0x00h bit0 (PWRDN\_EN) = 1

To enter SLEEP, program register 0x01h bit1 (SLP\_ENTR) = 1.

I<sup>2</sup>C is disabled in SLEEP mode, to the only way to exit SLEEP mode is to toggle the PWREN pin.

### THERMAL State

In the THERMAL state the chip has exceeded the thermal shutdown temperature. To protect the device, all the regulators are shut down and all three nRESETx pins are asserted low. This state can be disabled by setting register 0x0Ah bit4 (TSD\_nMASK) = 0. Note that thermal shutdown fault flag, TSD\_SHUTDOWN, still provides the thermal status even TSD\_nMASK = 0.

### OVUVFLT State

In the OVUVFLT state one of the regulators has exceeded an OV level at any time or UV level after the soft start ramp has completed. All regulators shutdown and all three nRESETx outputs are asserted low when the IC enters OVUVFLT state. The OVUVFLT state is timed to retry after 100ms and enter the ACTIVE state. If the OV or UV condition still exists in the ACTIVE state the IC returns back to the OVUVFLT state. The cycle continues until the OV or UV fault is removed or the input power is removed. This state can be disabled by setting the OV\_nMASK or UV\_nMASK non-volatile bits low. The IC does not directly enter OVUVFLT in an overcurrent condition, but does enter this state due to the resulting UV condition.

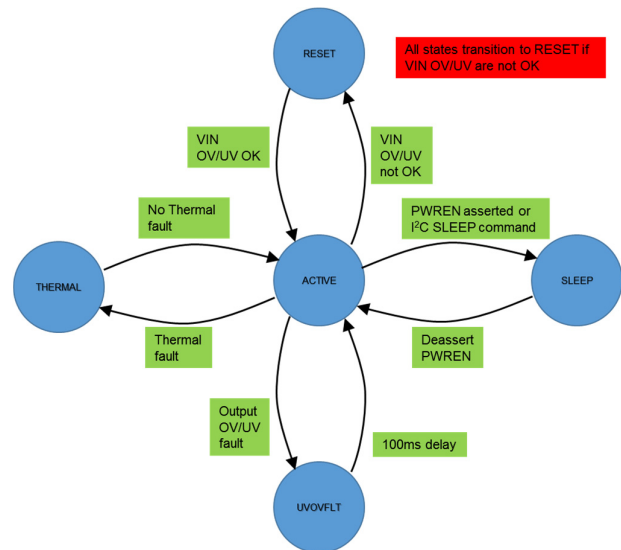


Figure 3. State Machine

### Sequencing

The ACT8870 provides the end user with extremely versatile sequencing capability that can be optimized for many different applications. Each of the seven outputs has four basic sequencing parameters: input trigger, turn-on delay, softstart time, and output voltage. Each of these parameters is controlled via the ICs internal registers. As an example, the ACT8870QJ101-T sequencing and output voltages are optimized for the Atmel SAMA5D3D3 processor. The specifics for this IC as well as others are detailed at the end of the datasheet. Contact [sales@active-semi.com](mailto:sales@active-semi.com) for custom sequencing configurations. Refer to the Active-Semi Application Note describing the Register Map for full details on I<sup>2</sup>C functionality and programming ranges.

**Input trigger.** The input trigger for a regulator is the event that turns that regulator on. Each output can have a separate input trigger. The input trigger can be the internal power ok (POK) signal from one of the other regulators, the internal VIN POK signal, or an external signal applied to an input pin such as EXT\_PG or GPIO. This flexibility allows a wide range of sequencing possibilities, including have some of the outputs be sequenced with another external power supply or a control signal from the host. As an example, if the LDO1 input trigger is Buck1, LDO1 will not turn on until Buck1 is in regulation. Input triggers are defined at the factory and can only be changed with a custom CMI configuration. The nRESETx, POK, PG, and EXT\_EN outputs can be connected to a power supply's internal POK signal and used to trigger external supplies in the overall sequencing scheme.

**Turn-on Delay.** The turn-on delay is the time between an input trigger going active and the output starting to turn on. Each output's turn-on delay is configured via its I<sup>2</sup>C bit ONDLY. Turn-on delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

**Softstart Time.** The softstart time is the time it takes an output to ramp from 0V to its programmed voltage. Each output's softstart time is configured via its I<sup>2</sup>C bit SS\_RAMP. Softstart times can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

**Output Voltage.** The output voltage is each regulator's desired voltage. Each buck's output voltage is programmed via its I<sup>2</sup>C bits Bx\_VSET0 and Bx\_VSET1. The output regulates to Bx\_VSET0 in ACTIVE mode. They can be programmed to regulate to Bx\_VSET1 in DVS mode or SLEEP mode. Each output's voltage can be changed after the IC is powered on, but the new setting is volatile and is reset to the factory defaults when power is recycled. Output voltages can be changed on the fly. If a large output voltage change is required, it is best to make multiple smaller changes. This prevents the IC from detecting an instantaneous over or under voltage condition because the fault threshold are immediately changed, but the output takes time to respond.

### Dynamic Voltage Scaling

On-the-fly dynamic voltage scaling (DVS) for the four buck converters is available via the I<sup>2</sup>C interface. This allows systems to save power by quickly adjusting the microprocessor performance level when the workload changes. Note that DVS is not a different operating state. The IC operates in the ACTIVE state, but just regulates the outputs to a different voltage. For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

Enter DVS by programming register 0x00h bit1 (DVS\_EN) = 1 and then pulling the EXT\_EN pin high. Note that some CMI configurations may not require DVS\_EN = 1 and may use different input pins.

### Fault Protection

The ACT8870 contains several levels of fault protection, including the following:

Output Overvoltage

Output Undervoltage

Output Current Limit

Thermal Warning

Thermal Shutdown

There are three types of I<sup>2</sup>C register bits associated with each fault condition: fault flag bits, fault bits, and mask bits. The fault flag bits display the real-time fault status. Their status is valid regardless of whether or not that fault is masked. The mask bits either block or allow the fault to affect the fault bit. Each potential fault condition can be masked via I<sup>2</sup>C if desired. Any unmasked fault condition results in the fault bit going high, which asserts the IRQ pin. IRQ is typically active low. The IRQ pin only de-asserts after the fault condition is no longer present and the corresponding fault bit is read via I<sup>2</sup>C. Note that masked faults can still be read in the fault flag bit. Refer to Active-Semi Application Note describing the Register Map for full details on I<sup>2</sup>C functionality and programming ranges.

### Output Under/Over Voltage

The ACT8870 monitors the output voltages for under voltage and over voltage conditions. If one output enters an UV/OV fault condition, the IC shuts down all outputs for 100ms and restarts with the programmed power up sequence. If an output is in current limit, it is possible that its voltage can drop below the UV threshold which also shuts down all outputs. If that behavior is not desired, mask the appropriate fault bit. Each output still provides its real-time UV/OV fault status via its fault flag, even if the fault is masked. Masking an OV/UV fault just prevents the fault from being reported via the IRQ pin. A UV/OV fault condition pulls the nRESETx pins low. Note that nRESETx pins are configurable via CMI settings.

### Output Current Limit

The ACT8870 incorporates a three level overcurrent protection scheme for the buck converters and a single level scheme for the LDOs. For the buck converters, the overcurrent current threshold refers to the peak switch current. The first protection level is when a buck converter's peak switch current reaches 80% of the Cycle-by-Cycle current limit threshold for greater than 16 switching cycles. Under this condition, the IC reports the fault via the appropriate fault flag bit. If the fault is unmasked, it asserts the IRQ pin. This may or may not turn off that output or other outputs depending on the specific CMI. The next level is when the current increases to the Cycle-by-Cycle threshold. The buck converter limits the peak switch current in each switching cycle. This reduces the effective duty cycle



and causes the output voltage to drop, potentially creating an undervoltage condition. When the overcurrent condition results in an UV condition, and UV is not masked, the IC turns off all supplies off for 100ms and restarts. The third level is when the peak switch current reaches 120% of the Cycle-by-Cycle current limit threshold. This immediately shuts down the regulator and waits 14ms before restarting.

For LDOs, the overcurrent thresholds are set by each LDO's Output Current Limit setting. When the output current reaches the Current Limit threshold, the LDO limits the output current. This reduces the output voltage, creating an undervoltage condition, causing all supplies to turn off for 100ms before restarting.

The overcurrent fault limits for each output are adjustable via I<sup>2</sup>C. Overcurrent fault reporting can be masked via I<sup>2</sup>C, but the overcurrent limits are always active and will shut down the IC when exceeded.

### Thermal Warning and Thermal Shutdown

The ACT8870 monitors its internal die temperature and reports a warning via IRQ when the temperature rises above the Thermal Interrupt Threshold of typically 135 deg C. It reports a fault when the temperature rises above the Thermal Shutdown Temperature of typically 165 deg C. A temperature fault shuts down all outputs unless the fault is masked. Both the fault and the warning can be masked via I<sup>2</sup>C. The temperature warning and fault flags still provide real-time status even if the faults are masked. Masking just prevents the faults from being reported via the IRQ pin.

### Pin Descriptions

The ACT8870 input and output pins are configurable via CMI configurations. The following descriptions refer to the most common pin functions. Refer to the CMI Options section in the back of the datasheet for specific pin functionality for each CMI.

#### PWREN

The PWREN pin controls the IC's SLEEP state. When I<sup>2</sup>C bit PWREN\_MODE = 0, the PWREN pin moves the IC between the SLEEP and ACTIVE states.

PWREN must be enabled via the PWRDN\_EN I<sup>2</sup>C bit after power up. PWREN is ignored if the PWRDN\_EN bit is low. The PWREN polarity is controlled by the PWREN\_POL I<sup>2</sup>C bit. PWREN is active low when PWREN\_POL is high, and active high when PWREN\_POL is low. The host processor can read the PWREN status via I<sup>2</sup>C in the PWREN\_STAT I<sup>2</sup>C bit.

PWREN is referenced to the VIO\_IN pin, and is 5.5V tolerant meaning that PWREN can go to 5.5V even if VIO\_IN is less than 5.5V. PWREN has a 10us bidirectional filter to prevent noise from triggering

unwanted operation.

#### EXT\_PG

The EXT\_PG pin is a dual purpose input. It functions as either a power good input from an external supply or a dynamic scaling control input. Configure EXT\_PG as a power good input by setting I<sup>2</sup>C bit DVS\_EN = 0. When configured as a power good input, EXT\_PG can be used as an input to the nRESETx pins. EXT\_PG polarity is controlled by the EXT\_PG\_POL bit. EXT\_PG is active high when EXT\_PG\_POL = 0 and active low when EXT\_PG\_POL = 1.

Configure EXT\_PG as a dynamic voltage scaling (DVS) control input by setting I<sup>2</sup>C bit DVS\_EN = 1. When EXT\_PG is de-asserted, all buck regulators regulate to their VSET0 voltage. When EXT\_PG is asserted, the buck regulators regulate to their VSET1 voltage. Note that EXT\_PG input is only valid for DVS toggling when the IC is in the ACTIVE state of operation. I<sup>2</sup>C bit EXT\_PG\_POL has no effect in DVS Mode.

EXT\_PG is referenced to the VIO\_IN pin, and is 5.5V tolerant meaning that EXT\_PG can go to 5.5V even if VIO\_IN is less than 5.5V. The EXT\_PG input has a 10us bidirectional filter to prevent noise from triggering unwanted operation.

#### VIO\_IN

VIO\_IN is the input bias supply for the IC. Apply an input voltage between 1.62V and 5.5V. Bypass to AGND with a high quality, 1uF ceramic capacitor.

#### MODE

Setting MODE = 0 configures Buck1 as a standard integrated buck regulator. Setting MODE = 1 configures Buck1 as an integrated bypass switch. In bypass mode, the Buck1 P-ch power FET is used to sequence the 3.3V supply to the downstream load. This provides full sequencing flexibility for 3.3V systems by allowing the 3.3V input to be used as the input supply for the other regulators but still be sequenced in any order for the downstream loads. Bypass mode is only valid for a 3.3V input voltage. The MODE pin must be tied directly to VIN or AGND. MODE is only sampled when VIN reaches its UVLO threshold during power. Changing MODE after power up has no effect on functionality. I<sup>2</sup>C bit MODE\_STAT shows the status of the MODE pin when it was read at startup.

#### GPIO

The GPIO pin can be configured as a digital input or an open drain output. It has multiple uses, including a sequencing input, sequencing output, status output, or control input to toggle a supply's output voltage. Set I<sup>2</sup>C bit GPIO\_OUT = 0 to configure GPIO as an input. When using GPIO as an output, GPIO\_OUT = 0 configures it as an open drain output, and GPIO\_OUT = 1 configures

it as a logic low output. When used as either an input or an output, I<sup>2</sup>C bit GPIO\_STAT always provides the real-time status of the GPIO pin. GPIO\_STAT = 0 when GPIO pin is a logic 0. GPIO\_STAT = 1 when GPIO pin is a logic 1.

## IRQ

The IRQ pin is an output that issues an interrupt to the host CPU/Controller when an ACT8870 fault or warning condition occurs.

IRQ is triggered by:

1. Die temperature exceeding Thermal Interrupt Threshold of 135C.
2. Any buck regulator reaching peak current limit, ILIMSET, for 16 cycles after softstart.
3. Any LDO regulator reaching current limit, LDOx\_ILIM, for more than 16us after softstart.
4. BUCK1 PMOS switch exceeding Current Detection threshold 75% of ILIMSET when system is configured in bypass mode.

IRQ is masked by the I<sup>2</sup>C register 0x00h bit2 (IRQ\_nMASK) by default to mask all IRQ conditions. To enable IRQ functionality, set IRQ\_nMASK = 1. IRQ is an active-low open drain 5.5V compatible output.

## POK

POK indicates that the voltage on the VIN pin is inside the POK UV and OV Interrupt Thresholds. If the VIN voltage is above or below these values, POK pulls low to interrupt the host CPU/Controller. POK is masked by the I<sup>2</sup>C bit POK\_nMASK by default. To enable POK functionality, set I<sup>2</sup>C bit POK\_nMASK = 1. I<sup>2</sup>C bits POK\_OV and POK\_UV provide real-time UV and OV status, even when POK is masked. The POK UV and OV threshold are configurable via the I<sup>2</sup>C bits POK\_UV\_SET and POK\_OV\_SET.

POK is an open drain output and is 5.5V tolerant meaning that POK can be pulled up to 5.5V even if VIO\_IN is less than 5.5V.

## nRESET\_AUX1 and nRESET\_AUX2

nRESET\_AUX1 and nRESET\_AUX2 pins can be used to signal that the IC is in the SLEEP state or that the input voltage is above or below the UV or OV threshold. They can also be tied to one or a combination of the power supply's internal POK signal. These outputs are immediately asserted low, but follow a programmed delay when de-asserted. The nRESET\_AUX1 delay time is controlled by the I<sup>2</sup>C bits RST\_AUX1\_DLY[2:0], which programs the delay between 400us and 2mS in 227us steps. The nRESET\_AUX2 delay time is

controlled by the I<sup>2</sup>C bits RST\_AUX2\_DLY[2:0], which programs the delay between 200us and 1ms in 114us steps. These pins are open drain output and 5.5V tolerant meaning that they can be pulled up to 5.5V even if VIO\_IN is less than 5.5V.

## nRESET

nRESET issues the main reset to the CPU/controller. nRESET is immediately asserted low when either the VIN voltage is above or below the UV or OV thresholds or any valid output supply voltage is below its Power Good threshold. After startup, nRESET de-asserts after a programmable delay time when VIN and all outputs are above their respective UVLO thresholds. The nRESET delay time is controlled by the I<sup>2</sup>C bits nRST\_DLY[2:0], which programs the delay between 200us and 1ms in 114us steps. nRESET is configurable, so refer to the CMI Options section in the back of the datasheet for its specific functionality for each CMI. nRESET is an open drain output and is 5.5V tolerant meaning that nRESET can be pulled up to 5.5V even if VIO\_IN is less than 5.5V.

## EXT\_EN

EXT\_EN is used to control an external regulator or to provide a control signal to other system components. Depending on the MODE pin status, EXT\_EN is either an exact output of the ACT8870's internal BUCK1 enable signal or an exact output of the bypass switch enable signal. The I<sup>2</sup>C bit EXT\_EN\_POL controls the EXT\_EN polarity. EXT\_EN is active high when EXT\_EN\_POL is low and EXT\_EN is active low when EXT\_EN\_POL is high. EXT\_EN is a push-pull CMOS output using VIO\_IN supply. Note that the EXT\_EN output is enabled and valid in all modes of operation. EXT\_EN is configurable, so refer to the CMI Options section in the back of the datasheet for its specific functionality for each CMI.

PG signals the status of a regulator's Power Good / UV comparator. When the regulator is below the Power Good threshold, the PG pin is pulled low. When above the threshold, the PG pin is open drain. The PG functionality is enabled by default, but can be disabled by I<sup>2</sup>C. Disable PG for each regulator using the regulator's UV\_FLTMSK bit. PG is configurable, so refer to the back of the datasheet for its specific functionality for each CMI. PG is an open drain output and is 5V tolerant meaning that PG can be pulled up to 5.5V even if VIO\_IN is less than 5.5V.

## Step-down dc/dc Converters

### General Description

The ACT8870 contains four fully integrated step-down converters. Buck1 is a 4A output, while Buck2, Buck3, and Buck4 are 2.5A outputs. All buck converters are fixed frequency, current-mode controlled, synchronous