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IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

In this document where the previous NXP references remain, please use the new links as shown below.

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Thank you for your cooperation and understanding,

WeEn Semiconductors

ACTT6G-800E

AC Thyristor Triac power switch

15 August 2014 **Product data sheet**

1. General description

AC Thyristor Triac power switch in a SOT226A (I2PAK) plastic package with self-protective clamping capabilities against low and high energy transients.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Direct interfacing with low power drivers and microcontrollers
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls

4. Quick reference data

Table 1. Quick reference data

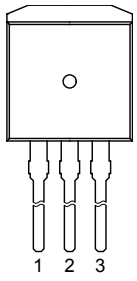
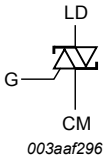
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5		-	-	51	A
T_j	junction temperature			-	-	125	°C
$I_{T(RMS)}$	RMS on-state current	full sine wave; T_{mb} ≤ 108 °C; Fig. 1; Fig. 2; Fig. 3		-	-	6	A
V_{PP}	peak pulse voltage	T_j = 25 °C; non-repetitive, off-state; Fig. 6		-	-	2	kV

Scan or click this QR code to view the latest information for this product

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 8		-	-	10	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 13		500	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 6 A; dV_{com}/dt = 1 V/µs; gate open circuit; Fig. 14; Fig. 15		10	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 **I2PAK (SOT226A)**	
2	LD	load		
3	G	gate		
mb	LD	mounting base; load		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACTT6G-800E	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 108$ °C; Fig. 1; Fig. 2; Fig. 3		-	6	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	56	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5		-	51	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse		-	13	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 9$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs		-	100	A/µs
I_{GM}	peak gate current	t = 20 µs		-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C
V_{PP}	peak pulse voltage	$T_j = 25$ °C; non-repetitive, off-state; Fig. 6		-	2	kV

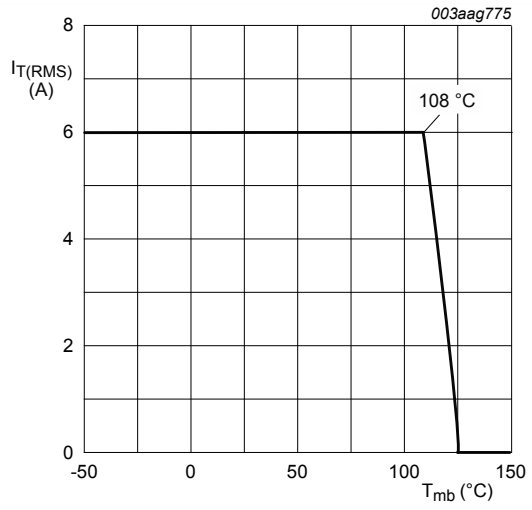
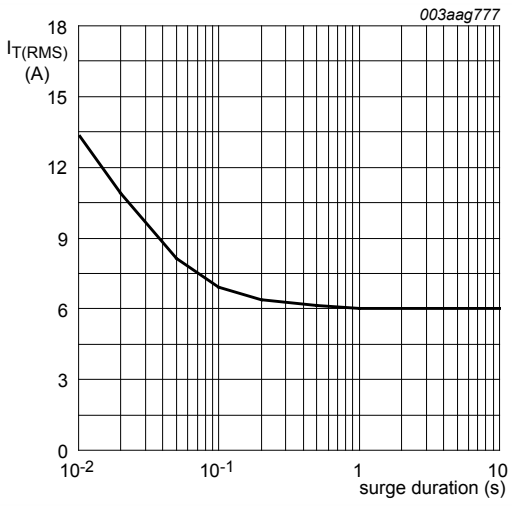
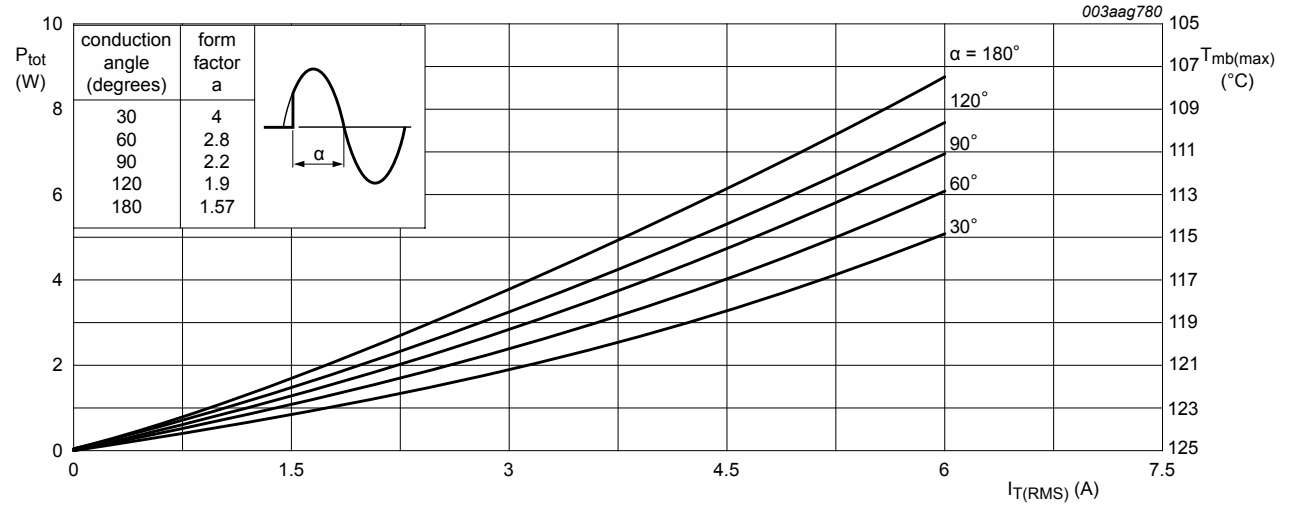


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz; T_{mb} = 108°C

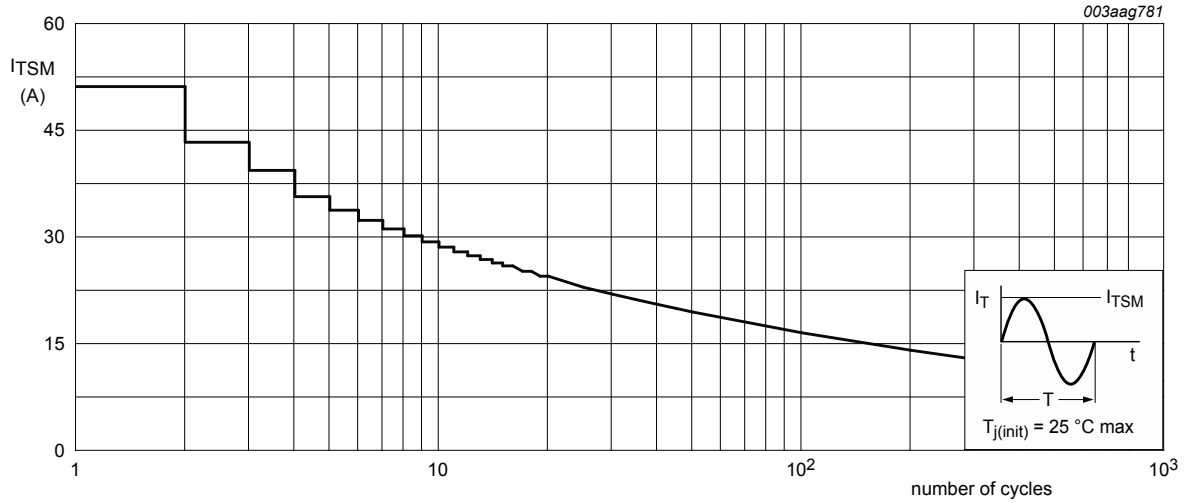
Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle

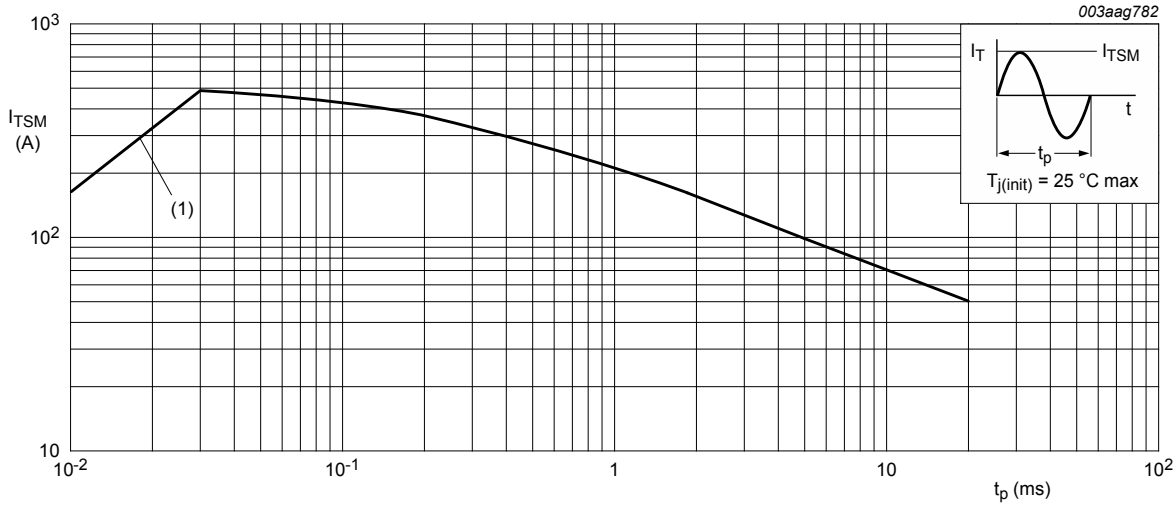
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

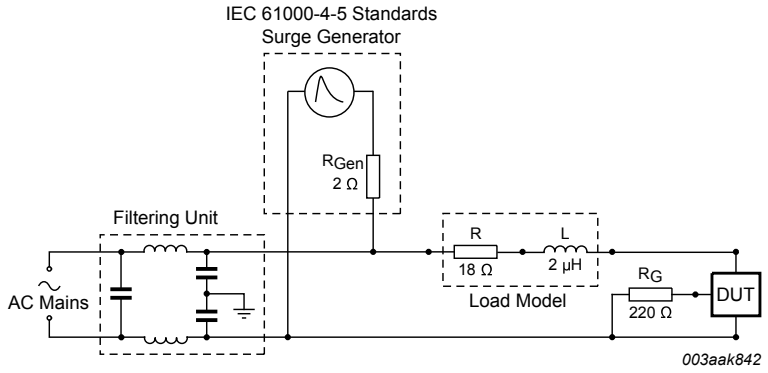
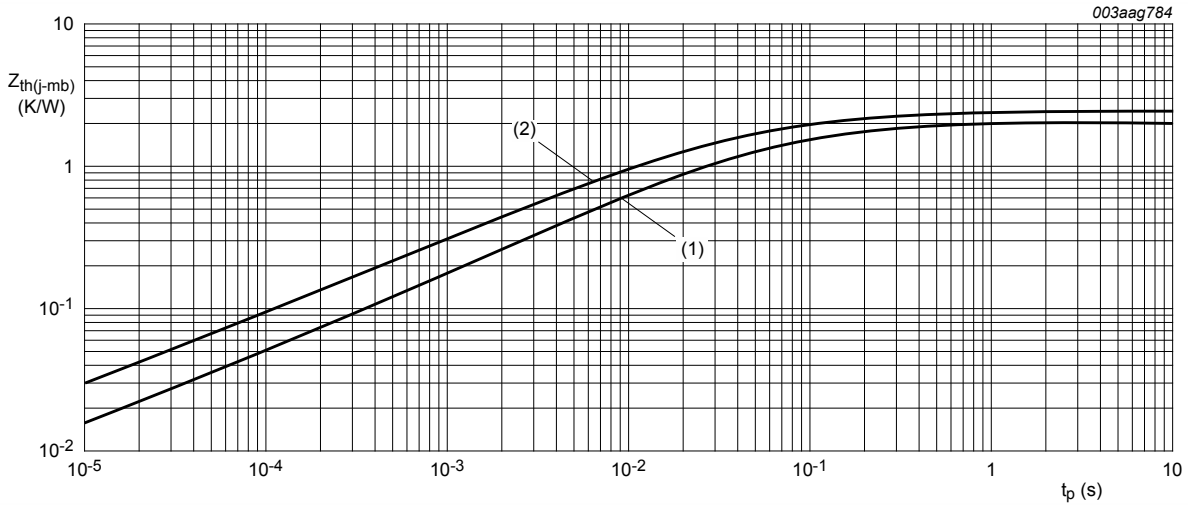


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	half cycle; Fig. 7		-	-	2.4	K/W
		full cycle; Fig. 7		-	-	2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	60	-	K/W



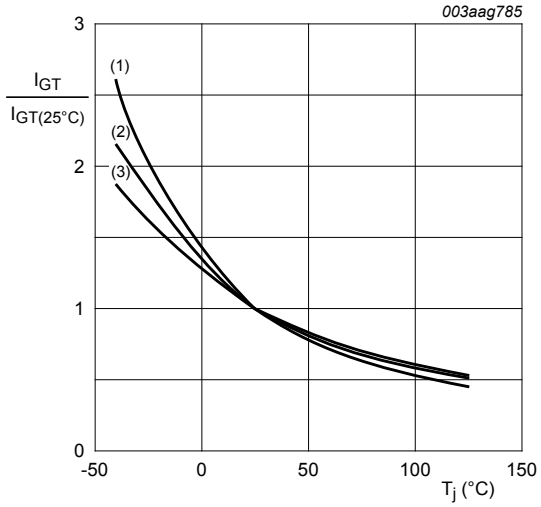
(1) Bidirectional (full cycle)
(2) Unidirectional (half cycle)

Fig. 7. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 8		-	-	10	mA
I_L	latching current	V_D = 12 V; I_G = 100 mA; LD+ G+; T_j = 25 °C; Fig. 9		-	-	30	mA
		V_D = 12 V; I_G = 100 mA; LD+ G-; T_j = 25 °C; Fig. 9		-	-	40	mA
		V_D = 12 V; I_G = 100 mA; LD- G-; T_j = 25 °C; Fig. 9		-	-	30	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	-	25	mA
V_T	on-state voltage	I_T = 8 A; T_j = 25 °C; Fig. 11		-	-	1.7	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 100 mA; T_j = 25 °C; Fig. 12		-	0.8	1	V
		V_D = 400 V; I_T = 100 mA; T_j = 125 °C; Fig. 12		0.2	0.45	-	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C		-	-	10	µA
		V_D = 800 V; T_j = 125 °C		-	-	0.5	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 13		500	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 6 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit; Fig. 14; Fig. 15		3.5	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 6 A; dV_{com}/dt = 10 V/µs; gate open circuit; Fig. 14; Fig. 15		5	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 6 A; dV_{com}/dt = 1 V/µs; gate open circuit; Fig. 14; Fig. 15		10	-	-	A/ms



(1) LD- G-
(2) LD+ G+
(3) LD+ G-

Fig. 8. Normalized gate trigger current as a function of junction temperature

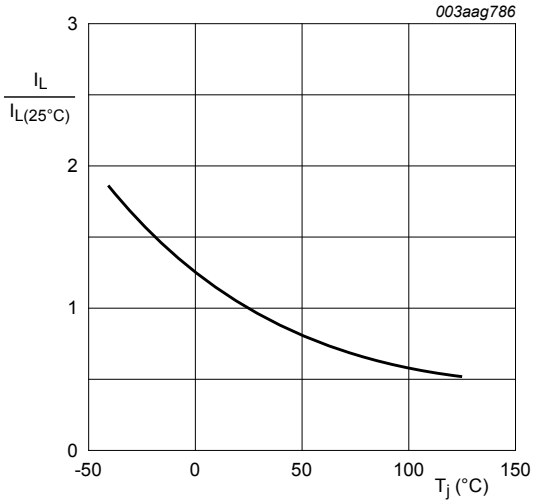


Fig. 9. Normalized latching current as a function of junction temperature

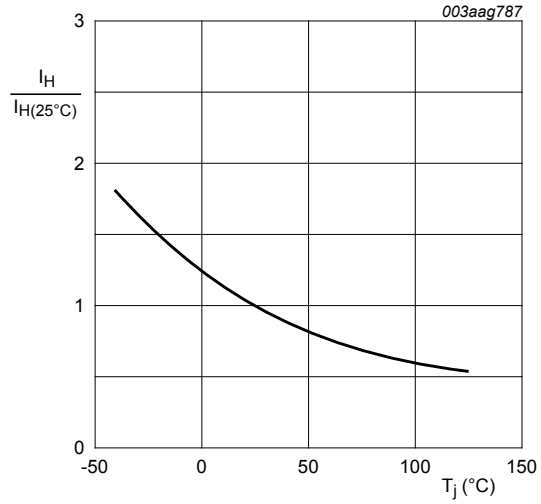
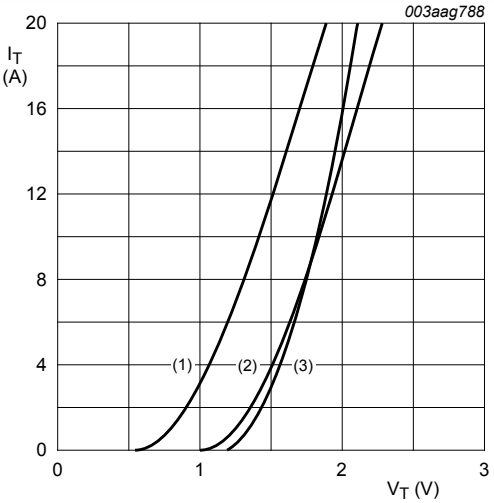


Fig. 10. Normalized holding current as a function of junction temperature



V_o = 1.109 V; R_s = 0.076 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 11. On-state current as a function of on-state voltage

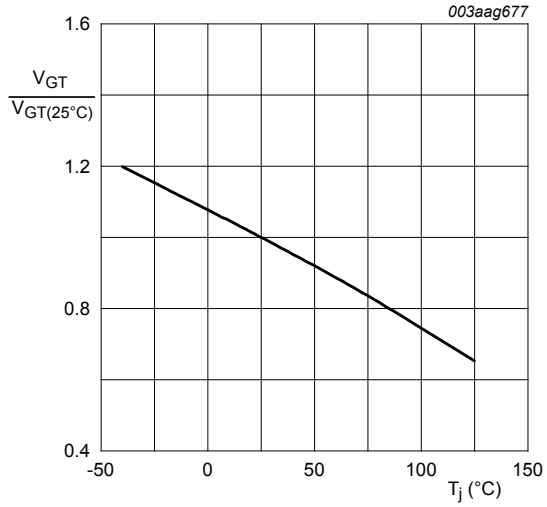
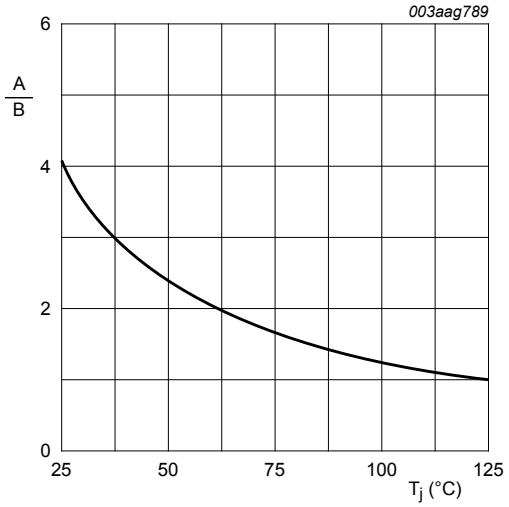


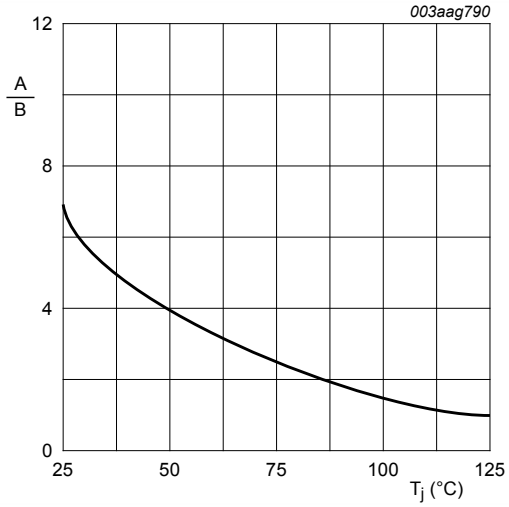
Fig. 12. Normalized gate trigger voltage as a function of junction temperature



A = dV_D/dt at condition T_j °C

B = dV_D/dt at condition T_j [125] °C

Fig. 13. Normalized rate of rise of off-state voltage as a function of junction temperature

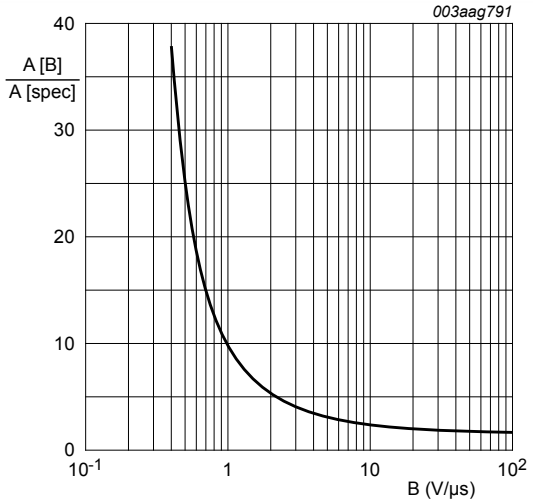


A = dI_{com}/dt at condition T_j °C

B = dI_{com}/dt at condition T_j [125] °C

V_D = 400 V

Fig. 14. Normalized critical rate of rise of commutating current as a function of junction temperature



A [B] is dI_{com}/dt at condition B, dV_{com}/dt

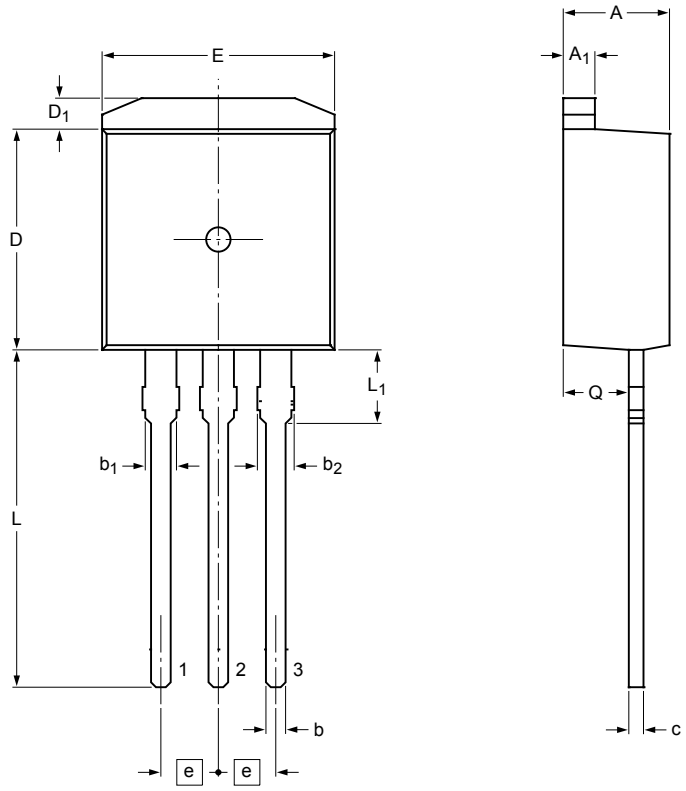
A [spec] is the specified data sheet value of dI_{com}/dt

turn-off time < 20 ms

Fig. 15. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values

10. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-262 **SOT226A**



0 5 10 mm

scale

Dimensions

Unit		A	A_1	b	b_1	b_2	c	D	D_1	E	e	L	L_1	Q
mm	max	4.7	1.40	0.95	1.40	1.7	0.65	9.4	1.32	10.30	2.54 (REF)	15.0	3.0 (REF)	2.6
	nom	4.3	1.15	0.70	1.14	1.3	0.45	8.6	1.02	9.65		12.5		2.2
	min													

sot226a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT226A		TO-262				~~09-08-17~~ 09-08-25

Fig. 16. Package outline I2PAK (SOT226A)

11. Legal information

11.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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12. Contents

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