Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Stereo Audio, 24-Bit, 96 kHz, Multibit Σ-Δ ADC

AD1871

FEATURES

- 5.0 V Stereo Audio ADC
  - with 3.3 V Tolerant Digital Interface
- Supports 96 kHz Sample Rates
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Sigma-Delta Modulators with
  - "Perfect Differential Linearity Restoration" for Reduced Idle Tones and Noise Floor
- 105 dB (Typ) Dynamic Range
- Supports 256/512 and 768 × f_S Master Clocks
- Flexible Serial Data Port
  - Allows Right-Justified, Left-Justified, I^2S Compatible and DSP Serial Port Modes
  - Cascadable (up to Four Devices) from a Single DSP SPORT
- Device Control via SPI Compatible Serial Port or
  - Optional Control Pins
- On-Chip Reference
- 28-Lead SSOP Package

APPLICATIONS

- Professional Audio
- Mixing Consoles
- Musical Instruments
- Digital Audio Recorders, Including
  - CD-R, MD, DVD-R, DAT, HDD
- Home Theater Systems
- Automotive Audio Systems
- Multimedia

PRODUCT OVERVIEW

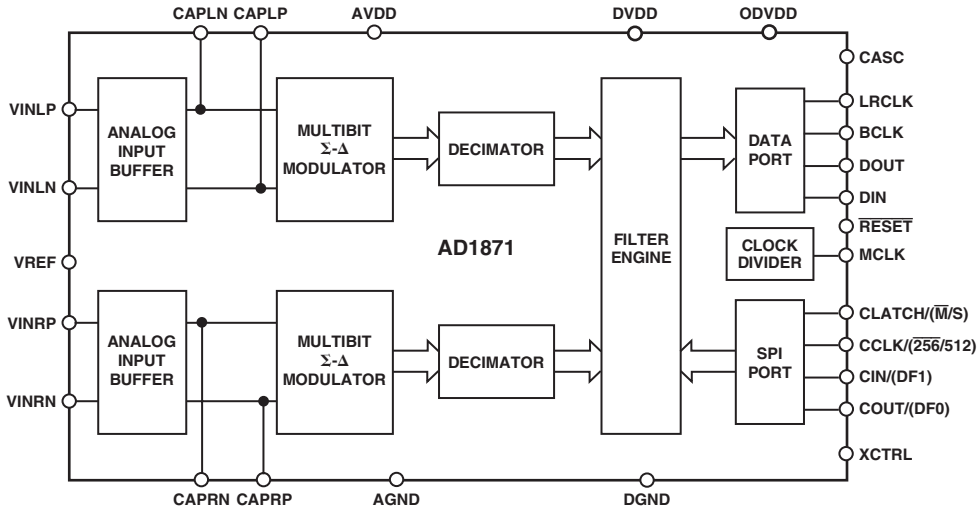
The AD1871 is a stereo audio ADC intended for digital audio applications requiring high performance analog-to-digital conversion. It features two 24-bit conversion channels each with programmable gain amplifier (PGA), multibit sigma-delta modulator, and decimation filters. Each channel provides 105 db of dynamic range, making the AD1871 suitable for applications such as digital audio recorders and mixing consoles.

Each of the AD1871's input channels (left and right) can be configured as either differential or single-ended (two inputs muxed with internal single-ended-to-differential conversion). The input PGA features a gain range of 0 dB to 12 dB in steps of 3 dB. The Σ-Δ modulator features a proprietary multibit architecture that realizes optimum performance over an audio bandwidth with standard audio sampling rates of 32 kHz up to 96 kHz. The decimation filter response features very low pass-band ripple and excellent stop-band attenuation.

The AD1871's audio data interface supports all common interface formats such as I^2S, left-justified, right-justified as well as other modes that allow for convenient connection to general-purpose digital signal processors (DSPs). The AD1871 also features an SPI compatible serial control port that allows for convenient control of device parameters and functionality such as sample word-width, PGA settings, interface modes, and so on.

The AD1871 operates from a single 5 V power supply—with an optional digital interfacing capability of 3.3 V. It is housed in a 28-lead SSOP package and is characterized for operation over the temperature range –40°C to +105°C.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD1871* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD1871 Evaluation Board
- ADUSB2EBZ Evaluation Board

DOCUMENTATION

Application Notes

- AN-1006: Using the EVAL-ADUSB2EBZ
- AN-211: The Alexander Current-Feedback Audio Power Amplifier
- AN-327: DAC ICs: How Many Bits Is Enough?

Data Sheet

- AD1871: Stereo Audio, 24-bit, 96 kHz, Multi-bit Sigma Delta ADC Data Sheet

DESIGN RESOURCES

- AD1871 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD1871 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

AD1871–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages . . . . . 5.0 V
Ambient Temperature . . . . . 25°C
Input Clock (f_{CLKIN}) [$256 \times f_S$] . . . . . 12.288 MHz
Input Signal . . . . . 991.768 Hz
. . . . . –0.5 dB Full Scale (dBFS) (Differential, PGA/MUX Enabled)
Measurement Bandwidth . . . . . 23.2 Hz to 19.998 kHz
Word Width . . . . . 24 Bits
Load Capacitance on Digital Outputs . . . . . 100 pF
Input Voltage High (V_{IH}) . . . . . 2.4 V
Input Voltage Low (V_{IL}) . . . . . 0.8 V
Master Mode, Data I^2S Justified

ANALOG PERFORMANCE

Parameter	Min	Typ	Max	Unit	Conditions
RESOLUTION		24		Bits	
DIFFERENTIAL INPUT					PGA/MUX Enabled
Dynamic Range					(20 Hz to 20 kHz, –60 dB Input)
Unweighted	98	103		dB	
A-Weighted	100	105		dB	
Signal-to-Noise Ratio		106		dB	
Total Harmonic Distortion + Noise		–85		dB	Input = –0.5 dBFS
(THD+N)		–103		dB	Input = –20 dBFS
Multibit Modulator Only					Modulator Output @ 5.6448 MHz
Dynamic Range (A-Weighted)		102		dB	
SINGLE-ENDED INPUT					PGA/MUX Enabled
Dynamic Range					(20 Hz to 20 kHz, –60 dB Input)
Unweighted		103		dB	
A-Weighted		105		dB	
Signal-to-Noise Ratio		106		dB	
Total Harmonic Distortion + Noise		–85		dB	Input = –0.5 dBFS
(THD+N)		–103		dB	Input = –20 dBFS
DIFFERENTIAL INPUT (BYPASS)					PGA/MUX Disabled
Dynamic Range					(20 Hz to 20 kHz, –60 dB Input)
Unweighted		103		dB	
A-Weighted		106		dB	
Signal-to-Noise Ratio		106		dB	
Total Harmonic Distortion + Noise		–86		dB	Input = –0.5 dBFS
(THD+N)		–104		dB	Input = –20 dBFS
DIFFERENTIAL INPUT (f_S = 96 kHz)					PGA/MUX Enabled; AMC = 1
Dynamic Range					(20 Hz to 20 kHz, –60 dB Input)
Unweighted		103		dB	
A-Weighted		106		dB	
Signal-to-Noise Ratio		106		dB	
Total Harmonic Distortion + Noise		–87		dB	Input = –0.5 dBFS
(THD+N)		–104		dB	Input = –20 dBFS
Analog Inputs					
Differential Input Range (± Full Scale)	–2.828		+2.828	V	
Input Impedance (PGA/MUX)		8		kΩ	Differential
Input Impedance (ByPass)		40		kΩ	Differential
Input Impedance (PGA/MUX)		4		kΩ	Single Ended
V_{REF}	2.138	2.25	2.363	V	
DC Accuracy					
Gain Error		–10		%	
Interchannel Gain Mismatch	–0.2	–0.01	+0.2	dB	
Gain Drift		100		ppm/°C	
Crosstalk (EIAJ Method)		–100		dB	

LOW-PASS DIGITAL FILTER CHARACTERISTICS (f_S = 48 kHz)

Parameter	Min	Typ	Max	Unit
Decimation Factor		128		
Pass-Band Frequency		21.77		kHz
Stop-Band Frequency		26.23		kHz
Pass-Band Ripple		±0.01		dB
Stop-Band Attenuation		120		dB
Group Delay		910		µs

LOW-PASS DIGITAL FILTER CHARACTERISTICS (f_S = 96 kHz)

Parameter	Min	Typ	Max	Unit
Decimation Factor		64		
Pass-Band Frequency		43.54		kHz
Stop-Band Frequency		52.46		kHz
Pass-Band Ripple		±0.01		dB
Stop-Band Attenuation		120		dB
Group Delay		460		µs

HIGH-PASS DIGITAL FILTER CHARACTERISTICS (f_S = 48 kHz)

Parameter	Min	Typ	Max	Unit
Cutoff Frequency		2		Hz

HIGH-PASS DIGITAL FILTER CHARACTERISTICS (f_S = 96 kHz)

Parameter	Min	Typ	Max	Unit
Cutoff Frequency		4		Hz

MASTER CLOCK (MCLK) AND RESET TIMING

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{MCH}	MCLK High Width	20			ns	
t_{MCL}	MCLK Low Width	20			ns	
t_{PDR}	$\overline{\text{RESET}}$ Low Pulsewidth	20			ns	

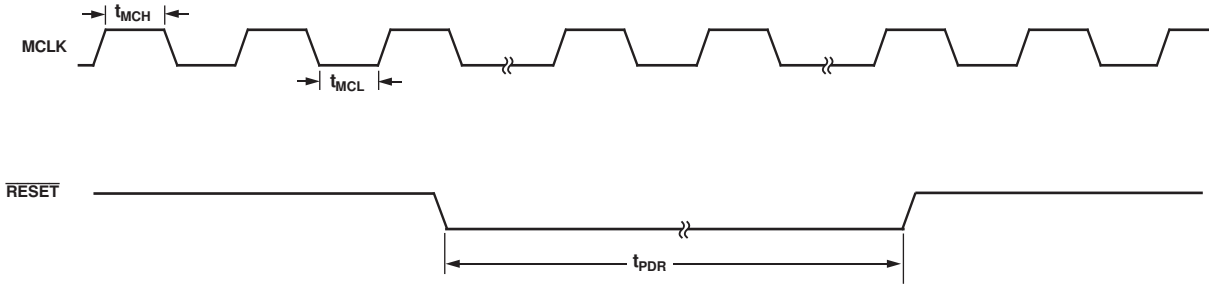


Figure 1. MCLK/$\overline{RESET}$ Timing

DATA INTERFACE TIMING (STANDALONE MODE–MASTER)

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{BDLY}	BCLK Delay	20			ns	From MCLK Rising
t_{BLDLY}	LRCLK Delay to Low	10			ns	From BCLK Falling
t_{BDDLY}	DOUT Delay	10			ns	From BCLK Falling

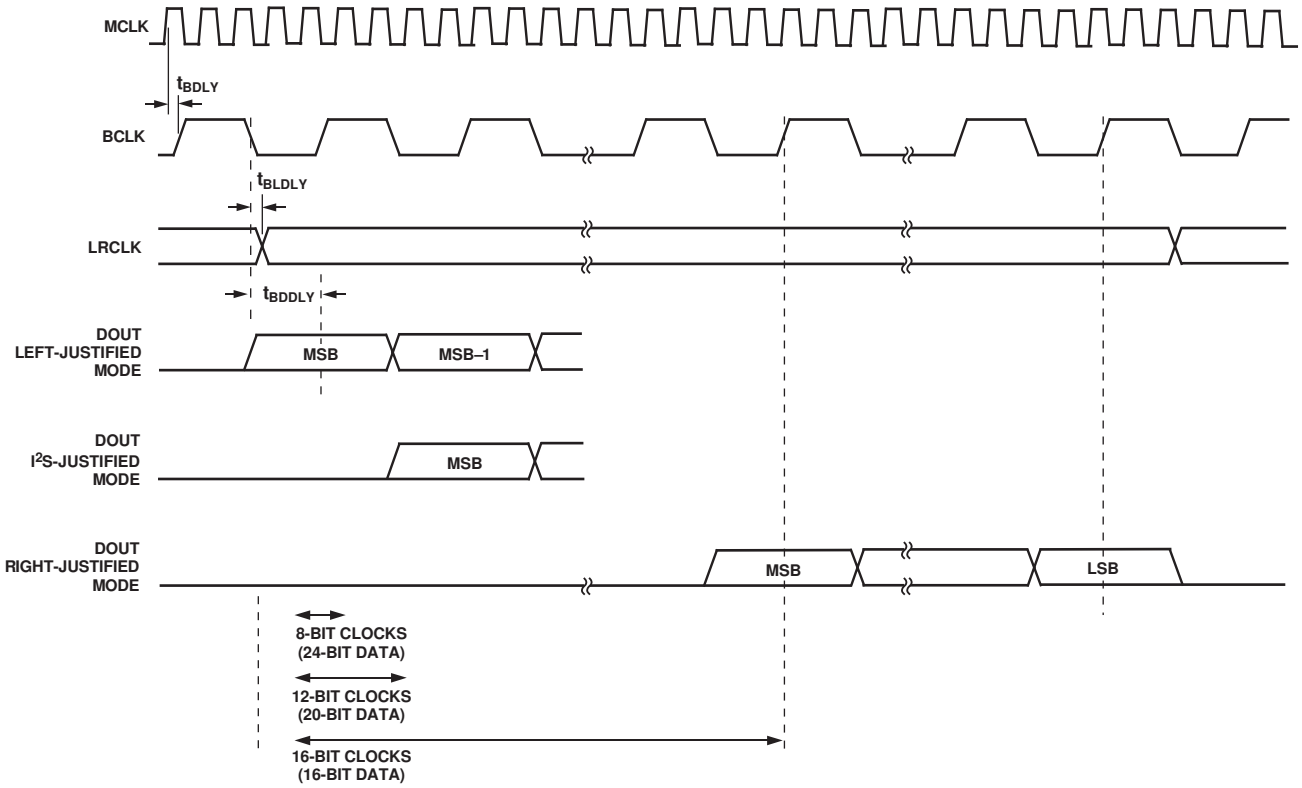


Figure 2. Master Data Interface Timing

DATA INTERFACE TIMING (STANDALONE MODE–SLAVE)

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{BCH}	BCLK High Width		30		ns	
t_{BCL}	BCLK Low Width		30		ns	
t_{BDSD}	DOUT Delay	20			ns	From BCLK Falling
t_{LRS}	LRCLK Setup	10			ns	To BCLK Rising
t_{LRH}	LRCLK Hold	5			ns	From BCLK Rising

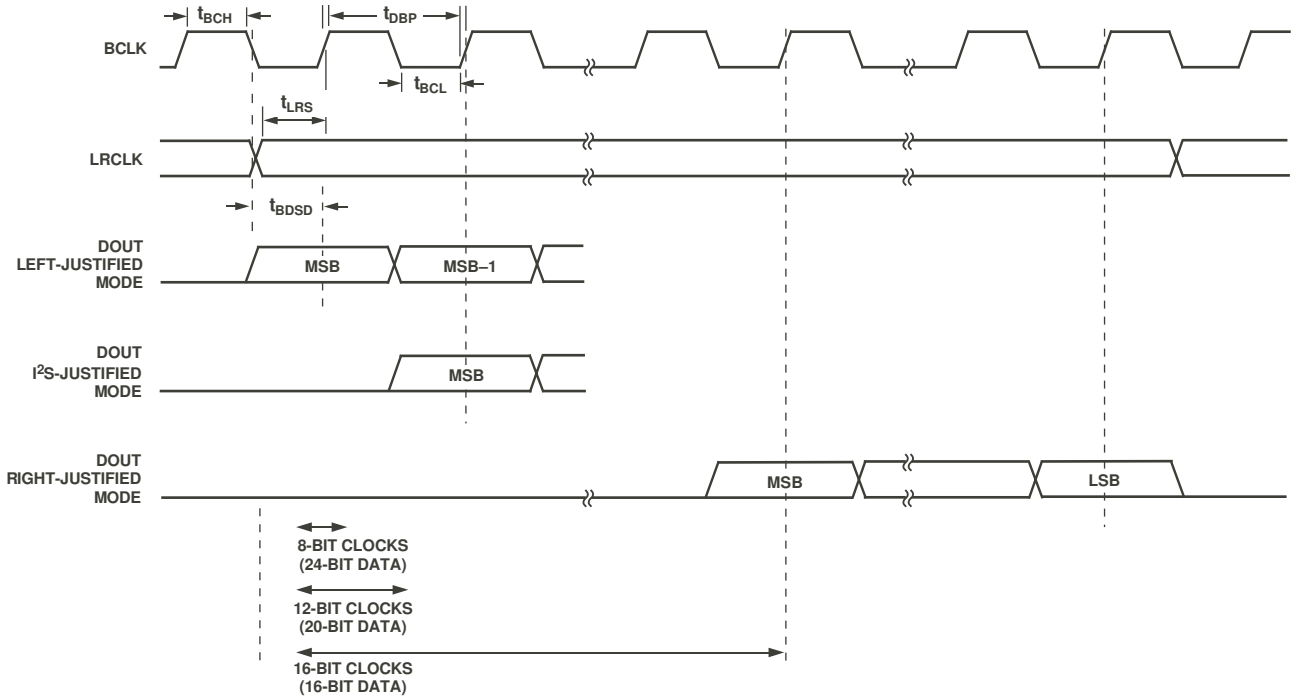


Figure 3. Slave Data Interface Timing

DATA INTERFACE TIMING (CASCADE MODE–MASTER)

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{BCHDC}	BCLK High Delay	20			ns	From MCLK Rising
t_{BCLDC}	BCLK Low Delay	20			ns	From MCLK Falling
t_{BLRDC}	LRCLK Delay	10			ns	From BCLK Rising
t_{BDDC}	DOUT Delay	10			ns	From BCLK Rising
t_{BDIS}	DIN Setup	10			ns	To BCLK Rising
t_{BDIH}	DIN Hold	10			ns	From BCLK Rising

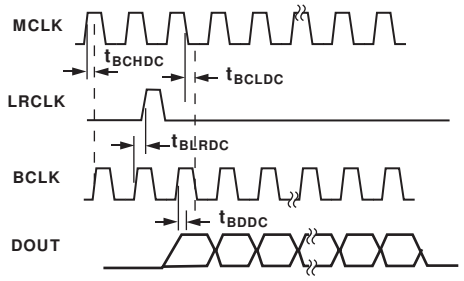


Figure 4. Master Cascade Interface Timing

DATA INTERFACE TIMING (CASCADE MODE–SLAVE)

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{BCHC}	BCLK High Width		30		ns	
t_{BCLC}	BCLK Low Width		30		ns	
t_{BDSDC}	DOUT Delay	20			ns	From BCLK Rising
t_{LRSC}	LRCLK Setup	10			ns	To BCLK Rising
t_{LRHC}	LRCLK Hold	5			ns	From BCLK Rising
t_{BDIS}	DIN Setup	10			ns	To BCLK Rising
t_{BDIH}	DIN Hold	10			ns	From BCLK Rising

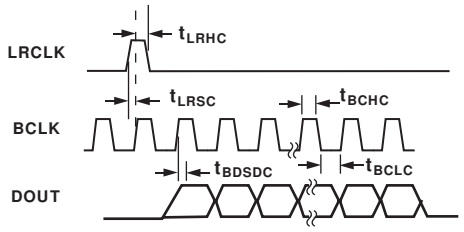


Figure 5. Slave Cascade Interface Timing

DATA INTERFACE TIMING (MODULATOR MODE)

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{MOCH}	MODCLK High Width		MCLK		ns	
t_{MOCL}	MODCLK Low Width		MCLK		ns	
t_{MHDD}	MOD DATA High Delay		30		ns	From MCLK Rising
t_{MLDD}	MOD DATA Low Delay		20		ns	From MCLK Falling
t_{MMDR}	MODCLK Delay Rising		30		ns	MCLK Falling to MODCLK Rising
t_{MMDF}	MODCLK Delay Falling		20		ns	MCLK Falling to MODCLK Falling

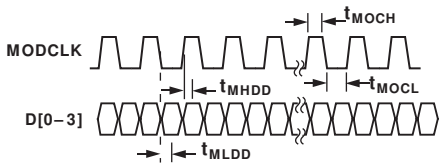


Figure 6. Modulator Mode Timing

CONTROL INTERFACE (SPI) TIMING

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{CCH}	CCLK High Width	40			ns	
t_{CCL}	CCLK Low Width	40			ns	
t_{CCP}	CCLK Period	80			ns	
t_{CDS}	CDATA Setup Time	10			ns	To CCLK Rising
t_{CDH}	CDATA Hold Time	10			ns	From CCLK Rising
t_{CLS}	CLATCH Setup Time	10			ns	To CCLK Rising
t_{CLH}	CLATCH Hold Time	10			ns	From CCLK Rising
t_{COE}	COUT Enable	15			ns	From CLATCH Falling
t_{COD}	COUT Delay	20			ns	From CCLK Falling
t_{COTS}	COUT Three-State	25			ns	From CLATCH Rising

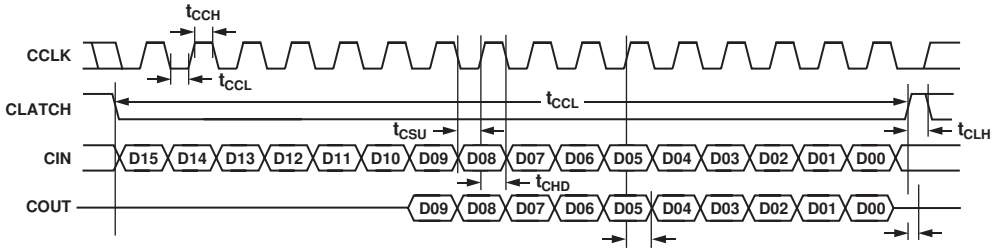


Figure 7. Control Interface Timing

DIGITAL I/O

Parameter	Min	Typ	Max	Unit
Input Voltage High (V_{IH})	2.4			V
Input Voltage Low (V_{IL})			0.8	V
Input Leakage (I_{IH} @ V_{IH} = 5 V)			10	µA
Input Leakage (I_{IL} @ V_{IL} = 0 V)			10	µA
Output Voltage High (V_{OH} @ I_{OH} = –2 mA)	ODVDD – 0.4 V			V
Output Voltage Low (V_{OL} @ I_{OL} = +2 mA)			0.4	V
Input Capacitance			15	pF

POWER

Parameter	Min	Typ	Max	Unit
Supplies				
Voltage, AVDD, and DVDD	4.5	5	5.5	V
Voltage, ODVDD	2.7		5.5	V
Analog Current		40	45	mA
Analog Current—Power-Down (MCLK Running)		4.0	6.0	µA
Digital Current, DVDD		18	22	mA
Digital Current, ODVDD		0.5	1.0	mA
Digital Current—Power-Down (MCLK Running) DVDD*		0.8	2.0	mA
Digital Current—Power-Down (MCLK Running) ODVDD*		1.0	15.0	µA
Power Supply Rejection				
1 kHz 300 mV p-p Signal at Analog Supply Pins		–86		dB
20 kHz 300 mV p-p Signal at Analog Supply Pins		–77		dB

*$\overline{\text{RESET}}$ held low.

TEMPERATURE RANGE

Parameter	Min	Typ	Max	Unit
Specifications Guaranteed		25		°C
Functionality Guaranteed	–40		+105	°C
Storage	–65		+150	°C

Specifications subject to change without notice.

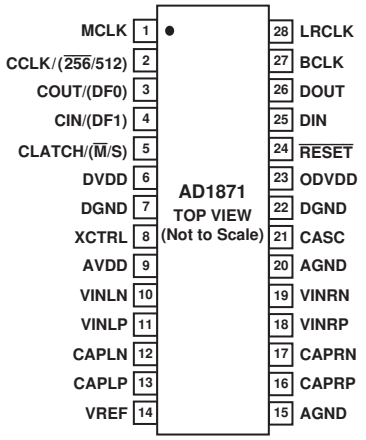
ABSOLUTE MAXIMUM RATINGS

	Min	Typ	Max	Unit
DVDD to DGND and ODVDD to DGND	0		6	V
AVDD to AGND	0		6	V
Digital Inputs	DGND – 0.3		DVDD + 0.3	V
Analog Inputs	AGND – 0.3		AVDD + 0.3	V
AGND to DGND	–0.3		+0.3	V
Reference Voltage		Indefinite Short Circuit to Ground		
Soldering (10 sec)			300	°C

ORDERING GUIDE

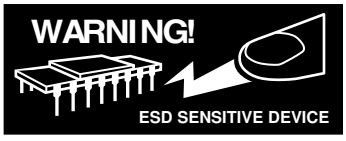
Model	Temperature	Package Description	Package Option
AD1871YRS	–40°C to +105°C	SSOP	RS-28
AD1871YRS-REEL	–40°C to +105°C	SSOP	RS-28 in 13″ Reel (1500 pieces)
EVAL-AD1871EB		Evaluation Board	

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1871 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin No.	Input/ Output	Mnemonic	Description
1	I	MCLK	Master Clock. The master clock input determines the sample rate of the device. MCLK can be 256, 512, or 768 times the sampling frequency.
2	I	CCLK[1]	Control Port Bit Clock—clock signal for control port (SPI) interface. This pin is reconfigured in the External Control Mode (Pin XCTRL is high), see below.
3	I/O	COUT[1, 2]	Control Port Data Out—serial data output from the control port (SPI) interface (in readback). This pin is reconfigured in the External Control Mode (Pin XCTRL is high), see below; or in Modulator Mode (Bit MME of Control Register II is set), see below.
4	I	CIN[1]	Control Port Data Input—serial data input for control port (SPI) interface. This pin is reconfigured in the External Control Mode (Pin XCTRL is high), see below.
5	I	CLATCH[1]	Control Port Frame Sync—frame sync (framing signal) for control port (SPI) interface. This pin is reconfigured in the External Control Mode (Pin XCTRL is high), see below.
6	I	DVDD	5 V Digital Core Supply
7	I	DGND	Digital Ground
8	I	XCTRL	External Control Enable. This pin is used to select the Control Mode for the device. When XCTRL is low, control is via the SPI compatible control port (Pins CCLK, CLATCH, CIN, and COUT). When XCTRL is enabled (high), control of several device functions is possible by hardware pin strapping (Pins $\overline{256}$/512, $\overline{M}$/S, DF1, and DF0). In External Control Mode, all other functions are in default state (please refer to the Control Register Descriptions and External Control section).
9	I	AVDD	5 V Analog Supply
10	I	VINLN	Left Channel, Negative Input (via MUX/PGA)
11	I	VINLP	Left Channel, Positive Input (via MUX/PGA)
12	I/O	CAPLN	Left External Filter Capacitor (Negative Input to Modulator)
13	I/O	CAPLP	Left External Filter Capacitor (Positive Input to Modulator)
14	O	VREF	Reference Voltage Output. It is recommended to connect a capacitor combination of 10 µF in parallel with 0.1 µF between VREF and AGND (Pin 15). (See Layout Recommendations.)
15	I	AGND	Analog Ground
16	I/O	CAPRP	Right External Filter Capacitor (Positive Input to Modulator)
17	I/O	CAPRN	Right External Filter Capacitor (Negative Input to Modulator)
18	I	VINRP	Right Channel, Positive Input (via MUX/PGA)
19	I	VINRN	Right Channel, Negative Input (via MUX/PGA)
20	I	AGND	Analog Ground
21	I	CASC	Cascade Enable. This pin enables cascading of up to four AD1871 devices to a single DSP serial port (see Cascading section).
22	I	DGND	Digital Ground
23	I	ODVDD	Digital Interface Supply. The digital interface can operate from 3.3 V to 5.0 V (nominal).
24	I	$\overline{\text{RESET}}$	Reset
25	I/O	DIN[2]	Serial Data Input. Serial data input pin, only valid when the device is configured in Cascade Mode (Pin CASC is high). This pin is reconfigured in Modulator Mode (Bit MME of Control Register II is set), see below.
26	O	DOUT[2]	Audio Serial Data Output. This pin is reconfigured in Modulator Mode (Bit MME of Control Register II is set), see below.
27	I/O	BCLK[2]	Audio Serial Bit Clock. The bit clock is the audio data serial clock and determines the rate of audio data transfer. This pin is reconfigured in Modulator Mode (Bit MME of Control Register II is set), see below.
28	I/O	LRCLK[2]	Left/Right Clock. This clock, also known as the word clock, determines the sampling rate. It is an output or input depending on the status of $\overline{\text{Master}}$/Slave. This pin is reconfigured in Modulator Mode (Bit MME of Control Register II is set), see below.

NOTES
[1]External Control Mode (See pg 11)
[2]Modulator Mode (See pg 11)

Pin Function Redefinition in External Control Mode

Pin No.	Input/ Output	Mnemonic	Description
2	I	$\overline{256}$/512	Clock Rate Select. This pin is used to select between an MCLK of 256 × f_S (pin low) or 512 × f_S (pin high).
3	I	DF0	Data Format Select 0. This pin is used as the low bit (DF0) of the data format selection (see section on External Control).
4	I	DF1	Data Format Select 1. This pin is used as the high bit (DF1) of the data format selection (see section on External Control).
5	I	$\overline{M}$/S	Master/Slave Select. This pin is used to select between the Master (pin low) or Slave (pin high) Modes.

Pin Function Redefinition in Modulator Mode

Pin No.	Input/ Output	Mnemonic	Description
3	O	MODCLK	This pin provides a clock output that allows the user to decode the left and right channel modulator outputs. It is similar to a left/right clock but runs (nominally) at 5.6448 MHz and gates a 4-bit modulator output word in each phase (see section on Modulator Mode).
25	O	D3	Bit 3 of the Modulator Output Word
26	O	D2	Bit 2 of the Modulator Output Word
27	O	D1	Bit 1 of the Modulator Output Word
28	O	D0	Bit 0 of the Modulator Output Word

TERMINOLOGY

Dynamic Range

The ratio of a full-scale input signal to the integrated input noise in the pass band (20 Hz to 20 kHz), expressed in decibels (dB). Dynamic range is measured with a –60 dB input signal and is equal to (S/[THD+N]) + 60 dB. Note that spurious harmonics are below the noise with a –60 dB input, so the noise level establishes the dynamic range. The dynamic range is specified with and without an A-Weight filter applied.

Signal to (Total Harmonic Distortion + Noise) (S/[THD+N])

The ratio of the root-mean-square (rms) value of the fundamental input signal to the rms sum of all other spectral components in the pass band, expressed in decibels (dB).

Pass Band

The region of the frequency spectrum unaffected by the attenuation of the digital decimator's filter.

Pass-Band Ripple

The peak-to-peak variation in amplitude response from equal-amplitude input signal frequencies within the pass band, expressed in decibels.

Stop Band

The region of the frequency spectrum attenuated by the digital decimator's filter to the degree specified by stop-band attenuation.

Gain Error

With a near full-scale input, the ratio of the actual output to the expected output, expressed as a percentage.

Interchannel Gain Mismatch

With identical near full-scale inputs, the ratio of the outputs of the two stereo channels, expressed in decibels.

Gain Drift

Change in response to a near full-scale input with a change in temperature, expressed as parts-per-million (ppm) per °C.

Crosstalk (EIAJ Method)

Ratio of response on one channel with a grounded input to a full-scale 1 kHz sine-wave input on the other channel, expressed in decibels.

Power Supply Rejection

With no analog input, signal present at the output when a 300 mV p-p signal is applied to power supply pins, expressed in decibels of full scale.

Group Delay

Intuitively, the time interval required for an input pulse to appear at the converter's output, expressed in milliseconds (ms). More precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

GLOSSARY

ADC—Analog-to-Digital Converter

DSP—Digital Signal Processor

IMCLK—Internal master clock signal, used to clock the decimating filter section. (Its frequency must be $256 \times f_S$.)

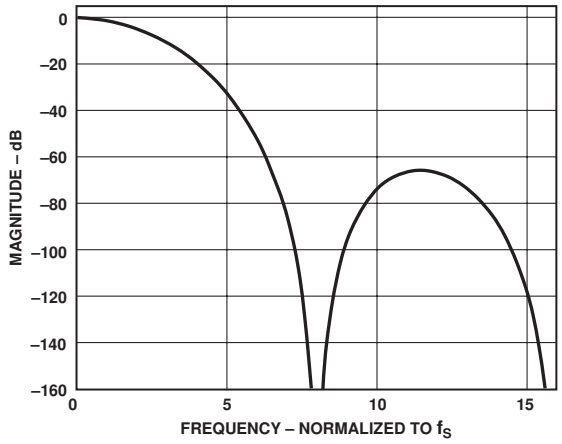
MCLK—External master clock signal applied to the AD1871. Its frequency can be 256, 512, or $768 \times f_S$. MCLK is divided internally to give an IMCLK frequency that must be $256 \times f_S$.

MODCLK—This is the Σ-Δ modulator clock that determines the sample rate of the modulator. Ideally, it should not exceed the lower of 6.144 MHz or $128 \times f_S$. The MODCLK is derived from the IMCLK by a divider that can be selected as /2 or /4.

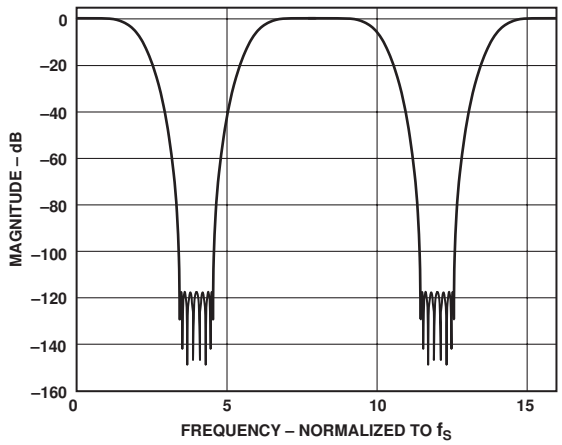
MUX—Multiplexer

PGA—Programmable Gain Amplifier

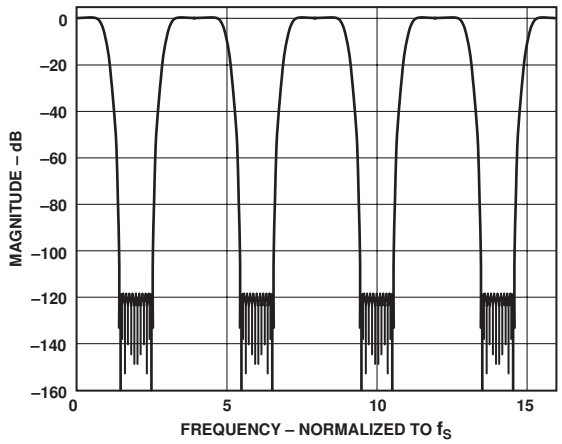
FILTER RESPONSES



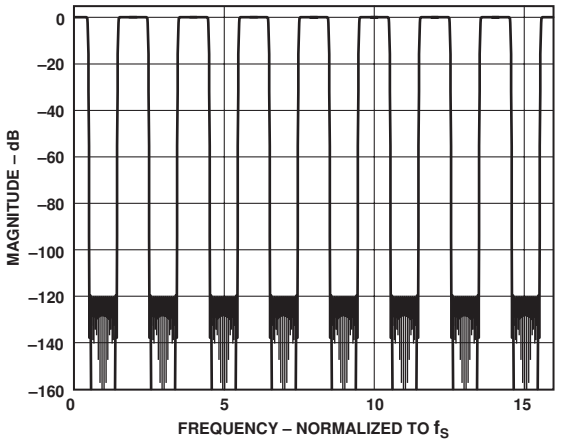
TPC 1. Sinc Filter Response (AMC = 0)



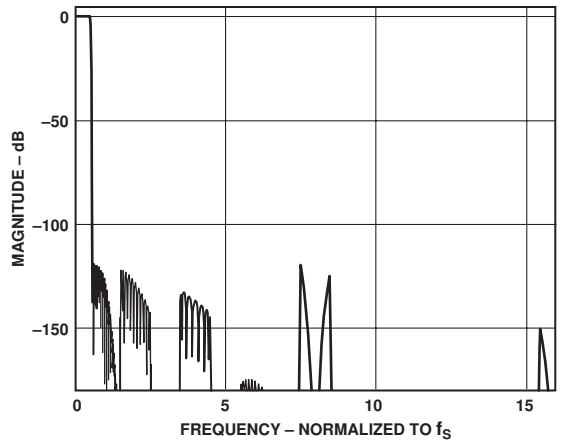
TPC 2. First Half-Band Filter Response



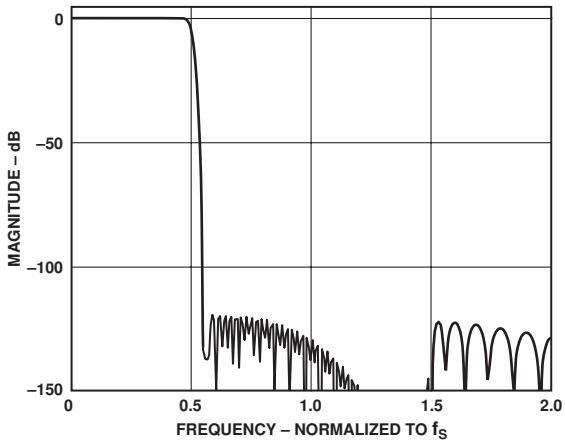
TPC 3. Comb Compensation Filter Response



TPC 4. Second Half-Band Filter Response

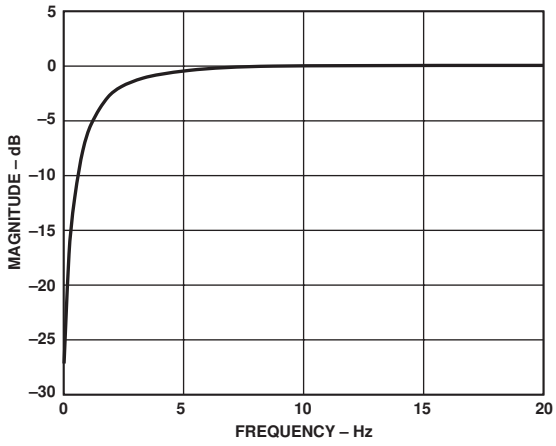


TPC 5. Composite Filter Response (AMC = 0)

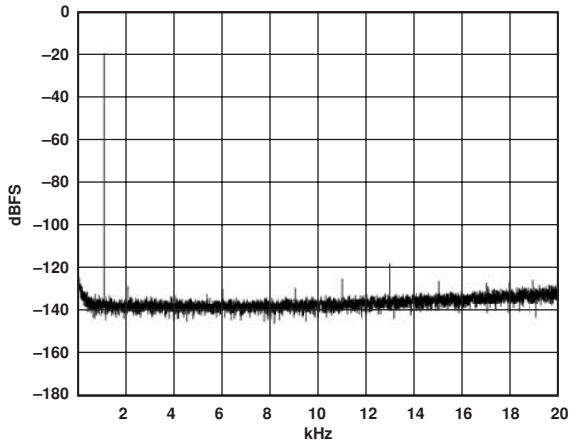


TPC 6. Composite Filter Response (Pass Band Section) (AMC = 0)

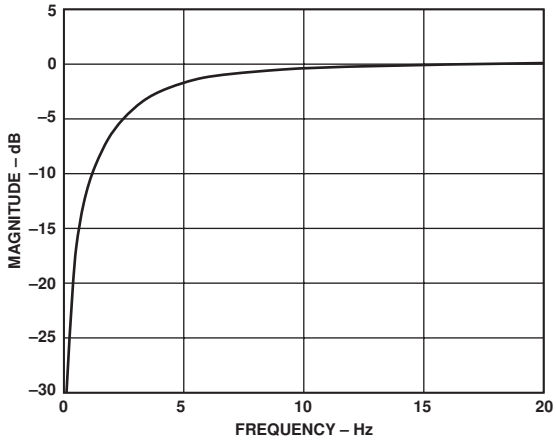
DEVICE PERFORMANCE CURVES



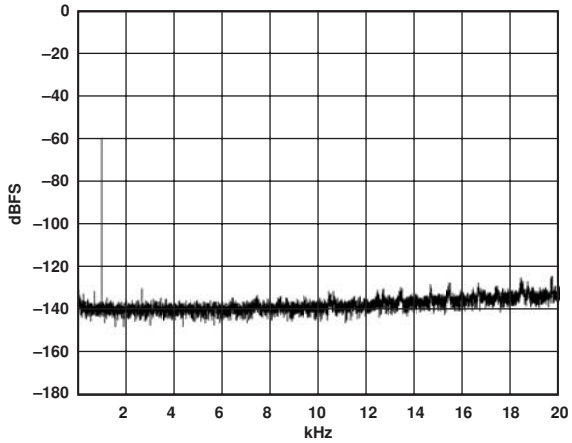
TPC 7. High-Pass Filter Response, f_S = 48 kHz



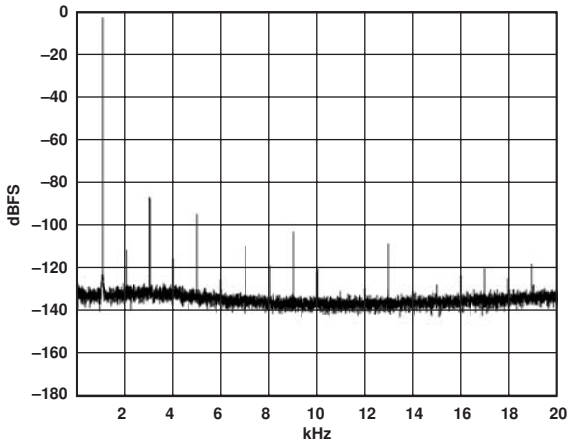
TPC 10. 1 kHz Tone at –20 dBFS, (32 k-Point FFT), f_S = 48 kHz



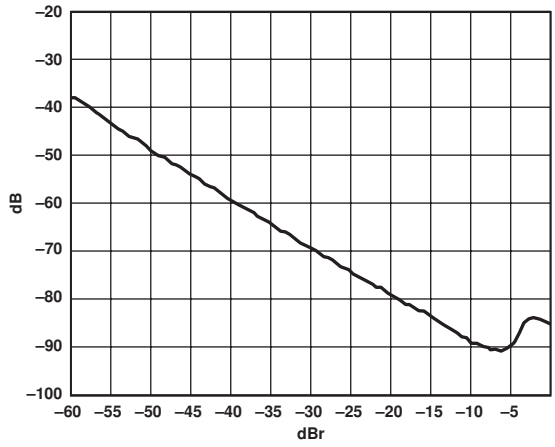
TPC 8. High-Pass Filter Response, f_S = 96 kHz



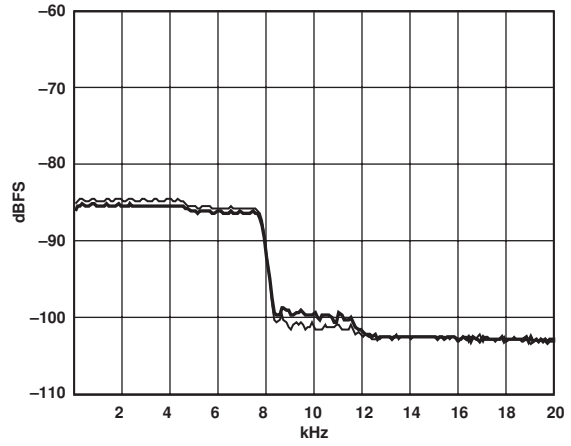
TPC 11. 1 kHz Tone at –60 dBFS, (32 k-Point FFT), f_S = 48 kHz



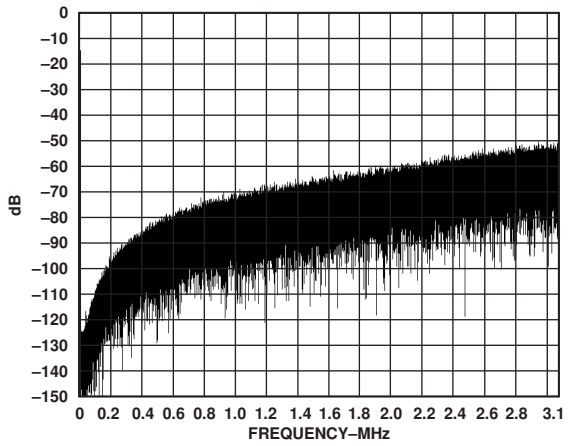
TPC 9. 1 kHz Tone at –0.5 dBFS, (32 k-Point FFT), f_S = 48 kHz



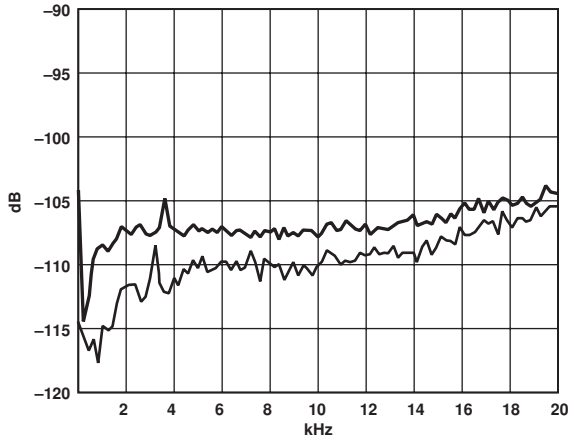
TPC 12. THD+N vs. Input Amplitude at 1 kHz, f_S = 48 kHz



TPC 13. THD+N vs. Input Frequency at –0.5 dBFS, f_S = 48 kHz



TPC 15. FFT of Modulator Output at –0.5 dBFS, f_S = 6.144 MHz



TPC 14. Channel Separation vs. Frequency at –0.5 dBFS, f_S = 48 kHz

FUNCTIONAL DESCRIPTION

Clocking Scheme

The MCLK pin is the input for the master clock frequency to the device. Nominally the MCLK frequency will be $256 \times f_S$ for correct operation of the device. However, if the user's MCLK is a multiple of $256 \times f_S$ (perhaps $512 \times f_S$ or $768 \times f_S$), it is possible to divide down the MCLK frequency to a suitable internal master clock frequency (IMCLK) using the MCLK divider block as shown in Figure 8. The divide options can be chosen from pass-through (/1), /2, or /3 corresponding with $256 \times f_S$, $512 \times f_S$, or $768 \times f_S$ MCLKs, respectively. The MCLK divider can be controlled using the MCD1–MCD0 Bits of Control Register III. (see Table XIII.)

The resulting internal MCLK (IMCLK) is used to run the decimating and filtering engine and must be chosen to be at a ratio of $256 \times f_S$.

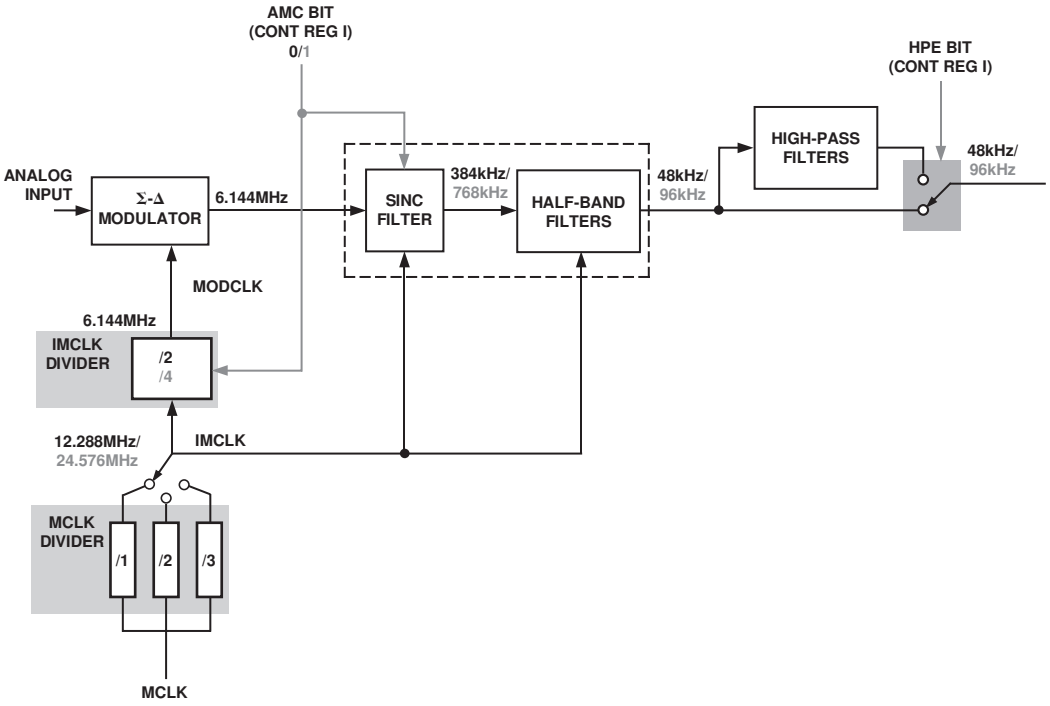


Figure 8. Clocking Scheme to Modulator and Filter Engine

Modulator

The AD1871's analog Σ-Δ modulator section comprises a second order multibit implementation using Analog Device's proprietary technology for best performance. As shown in Figure 9, the two analog integrator blocks are followed by a Flash ADC section that generates the multibit samples. The output of the Flash ADC, which is thermometer encoded, is decoded to binary for output to the filter sections and is scrambled for feedback to the two integrator stages.

The modulator is optimized for operation at a sampling rate of 6.144 MHz (which is $128 \times f_S$ at 48 kHz sampling and $64 \times f_S$ at 96 kHz sampling). The modulator clock control (AMC Bit in Control Register I) is used to select the modulator clock (MODCLK) as a ratio from the IMCLK. The modulator clock divider options are /2 (default) for 48 kHz operation and /4 for 96 kHz operation. When operating with an IMCLK of 12.288 MHz, the default divider setting (/2) gives a modulator clock of 6.144 MHz. When operating with an IMCLK of 24.576 MHz, the alternate divider setting (/4) gives a modulator clock of 6.144 MHz (see Figure 8).

If it is required to operate the device at a different output sample rate than those detailed above, perhaps 44.1 kHz or 88.2 kHz, the decimation filter cutoff characteristics can then be determined from the normalized frequency response plot shown in TPC 6.

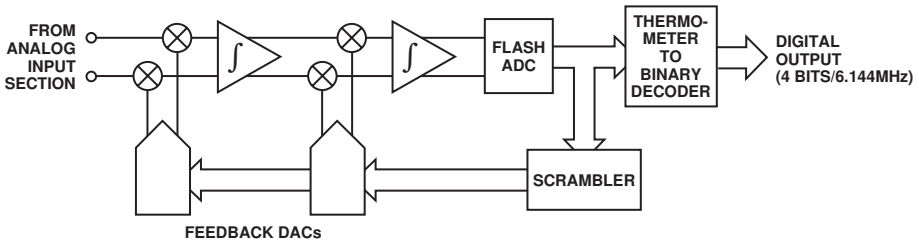


Figure 9. Modulator Block Diagram

Digital Decimating Filters

The filtering and decimation of the AD1871's modulator data stream is implemented in an embedded DSP engine. The first stage of filtering is the sinc filtering, which has selectable decimation (selected by the modulator clock control bit (AMC, see Modulator section). The default decimation in the sinc stage provides a sample rate reduction of 16; this corresponds with a MODCLK rate of $128 \times f_S$. The alternate setting of the AMC Bit gives a sinc decimation factor of 8 that corresponds with a MODCLK rate of $64 \times f_S$. The output of the sinc decimator stage is at a rate of $8 \times f_S$.

The filter engine implements two half-band FIR filter sections and a sinc compensation stage that together give a further decimation factor of 8. Please refer to TPCs 1 through 4 for details on the responses of the sinc and FIR filter sections. TPC 5 gives the composite response of the sinc and FIR filters.

High-Pass Filter

The AD1871 features an optional high-pass filter section that provides the ability of rejecting dc from the output data stream. The high-pass filter is enabled by setting Bit 8 (HPE) of Control Register I to 1. Please refer to TPC 7 and TPC 8 for details of the high-pass filter characteristics.

ADC Coding

The ADC's output data stream is in a two's complement encoded format. The word width can be selected from 16 bits, 20 bits, or 24 bits (see Table VI and Table VII). The coding scheme is detailed in Table I.

Table I. ADC Coding

Code	Level
011111.....1111	+Full Scale
000000.....0000	0 (Ref Level)
100000.....0001	–Full Scale

Analog Input Section

The analog input section comprises a differential PGA stage. It can also be configured for single-ended inputs, allowing two such inputs to be selected via a multiplex switch. The PGA has five gain settings (see Table V) ranging from 0 dB to 12 dB in 3 dB steps.

In Differential Mode, the VINxP and VINxN input pins are connected to a pair of inverting amplifiers whose outputs are connected to the CAPxN and CAPxP pins, respectively. (See Figure 10.)

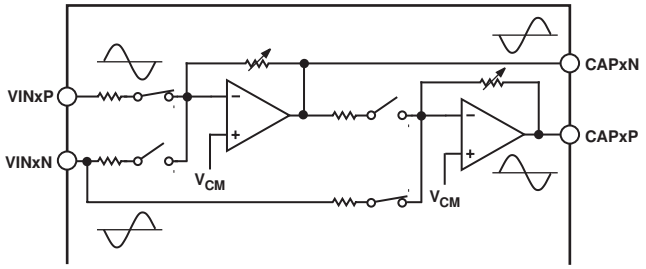


Figure 10. Differential Analog Input

In Single-Ended Mode, either VINxP or VINxN can be selected as the input. The pair of input inverting amplifiers is reconfigured as a single-ended-to-differential conversion stage. Again the outputs of the differential section are connected to Pins CAPxP and CAPxN (see Figure 11).

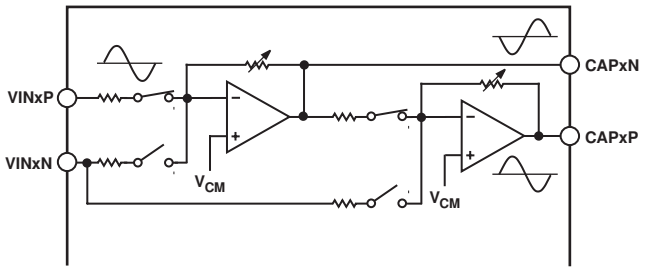


Figure 11. Single-Ended Analog Input

The analog input section is enabled (powered ON) by default on reset. If it is required to bypass the analog input section by using the modulator input pins (CAPxP and CAPxN) directly, then the analog input section must be powered down by setting Bits MER and MEL in Control Register III.

Serial Data Interface

The AD1871's serial data interface consists of three pins (LRCLK, BCLK, and SDATA). LRCLK is the framing signal for left and right channel samples and its frequency is equal to the sampling frequency (f_S). BCLK is the serial clock used to clock the data samples from the AD1871 and its frequency is equal to $64 \times f_S$ (giving 32 BCLK periods for each of the left and right channels). SDATA outputs the left and right channel sample data coincident with the falling edge of BCLK.

The serial data interface supports all the popular audio interface standards, such as I^2S, left-justified (LJ), and right-justified (RJ), as well as the serial interfaces of modern DSPs. The Interface Mode is selected by programming the Bits DF1–DF0 of Control Register II (see Tables VI and VIII).

The data sample width can be selected from 16, 20, or 24 bits by programming Bits WW1–WW0 of Control Register II (see Tables VI and VII).

I²S Mode

In I²S Mode, the data is left-justified, MSB first, with the MSB placed in the second BCLK period following the transition of the LRCLK. A high-to-low transition of the LRCLK signifies the beginning of the left channel data transfer, while a low-to-high transition on the LRCLK signifies the beginning of the right channel data transfer (see Figure 12).

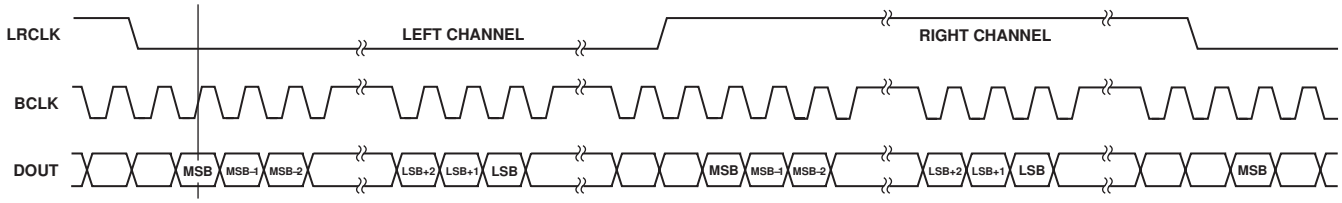


Figure 12. I²S Mode

LJ Mode

In LJ Mode, the data is left-justified, MSB first, with the MSB placed in the first BCLK period following the transition of the LRCLK. A high-to-low transition of the LRCLK signifies the beginning of the right channel data transfer, while a low-to-high transition on the LRCLK signifies the beginning of the left channel data transfer (see Figure 13).

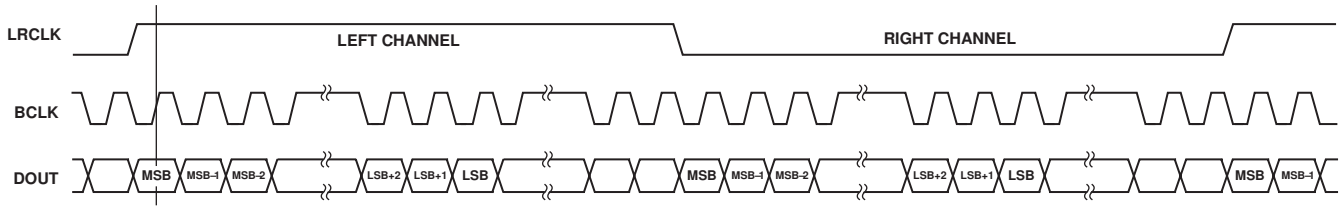


Figure 13. Left-Justified Mode

RJ Mode

In RJ Mode, the data is right-justified, LSB last, with the LSB placed in the last BCLK period preceding the transition of the LRCLK. A high-to-low transition of the LRCLK signifies the beginning of the right channel data transfer, while a low-to-high transition on the LRCLK signifies the beginning of the left channel data transfer (see Figure 14).

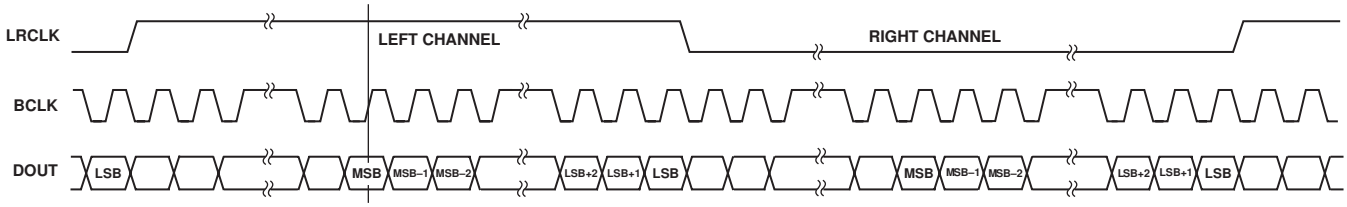


Figure 14. Right-Justified Mode

DSP Mode

In DSP Mode, the LRCLK signal becomes a frame sync signal that pulses high for the BCLK period prior to the MSB (or in the BCLK period of the previous LSB–32 bits). The data is left-justified, MSB first, with the MSB placed in the BCLK period following the LRCLK pulse (see Figure 15).

In I²S and LJ Modes, since the data is left-justified, differences in data word-width between the AD1871 and the controller are not catastrophic since the MSBs are guaranteed to be transferred. There may, however, be a slight reduction in performance depending on the scale of the mismatch. In RJ Mode, however, differences in word-width between the AD1871 and controller have a catastrophic effect on signal performance as the MSBs of each sample may be lost due to the mismatch.

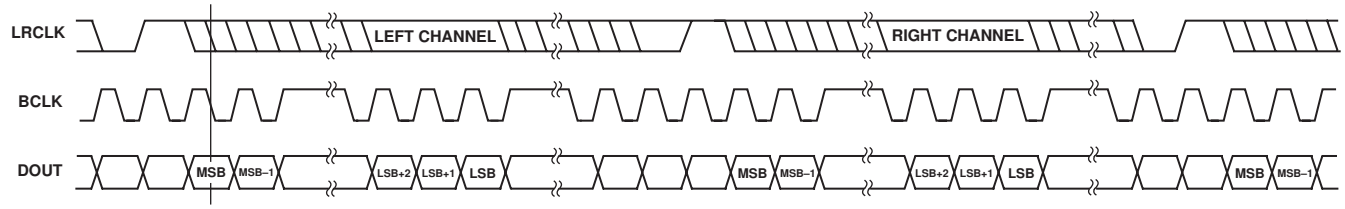


Figure 15. DSP Mode

Cascade Mode

The AD1871 supports cascading of up to four devices in a daisy-chain configuration to the serial port of a DSP. In Cascade Mode, each device loads an internal 64-Bit Shift Register with the results of the left and right channel conversions. The 64-Bit Register is split into two subframes of 32 bits each; the first for left channel data and the second for right channel data. The results are left-justified, MSB first within the subframes, and the word-width setting in Control Register II applies. Remaining bits within the subframe, beyond the conversion word-width, are set to zero. Please refer to Figure 16.

Up to four devices can be connected in a daisy chain as shown in Figure 17. All devices must be set in Cascade Mode by tying the CASC pin of each device to a logic high. The first device in the chain (Device 4) has its DIN pin tied to logic low. Its DOUT pin is connected to the DIN pin of Device 3 whose DOUT is in turn connected to the DIN pin of Device 2. This daisy chaining is continued until the DOUT of Device 1 is connected to the DSP's serial port RX data line (DR0). The DSP's RX serial clock (RXCLK0) is connected to the BCLK pin of all AD1871 devices and the DSP's RX frame sync (RFS0) is connected to the LRCLK pin of all AD1871 devices.

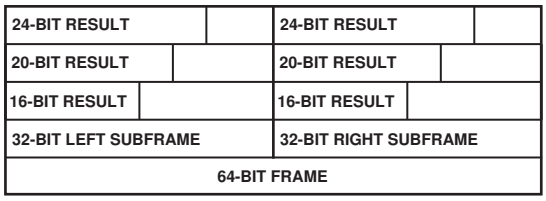


Figure 16. DSP Mode

The DSP can be the master and supply the frame sync and serial clock to the AD1871s, or one of the AD1871s can be set as the master with the DSP and all other AD1871s set to slave. Each sampling period begins with a frame sync being generated either by the DSP or one of the AD1871s, depending on the Master/Slave selection. The frame-sync pulse causes each device to load the 64-Bit Data I/O Register with the left and right ADC results. These results are then clocked toward the DSP where they are received in the following order: Device 1, Left; Device 1, Right; Device 2, Left; Device 2, Right; Device 3, Left; Device 3, Right; Device 4, Left; and Device 4, Right.

The DSP's serial port must be programmed to accept 32-bit word lengths regardless of the AD1871 word length. The number of sample words to be accepted per sample interval will be determined by the number of AD1871 devices in cascade, up to a maximum of eight words corresponding with the maximum number of four devices.

Figure 17 also shows the connection of a separate DSP serial port interface to the control port (SPI) interface of the cascaded AD1871s. Again this cascade is implemented as a daisy chain, where the control words for the four devices are output in sequence (depending on the hookup – 1, 2, 3, and 4 in the example) to be latched simultaneously at each device by the common CLATCH. In this mode, it is necessary to send a control word for each device (16 bits × the number of devices) from the SPI port of the control host. The CLATCH signal can be controlled from a separate programmable output line. It is also possible to have individual read/write of the AD1871s using separate CLATCH controls for each device.

When using Cascade Mode, the data interface defaults to left-justified, MSB first data, regardless of the state of the Interface Mode selection (by SPI or external control).

The timing relationships of the Cascade Mode are shown in Figure 18.

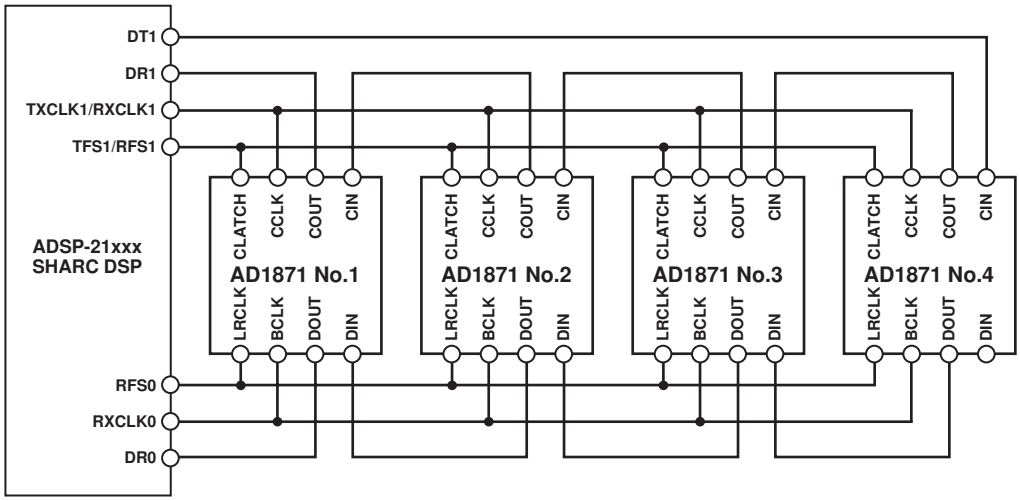


Figure 17. DSP Mode

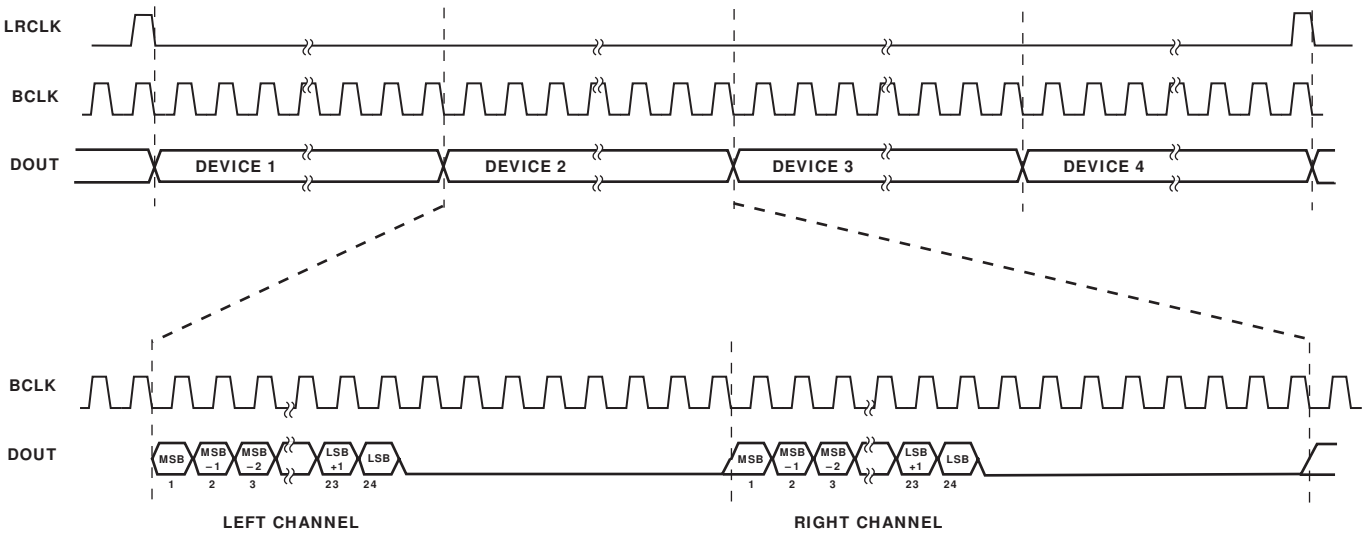


Figure 18. Cascade Mode Data Interface Timing

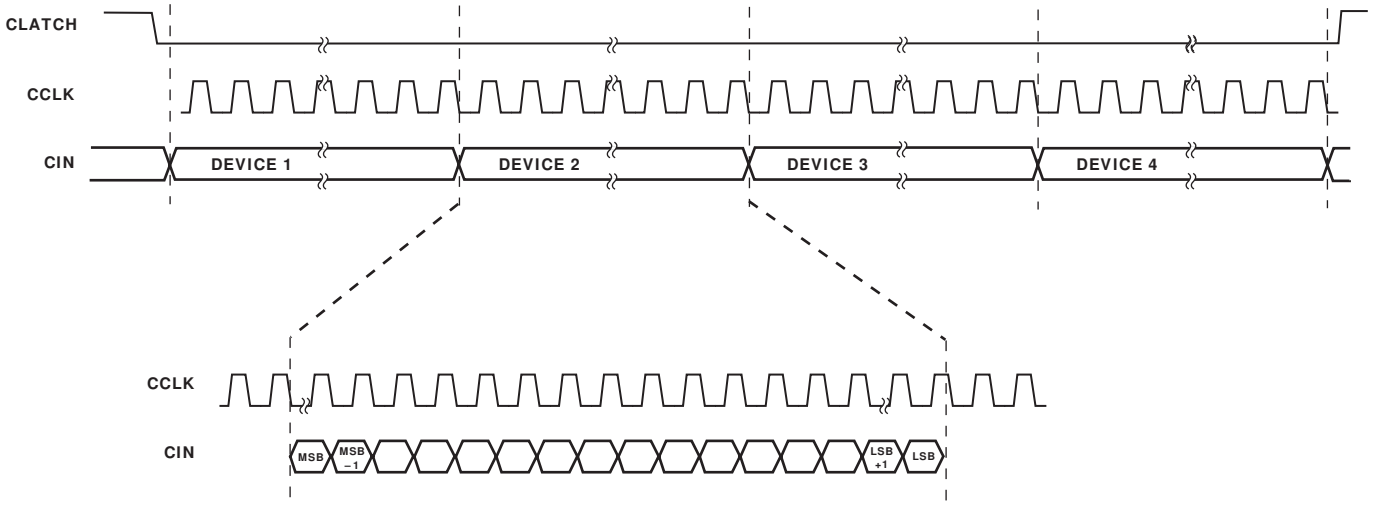


Figure 19. Cascade Mode Control Port Timing

CONTROL/STATUS REGISTERS

The AD1871's Operating Mode is set by programming three, 10-bit Control Registers via an SPI compatible port. Table III details the format of the AD1871 control words, which are 16 bits wide with a 4-bit address field in Positions 15 through 12, a Read/$\overline{\text{Write}}$ Bit in Position 11, a Reserved Bit in Position 10, and 10 bits of register data (corresponding to the control register width) in Positions 9 through 0. The three control words occupy Addresses 0000b through 0010b in the register map (see Table II).

The AD1871 also features two readback (status) registers that can be enabled to track the peak reading on each of the channels (left and right). These 6-bit results are read back via the SPI compatible port in a 16-bit frame similar to that of the control words.

The SPI compatible control port features four signals (CCLK, CLATCH, CDATA, and COUT). The CLATCH signal is an enable line that must be low to allow communication to or from the control port. The CCLK is the serial clock that clocks in serial data via the CDATA pin and clocks out serial data via the COUT pin. Figures 20 and 21 show details of the control port timing.

Table II. Register Address Map

Address	Control Register
0000	Control Register I
0001	Control Register II
0010	Control Register III
0011	Peak Reading Register I
0100	Peak Reading Register II

Table III. Control/Status Word Format

15-12	11	10	9 6 5 4 3 2 1 0
Address	R/$\overline{W}$	Reserved	Control/Status Data Bits (9–0)

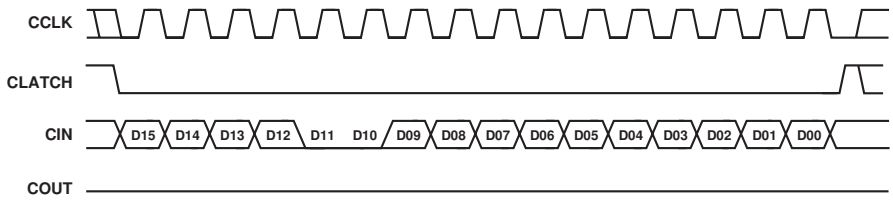


Figure 20. Writing to Register Using Control Port

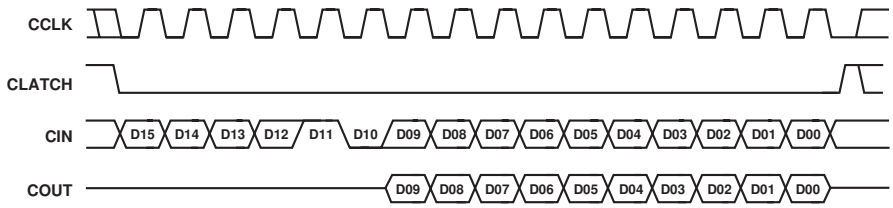


Figure 21. Reading from Register Using Control Port

Table IV. Control Register I (Address 0000b, Write Only)

15–12	11	10	9	8	7	6	5	4	3	2	1	0
0000	0	0	PRE	HPE	PD	AMC	AGL2	AGL1	AGL0	AGR2	AGR1	AGR0

9	PRE	Peak Reading Enable (0 = Disabled (Default); 1 = Enabled)
8	HPE	High-Pass Filter Enable (0 = Disabled (Default); 1 = Enabled)
7	PD	Power-Down Control (1 = Power-Down; 0 = Normal Operation (Default))
6	AMC	ADC Modulator Clock (1 = 64 × f_S; 0 = 128 × f_S (Default))
5–3	AGL2–AGL0	Input Gain (Left Channel, see Table V)
2–0	AGR2–AGL0	Input Gain (Right Channel, see Table V)

Control Register I

Control Register I contains bit settings for control of analog front end gain, modulator clock selection, power-down control, high-pass filtering, and peak hold.

Analog Gain Control

The AD1871 features an optional analog front end with selectable gain. Gain is selected using three control bits for each channel, giving five separate and independent gain settings on each channel. Bits 2 through 0 (AGR2–AGR0) set the analog gain for the right channel, while Bits 5 through 3 (AGL2–AGL0) set the analog gain for the left channel. Table V shows the analog gain corresponding to the bit settings in AGx2–ADx0.

Table V. Analog Gain Settings

AGx2	AGx1	AGx0	Gain (dB)
0	0	0	0 (Default)
0	0	1	3
0	1	0	6
0	1	1	9
1	0	0	12
1	0	1	0
1	1	0	0
1	1	1	0

Modulator Clock
The modulator clock can be chosen to be either $128 \times f_S$ or $64 \times f_S$. The AMC Bit (Bit 6) is used to select the modulator's clock rate. When AMC is set to 0 (default), the modulator clock is $128 \times f_S$. Otherwise, if set to 1, the modulator clock is $64 \times f_S$. This bit is normally set depending on whether the desired sampling frequency is 48 kHz or 96 kHz and is also influenced by the selected MCLK frequency. Please refer to the Functional Description section for more information on MCLK selection and sampling rates.

Power-Down
Power-down of the active clock signals within the AD1871 is effected by writing a Logic 1 to Bit 7 (PD). In Power-Down Mode, digital activity is suspended and analog sections are powered down, with the exception of the reference.

High-Pass Filter
The AD1871's digital filtering engine allows the insertion of a high-pass filter (HPF) to effectively block dc signals from the output digital waveform. Setting Bit 8 (HPE) enables the high-pass filter. For more details of the HPF, refer to the Functional Description section.

Peak Reading Enable
The AD1871 has two readback registers that can be enabled to store the peak readings of the left and right channel ADC results. To enable the peak readings to be captured, the Peak Reading Enable Bit (PRE), Bit 9, must be set to Logic 1. When set to Logic 0, the peak reading capture is disabled.

Table VI. Control Register II (Address 0001b)

15–12	11	10	9	8	7	6	5	4	3	2	1	0
0001	0	0			MME	DF1	DF0	WW1	WW0	$\overline{M}$/S	MUR	MUL

9–8		Reserved
7	MME	Modulator Mode Enable (0 = Normal Mode (Default), 1 = Mod Mode)
6–5	DF1–DF0	Data Format (See Table VIII)
4–3	WW1–WW0	Word Width (See Table VII)
2	$\overline{M}$/S	Master/Slave Select (0 = Master Mode (Default); 1 = Slave Mode)
1	MUR	Mute Control, Right Channel (0 = Disabled (Default); 1 = Enabled)
0	MUL	Mute Control, Left Channel (0 = Disabled (Default); 1 = Enabled)

Control Register II
Control Register II contains bit settings for control of left/right channel muting, data sample word width, data interface format, and direct modulator bitstream output.

Mute Control
The left and right data channels can be muted to digital zero by setting the MUL and MUR Bits (Bits 0 and 1), respectively. If a channel is muted, its output data stream will remain at digital zero, regardless of the amplitude of the input signal. Setting the bit to 1 mutes the channel while setting the bit to 0 restores normal operation.

Master/Slave Select
The AD1871 can operate as either a slave device or a master device. In Slave Mode, the controller must provide the LRCLK and BCLK to determine the sample rate and serial bit rate. In Master Mode, the AD1871 provides the LRCLK and BCLK as outputs that are applied to the controller. The AD1871 defaults to Master Mode ($\overline{M}$/S is low) on reset.

Word Width
The AD1871 allows the output sample word width to be selected from 16, 20, and 24 bits wide. Compact disc (CD) compatibility may require 16 bits, while many modern digital audio formats require 24-bit sample resolution. Bits WW1–WW0 are programmed to select the word width. Table VII details the Control Register Bit settings corresponding to the various word width selections.

Table VII. Word-Width Settings

WW1	WW0	Word Width (No. of Bits)
0	0	24 (Default)
0	1	20
1	0	16
1	1	Reserved

Data Format
The AD1871's serial data interface can be configured from a choice of popular interface formats, including I^2S, left-justified, right-justified, or DSP Modes. Bits DF1–DF0 are programmed to select the interface format (mode) as shown in Table VIII.

Table VIII. Data Interface Format Settings*

DF1	DF0	Interface Mode
0	0	I^2S (Default)
0	1	Right-Justified
1	0	DSP
1	1	Left-Justified

*Please refer to the Serial Data Interface section in the Functional Description for more details on the various interface modes.

Modulator Mode Enable
The AD1871 defaults to the conversion of the analog audio to linear, PCM-encoded digital outputs. Modulator Mode allows the user to bypass the digital decimation filter section and access the multibit sigma-delta modulator outputs directly. When in this mode, certain pins are redefined (see Modulator Mode) and the modulator output (at a nominal rate of $128 \times f_S$) is available on the modulator data pins (D[0–3]). To enable the Modulator Mode, set the MME Bit to high.

Table IX. Control Register III (Address 0010b)

15–12	11	10	9	8	7	6	5	4	3	2	1	0
0010	0	0			MCD1	MCD0	SEL	SER	MEL	MXL	MER	MXR

9–8	Reserved	(Should Be Programmed to 0)
7–6	MCD1–MCD0	Master Clock Divider (See Table XIII)
5	SEL	Single-Ended Enable, Left Channel (0 = Differential (Default); 1 = Single-Ended)
4	SER	Single-Ended Enable, Right Channel (0 = Differential (Default); 1 = Single-Ended)
3	MEL	Mux/PGA Disable, Left Channel (0 = Enabled (Default); 1 = Disabled)
2	MXL	Mux Select, Left Channel (0 = VINLP Selected (Default); 1 = VINLN Selected)
1	MER	Mux/PGA Disable, Right Channel (0 = Enabled (Default); 1 = Disabled)
0	MXR	Mux Select, Right Channel (0 = VINRP Selected (Default); 1 = VINRN Selected)

Control Register III

Control Register III contains bit settings for configuration of the analog input section (both left and right channels).

Mux Enable

The Mux Enable Left (MEL) and Mux Enable Right (MER) are used to enable the analog buffers. When these bits are set to 1, the analog input buffers are powered down and input signals must be applied directly to the modulator inputs via the CAPxP and CAPxN pins. (see Figure 23). When MEL and MER are set to 0 (default condition after reset), the analog input section is enabled, (see Table X).

Table X. Mux Control Settings

MEL	MER	Input Setting
0	X	Left Channel Analog Buffer Enabled
1	X	Left Channel Analog Buffer Disabled
X	0	Right Channel Analog Buffer Enabled
X	1	Right Channel Analog Buffer Disabled

Mux Select

The Mux Select Bits (MXL and MXR for left and right channels, respectively) are used to select the input from VINxP or VINxN when the input is configured as single-ended. When MXx is set to 0, the input is taken from VINxP. When MXx is set to 1, the input is taken from VINxN, (see Table XI).

Table XI. Mux Select Settings*

MXL	MXR	Input Setting
0	X	Left Channel Input from VINLP
1	X	Left Channel Input from VINLN
X	0	Right Channel Input from VINRP
X	1	Right Channel Input from VINRN

*Mux select settings are only valid when single-ended operation is enabled; SEL and SER are set to 1.

Single-Ended Mode Enable

The Single-Ended Mode Enable Bits (SEL and SER for left and right channels, respectively), when set to 1, are used to configure single-ended input on VINxP and VINxN (input is selected by state of MXL and MXR). In this mode, single-ended inputs taken from either VINxP or VINxN (selected using the Mux Select Bits—MXL and MXR) are internally converted to a differential format to be applied to the modulator section (see Table XII).

Table XII. Differential/Single-Ended Select

SEL	SER	Input Setting
0	X	Left Channel Input → Differential
1	X	Left Channel Input → Single-Ended
X	0	Right Channel Input → Differential
X	1	Right Channel Input → Single-Ended

Master Clock Divider

The master clock divider allows the division of the external MCLK frequency to a more suitable internal master clock frequency (IMCLK). IMCLK must be $256 \times f_S$; therefore, if the available MCLK is not at $256 \times f_S$ but is a multiple of this, the MCD allows conversion of MCLK to a suitable IMCLK at $256 \times f_S$ (see Table XIII).

Table XIII. Master Clock Divider Settings

MCD1	MCD0	MCLK Division
0	0	IMCLK = MCLK (/1)
0	1	IMCLK = MCLK/2
1	0	IMCLK = MCLK/3
1	1	IMCLK = MCLK (/1)

Table XIV. Peak Reading Register I (Address 0011b, Read-Only)

15–12	11	10	9	8	7	6	5	4	3	2	1	0
0011	1	0					A0P5	A0P4	A0P3	A0P2	A0P1	A0P0

9–6	Reserved	(Always Set to Zero)
5–0	A0P5–A0P0	Left Channel Peak Reading (Valid Only When PRE = 1)

Table XV. Peak Reading Register II (Address 0100b, Read-Only)

15–12	11	10	9	8	7	6	5	4	3	2	1	0
0100	1	0					A1P5	A1P4	A1P3	A1P2	A1P1	A1P0

9–6	Reserved	(Always Set to Zero)
5–0	A1P5–A1P0	Right Channel Peak Reading (Valid Only When PRE = 1)

Peak Reading Registers

The Peak Reading Registers are read-only registers that can be enabled to track-and-hold the peak ADC reading from each channel. The peak reading feature is enabled by setting Bit PRE in Control Register I. The peak reading value is contained in the six LSBs of the 10-bit readback word. The result is binary coded where each LSB is equivalent to –1 dBFS with all zeros corresponding to full scale (0 dBFS) and all ones corresponding to –63 dBFS (see Table XVI). When Bit PRE is set, the peak reading per channel is stored in the appropriate peak register. Once the register is read, the register value is set to zero and is updated by subsequent conversions.

Table XVI. Peak Reading Result Format

AxP	Code 5	4	3	2	1	0	Level
	0	0	0	0	0	0	0 dBFS
	0	0	0	0	0	1	–1 dBFS
	0	0	0	0	1	0	–2 dBFS
	1	1	1	1	1	0	–62 dBFS
	1	1	1	1	1	1	–63 dBFS

A Peak Reading Register read cycle is detailed in Figure 21.

EXTERNAL CONTROL

The AD1871 can be configured for external hardware control of a subset of the device functionality. This functionality includes $\overline{\text{Master}}$/Slave Mode select, MCLK select, and serial data format select. External control is enabled by tying the XCTRL Pin high as shown in Figure 22.

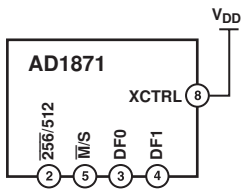


Figure 22. External Control Configuration

$\overline{\text{Master}}$/Slave Select

The $\overline{\text{Master}}$/Slave hardware select (Pin 5, CLATCH/[$\overline{\text{M}}$/S]) is equivalent to setting the $\overline{\text{M}}$/S Bit of Control Register II. If set low, the device is placed in Master Mode, whereby the LRCLK and BCLK signals are outputs from the AD1871.

When $\overline{\text{M}}$/S is set high, the device is in Slave Mode, whereby the LRCK and BCLK signals are inputs to the AD1871.

MCLK Mode Select

The MCLK Mode hardware select (Pin 2, CCLK/[$\overline{256}$/512]) is a subset of the MCLK Mode selection that is determined by Bits CM1–CM0 of Control Register X. When the hardware pin is low, the device operates with an MCLK that is $256 \times f_S$; if the pin is set high, the device operates with an MCLK that is $512 \times f_S$.

Serial Data Format Select

The Serial Data Format hardware select (Pins 3 and 4, DF0/COUT and DF1/CIN) is equivalent to setting Bits DF1–DF0 of Control Register II. See Table VIII.

In External Control Mode, all functions other than those selected by the hardware select pins ($\overline{\text{Master}}$/Slave Mode select, MCLK select, and Serial Data Format select) are in their default (power-on) state.

MODULATOR MODE

When the device is in Modulator Mode (MME Bit is set to 1), the D[0–3] pins are enabled as data outputs, while the COUT pin becomes MODCLK, a high speed sampling clock (nominally at $128 \times f_S$). The MODCLK enables successive data from the left and right channel modulators with left channel modulator data being valid in the low phase of MODCLK, while right channel modulator data is valid under the high phase of MODCLK (see Modulator Mode Timing in Figure 6).

The Modulator Mode is designed to be used for applications such as direct stream digital (DSD) where modulator data is stored directly to the recording media without decimation and filtering to a lower sample rate. DSD is specified at a rate of $64 \times f_S$, whereas the AD1871 outputs at $128 \times f_S$, requiring an intermediate remodulator that downsamples to $64 \times f_S$ and generates a single-bit output steam.