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FEATURES

- 5 V 3-Channel Audio DAC System
- Digital Audio Output (2-Channel or 6-Channel Packed Mode)
- Accepts Sample Rates up to 48 kHz
- 7 Biquad Filter Sections per Channel
- Dual Dynamic Processor with Arbitrary Input/Output Curve and Adjustable Time Constants
- 0 ms to 6 ms Variable Delay/Channel for Speaker Alignment
- Stereo Spreading Algorithm for Phat Stereo™ Effect
- Program RAM Allows Complete New Program Download via SPI Port
- Parameter RAM Allows Complete Control of More Than 200 Parameters via SPI Port
- SPI Port Features Safe-Upload Mode for Transparent Filter Updates
- 2 Control Registers Allow Complete Control of Modes and Memory Transfers
- Differential Output for Optimum Performance
- 112 dB Signal-to-Noise (Not Muted) at 48 kHz Sample Rate (A-Weighted Stereo)
- 70 dB Stop-Band Attenuation
- On-Chip Clickless Volume Control
- Hardware and Software Controllable Clickless Mute
- Digital De-emphasis Processing for 32 kHz, 44.1 kHz, 48 kHz Sample Rates
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S Compatible, and DSP Serial Port Modes
- Auxiliary Digital Input
- Graphical Custom Programming Tools
- 48-Lead LQFP Plastic Package

APPLICATIONS

- 2.0/2.1 Channel Audio Systems (2 Main Channels Plus Subwoofer)
- Multichannel Automotive Sound Systems
- Multimedia Audio
- Mini Component Stereo
- Home Theater Systems (AC-3 Postprocessor)
- Musical Instruments
- In-Seat Sound Systems (Aircraft, Motor Coaches)

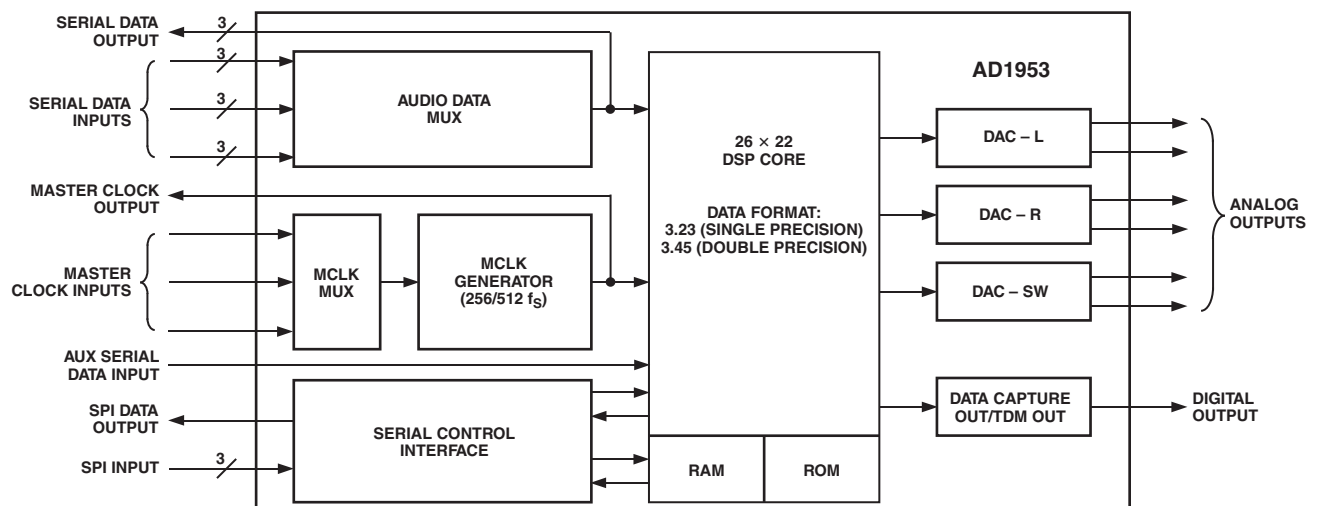
PRODUCT OVERVIEW

The AD1953 is a complete 26-bit, single-chip, 3-channel digital audio playback system with built-in DSP functionality for speaker equalization, dual-band compression/limiting, delay compensation, and image enhancement. These algorithms can be used to compensate for real-world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement of perceived audio quality.

The signal processing used in the AD1953 is comparable to that found in high end studio equipment. Most of the processing is done in full 48-bit double-precision mode, resulting in very good low level signal performance and the absence of limit cycles or idle tones. The compressor/limiter uses a sophisticated two-band algorithm often found in high end broadcast compressors.

(continued on page 9)

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD1953* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-211: The Alexander Current-Feedback Audio Power Amplifier
- AN-620: Using the AD1836 and AD1953 for a 4-In/9-Out Analog System with DSP

Data Sheet

- AD1953: SigmaDSP™ Three-Channel, 26-Bit Signal Processing DAC Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- Firmware Loader for SigmaDSPs

DESIGN RESOURCES

- AD1953 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD1953 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

AD1953

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12/14—Rev. 0 to Rev. A

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4/03—Revision 0: Initial Version

SPECIFICATIONS

TEST CONDITIONS, UNLESS OTHERWISE NOTED.

Supply Voltages (AVDD, DVDD)	5.0 V
Ambient Temperature	25°C
Input Clock	12.288 MHz
Input Signal	1.000 kHz 0 dB Full Scale
Input Sample Rate	48 kHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width	24 Bits
Load Capacitance	2200 pF
Load Impedance	2.74 kΩ
Input Voltage High	2.1 V
Input Voltage Low	0.8 V

ANALOG PERFORMANCE*

Parameter	Min	Typ	Max	Unit
RESOLUTION		24		Bits
SIGNAL-TO-NOISE RATIO (20 Hz to 20 kHz) (Left/Right Output)				
No Filter (Stereo)		109		dB
With A-Weighted Filter		112		dB
DYNAMIC RANGE (20 Hz to 20 kHz, -60 dB Input) (Left/Right Output)				
No Filter		109		dB
With A-Weighted Filter	108	112		dB
TOTAL HARMONIC DISTORTION PLUS NOISE (Left/Right Output)				
$V_O = -0.5$ dB	-93	-100		dB
SIGNAL-TO-NOISE RATIO (20 Hz to 20 kHz) (Subwoofer Output)				
No Filter (Stereo)		104		dB
With A-Weighted Filter		107		dB
DYNAMIC RANGE (20 Hz to 20 kHz, -60 dB Input) (Subwoofer Output)				
No Filter		104		dB
With A-Weighted Filter	104	107		dB
TOTAL HARMONIC DISTORTION PLUS NOISE (Subwoofer Output)				
$V_O = -0.5$ dB	-90	-96		dB
ANALOG OUTPUTS				
Differential Output Range (\pm Full Scale) (Left/Right Output)		2.72		V p-p
Differential Output Range (\pm Full Scale) (Subwoofer Output)		2.79		V p-p
CMOUT		2.50		V
DC ACCURACY				
Gain Error (Left/Right Channel)	-5		+5	%
Gain Error (Subwoofer Channel)	-8		+8	%
Interchannel Gain Mismatch	-0.250		+0.250	dB
Gain Drift		150		ppm/°C
DC Offset	-35		+35	mV
INTERCHANNEL CROSSTALK (EIAJ Method)		-120		dB
INTERCHANNEL PHASE DEVIATION		± 0.1		Degrees
MUTE ATTENUATION		-107		dB
DE-EMPHASIS GAIN ERROR			± 0.1	dB

*Performance of right and left channels is identical (exclusive of the Interchannel Gain Mismatch and Interchannel Phase Deviation specifications).
Specifications subject to change without notice.

AD1953

DIGITAL I/O

Parameter	Min	Typ	Max	Unit
Input Voltage High (V_{IH})	2.1			V
Input Voltage High (V_{IH}) – RESETB	2.25			V
Input Voltage Low (V_{IL})			0.8	V
Input Leakage (I_{IH} @ $V_{IH} = 2.1$ V)			10	μ A
Input Leakage (I_{IL} @ $V_{IL} = 0.8$ V)			10	μ A
High Level Output Voltage (V_{OH}), $I_{OH} = 2$ mA	DVDD – 0.5			V
Low Level Output Voltage (V_{OL}), $I_{OL} = 2$ mA			0.4	V
Input Capacitance			20	pF

Specifications subject to change without notice.

POWER

Parameter	Min	Typ	Max	Unit
SUPPLIES*				
Voltage: Analog, and Digital	4.5	5	5.5	V
Analog Current		42	48	mA
Analog Current, Power-Down		40	46	mA
Digital Current		66	76	mA
Digital Current, SPI Power-Down		6	10	mA
Digital Current, Reset Power-Down		54	62	mA
DISSIPATION				
Operation, Both Supplies		540		mW
Operation, Analog Supplies		210		mW
Operation, Digital Supplies		330		mW
SPI Power-Down, Both Supplies		230		mW
Reset Power-Down, Both Supplies		470		mW
POWER SUPPLY REJECTION RATIO				
1 kHz 300 mV p-p Signal at Analog Supply Pins		–80		dB
20 kHz 300 mV p-p Signal at Analog Supply Pins		–80		dB

*ODVDD current is dependent on load capacitance and clock rate.

Specifications subject to change without notice.

TEMPERATURE RANGE

Parameter	Min	Typ	Max	Unit
Specifications Guaranteed		25		$^{\circ}$ C
Functionality Guaranteed	–40		+105	$^{\circ}$ C
Storage	–55		+125	$^{\circ}$ C

Specifications subject to change without notice.

DIGITAL TIMING

Parameter	Min	Typ	Max	Unit
t _{DMD}	45		55	%
t _{DMD}	40		60	%
t _{DMD}			25	ns
t _{DBH}	10			ns
t _{DBH}	10			ns
t _{DBD}			25	ns
t _{DLS}	0			ns
t _{DLH}	10			ns
t _{DLD}			25	ns
t _{DDS}	0			ns
t _{DDH}	10			ns
t _{DDD}			25	ns
t _{TFS}			35	ns
t _{TBS}			35	ns
t _{TOS}			5	ns
t _{CCL}	12			ns
t _{CCH}	12			ns
t _{CLS}	10			ns
t _{CLH}	10			ns
t _{CLD}	10			ns
t _{CDS}	0			ns
t _{CDH}	10			ns
t _{COD}			35	ns
t _{COH}	2			ns
t _{DCD}			35	ns
t _{DCH}	2			ns
t _{PDRP}	5			ns

Specifications subject to change without notice.

DIGITAL FILTER CHARACTERISTICS at 44.1 kHz

Parameter	Min	Typ	Max	Unit
Pass-Band Ripple			±0.01	dB
Stop-Band Attenuation		70		dB
Pass Band		20		kHz
Stop Band		$0.4535 \times f_s$		kHz
		24		kHz
Group Delay		$0.5442 \times f_s$		sec
		$24.625/f_s$		sec

Specifications subject to change without notice.

AD1953

ABSOLUTE MAXIMUM RATINGS*

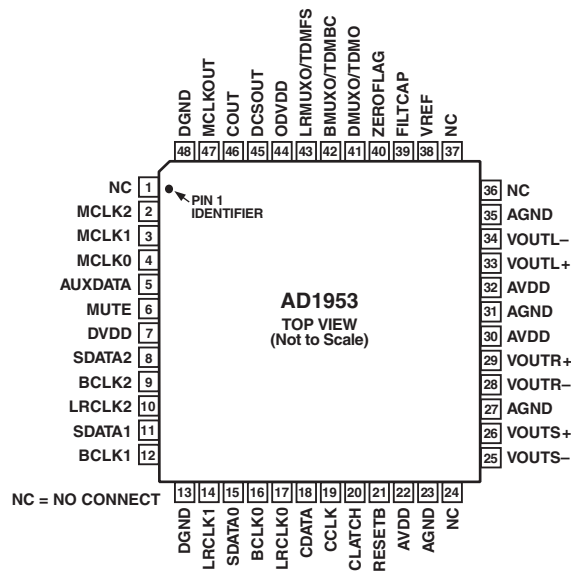
DVDD to DGND	−0.3 V to +6 V
ODVDD to DGND	−0.3 V to +6 V
AVDD to AGND	−0.3 V to +6 V
Digital Inputs	DGND − 0.3 V to DVDD + 0.3 V
Analog Inputs	AGND − 0.3 V to AVDD + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Reference Voltage	(AVDD + 0.3)/2 V
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Soldering	300°C/10 sec

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Characteristics (48-Lead LQFP)

	Min	Typ	Max	Unit
θ_{JA} (Thermal Resistance [Junction-to-Ambient])		76		°C/W
θ_{JC} (Thermal Resistance [Junction-to-Case])		17		°C/W

PIN CONFIGURATION 48-Lead LQFP



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1953 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



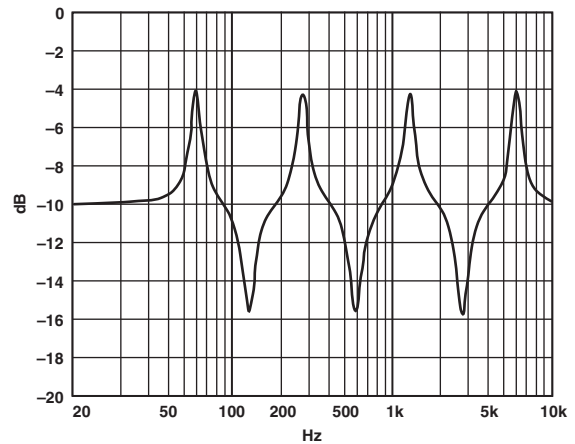
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Input/ Output	Description
1	NC		No Connect
2	MCLK2	IN	Master Clock Input 2 256/512 f_s
3	MCLK1	IN	Master Clock Input 1 256/512 f_s
4	MCLK0	IN	Master Clock Input 0 256/512 f_s
5	AUXDATA	IN	Auxiliary Serial Data Input
6	MUTE	IN	Mute Signal, Initiates Volume Ramp-Down
7	DVDD		Digital Supply for DSP Core, 4.5 V to 5.5 V
8	SDATA2	IN	Serial Data Input 2
9	BCLK2	IN	Bit Clock 2
10	LRCLK2	IN	Left/Right Clock 2
11	SDATA1	IN	Serial Data Input 1
12	BCLK1	IN	Bit Clock 1
13	DGND		Digital Ground
14	LRCLK1	IN	Left/Right Clock 1
15	SDATA0	IN	Serial Data Input 0
16	BCLK0	IN	Bit Clock 0
17	LRCLK0	IN	Left/Right Clock 0
18	CDATA	IN	SPI Data Input
19	CCLK	IN	SPI Data Bit Clock
20	CLATCH	IN	SPI Data Framing Signal
21	RESETB	IN	Reset Signal, Active Low
22	AVDD		Analog 5 V Supply
23	AGND		Analog GND
24	NC		No Connect
25	VOUTS-	OUT	Negative Sub Analog DAC Output
26	VOUTS+	OUT	Positive Sub Analog DAC Output
27	AGND		Analog GND
28	VOUTR-	OUT	Negative Left Analog DAC Output
29	VOUTR+	OUT	Positive Left Analog DAC Output
30	AVDD		Analog 5 V Supply
31	AGND		Analog GND
32	AVDD		Analog 5 V Supply
33	VOUTL+	OUT	Positive Left Analog DAC Output
34	VOUTL-	OUT	Negative Left Analog DAC Output
35	AGND		Analog GND
36	NC		No Connect
37	NC		No Connect
38	VREF	IN	Connection for Filtered AVDD/2
39	FILTCAP	IN	Connection for Noise Reduction Capacitor
40	ZEROFLAG	OUT	Zero Flag Output. High when both left and right channels are 0 for 1024 frames.
41	DMUXO/TDMO	OUT	Dual-function Pin: Serial Data MUX Output/TDM Mode Output Data
42	BMUXO/TDMBC	OUT	Dual-function Pin: Bit Clock MUX Output/TDM Mode Bit Clock Output (256 f_s)
43	LRMUXO/TDMFS	OUT	Dual-function Pin: Left/Right Clock MUX Output/TDM Mode Frame Sync Clock Output
44	ODVDD		Digital Supply Pin for Output Drivers, 2.5 V to 5.5 V
45	DCSOUT	OUT	Data Capture Serial Output for Data Capture Registers. Use in conjunction with selected LRCLK and BCLK to form a 3-wire output.
46	COUT	OUT	SPI Data Output, Three-States when Inactive
47	MCLKOUT	OUT	Master Clock Output 512/256 f_s (Frequency Selected by SPI Register)
48	DGND		Digital Ground

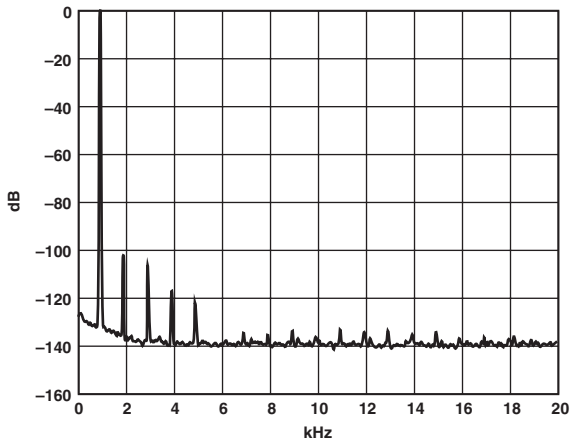
AD1953—Typical Performance Characteristics

PERFORMANCE PLOTS

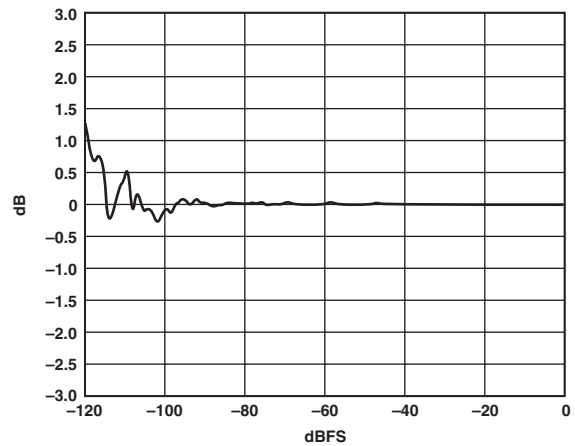
The following plots demonstrate the performance achieved on the actual silicon. TPC 1 shows an FFT of a full-scale 1 kHz signal with a THD+N of -100 dB, which is dominated by a second harmonic. TPC 2 shows an FFT of a -60 dB sine wave, demonstrating the lack of low level artifacts. TPC 3 shows a frequency response plot with the seven equalization biquads set to an alternating pattern of 6 dB boosts and cuts. TPC 4 shows a linearity plot, where the measurement was taken with the same equalization curve used to make TPC 3. When the biquad filters are not in use, the signal passes through the filters with no quantization effects. TPC 4 therefore demonstrates that using double-precision math in the biquad filters has virtually eliminated any quantization artifacts. TPC 5 shows a tone-burst applied to the compressor, with the attack and recovery characteristics plainly visible. The rms detector was programmed for normal rms time constants; the hold/decay feature was not used for this plot.



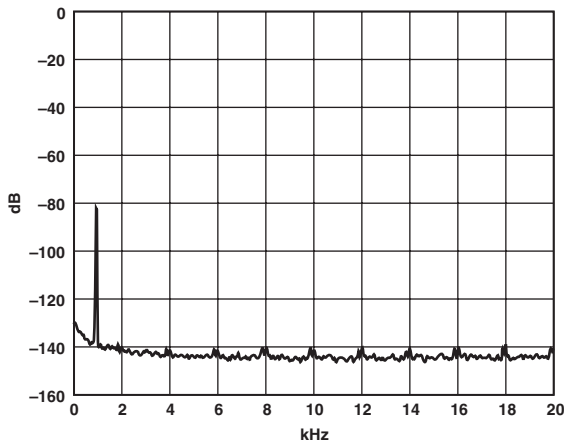
TPC 3. Frequency Response of EQ Biquad Filters



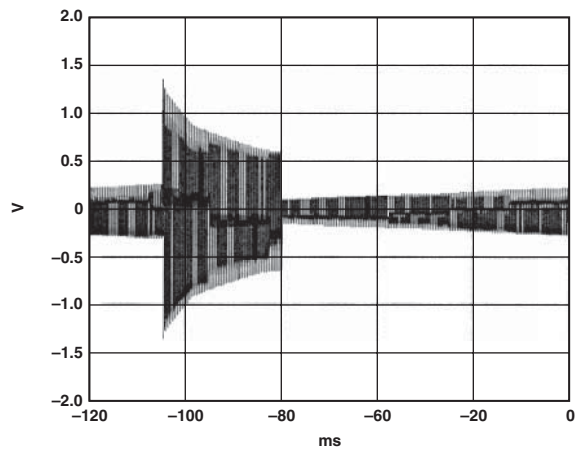
TPC 1. FFT of Full-Scale Sine Wave (32k Points)



TPC 4. Linearity Plot



TPC 2. FFT of -60 dB Sine Wave (32k Points)



TPC 5. Tone-Burst Response with Compressor Threshold Set to -20 dB

PRODUCT OVERVIEW *(continued from page 1)*

An extensive SPI port allows click-free parameter updates, along with readback capability from any point in the algorithm flow.

The AD1953 also includes ADI's patented multibit Σ - Δ DAC architecture. This architecture provides 112 dB SNR and dynamic range and THD+N of -100 dB. These specifications allow the AD1953 to be used in applications ranging from low end boom-boxes to high end professional mixing/editing systems.

The AD1953 has a digital output that allows it to be used purely as a DSP. This digital output can also be used to drive an external DAC to extend the number of channels beyond the three that are provided on the chip. This chip can be used with either its default signal processing program or with a custom user-designed program. Graphical programming tools are available from ADI for custom programming.

Features

The AD1953 is comprised of a 26-bit DSP (48-bit with double-precision) for interpolation and audio processing, three multibit Σ - Δ modulators, and analog output drive circuitry. Other features include an on-chip parameter RAM using a "safe-upload" feature for transparent and simultaneous updates of filter coefficients. Digital de-emphasis filters are also included. On-chip input selectors allow up to three sources of serial data and master clock to be selected. The 3-channel configuration is especially useful for 2.1 playback systems that include two satellite speakers and a subwoofer. The default program allows for independent equalization and compression/limiting for the satellite and subwoofer outputs. Figure 1 shows the block diagram of the device.

The AD1953 contains a program RAM that is booted from an internal program ROM on power-up. Signal-processing parameters are stored in a 256-location parameter RAM, which is initialized on power-up by an internal boot ROM. New values are written to the parameter RAM using the SPI port. The values stored in the parameter RAM control the IIR equalization filters, the dual-band compressor/limiter, the delay values, and the settings of the stereo spreading algorithm.

The AD1953 has a very sophisticated SPI port that supports complete read/write capability of both the program RAM and the parameter RAM. Two control registers are also provided to control the chip serial modes and various other optional features. Handshaking is included for ease of memory uploads/downloads.

The AD1953 contains eight independent data-capture circuits that can be programmed to tap the signal flow of the processor at any point in the DSP algorithm flow. Two of these data-capture circuits can be read back over the SPI port, and the other six are fed to a serial output pin operating either in TDM mode (for all six channels) or 2-channel mode for simple connection to an external DAC. This allows the basic functionality of the AD1953 to be easily extended.

The processor core in the AD1953 has been designed from the ground up for straightforward coding of sophisticated compression/limiting algorithms. The AD1953 contains two independent compressor/limiters with rms based amplitude detection and attack/hold/release controls, together with an arbitrary compression curve that is loaded by the user into a lookup table that resides in the parameter RAM. The compressor also features look-ahead compression, which prevents compressor overshoots.

The AD1953 has a very flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSP chips, AES/EBU receivers, and sample rate converters. The AD1953 can be configured in left-justified, I²S, right-justified, or DSP serial port compatible modes. It can support 16, 20, and 24 bits in all modes. The AD1953 accepts serial audio data in MSB first, twos complement format. The part can also be set up in a 4-channel serial input mode by simultaneously using the serial input mux and the auxiliary serial input.

The AD1953 operates from a single 5 V power supply. It is fabricated on a single monolithic integrated circuit and is housed in a 48-lead LQFP package for operation over the temperature range -40°C to $+105^{\circ}\text{C}$.

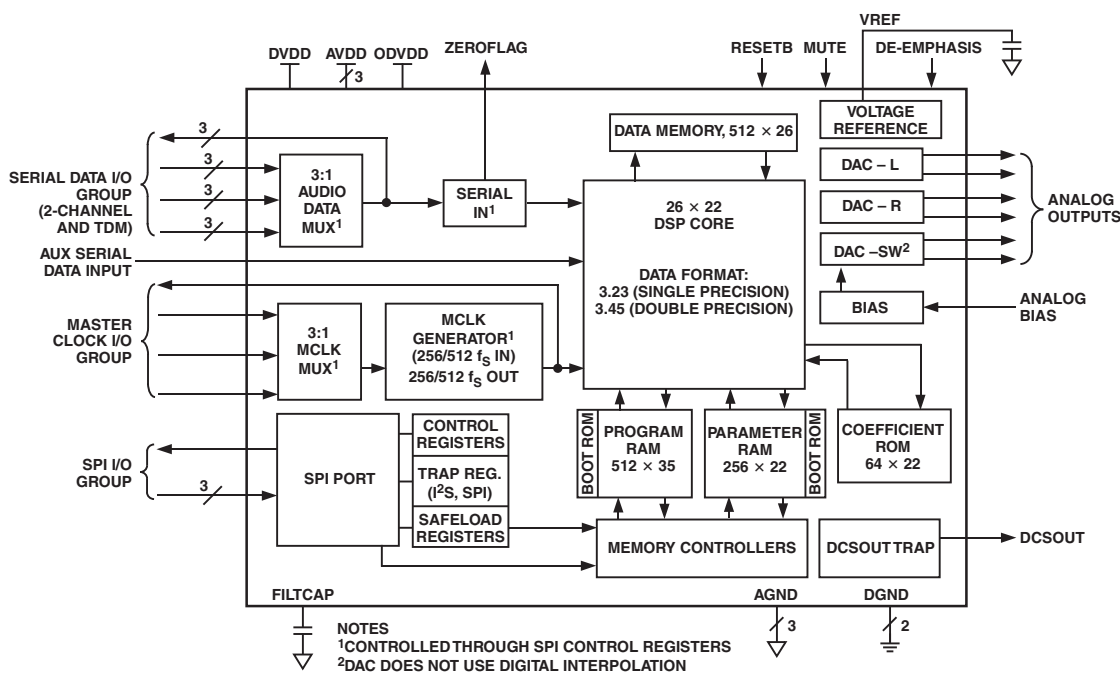


Figure 1. Block Diagram

AD1953

Pin Functions

All input pins have a logic threshold compatible with TTL input levels, and may therefore be used in systems with 3.3 V logic.

All digital output levels are controlled by the ODVDD pin, which may range from 2.7 V to 5.5 V, for compatibility with a wide range of external devices. (See Pin Function Descriptions.)

SDATA0, 1, 2—Serial Data Inputs.

One of these three inputs is selected by an internal MUX, set by writing to Bits <7:6> in Control Register 2. Default is 00, which selects SDATA0. The serial format is selected by writing to Bits <3:0> of Control Register 0. See SPI Read/Write Data Formats section for recommendations on how to change input sources without causing a click or pop noise.

LRCLK0, 1, 2—Left/Right Clocks for Framing the Input Data.

The active LRCLK input is selected by writing to Bits <7:6> in Control Register 2. Default is 00, which selects LRCLK0. The interpretation of the LRCLK changes according to the serial mode, set by writing to Control Register 0.

BCLK0, 1, 2—Serial Bit Clocks for Clocking in the Serial Data.

The active BCLK input is selected by writing to Bits <7:6> in Control Register 2. Default is 00, which selects BCLK0. The interpretation of BCLK changes according to the serial mode, which is set by writing to Control Register 0.

DMUXO/TDMO, LRMUXO/TDMFS, BMUXO/TDMBC

Dual-function pins:

- Function 1: Outputs of 3:1 MUX that selects one of the three serial input groups.
- Function 2: Used for 6-channel data capture outputs in TDM Data Capture Mode.

These three pins operate as MUX outputs when Bit <8> of Control Register 2 is a 1 and Bits <13:12> of Control Register 1 are 00. These pins may be used to send the selected serial input signals to other external devices. The default is OFF.

In TDM mode, TDMBC provides a $256 \times f_s$ clock signal, TDMFS provides a frame sync signal, and TDMO provides the TDM data for an external multichannel DAC or CODEC, such as the AD1833 or AD1836 respectively. These output pins are enabled by writing a 01 to Bits <13:12> of Control Register 1. The default mode is 00, or OFF.

In TDM mode, the internal signals that are captured are controlled by writing Program Counter Trap numbers to SPI addresses 268 to 273. When the internal Program Counter contents are equal to the Trap values written to the SPI port, the selected DSP register is transferred to parallel-to-serial registers and shifted out of the TDMO pin.

MCLK0, 1, 2—Master Clock Inputs.

Active input selected by writing to Bits <5:4> of Control Register 2. The default is 00, which selects MCLK0. The master clock frequency must be either $256 \times f_s$ or $512 \times f_s$, where f_s is the input sampling rate. The master clock frequency is programmed by writing to Bit <2> of Control Register 2. The default is 0, ($512 \times f_s$). See Initialization section for recommendations concerning how to change clock sources without causing an audio click or pop. Note that since the default MCLK source pin is MCLK0, there must be a clock signal present on this pin on power-up so that the AD1953 can complete its initialization routine.

MCLKO—Master Clock Output.

The master clock output pin may be programmed to produce either $256 \times f_s$, $512 \times f_s$, or a copy of the selected MCLK input pin. This pin is programmed by writing to Bits <1:0> of Control Register 2. The default is 00, which disables the MCLKO pin.

CDATA—Serial Data In for the SPI Control Port.

See SPI Port section for more information on SPI port timing.

COUT—Serial Data Output.

This is used for reading back registers and memory locations. It is three-stated when an SPI read is not active. See SPI Port section for more information on SPI port timing.

CCLK—SPI Bit Rate Clock.

This pin either may run continuously or be gated off between SPI transactions. See SPI Port section for more information on SPI port timing.

CLATCH—SPI Latch Signal.

This pin must go LOW at the beginning of an SPI transaction, and HIGH at the end of a transaction. Each SPI transaction may take a different number of CCLKs to complete, depending on the address and read/write bit that are sent at the beginning of the SPI transaction. Detailed SPI timing information is given in the SPI Port section.

RESETB—Active-Low Reset Signal.

After RESETB goes HIGH, the AD1953 goes through an initialization sequence where the program and parameter RAMs are initialized with the contents of the on-board boot ROMs. All SPI registers are set to 0, and the data RAMs are also zeroed. The initialization is complete after 1024 MCLK cycles. Since the MCLK IN FREQ SELECT (Bit <2> in Control Register 2) defaults to $512 \times f_s$ at power-up, this initialization will proceed at the external MCLK rate and will take 1024 MCLK cycles to complete, regardless of the absolute frequency of the external MCLK. New values should not be written to the SPI port until the initialization is complete.

ZEROFMAG—Zero-Input Indicator.

This pin will go HIGH if both serial inputs have been inactive (zero data) for 1024 LRCLK cycles. This pin may be used to drive an external mute FET for reduced noise during digital silence. This pin also functions as a test out pin, controlled by the test register at SPI address 511. While most test modes are not useful to the end user, one may be of some use. If the test register is programmed with the number 7 (decimal), the ZEROFMAG output will be switched to the output of the internal pseudo-random noise generator. This noise generator operates at a bit rate of $128 \times f_s$, and has a repeat time of once per 2^{24} cycles. This mode may be used to generate white noise (or, with appropriate filtering, pink noise) to be used as a test signal for measuring speakers or room acoustics.

DCSOUT—Data Capture Serial Out.

This pin will output the DSP's internal signals, which can be used by external DACs or other signal-processing devices. The signals that are captured and output on the DCSOUT pin are controlled by writing Program Counter Trap numbers to SPI addresses 263 (for the left output) and 264 (for the right output). When the internal Program Counter contents are equal to the Trap values written to the SPI port, the selected DSP register is transferred to the DCSOUT parallel-to-serial registers and

shifted out on the DCSOUT pin. Table XXI shows the Program Counter Trap values and register-select values that should be used to tap various internal points of the algorithm flow.

The DCSOUT pin is meant to be used in conjunction with the LRCLK and BCLK signals that are provided to the serial input port. The format of DCSOUT is the same as the format used for the serial port. In other words, if the serial port is running in I²S mode, then the DCSOUT pin, together with the LRCLK0 and BCLK0 pins (assuming input 0 is selected), will form a valid 3-wire I²S output.

The DCSOUT pin can be used for a variety of purposes. If the DCSOUT pin is used to drive another external DAC, then a 4.1 system is possible using a new program downloaded into the program RAM.

AUXDATA—Auxiliary Serial Data Input.

The AUXDATA pin may be used in conjunction with a custom program to access two extra channels of serial input data, allowing for a total of four input channels. The serial format is identical to the selected format of SDATA0, 1, 2. The AUXDATA pin is synchronous to the selected LRCLK and BCLK signal, and therefore should have the same timing as the main serial input signal.

MUTE—Mute Output Signal.

When this pin is asserted HIGH, a ramp sequence is started that gradually reduces the volume to zero. When deasserted, the volume ramps from zero back to the original volume setting. The ramp speed is timed so that it takes 10 ms to reach zero volume when starting from the default 0 dB volume setting.

VOUTL+, VOUTL-—Left-Channel Differential Analog Outputs. Full-scale outputs correspond to 1 V rms on each output pin, or 2 V rms differential, assuming a VREF input voltage of 2.5 V. The full-scale swing scales directly with VREF. These outputs are capable of driving a load of > 5 k Ω , with a maximum peak current of 1 mA from each pin. An external third-order filter is recommended for filtering out-of-band noise.

VOUTR+, VOUTR-—Right Channel Differential Outputs. Output characteristics are the same as for VOUTL+ and VOUTL-.

VOUTS+, VOUTS-—Sub Channel Differential Outputs.

These outputs are designed to drive loads of 10 k Ω or greater, with a peak current capability of 250 μ A. This output does not use digital interpolation, as it is intended for low frequency application. An external third-order filter with a cutoff frequency < 2 kHz is recommended.

VREF—Analog Reference Voltage Input.

The nominal VREF input voltage is 2.5 V; the analog gain scales directly with the voltage on this pin. When using the AD1953 to drive a power amplifier, it is recommended that the VREF voltage be derived by dividing down and heavily filtering the supply to the power amplifier. This provides a benefit if the compressor/limiter in the AD1953 is used to prevent amplifier clipping. In this case, if the DAC output voltage is scaled to the amplifier power supply, a fixed compressor threshold can be used to protect an amplifier whose supply may vary over a wide range. Any ac signal on this pin will cause distortion, and a large decoupling capacitor may therefore be necessary to ensure that the voltage on VREF is clean. The input impedance of VREF is greater than 1 M Ω .

FILTCAP—Filter Capacitor Point.

This pin is used to reduce the noise on an internal biasing point in order to provide the highest performance. It may not be necessary to connect this pin, depending on the quality of the layout and grounding used in the application circuit.

DVDD—Digital VDD for Core.
5 V nominal.

ODVDD—Digital VDD for All Digital Outputs.
Variable from 2.7 V to 5.5 V.

DGND (2)—Digital Ground.

AVDD (3)—Analog VDD.
5 V nominal. For best results, use a separate regulator for AVDD. Bypass capacitors should be placed close to the pins and connected directly to the analog ground plane.

AGND (3)—Analog Ground.
For best performance, separate nonoverlapping analog and digital ground planes should be used.

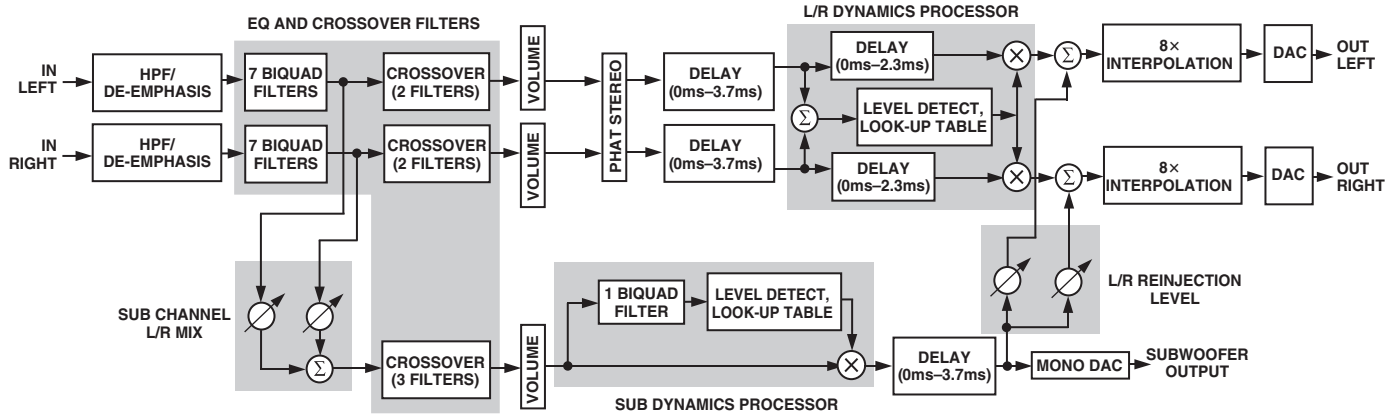


Figure 2. Signal Processing Flow

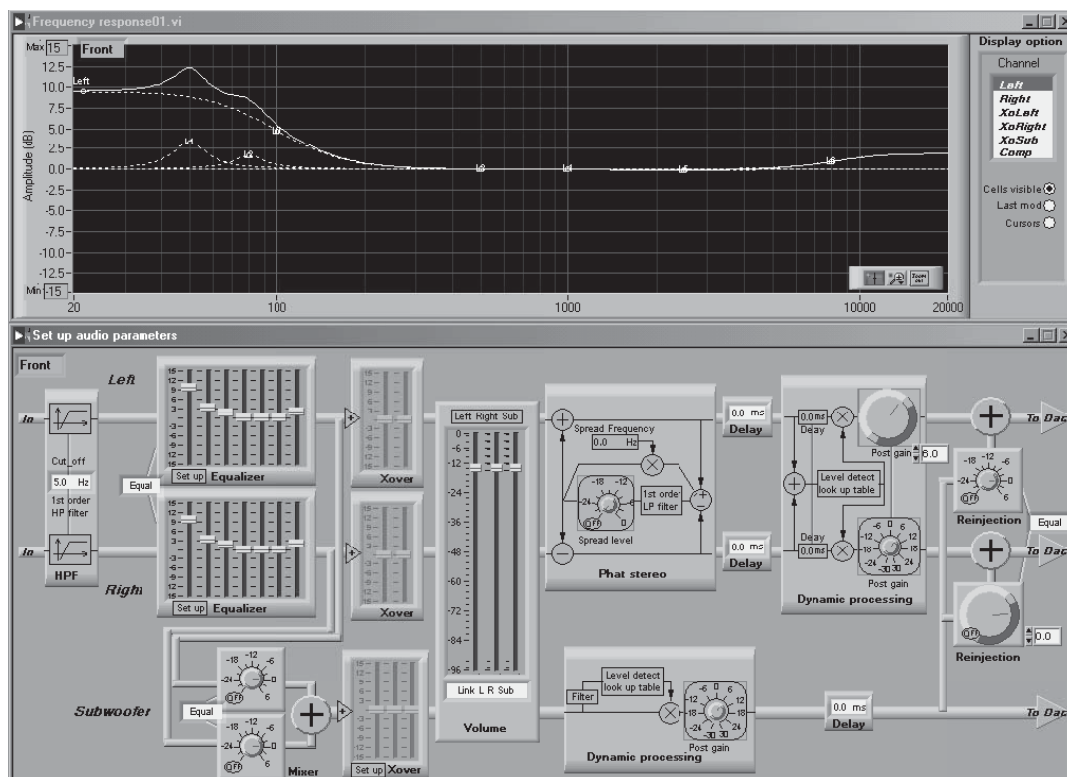


Figure 3. Graphical User Interface

SIGNAL PROCESSING

Signal Processing Overview

Figure 2 shows the signal processing flow diagram of the AD1953. The AD1953 is designed to provide all common signal-processing functions commonly used in 2.0 or 2.1 playback systems. A 7-biquad equalizer operates on the stereo input signal. The output of this equalizer is fed to a 2-biquad crossover filter for the main channels, and the mono sum of the left and right equalizer outputs is fed to a 3-biquad crossover filter for the Sub channel. Each of the three channels has independent delay compensation. There are two high quality compressor/limiters available: one operating on the left/right outputs and one operating on the subwoofer channel. The subwoofer output may be blended back into the left/right outputs for 2.0 playback systems. In this configuration, the two independent compressor/limiters provide 2-band compression, which significantly improves the sound

quality of compressed audio. In addition, the main channels have a stereo widening algorithm that increases the perceived spread of the stereo image.

Most of the signal processing functions are coded using full 48-bit double-precision arithmetic. The input word length is 24 bits, with two extra headroom bits added in the processor to allow internal gains up to 12 dB without clipping (additional gains can be accommodated by scaling down the input signal in the first biquad filter section).

A graphical user interface (GUI) is available for evaluation of the AD1953 (Figure 3). This GUI controls all of the functions of the chip in a very straightforward and user-friendly interface. No code needs to be written to use the GUI to control the chip. For more information on AD1953 software tools, visit, www.analog.com/SigmaStudio.

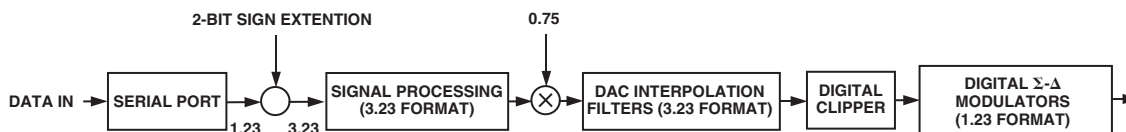


Figure 4. Numeric Precision and Clipping Structure

Each section of this flow diagram will be explained in detail on the following pages.

Numeric Formats

It is common in DSP systems to use a standardized method of specifying numeric formats. To better comprehend issues relating to precision and overflow, it is helpful to think in terms of fractional twos complement number systems. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point. In a twos complement system, there is also an implied offset of one-half of the binary range; for example, in a twos complement 1.23 system, the legal signal range is -1.0 to $(+1.0 - 1 \text{ LSB})$.

The AD1953 uses two different numeric formats; one for the coefficient values (stored in the parameter RAM) and one for the signal data values. The coefficient format is as follows:

Coefficient Format

Coefficient format: 2.20

Range: -2.0 to $(+2.0 - 1 \text{ LSB})$

Examples:

10000000000000000000000000000000 = -2.0

11000000000000000000000000000000 = -1.0

11111111111111111111111111111111 = (1 LSB below 0.0)

00000000000000000000000000000000 = 0.0

01000000000000000000000000000000 = 1.0

01111111111111111111111111111111 = $(2.0 - 1 \text{ LSB})$

This format is used because standard biquad filters require coefficients that range between $+2.0$ and -2.0 . It also allows gain to be inserted at various places in the signal path.

Internal DSP Signal Data Format

Input data format: 1.23

This is sign-extended when written to the data memory of the AD1953.

Internal DSP signal data format: 3.23

Range: -4.0 to $(+4.0 - 1 \text{ LSB})$

Examples:

10000000000000000000000000000000 = -4.0

11000000000000000000000000000000 = -2.0

11100000000000000000000000000000 = -1.0

11111111111111111111111111111111 = (1 LSB below 0.0)

00000000000000000000000000000000 = 0.0

00100000000000000000000000000000 = 1.0

01000000000000000000000000000000 = 2.0

01111111111111111111111111111111 = $(4.0 - 1 \text{ LSB})$.

The sign-extension between the serial port and the DSP core allows for up to 12 dB of gain in the signal path without internal clipping. Gains greater than 12 dB can be accommodated by scaling the input down in the first biquad filter, and scaling the signal back up at the end of the biquad filter section.

A digital clipper circuit is used between the output of the DSP core and the input to the DAC Σ - Δ modulators to prevent overloading the DAC circuitry (see Figure 4). Note that there is a gain factor of 0.75 used in the DAC interpolation filters, and therefore signal values of up to $1/0.75$ will pass through the DSP without clipping. Since the DAC is designed to produce an analog output of 2 V rms (differential) with a 0 dB digital input, signals between 0 dB and $1/0.75$ (approximately 3 dB) will produce larger analog outputs and result in slightly degraded analog performance. This extra analog range is necessary in order to pass 0 dBFS square waves through the system, as these square waves cause overshoots in the interpolation filters that would otherwise briefly clip the digital DAC circuitry.

A separate digital clipper circuit is used in the DSP core to ensure that any accumulator values that exceed the numeric 3.23 format range are clipped when taken from the accumulator.

High-Pass Filter

The high-pass filter is a first-order double-precision design. The purpose of the high-pass filter is to remove digital dc from the input. If this dc were allowed to pass, the detectors used in the compressor/limiter would give an incorrect reading for low signal levels.

The high-pass filter is controlled by a single parameter (α_{HPF}), which is programmed by writing to SPI location 180 in 2.20 twos complement format. The following equation can be used to calculate the parameter α_{HPF} from the -3 dB point of the filter:

$$\alpha_{HPF} = 1.0 - \text{EXP} \left(\frac{-2.0 \times \pi \times \text{HPF_CUTOFF}}{f_s} \right)$$

where EXP is the exponential operator, HPF_CUTOFF is the high-pass cutoff in Hz, and f_s is the audio sampling rate.

The default value for the -3 dB cutoff of the high-pass filter is 2.75 Hz at a sampling rate of 44.1 kHz.

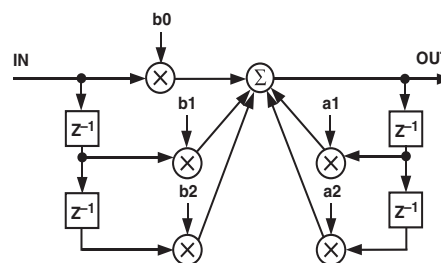


Figure 5. Biquad Filter

Biquad Filters

Each of the two input channels has seven second-order biquad sections in the signal path. In addition, the left and right channels have two additional biquad filters that may be used either as crossover filters or as additional equalization filters. The sub channel has three additional biquad filters, also to be used as equalization and/or crossover filters. In a typical scenario, the

AD1953

first seven biquads would be used for speaker equalization and/or tone controls, and the remaining filters would be programmed to function as crossover filters. Note that there is a common equalization section used for both the main and sub channels, followed by crossover filters. This arrangement prevents any interaction from occurring between the crossover filters and the equalization filters. One section of the biquad IIR filter is shown in Figure 5.

This section implements the transfer function:

$$H(Z) = \frac{(b_0 + b_1 \times Z^{-1} + b_2 \times Z^{-2})}{(1 - a_1 \times Z^{-1} - a_2 \times Z^{-2})}$$

The coefficients a_1 , a_2 , b_0 , b_1 , and b_2 are all in twos complement 2.20 format with a range from -2 to $(+2 - 1 \text{ LSB})$. The negative sign on the a_1 and a_2 coefficients is the result of adding both the feed-forward “b” terms as well as the feedback “a” terms. Some digital filter packages automatically produce the correct a_1 and a_2 coefficients for the topology of Figure 5, while others assume a denominator of the form $1 + a_1 \times Z^{-1} + a_2 \times Z^{-2}$. In this case, it may be necessary to invert the a_1 and a_2 terms for proper operation.

The biquad structure shown in Figure 5 is coded using double-precision math to avoid limit cycles from occurring when low frequency filters are used. The coefficients are programmed by writing to the appropriate location in the parameter RAM through the SPI port (see Table VI). There are two possible scenarios for controlling the biquad filters:

1. Dynamic Adjustment (for example, Bass/Treble control or Parametric Equalizer)

When using dynamic filter adjustment, it is highly recommended that the user employ the safeload mechanism to avoid temporary instability when the filters are dynamically updated. This can occur if some, but not all, of the coefficients are updated to new values when the DSP calculates the filter output. The operation of the Safeload registers is detailed in the Options for Parameter Updates section.

2. Setting Static EQ Curve after Power-Up

If many of the biquad filters need to be initialized after power-up (for example, to implement a static speaker-correction curve), the recommended procedure is to set the processor shutdown bit, wait for the volume to ramp down (about 20 ms), and then write directly to the parameter RAM in Burst Mode. After the RAM is loaded, the shutdown bit can be deasserted, causing the volume to ramp back up to the initial value. This entire procedure is click-free and faster than using the Safeload mechanism.

The datapaths of the AD1953 contain an extra two bits on top of the 24 bits that are input to the serial port. This allows up to 12 dB of boost without clipping. However, it is important to remember that it is possible to design a filter that has less than 12 dB of gain at the final filter output, but more than 12 dB of gain at the output of one or more intermediate biquad filter sections. For this reason, it is important to cascade the filter sections in the correct order, putting the sections with the largest peak gains at the end of the chain rather than at the beginning. This is standard practice when coding IIR filters and is covered in basic books on DSP coding.

If gains larger than 12 dB cannot be avoided, then the coefficients b_0 through b_2 of the first biquad section may be scaled down to fit the signal into the 12 dB maximum signal range, and then scaled back up at the end of the filter chain.

Volume

Eight separate SPI registers are available to control the volume. Three registers are used by the on-board program—one each for the Left, Right, and Sub channels. These registers are special in that they include automatic digital ramp circuitry for clickless volume adjustment. The volume control word is in 2.20 format, and gains from $+2.0$ to -2.0 are possible. The default value is 1.0. It takes 1024 audio frames to adjust the volume from 2.0 down to 0; in the normal case where the max volume is set to 1.0, it will take 512 audio frames for this ramp to reach zero. Note that a Mute command is the same as setting the volume to zero, except that when the part is unmuted, the volume returns to its original value. These volume ramp times assume that the AD1953 is set for the fast volume ramp speed. If the slow setting is selected, it will take 8192 audio frames to reach zero from a setting of 2.0. Correspondingly, it will take 4096 frames to reach 0 volume from the normal setting of 1.0.

The volume blocks are placed after the biquad filter sections to maximize the level of the signal that is passed through the filter sections. In a typical situation, the nominal volume setting might be -15 dB , allowing a substantial increase in volume when the user increases the volume. The AD1953 was designed with an analog dynamic range of $> 112 \text{ dB}$, so that in the typical situation with the volume set to -15 dB , the signal-to-noise ratio at the output will still exceed 97 dB. Greater output dynamic ranges are possible if the compressor/limiter is used, as the post-compression gain parameter can boost the signal back up to a higher level. In this case, the compressor will prevent the output from clipping when the volume is turned up and the input signal is large.

Stereo Image Expander

The image-enhancement processing is based on ADI’s patented Phat Stereo algorithm. The block diagram is shown in Figure 6.

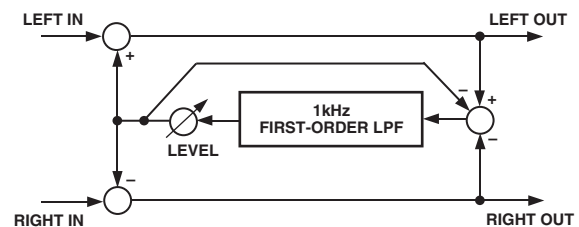


Figure 6. Stereo Image Expander

The algorithm works by increasing the phase shift for low frequency signals that are panned left or right in the stereo mix. Since the ear is responsive to interaural phase shifts below 1 kHz, this increase in phase shifts results in a widening of the stereo image. Note that signals panned to the center are not processed, resulting in a more natural sound. There are two parameters that control the Phat Stereo algorithm: the Level variable, which controls how much out-of-phase information is added to the left and right channels, and the cutoff frequency of the first-order low-pass filter, which determines the frequency range of the added out-of-phase signals. For best results, the cutoff frequency should be in the range of 500 Hz to 2 kHz. These parameters are controlled by altering the parameter RAM locations that store the parameters `spread_level` and `alpha_spread`.

The *spread_level* is a linear number in 2.20 format that multiplies the processed left-right signal before it is added to or subtracted from the main channels. The parameter *alpha_spread* is related to the cutoff frequency of the first-order low-pass filter by the equation

$$Alpha_spread = 1.0 - EXP\left(\frac{-2.0 \times \pi \times spread_freq}{f_s}\right)$$

where *EXP* is the exponential operator, *spread_freq* is the low-pass cutoff in Hz, and *f_s* is the audio sampling rate.

Note that the stereo spreading algorithm assumes that frequencies below 1 kHz are present in the main satellite speakers. In some systems, the crossover frequency between the satellite and subwoofer speakers is quite high (> 500 Hz). In this case, the stereo spreading algorithm will not be effective, as the frequencies that contribute to the spreading effect will be coming mostly from the subwoofer, which is a mono source.

Delay

Each of the three DAC channels has a delay block that allows the user to introduce a delay of up to 165 audio samples. The delay values are programmed by entering the delay (in samples) into the appropriate location of the parameter RAM. With a 44.1 kHz sample rate, a delay of 165 samples corresponds to a time delay of 3.74 ms. Since sound travels at approximately 1 foot/ms, this can be used to compensate for speaker placements that are off by as much as 3.74 feet.

An additional 100 samples of delay are used in the look-ahead portion of the compressor/limiter, but only for the main two channels. This can be used to increase the total delay for the left and right channels to 265 samples, or 6 ms at 44.1 kHz.

Main Compressor/Limiter

The compressor used in the AD1953 is quite sophisticated and is comparable in many ways to professional compressor/limiters used in the professional audio and broadcast fields. It uses rms/peak detection with adjustable attack/hold/release, look-ahead compression, and table-based entry of the input/output curve for complete flexibility.

The AD1953 uses two compressor/limiters, one in the subwoofer DAC and one in the main left/right DAC. It is well known that having independent compressors operating over different frequency ranges results in a superior perceived sound. With a single-band compressor, loud bass information will modulate the gain of the entire audio signal, resulting in suboptimal maximum perceived loudness as well as gain pumping or modulation effects. With independent compressors operating separately on the low and high frequencies, this problem is dramatically reduced. If the AD1953 is being operated in 2-channel mode, an extra path is added so that the subwoofer channel can be added back into the main channel. This maintains the advantage of using a 2-band compressor, even in a 2.0 system configuration.

Figure 7 shows the traditional basic analog compressor/limiter. It uses a voltage controlled amplifier to adjust gain and a feed-forward detector path using an rms detector with adjustable time constants, followed by a nonlinear circuit to implement the desired input/output relationship. A simple compressor will have a single threshold above which the gain is reduced. The amount of compression above the threshold is called the compression ratio and is defined as dB change in input/dB change in output.

For example, if the input to a 2:1 compressor is increased by 2 dB, the output will rise by 1 dB for signals above the threshold.

A single “hard” threshold results in more audible behavior than a so-called “soft-knee” compressor, where the compression is introduced more gradually. In an analog compressor, the soft-knee characteristic is usually made by using diodes in their exponential turn-on region.

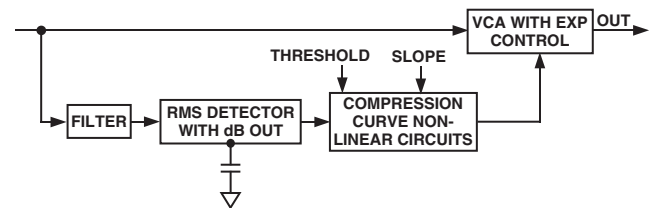


Figure 7. Analog Compressor

The best analog compressors use rms detection as the signal amplitude detector. RMS detectors are the only class of detectors that are not sensitive to the phase of the harmonics in a complex signal. The ear also bases its loudness judgment on the overall signal power. Using an rms detector therefore results in the best audible performance. Compressors that are based on peak detection, while good for preventing clipping, are generally quite poor when it comes to audible performance.

RMS detectors have a certain time constant that determines how rapidly they can respond to transient signals. There is always a trade-off between speed of response and distortion. Figure 8 shows this trade-off.

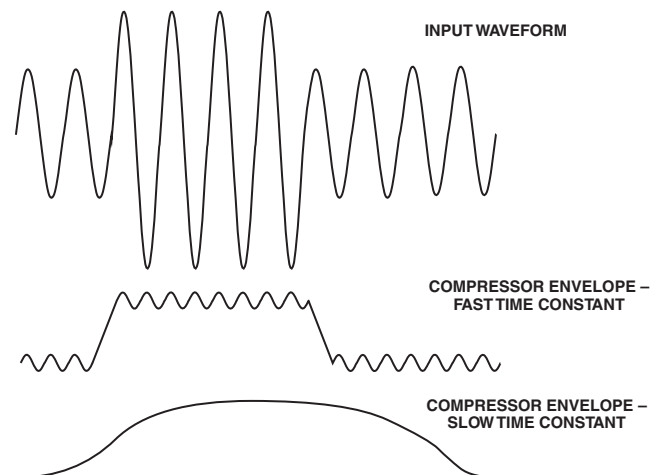


Figure 8. Effect of RMS Time Constant on Distortion

In the case of a fast-responding rms detector, the detector envelope will have a signal component in addition to the desired dc component. This signal component (which, for an rms detector, is at twice the input frequency) will result in harmonic distortion when multiplied by this detector signal.

The AD1953 uses a modified rms algorithm to improve the relationship between acquisition time and distortion. It uses a peak-riding circuit together with a hold circuit to modify the rms signal, as shown in Figure 9. Figure 8 shows two envelopes—one with the harmonic distortion and another, flatter envelope, which is produced by the AD1953.

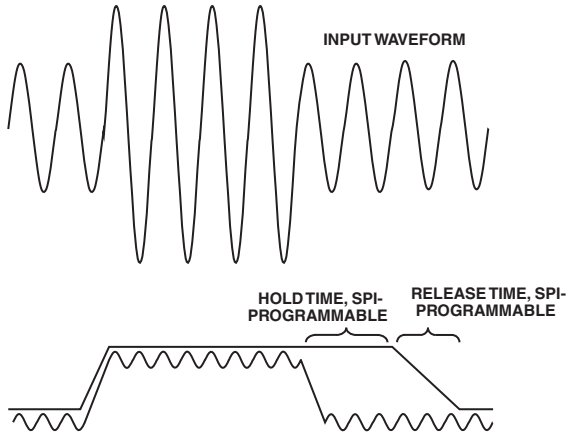


Figure 9. Using the Hold and Release Time Feature

Using this idea of a modified rms algorithm, the true rms value is still obtained for all but the lowest frequency signals, while the distortion due to rms ripple is reduced. It also allows the user to set the hold and release times of the compressor independently.

The detector path of the AD1953 is shown in Figure 10. The rms detector is controlled by three parameters stored in parameter RAM: the rms time constant, the hold time, and the release rate. The log output of the rms detector is applied to a look-up table with interpolation. The higher bits of the rms output form an offset into this table, and the lower bits are used to interpolate between the table entries to form a high precision gain word. The look-up table resides in the parameter RAM and is loaded by the user to give the desired curve. The look-up table contains 33 data locations, and the LSB of the address in the look-up table corresponds to a 3 dB change in the amplitude of the detector signal. This gives the user the ability to program an input/output curve over a 99 dB range. For the main compressor, the table resides in locations 110 to 142 in the SPI parameter RAM.

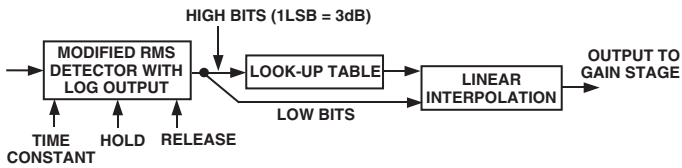


Figure 10. Gain Derived from Interpolated Look-Up Table

One subtlety of the table look-up involves the difference between the rms value of a sine wave and that of a square wave. If a full-scale square wave is applied to the AD1953, the rms value of this signal will be 3 dB higher than the rms value of a 0 dBFS sine wave. Therefore, the table will range from +9 dB (location 142) to -87 dB (location 110).

The entries in the table are linear gain words in 2.20 format. Figure 11 shows an example of the table entries for a simple above-threshold compressor.

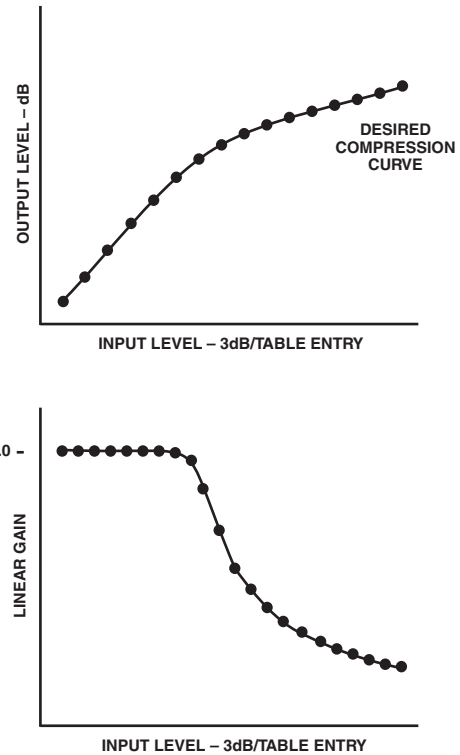


Figure 11. Example of Table Entry for a Given Compression Curve

Note that the maximum gain that can be entered in the table is 2.0 (minus 1 LSB). If more gain is required, the entire compression curve may be shifted upward by using the post-compression gain block following the compressor/limiter.

The AD1953 compressor/limiter also includes a look-ahead compression feature. The idea behind look-ahead compression is to prevent compressor overshoots by applying some digital delay to the signal before the gain-control multiplier, but not to the detector path. In this way, the detector can acquire the new amplitude of the input signal before the signal actually reaches the multiplier. A comparison of a tone burst fed to a conventional compressor versus a look-ahead compressor is shown in Figure 12.

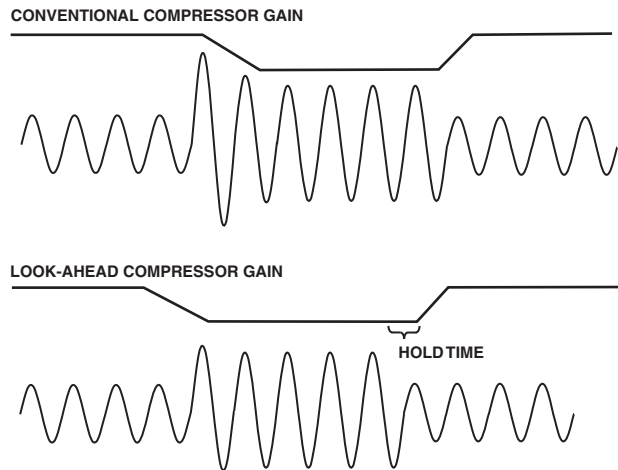


Figure 12. Conventional Compression vs. Look-Ahead Compression

In the look-ahead compressor, the gain has already been reduced by the time the tone-burst signal arrives at the multiplier input. Note that when using a look-ahead compressor, it is important to set the detector hold time to a value that is at least the same as the look-ahead delay time, or else the compressor release will start too soon, resulting in an expanded “tail” of a tone burst signal. The complete flow of the left/right dynamics processor is shown in Figure 13.

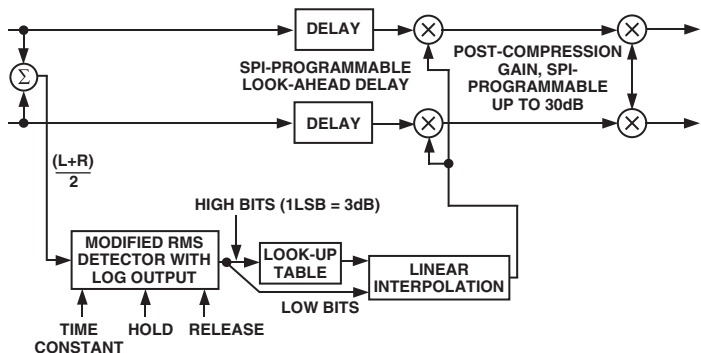


Figure 13. Complete Dynamics Flow, Main Channels

The detector path works from a sum of left and right channels ((L+R)/2). This is the normal way that compressors are built, and it counts on the fact that the main instruments in any stereo mix are seldom recorded deliberately out of phase, especially in the lower frequencies, which tend to dominate the energy spectrum of real music.

The compressor is followed by a block known as post-compression gain. Most compressors are used to reduce the dynamic range of music by lowering the gain during loud signal passages. This results in an overall loss of volume. This loss can be made up by introducing gain after the compressor. In the AD1953, the coefficient format used is 2.20, which has a maximum floating-point representation of slightly less than 2.0. This means the maximum gain that can be achieved in a single instruction is 6 dB. To get more gain, the program in the AD1953 uses a cascade of five multipliers to achieve up to 30 dB of post-compression gain.

To program the compressor/limiter, the following formulas may be used to determine the 22-bit numbers (in 2.20 format) to be entered into the parameter RAM.

RMS Time Constant

This can be best expressed by entering the time constant in terms of dB/sec “raw” release rate (without the peak-riding circuit). The attack rate is a rather complicated formula that depends on the change in amplitude of the input sine wave.

$$rms_tconst_parameter = 1.0 - 10^{\left(\frac{release_rate}{10.0 \times f_s}\right)}$$

where

rms_tconst_parameter = fractional number to enter into the SPI RAM (after converting to 22-bit 2.20 format)

release_rate = release rate of the raw rms detector in dB/sec. This must be negative. *f_s* = audio sampling rate.

RMS Hold Time

$$rms_holdtime_parameter = \text{int}(f_s \times hold_time)$$

where

rms_holdtime_parameter = integer number to enter into the SPI RAM

f_s = audio sample rate

Hold_time = absolute time to wait before starting the release ramp-down of the detector output

int() = integer part of expression

RMS Release Rate

$$rms_decay_parameter = \text{int}(rms_decay / 1.096)$$

Where *rms_decay_parameter* = decimal integer number to enter into the SPI RAM

rms_decay = decay rate in dB/sec

int() = integer part of expression

Look-Ahead Delay

$$Lookahead_delay_parameter = Lookahead_delay \times f_s$$

Where *Lookahead_delay* = predictive compressor delay in absolute time

f_s = audio sample rate

The maximum *Lookahead_delay_parameter* value is 100.

Post-Compression Gain

$$Post_compression_gain_parameter =$$

$$Post_compression_gain_linear^{(1/5)}$$

Where *Post_compression_gain_linear* is the linear post-compression gain

^ = raise to the power

Subwoofer Compressor/Limiter

The subwoofer compressor/limiter differs from the left/right compressor in the following ways:

1. The subwoofer compressor operates on a weighted sum of left and right inputs (*aa* × Left + *bb* × Right), where *aa* and *bb* are both programmable.
2. The detector input has a biquad filter in series with the input in order to implement frequency-dependent compression thresholds.
3. There is no predictive compression, as presumably the input signals are filtered to pass only low frequencies, and therefore transient overshoots are not a problem.

The subwoofer compressor signal flow is shown in Figure 14.

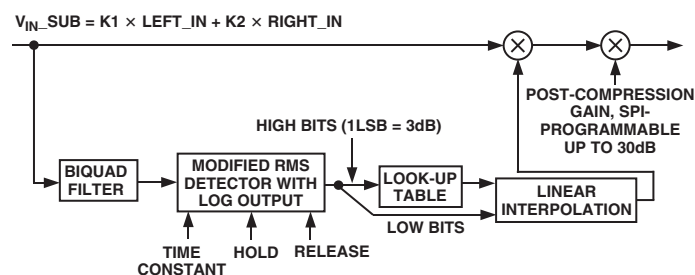


Figure 14. Signal Flow for Subwoofer Compressor

The biquad filter before the detector can be used to implement a frequency-dependent compression threshold. For example, assume that the overload point of the woofer is strongly frequency-dependent. In this case, one would have to set the compressor threshold to a value that corresponded to the most sensitive overload frequency of the woofer. If the input signal happened to be mostly in a frequency range where the woofer

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was not so sensitive to overload, then the compressor would be too pessimistic and the volume of the woofer would be reduced. If, on the other hand, the biquad filter were designed to follow the woofer excursion curve of the speaker, then the volume of the woofer could be maximized under all conditions. This is illustrated in Figure 15.

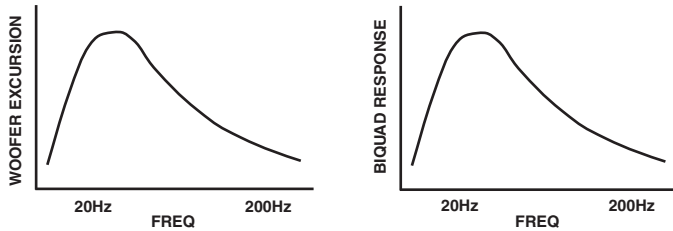


Figure 15. Optimizing Woofer Loudness Using the Subwoofer RMS Biquad Filter

When using a filter in front of the detector, a confusing side-effect occurs. If one measures the frequency response by using a swept sine wave with an amplitude large enough to be above the compressor threshold, the resulting frequency response will not look flat. However, this is not real in the sense that, as the sine wave is swept through the system, the gain is being slowly modulated up and down according to the response of the biquad filter in front of the detector. If one measures the response using a pink-noise generator, the result will look much better, as the detector will settle on only one gain value. The perceptual effect of the swept-sine-wave test is not at all what would be predicted by simply looking at the frequency response curve; it is only the signal-path filters that will affect the perception of frequency response, not the detector-path filters.

De-emphasis Filtering

The standard for encoding CDs allows the use of a pre-emphasis curve during encoding, which must be compensated for by a de-emphasis curve during playback. The de-emphasis curve is defined as a first-order shelving filter with a single pole at $(1/(2 \times \pi \times 50 \mu\text{s}))$ followed by a single zero at $(1/(2 \times \pi \times 15 \mu\text{s}))$. This curve may be accurately modeled using a first-order digital filter. This filter is included in the AD1953; it is not part of the bank of biquad filters, and so does not take away from the number of available filters.

Since the specification of the de-emphasis filter is based on an analog filter, the response of the filter should not depend on the incoming sampling rate. However, when the de-emphasis filter is implemented digitally, the response will scale with the sampling rate unless the filter coefficients are altered to suit each possible input sampling rate. For this reason, the AD1953 includes three separate de-emphasis curves; one each for sampling rates of 32 kHz, 44.1 kHz, and 48 kHz. These curves are selected by writing to Bits <5:4> of Control Register 1 over the SPI port.

Using the Sub Reinjection Paths for Systems with No Subwoofer

Many systems will not use a subwoofer, but would still benefit from 2-band compression/limiting. This can be accommodated by using sub reinjection paths in the program flow. These parameters are programmed by entering two numbers (in 2.20 format) into the parameter RAM. Note that if the biquad filters are not properly designed, the frequency response at the crossover point may not be flat. Many crossover filters are designed to be flat in the sense of adding the powers together, but nonflat if

the sum is done in voltage mode. The user must take care to design an appropriate set of crossover filters.

Interpolation Filters

The left and right channels have a 128:1 interpolation filter with 70 dB stop-band attenuation that precedes the digital $\Sigma\text{-}\Delta$ modulator. This filter has a group delay of approximately $24.185/f_s$, where f_s is the sampling rate. The sub channel does not use an interpolation filter. The reason for this (besides saving valuable MIPS) is that it is expected that the bandwidth of the sub output will be limited to less than 1 kHz. With no interpolation filter, the first “image” will therefore be at 43.1 kHz (which is $f_s - 1$ kHz, for CD audio). The standard external filter used for both the main and sub channels is a third-order, single op amp filter. If the cutoff frequency of the external subwoofer filter is 2 kHz, then there are more than four octaves between 2 kHz and the first image at 43.1 kHz. A third-order filter will roll off by approximately $18 \text{ dB/oct} \times 4 \text{ octaves} = 72 \text{ dB}$ attenuation. This is approximately the same as the digital attenuation used in the main channel filters, so no internal interpolation filter is required to remove the out-of-band images.

Note that by having interpolation filters in the main channels but not the subwoofer channel, there is a potential time-delay mismatch between the main and sub channels. The group delay of the digital interpolation filters used in the main left/right channels is about 0.5 ms. This must be compared to the group delay of the external analog filter used in the subwoofer path. If the group delay mismatch causes a frequency response error (when the two signals are “acoustically added”), the programmable delay feature can be used to put extra delay in either the subwoofer path or the main left/right path.

SPI PORT

Overview

The AD1953 has many different control options. Most signal-processing parameters are controlled by writing new values to the parameter RAM using the SPI port. Other functions such as volume and de-emphasis filtering are programmed by writing to SPI control registers.

The SPI port uses a 4-wire interface, consisting of CLATCH, CCLK, CDATA, and COUT signals. The CLATCH signal goes LOW at the beginning of a transaction and HIGH at the end of a transaction. The CCLK signal latches the serial input data on a low-to-high transition. The CDATA signal carries the serial input data, and the COUT signal is the serial output data. The COUT signal remains three-stated until a read operation is requested. This allows other SPI compatible peripherals to share the same readback line.

The SPI port is capable of full read/write operation for all of the memories (parameter and program) and some of the SPI registers (Control Register 1 and data capture registers). The memories may be accessed in both a single-address mode or in burst mode. All SPI transactions follow the same basic format, shown in Table I.

The Wb/R bit is low for a write, and high for a read operation. The 10-bit address word is decoded into a location in one of the two memories (parameter or program) or one of the SPI registers. The number of data bytes varies according to the register or memory being accessed. In burst-write mode (available for loading the RAMs only), an initial address is given followed by a continuous sequence of data for consecutive RAM locations.

The detailed data format diagram for continuous-mode operation is given in SPI Read/Write data formats.

A sample timing diagram for a single SPI WRITE operation to the parameter RAM is shown in Figure 16.

Table I. SPI Word Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
00000, R/Wb, adr[9:8]	Adr[7:0]	Data	Data	Data

A sample timing diagram of a single SPI READ operation is shown in Figure 17. The COUT pin goes from three-state driven at the beginning of Byte 2. Bytes 0 and 1 contain the address and R/W bit, and Bytes 2 to 4 carry the data. The exact format is shown in Tables VIII to XIX.

The AD1953 has several mechanisms for updating signal-processing parameters in real time without causing loud pops or

clicks. In cases where large blocks of data need to be downloaded, the DSP core can be shut down and new data loaded, and the core can then be restarted. The shutdown and restart mechanisms employ a gradual volume ramp to prevent clicks and pops. In cases where only a few parameters need to be changed (for example, a single biquad filter), a safeload mechanism is used that allows a block of SPI registers to be transferred to the parameter RAM within a single audio frame while the core is running. The safeload mode uses internal logic to prevent contention between the DSP core and the SPI port.

SPI Address Decoding

Table II shows the address decoding used in the SPI port. The SPI address space encompasses a set of registers and two RAMs, one for holding signal-processing parameters and one for holding the program instructions. Both of the RAMs are loaded on power-up from on-board boot ROMs.

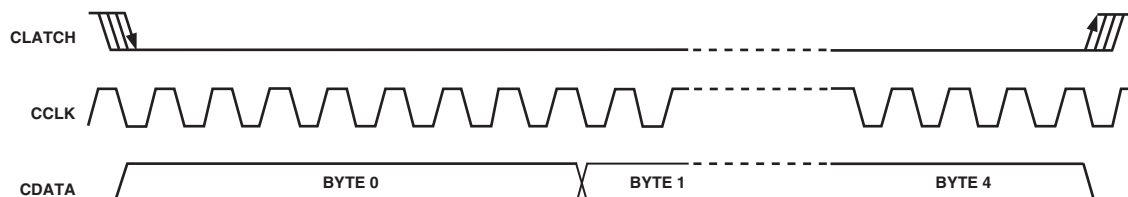


Figure 16. Sample of SPI WRITE Format (Single-Write Mode)

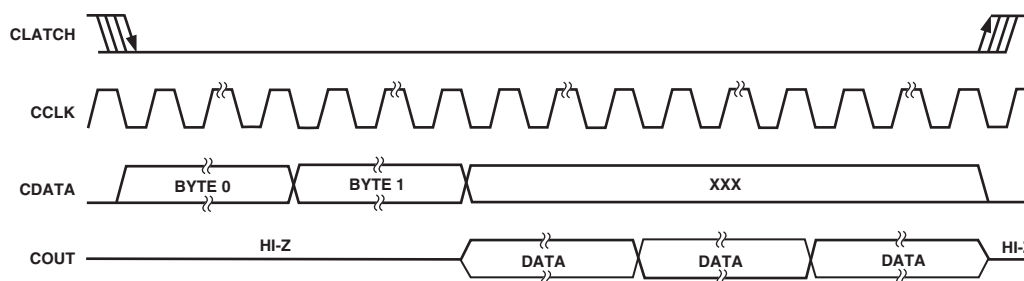


Figure 17. Sample of SPI READ Format (Single-Read Mode)

Table II. SPI Port Address Decoding

SPI Address	Register Name	Read/Write Word Length
0–255	Parameter RAM	Write: 22 Bits Read: 22 Bits
256	SPI Control Register 1	Write: 14 Bits Read: 2 Bits
257	SPI Control Register 2	Write: 10 Bits Read: N/A
258	Volume 0	Write: 22 Bits Read: N/A
259	Volume 1	Write: 22 Bits Read: N/A
260	Volume 2	Write: 22 Bits Read: N/A
261	Volume 3	Write: 22 Bits Read: N/A
262	Volume 4	Write: 22 Bits Read: N/A
263	Volume 5	Write: 22 Bits Read: N/A
264	Volume 6	Write: 22 Bits Read: N/A
265	Volume 7	Write: 22 Bits Read: N/A
266	Data Capture (SPI Out) #1	Write: 9-Bit Program Counter Value, 2-Bit Register Address Read: 24 Bits
267	Data Capture (SPI Out) #2	Write: 9-Bit Program Counter Value, 2-Bit Register Address Read: 24 Bits
268	Data Capture (Serial Out) Slot 0	Write: 9-Bit Program Counter Value, 2-Bit Register Address Read: N/A
269	Data Capture (Serial Out) Slot 1	Write: 9-Bit Program Counter Value, 2-Bit Register Address Read: N/A
270	Data Capture (Serial Out) Slot 2	Write: 9-Bit Program Counter Value, 2-Bit Register Address Read: N/A
271	Data Capture (Serial Out) Slot 3	Write: 9-Bit Program Counter Value, 2-Bit Register Address Read: N/A
272	Data Capture (Serial Out) Slot 4	Write: 9-Bit Program Counter Value, 2-Bit Register Address Read: N/A
273	Data Capture (Serial Out) Slot 5	Write: 9-Bit Program Counter Value, 2-Bit Register Address Read: N/A
274	Parameter RAM Safeload Register 0	Write: 8-Bit Parameter RAM Address, 22-Bit Parameter Data Read: N/A
275	Parameter RAM Safeload Register 1	Write: 8-Bit Parameter RAM Address, 22-Bit Parameter Data Read: N/A
276	Parameter RAM Safeload Register 2	Write: 8-Bit Parameter RAM Address, 22-Bit Parameter Data Read: N/A
277	Parameter RAM Safeload Register 3	Write: 8-Bit Parameter RAM Address, 22-Bit Parameter Data Read: N/A
278	Parameter RAM Safeload Register 4	Write: 8-Bit Parameter RAM Address, 22-Bit Parameter Data Read: N/A
279–510	Unused	
511	Test Register	Write: 8 Bits Read: N/A
512–1024	Program RAM	Write: 35 Bits Read: 35 Bits

Control Register 1

Control Register 1 is a 14-bit register that controls data capture modes, serial modes, de-emphasis, mute, power-down, and SPI-to-memory transfers. Table III documents the contents of this register. Table IV details the two bits in the register's read operation.

Bits <1:0> set the wordlength, which is used in right-justified serial modes to determine where the MSB is located relative to the start of the audio frame.

Bits <3:2> select one of four serial modes, which are discussed in the Serial Data Input Port section.

The de-emphasis curve selection Bits <5:4> turn on the internal de-emphasis filter for one of three possible sample rates.

Bit <6>, the soft power-down bit, stops the internal clocks to the DSP core, but does not reset the part. The digital power consumption is reduced to a low level when this bit is asserted. Reset can only be asserted using the external reset pin.

Soft mute (Bit <7>) is used to initiate a volume ramp-down sequence. If the initial volume was set to 1.0, this operation will take 512 audio frames to complete. When this bit is deasserted, a ramp-up sequence is initiated until the volume returns to its original setting.

The initiate-safe-transfer Bit <9> will request a data transfer from the SPI safeload registers to the parameter RAM. The safeload registers contain address-data pairs, and only those registers that have been written to since the last transfer operation will be uploaded. The user may poll for this operation being complete by reading Bit <0> of Control Register 1. The Safeload Mechanism section goes into more detail on this feature.

Bit <10>, the halt program bit, is used to initiate a volume ramp-down followed by a shutdown of the DSP core. The user may poll for this operation being complete by reading Bit <1> of Control Register 1.

The Data Capture Serial Out mode is controlled with Bits <13:12>. This function can be used to send data that is captured using the data-capture feature to external devices such as an external stereo DAC or multichannel codec. The Data Capture Registers and Outputs section gives more information about the TDM and data capture features.

Table III. Control Register 1 Write Definition

Register Bits	Function
13:12	Data Capture Serial Out Mode Control 00 = none 01 = TDM 6-channel out, uses Pins 41–43 10 = 2-channel out, uses Pin 45 11 = Unused
11	Unused
10	Halt Program (1 = Halt)
9	Initiate Safe Transfer (1 = Transfer)
8	Unused
7	Soft Mute (1 = Start Mute Sequence)
6	Soft Power-Down (1 = Power Down)
5:4	De-emphasis Curve Select 00 = none 01 = 44.1 kHz 10 = 32 kHz 11 = 48 kHz
3:2	Serial In Mode 00 = I ² S 01 = Right-Justified 10 = DSP 11 = Left-Justified
1:0	Word Length 00 = 24 Bits 01 = 20 Bits 10 = 16 Bits 11 = 16 Bits

Table IV. Control Register 1 READ Definition

Register Bits	Function
1	DSP Core Shutdown Complete 1 = Shutdown Complete 0 = Not Shut Down
0	Safe Memory Load Complete 1 = Complete (Note: Cleared after Read) 0 = Not Complete

Bit 0 is asserted when all requested safeload registers have been transferred to the parameter RAM. It is cleared after the read operation is complete.

Bit 1 is asserted after the requested shutdown of the DSP is completed. When this bit is set, the user is free to write or read any RAM location without causing an audio pop or click.

Table V. Control Register 2 WRITE Definition

Register Bits	Function
9	Volume Ramp Speed 1 = 160 ms Full-Ramp Time 0 = 20 ms Full-Ramp Time
8	Serial Port Output Enable 1 = Enabled 0 = Disabled
7:6	Serial Port Input Select 00 = IN0 01 = IN1 10 = IN2 11 = NA
5:4	MCLK Input Select 00 = MCLK0 01 = MCLK1 10 = MCLK2 11 = NA
3	Reserved
2	MCLK In Frequency Select 0 = $512 \times f_s$ 1 = $256 \times f_s$
1:0	MCLK Out Frequency Select 00 Disabled 01 $512 \times f_s$ 10 $256 \times f_s$ 11 MCLKO = MCLK_In (Feedthrough)

Control Register 2

Table V documents the contents of Control Register 2. Bits <1:0> set the frequency of the MCLKO pin. If these bits are set to 00, the MCLKO pin is disabled (default). When set to 01, the MCLKO pin is set to $512 \times f_s$, which is the same as the internal master clock used by the DSP core. When set to 10, this pin is set to $256 \times f_s$, derived by dividing the internal DSP clock by 2. In this mode, the output $256 \times f_s$ clock will be inverted with respect to the input $256 \times f_s$ clock. This is not the case with the feedthrough mode. When set to 11, the MCLKO pin mirrors the selected MCLK input pin (it's the output of the MCLK MUX selector). Note that the internal DSP master clock may either be the same as the selected MCLK pin (when MCLK frequency select is set to $512 \times f_s$ mode) or may be derived from the MCLK pin using internal clock doubler (when MCLK frequency select is set to $256 \times f_s$).

Bit <2> selects one of two possible MCLK input frequencies. When set to 0 (default), the MCLK frequency is set to $512 \times f_s$. In this mode, the internal DSP clock and the external MCLK are at the same frequency. When set to 1, the MCLK frequency is set to $256 \times f_s$, and an internal clock doubler is used to generate the DSP clock.

Bits <5:4> select one of three clock input sources using an internal MUX. To avoid click and pop noises when switching MCLK sources, it is recommended that the user put the DSP core in shutdown before switching MCLK sources.

Bits <7:6> select one of three serial input sources using an internal MUX. Each source selection includes a separate SDATA, LRCLK, and BCLK input. To avoid click and pop noises when switching serial sources, it is recommended that the user put the DSP core in shutdown before writing to these bits.

Bit <8> is used to enable the three serial output pins. These pins are connected to the output of the serial input MUX, which is set by Bits <7:6>. The default is 0 (disabled).

Bit <9> changes the default setting of the volume ramp speed. When set to 0, it will take 1024 LRCLK periods to go from full volume (6 dB) to infinite attention. When set to 1, the same operation will take 8192 LRCLK periods.

Volume Registers

The AD1953 contains eight 22-bit volume registers, one each for the left, right, and subwoofer channels and an additional five registers to be used by custom programs used in multichannel applications. These registers are special because when the volume is changed from an initial value to a new value, a linear ramp is used to interpolate between the two values. This feature prevents audible clicks and pops when changing volume. The ramp is set so that it takes 512 audio frames to decrement from a volume of 1.0 (default) down to 0 (muted). The volume registers are formatted in 2.20 twos complement, meaning that 010000000000000000000000 is interpreted as 1.0. Negative values can also be written to the volume register, causing an inversion of the signal. Negative values work as expected with the ramp feature; to go from +1.0 to -1.0 will take 1024 LRCLKs, and the volume will pass through 0 on the way.

Parameter RAM Contents

Table VI shows the contents of the parameter RAM. The parameter RAM is 22 bits wide and occupies SPI addresses

0–255. The low addresses of the RAM are used to control the biquad filters. There are 22 biquad filters in all, and each biquad has five coefficients, resulting in a total memory usage of 110 coefficients. There are also two tables of 33 coefficients each that define the main and sub compressor input/output characteristics. These are loaded with 1.0 on power-up, resulting in no compression. Other RAM entries control other compressor characteristics, as well as delay and spatialization settings.

The parameter RAM is initialized on power-up by an on-board boot ROM. The default values (shown in the table) yield no equalization, no compression, no spatialization, no delay, and “normal” detector time constants in the compressor sections. The functionality of the AD1953 on power-up is basically that of a normal audio DAC with no signal-processing capability.

The data format of the Parameter RAM is twos complement 2.20 format. This means that the coefficients may range from +2.0 (–1 LSB) to –2.0, with 1.0 represented by the binary word 010000000000000000000000.

Table VI. Parameter RAM Contents

Address	Function	Default Value in Fractional 2.20 Format
0	IIR0 Left b0	1.0
1	IIR0 Left b1	0
2	IIR0 Left b2	0
3	IIR0 Left a1	0
4	IIR0 Left a2	0
5	IIR1 Left b0	1.0
6	IIR1 Left b1	0
7	IIR1 Left b2	0
8	IIR1 Left a1	0
9	IIR1 Left a2	0
10	IIR2 Left b0	1.0
11	IIR2 Left b1	0
12	IIR2 Left b2	0
13	IIR2 Left a1	0
14	IIR2 Left a2	0
15	IIR3 Left b0	1.0
16	IIR3 Left b1	0
17	IIR3 Left b2	0
18	IIR3 Left a1	0
19	IIR3 Left a2	0
20	IIR4 Left b0	1.0
21	IIR4 Left b1	0
22	IIR4 Left b2	0
23	IIR4 Left a1	0
24	IIR4 Left a2	0
25	IIR5 Left b0	1.0
26	IIR5 Left b1	0
27	IIR5 Left b2	0
28	IIR5 Left a1	0
29	IIR5 Left a2	0
30	IIR6 Left b0	1.0
31	IIR6 Left b1	0
32	IIR6 Left b2	0
33	IIR6 Left a1	0
34	IIR6 Left a2	0
35	IIR0 Right b0	1.0

Table VI. Parameter RAM Contents (continued)

Address	Function	Default Value in Fractional 2.20 Format
36	IIR0 Right b1	0
37	IIR0 Right b2	0
38	IIR0 Right a1	0
39	IIR0 Right a2	0
40	IIR1 Right b0	1.0
41	IIR1 Right b1	0
42	IIR1 Right b2	0
43	IIR1 Right a1	0
44	IIR1 Right a2	0
45	IIR2 Right b0	1.0
46	IIR2 Right b1	0
47	IIR2 Right b2	0
48	IIR2 Right a1	0
49	IIR2 Right a2	0
50	IIR3 Right b0	1.0
51	IIR3 Right b1	0
52	IIR3 Right b2	0
53	IIR3 Right a1	0
54	IIR3 Right a2	0
55	IIR4 Right b0	1.0
56	IIR4 Right b1	0
57	IIR4 Right b2	0
58	IIR4 Right a1	0
59	IIR4 Right a2	0
60	IIR5 Right b0	1.0
61	IIR5 Right b1	0
62	IIR5 Right b2	0
63	IIR5 Right a1	0
64	IIR5 Right a2	0
65	IIR6 Right b0	1.0
66	IIR6 Right b1	0
67	IIR6 Right b2	0
68	IIR6 Right a1	0
69	IIR6 Right a2	0
70	IIR0 Xover Left b0	1.0
71	IIR0 Xover Left b1	0

Table VI. Parameter RAM Contents (continued)

Address	Function	Default Value in Fractional 2.20 Format
72	IIR0 Xover Left b2	0
73	IIR0 Xover Left a1	0
74	IIR0 Xover Left a2	0
75	IIR1 Xover Left b0	1.0
76	IIR1 Xover Left b1	0
77	IIR1 Xover Left b2	0
78	IIR1 Xover Left a1	0
79	IIR1 Xover Left a2	0
80	IIR0 Xover Right b0	1.0
81	IIR0 Xover Right b1	0
82	IIR0 Xover Right b2	0
83	IIR0 Xover Right a1	0
84	IIR0 Xover Right a2	0
85	IIR1 Xover Right b0	1.0
86	IIR1 Xover Right b1	0
87	IIR1 Xover Right b2	0
88	IIR1 Xover Right a1	0
89	IIR1 Xover Right a2	0
90	IIR0 Xover Sub b0	1.0
91	IIR0 Xover Sub b1	0
92	IIR0 Xover Sub b2	0
93	IIR0 Xover Sub a1	0
94	IIR0 Xover Sub a2	0
95	IIR1 Xover Sub b0	1.0
96	IIR1 Xover Sub b1	0
97	IIR1 Xover Sub b2	0
98	IIR1 Xover Sub a1	0
99	IIR1 Xover Sub a2	0
100	IIR2 Xover Sub b0	1.0
101	IIR2 Xover Sub b1	0
102	IIR2 Xover Sub b2	0
103	IIR2 Xover Sub a1	0
104	IIR2 Xover Sub a2	0
105	IIR Sub rms b0	1.0
106	IIR Sub rms b1	0
107	IIR Sub rms b2	0
108	IIR Sub rms a1	0
109	IIR Sub rms a2	0

Table VI. Parameter RAM Contents (continued)

Address	Function	Default Value in Fractional 2.20 Format
110–142	Main Compressor Look-Up Table Base	1.0 (all)
143	Main Compressor Attack/rms Time Constant	5.75×10^{-4} (120 dB/sec)
144	Main Post-Compressor Gain	1.0
145–177	Subwoofer Compressor Look-Up Table Base	1.0 (all)
178	Sub Compressor Attack/RMS Time Constant	5.75×10^{-4} (120 dB/sec)
179	Post-Compressor Gain (SUB)	1.0
180	High-Pass Filter Cutoff Frequency	3.92×10^{-4}
181	Main Compressor Look-Ahead Delay	0
182	Delay Left	0
183	Delay Right	0
184	Delay Sub	0
185	Stereo Spreading Coefficient	0
186	Stereo Spreading Frequency Control	0.112694
187	Subwoofer Reinjection to Main Left	0.0
188	Subwoofer Reinjection to Main Right	0.0
189	Subwoofer Channel Input Gain from Left IN	0.5
190	Subwoofer Channel Input Gain from Right IN	0.5
191	Main Detector Hold Time, Samples (4095 MAX)	0^1
192	Sub Detector Hold Time, Samples (4095 MAX)	0^1
193	Main Detector Decay Time	0x3FFFFFF (4.597 × 10 ⁶ dB/sec) ^{1,2}
194	Sub Detector Decay Time	0x3FFFFFF (4.597 × 10 ⁶ dB/sec) ^{1,2}

NOTES

¹The detector hold and decay times are integer values, while the rest of the parameters are fractional twos complement values.

²The default decay time of the hold/release circuit is set fast enough that the decay is dominated by the time constant of the rms detector.

Options for Parameter Updates

The parameter and program RAMs can be written and read using one of several methods.

1. Direct Read/Write. This method allows direct access to the RAMs. Since the RAMs are also being used during real-time DSP operation, a glitch will likely occur at the output. This method is not recommended.
2. Direct Read/Write after Core Shutdown. This method avoids the glitch while accessing the internal RAMs by first shutting down the core. This is recommended for transferring large amounts of data, such as initializing the parameter RAM at power-up or downloading a completely new program. These

transfers can be sped up by using burst mode, where an initial address followed by blocks of data are sent to the RAM.

3. Safeload Writes Up to five SPI registers are loaded with address/data intended for the parameter RAM. The data is then transferred to the requested address when the RAM is not busy. This method can be used for dynamic updates while live program material is playing through the AD1953. For example, a complete update of one biquad section can occur in one audio frame while the RAM is not busy. This method is not available for writing to the program RAM or control registers. The next section discusses these options in more detail.