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Fully Accurate, 12-/14-/16-Bit V_{OUT} *nano*DAC, Quad, SPI Interface, 4.5 V to 5.5 V in TSSOP

Data Sheet

AD5024/AD5044/AD5064

FEATURES

- Low power quad 12-/14-/16-bit DAC, ±1 LSB INL
- Pin compatible and performance upgrade to AD5666
- Individual and common voltage reference pin options
- Rail-to-rail operation
- 4.5 V to 5.5 V power supply
- Power-on reset to zero scale or midscale
- 3 power-down functions and per-channel power-down
- Hardware $\overline{LDAC}$ with software $\overline{LDAC}$ override function
- $\overline{CLR}$ function to programmable code
- SDO daisy-chaining option
- 14-/16-lead TSSOP
- Internal reference buffer and internal output amplifier

APPLICATIONS

- Process control
- Data acquisition systems
- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
- Programmable attenuators

GENERAL DESCRIPTION

The AD5024/AD5044/AD5064/AD5064-1 are low power, quad 12-/14-/16-bit buffered voltage output *nano*DAC® converters that offer relative accuracy specifications of 1 LSB INL and 1 LSB DNL with the AD5024/AD5044/AD5064 individual reference pin and the AD5064-1 common reference pin options. The AD5024/AD5044/AD5064/AD5064-1 can operate from a single 4.5 V to 5.5 V supply. The AD5024/AD5044/AD5064/AD5064-1 also offer a differential accuracy specification of ±1 LSB. The devices use a versatile 3-wire, low power Schmitt trigger serial interface that operates at clock rates up to 50 MHz and is compatible with standard SPI, QSPI™, MICROWIRE, and DSP interface standards. Integrated reference buffers and output amplifiers are also provided on-chip. The AD5024/AD5044/AD5064/AD5064-1 incorporate a power-on reset circuit that ensures the DAC output powers up to zero scale or midscale and remains there until a valid write takes place to the device. The AD5024/AD5044/AD5064/AD5064-1 contain a power-down feature that reduces the current consumption of the device to typically 400 nA at 5 V and provides software selectable output loads while in power-down mode. Total unadjusted error for the devices is <2 mV.

FUNCTIONAL BLOCK DIAGRAMS

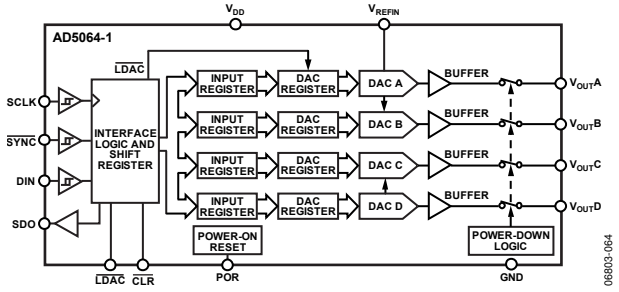

Figure 1. AD5064-1 Functional Equivalent and Pin Compatible with AD5666

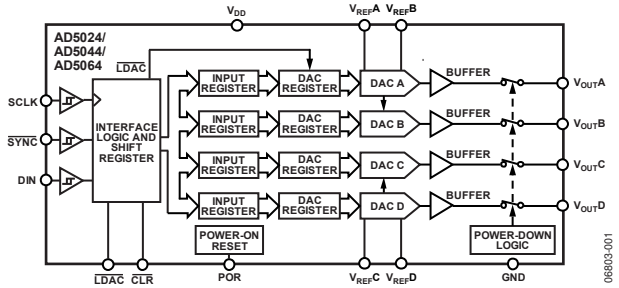

Figure 2. AD5024/AD5044/AD5064 with Individual Reference Pins

PRODUCT HIGHLIGHTS

1. Quad channel available in 14-/16-lead TSSOPs.
2. 16-bit accurate, 1 LSB INL.
3. High speed serial interface with clock speeds up to 50 MHz.
4. Reset to known output voltage (zero scale or midscale).

Table 1. Related Devices

Device No.	Description
AD5666	Quad,16-bit buffered DAC, 16 LSB INL, TSSOP
AD5025/AD5045/AD5065	Dual, 16-bit buffered DACs, 1 LSB INL, TSSOP
AD5062, AD5063	16-bit *nano*DAC, 1 LSB INL, SOT-23, MSOP
AD5061	16-bit *nano*DAC, 4 LSB INL, SOT-23
AD5040/AD5060	14-/16-bit *nano*DAC, 1 LSB INL, SOT-23

Rev. G

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SPECIFICATIONS

V_{DD} = 4.5 V to 5.5 V, R_L = 5 kΩ to GND, C_L = 200 pF to GND, 2.5 V ≤ V_{REFIN} ≤ V_{DD}, unless otherwise specified. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	B Grade[1]			A Grade[1, 2]				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE[3]								
Resolution	16			16			Bits	AD5064/AD5064-1
	14						Bits	AD5044
	12						Bits	AD5024
Relative Accuracy (INL)[4]		±0.5	±1		±0.5	±4	LSB	AD5064/AD5064-1; T_A = −40°C to +105°C
		±0.5	±2		±0.5	±4	LSB	AD5064/AD5064-1; T_A = −40°C to +125°C
		±0.25	±1				LSB	AD5044
		±0.12	±0.5				LSB	AD5024
Differential Nonlinearity (DNL)[4]		±0.2	±1		±0.2	±1	LSB	
Total Unadjusted Error			±2			±2	mV	V_{REF} = 2.5 V, V_{DD} = 5.5 V
Offset Error[4, 5]		±0.2	±1.8		±0.2	±1.8	mV	
Offset Error Temperature Coefficient[4, 6]		±2			±2		µV/°C	
Full-Scale Error[4]		±0.01	±0.07		±0.01	±0.07	% FSR	All 1s loaded to DAC register, $V_{REF} < V_{DD}$
Gain Error[4]		±0.005	±0.05		±0.005	±0.05	% FSR	$V_{REF} < V_{DD}$
Gain Temperature Coefficient[4, 6]		±1			±1		ppm FSR/°C	
DC Crosstalk[4, 6]			40			40	µV	Due to single-channel, full-scale output change, R_L = 5 kΩ to GND or V_{DD}
			40			40	µV/mA	Due to load current change
			40			40	µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[6]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Capacitive Load Stability			1			1	nF	R_L = 5 kΩ, R_L =100 kΩ, and R_L = ∞
DC Output Impedance								
Normal Mode		0.5			0.5		Ω	
Power-Down Mode								
Output Connected to 100 kΩ Network		100			100		kΩ	Output impedance tolerance ± 20 kΩ
Output Connected to 1 kΩ Network		1			1		kΩ	Output impedance tolerance ± 400 Ω
Short-Circuit Current		60			60		mA	DAC = full scale, output shorted to GND
		45			45		mA	DAC = zero scale, output shorted to V_{DD}
Power-Up Time[7]		4.5			4.5		µs	
DC PSRR		−92			−92		dB	V_{DD} ± 10%, DAC = full scale, $V_{REF} < V_{DD}$
REFERENCE INPUTS								
Reference Input Range	2.2		V_{DD}	2.2		V_{DD}	V	
Reference Current		35	50		35	50	µA	Per DAC channel; individual reference option
		140	160		140	160	µA	Single reference option
Reference Input Impedance		120			120		kΩ	Individual reference option
		32			32		kΩ	Single reference option
LOGIC INPUTS								
Input Current[8]			±1			±1	µA	
Input Low Voltage, V_{INL}			0.8			0.8	V	
Input High Voltage, V_{INH}	2.2			2.2			V	
Pin Capacitance[6]		4			4		pF	

Parameter	B Grade[1] Min	B Grade[1] Typ	B Grade[1] Max	A Grade[1, 2] Min	A Grade[1, 2] Typ	A Grade[1, 2] Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (SDO)[9]								
Output Low Voltage, V_{OL}			0.4			0.4	V	I_{SINK} = 2 mA
Output High Voltage, V_{OH}	V_{DD} − 1			V_{DD} − 1				I_{SOURCE} = 2 mA
High Impedance Leakage Current		±0.002	±1		±0.002	±1	µA	
High Impedance Output Capacitance[6]		7			7		pF	
POWER REQUIREMENTS								
V_{DD}	4.5		5.5	4.5		5.5	V	DAC active, excludes load current
I_{DD}[10]								$V_{IH} = V_{DD}$, V_{IL} = GND, Code = midscale
Normal Mode		4	6		4	6	mA	
All Power-Down Modes[11]		0.4	2		0.4	2	µA	T_A = −40°C to +105°C
			30			30	µA	T_A = −40°C to +125°C

[1] Temperature range is −40°C to +125°C, typical at 25°C.
[2] A grade offered in AD5064 only.
[3] Linearity and total unadjusted error are calculated using a reduced code range—AD5064/AD5064-1: Code 512 to Code 65,024; AD5044: Code 128 to Code 16,256; AD5024: Code 32 to Code 4064. Output unloaded.
[4] See the Terminology section.
[5] Offset error calculated using a reduced code range—AD5064/AD5064-1: Code 512 to Code 65,024; AD5044: Code 128 to Code 16,256; AD5024: Code 32 to Code 4064. Output unloaded
[6] Guaranteed by design and characterization; not production tested.
[7] Time to exit power-down mode to normal mode; 32nd clock edge to 90% of DAC midscale value, output unloaded.
[8] Current flowing into individual digital pins. V_{DD} = 5.5 V; V_{REF} = 4.096 V; Code = midscale.
[9] AD5064-1 only.
[10] Interface inactive. All DACs active. DAC outputs unloaded.
[11] All four DACs powered down.

AC CHARACTERISTICS

V_{DD} = 4.5 V to 5.5 V, R_L = 5 kΩ to GND, C_L = 200 pF to GND, 2.5 V ≤ V_{REFIN} ≤ V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments[3]
Output Voltage Settling Time		5.8	8	µs	¼ to ¾ scale and ¾ to ¼ scale settling to ±1 LSB, R_L = 5 kΩ, single-channel update
		10.7	13	µs	¼ to ¾ scale and ¾ to ¼ scale settling to ±1 LSB, R_L = 5 kΩ, all channel update
Slew Rate		1.5		V/µs	
Digital-to-Analog Glitch Impulse		3		nV-sec	1 LSB change around major carry
Reference Feedthrough		−90		dB	V_{REF} = 3 V ± 0.86 V p-p, frequency = 100 Hz to 100 kHz
Digital Feedthrough		0.1		nV-sec	
Digital Crosstalk		1.9		nV-sec	
Analog Crosstalk		2		nV-sec	
DAC-to-DAC Crosstalk		3.5		nV-sec	
AC Crosstalk		6		nV-sec	
Multiplying Bandwidth		340		kHz	V_{REF} = 3 V ± 0.86 V p-p
Total Harmonic Distortion		−80		dB	V_{REF} = 3 V ± 0.2 V p-p, frequency = 10 kHz
Output Noise Spectral Density		64		nV/√Hz	DAC code = 0x8400, frequency = 1 kHz
		60		nV/√Hz	DAC code = 0x8400, frequency = 10 kHz
Output Noise		6		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +125°C, typical at 25°C.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 4 and Figure 5. V_{DD} = 4.5 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1]	Symbol	Min	Typ	Max	Unit
SCLK Cycle Time	t_1	20			ns
SCLK High Time	t_2	10			ns
SCLK Low Time	t_3	10			ns
$\overline{SYNC}$ to SCLK Falling Edge Setup Time	t_4	17			ns
Data Setup Time	t_5	5			ns
Data Hold Time	t_6	5			ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_7	5		30	ns
Minimum $\overline{SYNC}$ High Time (Single Channel Update)	t_8	3			µs
Minimum $\overline{SYNC}$ High Time (All Channel Update)	t_8	8			µs
$\overline{SYNC}$ Rising Edge to SCLK Fall Ignore	t_9	17			ns
$\overline{LDAC}$ Pulse Width Low	t_{10}	20			ns
SCLK Falling Edge to $\overline{LDAC}$ Rising Edge	t_{11}	20			ns
$\overline{CLR}$ Minimum Pulse Width Low	t_{12}	10			ns
SCLK Falling Edge to $\overline{LDAC}$ Falling Edge	t_{13}	10			ns
$\overline{CLR}$ Pulse Activation Time	t_{14}	10.6			µs
SCLK Rising Edge to SDO Valid	t_{15}[2, 3]			22	ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_{16}[2]	5			ns
$\overline{SYNC}$ Rising Edge to SCLK Rising Edge	t_{17}[2]	8			ns
$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$/$\overline{CLR}$ Falling Edge (Single Channel Update)	t_{18}[2]	2			µs
$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$/$\overline{CLR}$ Falling Edge (All Channel Update)	t_{18}[2]	8			µs
Power-up Time[4]		4.5			µs

[1] Maximum SCLK frequency is 50 MHz at V_{DD} = 4.5 V to 5.5 V. Guaranteed by design and characterization; not production tested.
[2] Daisy-chain mode only.
[3] Measured with the load circuit of Figure 3. t_{15} determines the maximum SCLK frequency in daisy-chain mode. AD5064-1 only.
[4] Time to exit power-down mode to normal mode of AD5024/AD5044/AD5064/AD5064-1, 32nd clock edge to 90% of DAC midscale value, with output unloaded.

Circuit and Timing Diagrams

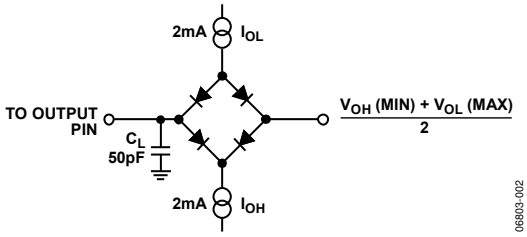
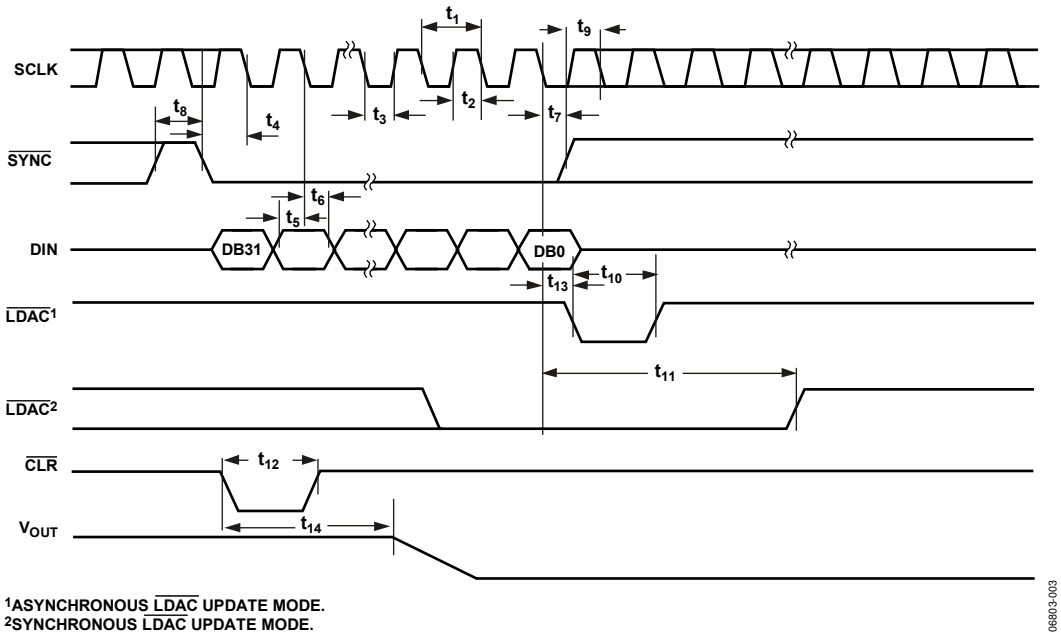
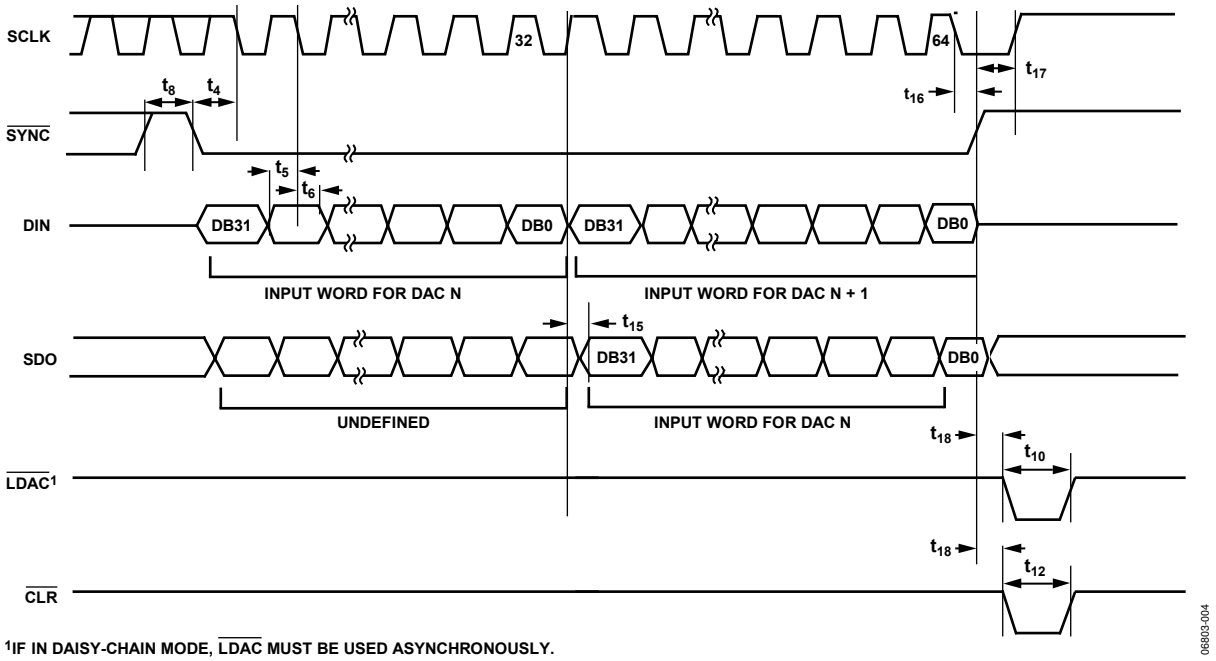


Figure 3. Load Circuit for Digital Output (SDO) Timing Specifications



1ASYNCHRONOUS LDAC UPDATE MODE.
2SYNCHRONOUS LDAC UPDATE MODE.

Figure 4. Serial Write Operation



1IF IN DAISY-CHAIN MODE, LDAC MUST BE USED ASYNCHRONOUSLY.

Figure 5. Daisy-Chain Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\ MAX}$)	150°C
TSSOP	
Power Dissipation	$(T_{J\ MAX} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	113°C/W
Reflow Soldering Peak Temperature	
Pb-Free	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

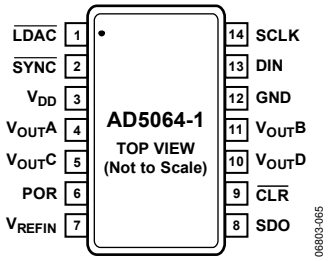


Figure 6. 14-Lead TSSOP (RU-14)

Table 6. 14-Lead TSSOP (RU-14) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{LDAC}}$	$\overline{\text{LDAC}}$ can be operated in two modes, asynchronously and synchronously, as shown in Figure 4. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. This pin can also be tied permanently low in standalone mode. When daisy-chain mode is enabled, this pin cannot be tied permanently low; the $\overline{\text{LDAC}}$ pin should be used in asynchronous $\overline{\text{LDAC}}$ update mode, as shown in Figure 5, and the $\overline{\text{LDAC}}$ pin must be brought high after pulsing.
2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{SYNC}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
3	V_{DD}	Power Supply Input. These devices can be operated from 4.5 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
5	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
6	POR	Power-On Reset Pin. Tying this pin to GND powers up all four DACs to zero scale. Tying this pin to V_{DD} powers up all four DACs to midscale.
7	V_{REFIN}	This is a common pin for reference input for DAC A, DAC B, DAC C, and DAC D.
8	SDO	Serial Data Output. Can be used to daisy-chain a number of AD5064-1 devices together. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock.
9	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the clear code register—zero, midscale, or full scale. Default setting clears the output to 0 V.
10	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
11	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
12	GND	Ground Reference Point for All Circuitry on the Device.
13	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the shift register on the falling edge of the serial clock input.
14	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.

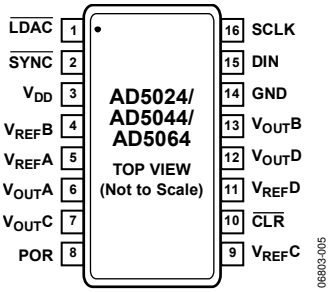


Figure 7. 16-Lead TSSOP (RU-16) Pin Configuration

Table 7. 16-Lead TSSOP (RU-16) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{LDAC}}$	$\overline{\text{LDAC}}$ can be operated in two modes, asynchronously and synchronously, as shown in Figure 4. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. This pin can also be tied permanently low in standalone mode.
2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{SYNC}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
3	V_{DD}	Power Supply Input. These devices can be operated from 4.5 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	$V_{REF}B$	DAC B Reference Input. This is the reference voltage input pin for DAC B.
5	$V_{REF}A$	DAC A Reference Input. This is the reference voltage input pin for DAC A.
6	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
7	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
8	POR	Power-On Reset. Tying this pin to GND powers up the device to 0 V. Tying this pin to V_{DD} powers up the device to midscale.
9	$V_{REF}C$	DAC C Reference Input. This is the reference voltage input pin for DAC C.
10	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the clear code register—zero, midscale, or full scale. Default setting clears the output to 0 V.
11	$V_{REF}D$	DAC D Reference Input. This is the reference voltage input pin for DAC D.
12	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
13	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
14	GND	Ground Reference Point for All Circuitry on the Device.
15	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the shift register on the falling edge of the serial clock input.
16	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

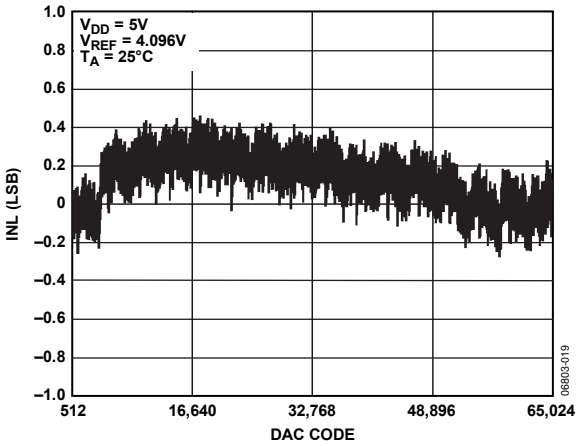


Figure 8. AD5064/AD5064-1 INL

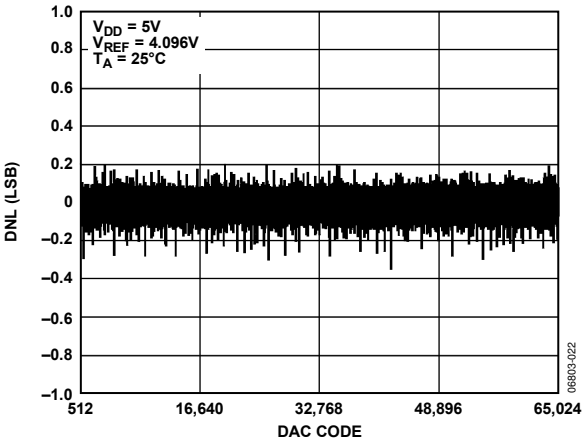


Figure 11. AD5064/AD5064-1 DNL

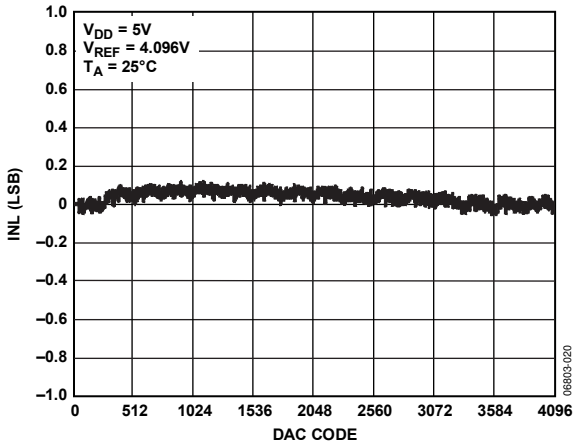


Figure 9. AD5044 INL

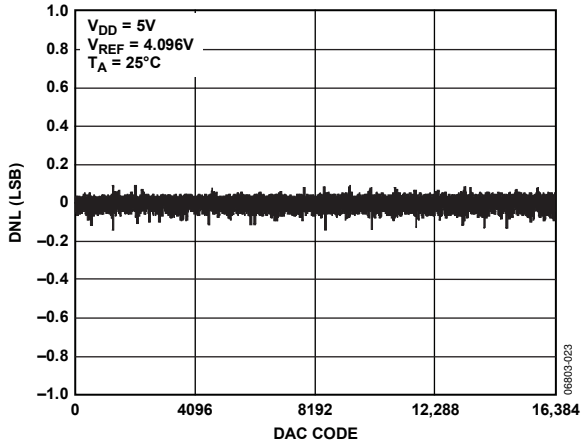


Figure 12. AD5044 DNL

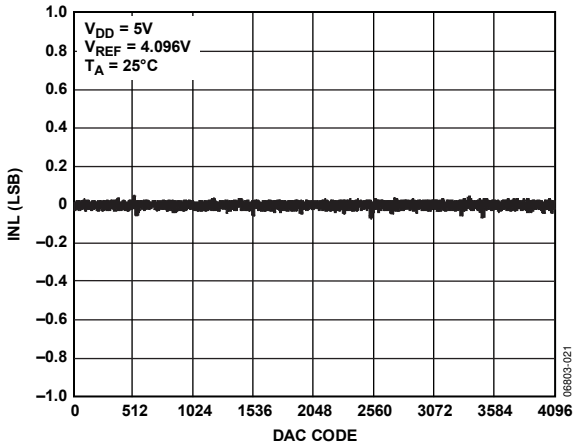


Figure 10. AD5024 INL

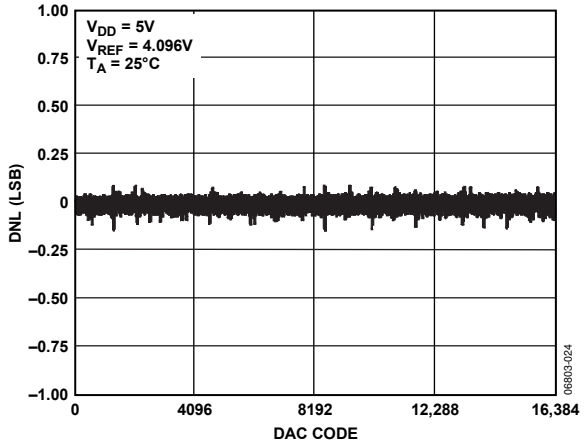


Figure 13. AD5024 DNL

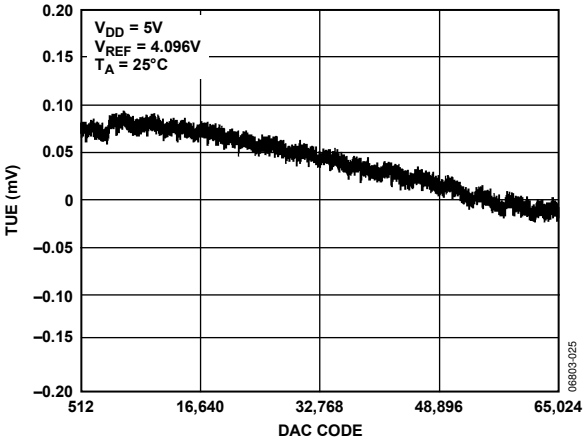


Figure 14. Total Unadjusted Error (TUE)

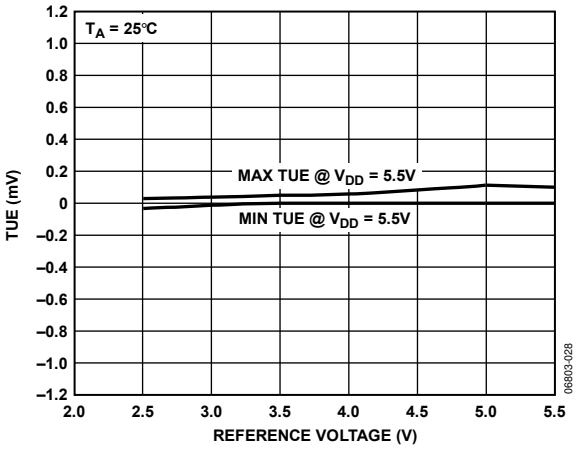


Figure 17. TUE vs. Reference Input Voltage

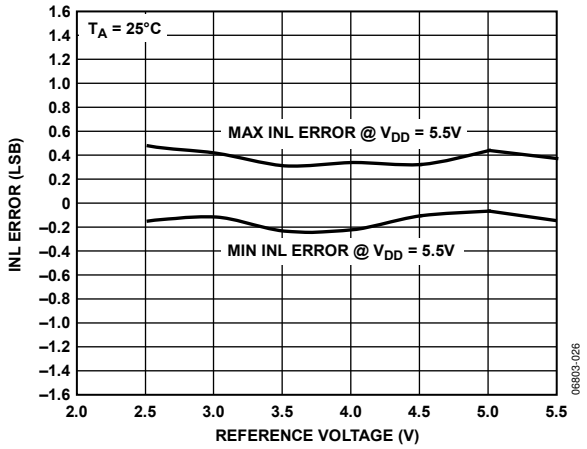


Figure 15. INL vs. Reference Input Voltage

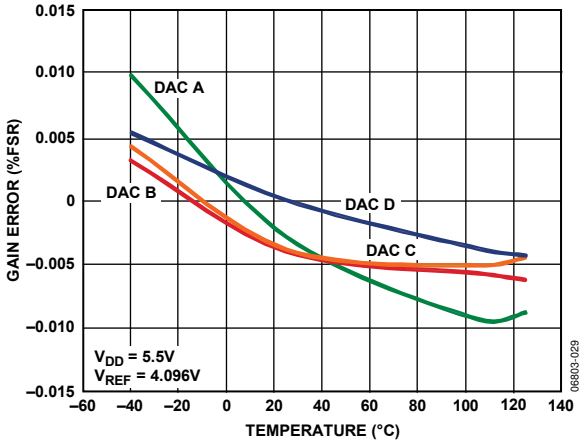


Figure 18. Gain Error vs. Temperature

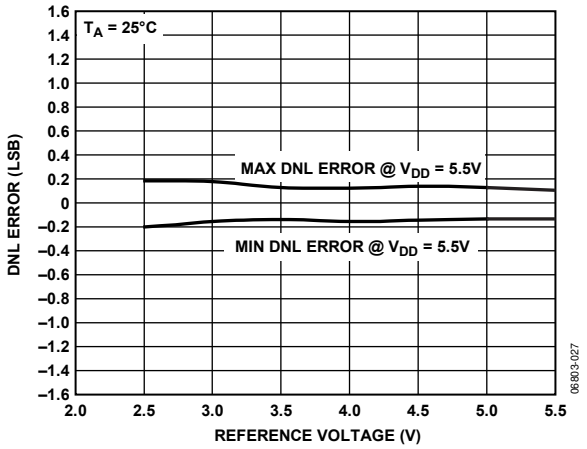


Figure 16. DNL vs. Reference Input Voltage

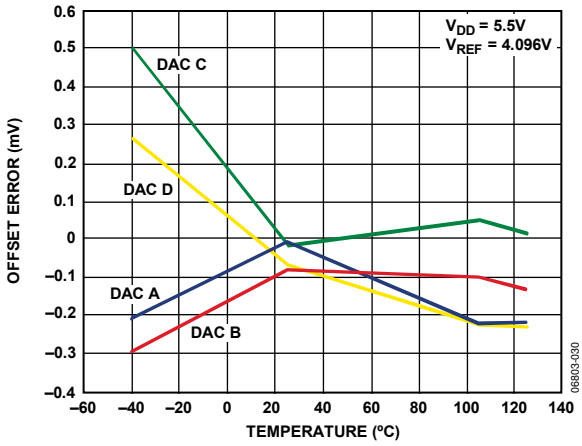


Figure 19. Offset Error vs. Temperature

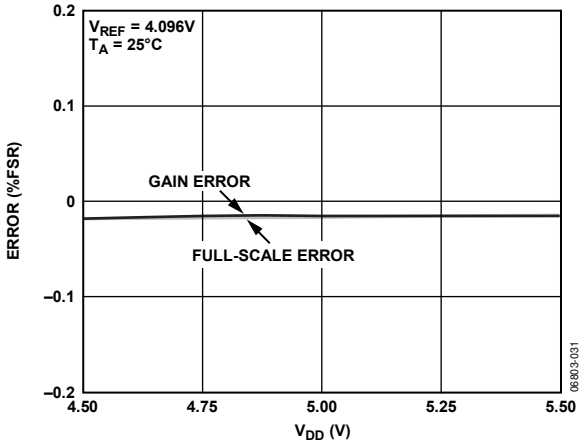


Figure 20. Gain Error and Full-Scale Error vs. Supply Voltage

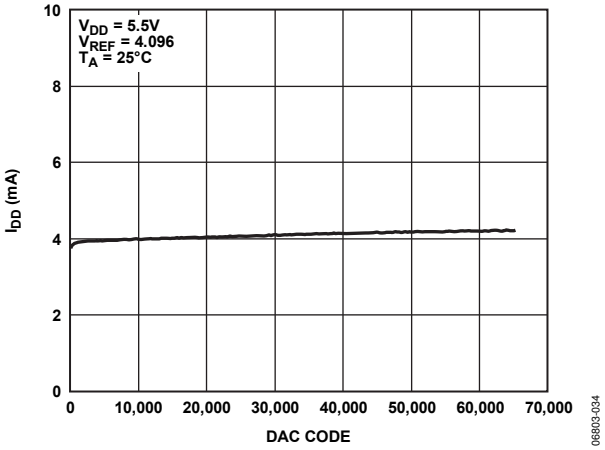


Figure 23. Supply Current vs. Code

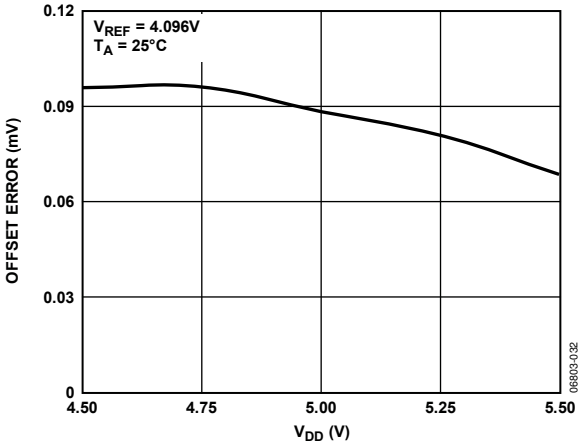


Figure 21. Offset Error Voltage vs. Supply Voltage

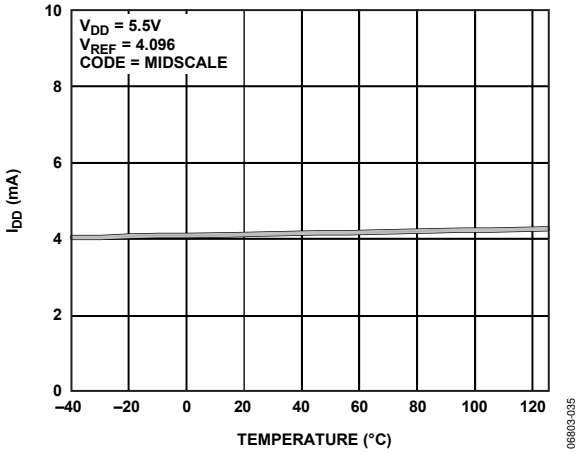


Figure 24. Supply Current vs. Temperature

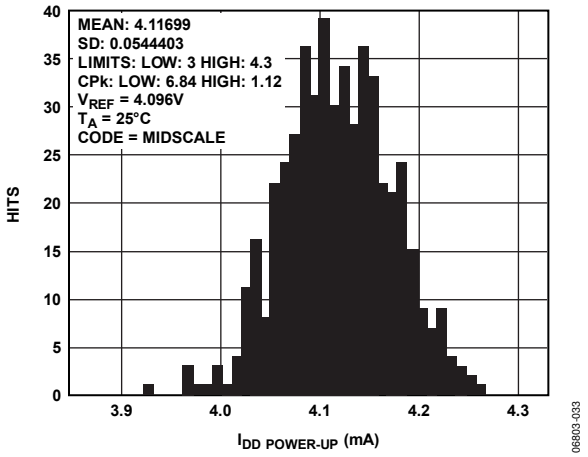


Figure 22. I_{DD} Histogram, V_{DD} = 5.0 V

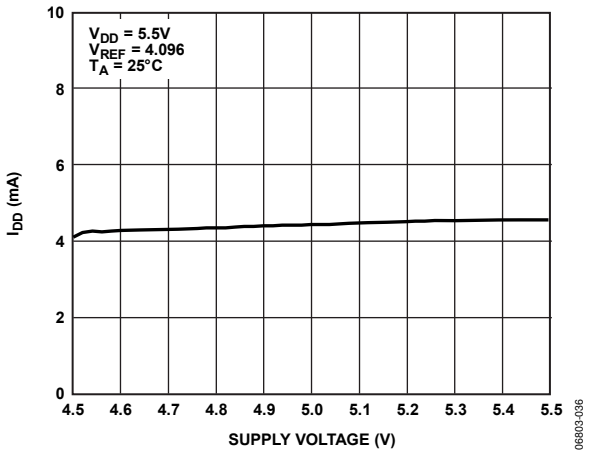


Figure 25. Supply Current vs. Supply Voltage

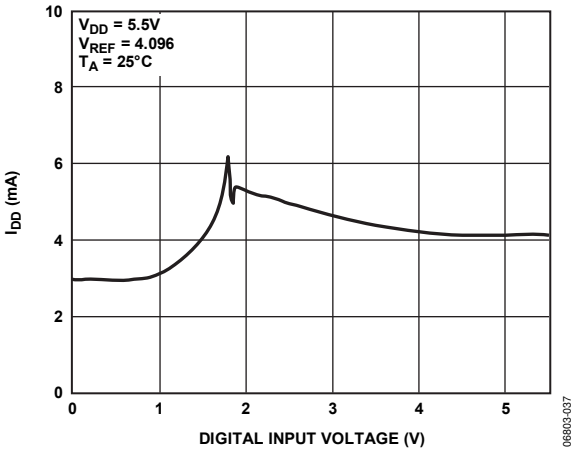


Figure 26. Supply Current vs. Digital Input Voltage

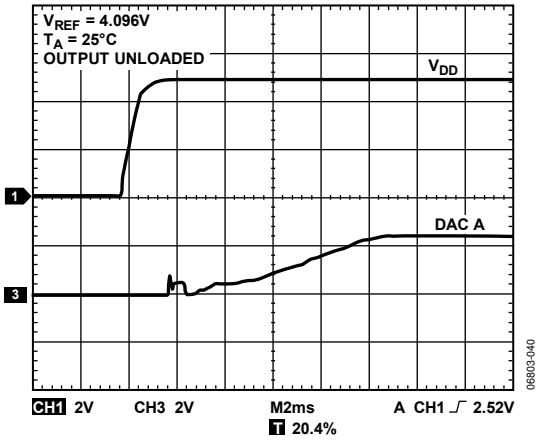


Figure 29. Power-On Reset to Midscale

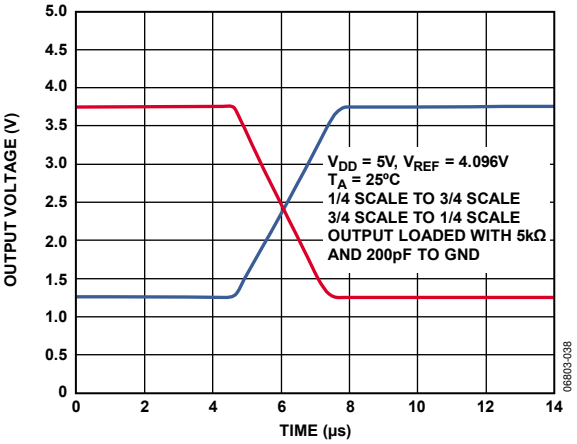


Figure 27. Settling Time

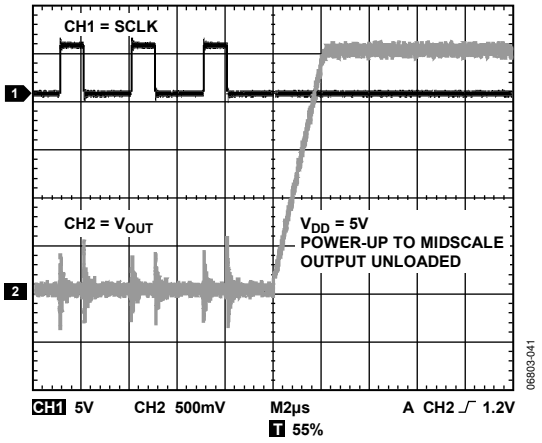


Figure 30. Exiting Power-Down to Midscale

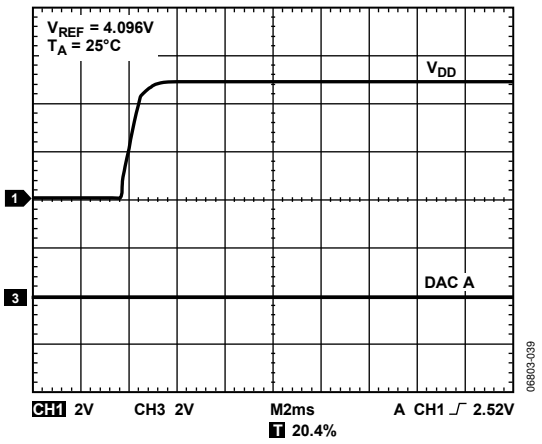


Figure 28. Power-On Reset to 0 V

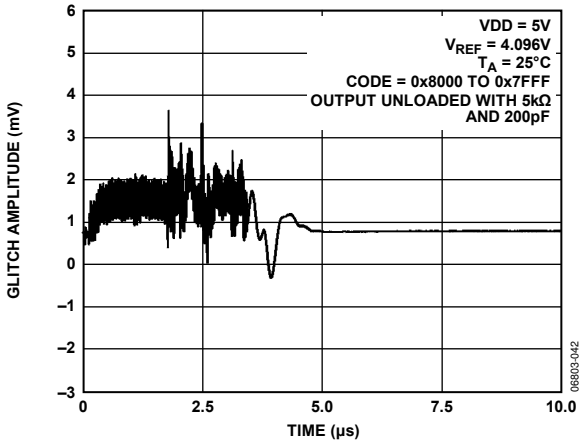


Figure 31. Digital-to-Analog Glitch Impulse

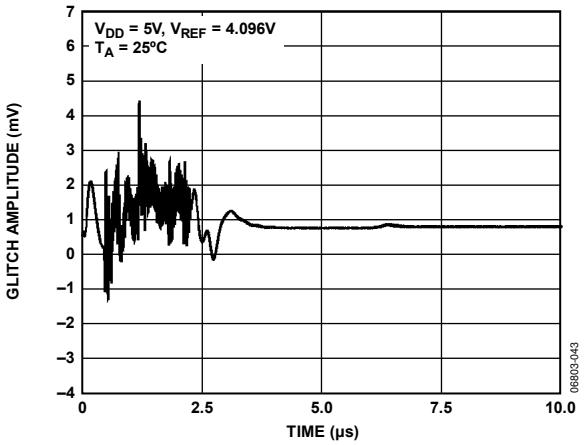


Figure 32. Analog Crosstalk

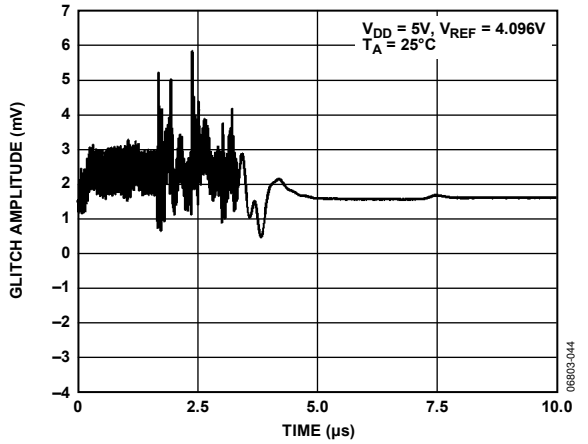


Figure 33. DAC-to-DAC Crosstalk

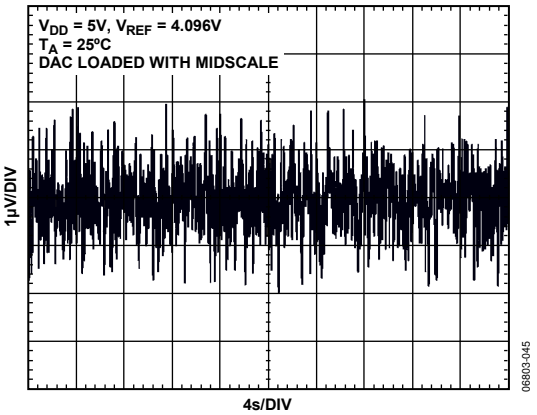


Figure 34. 0.1 Hz to 10 Hz Output Noise Plot

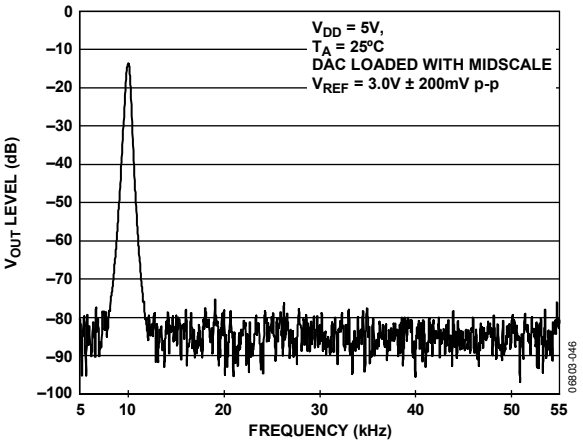


Figure 35. Total Harmonic Distortion

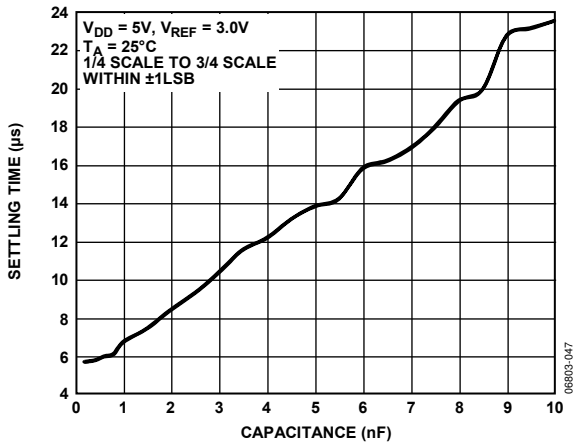


Figure 36. Settling Time vs. Capacitive Load

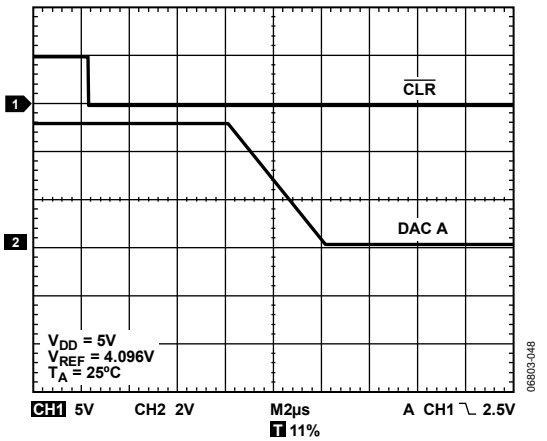


Figure 37. Hardware $\overline{CLR}$

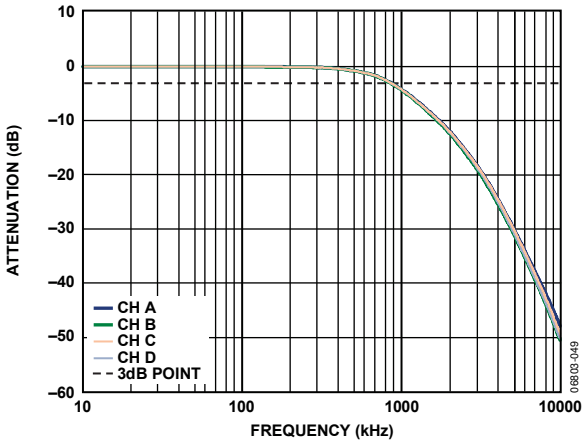


Figure 38. Multiplying Bandwidth

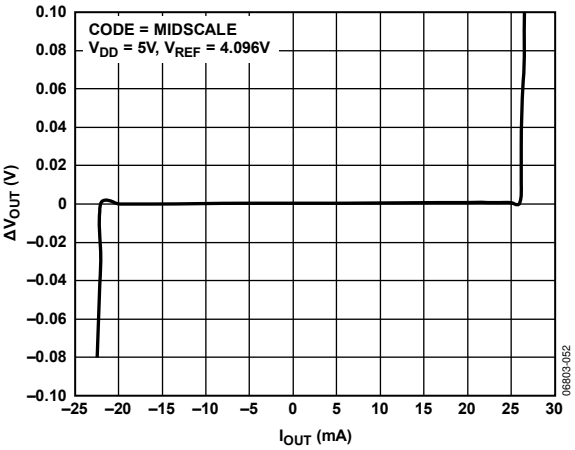


Figure 41. Typical Current Limiting Plot

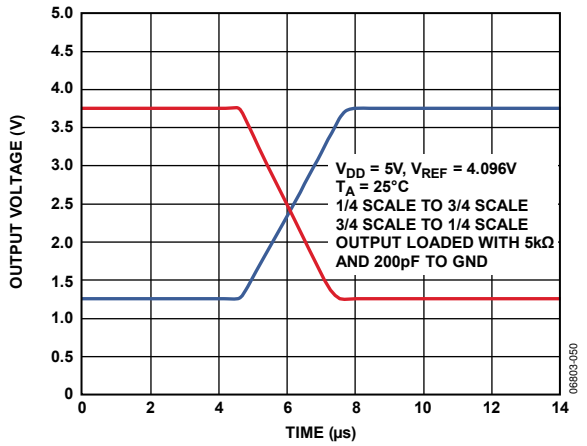


Figure 39. Typical Output Slew Rate

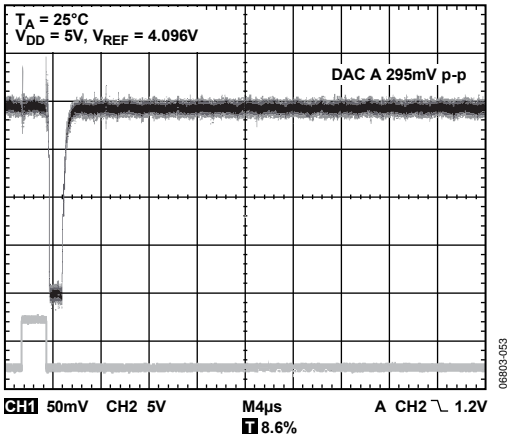


Figure 42. Glitch Upon Entering Power-Down (1 kΩ to GND) from Zero Scale, No Load

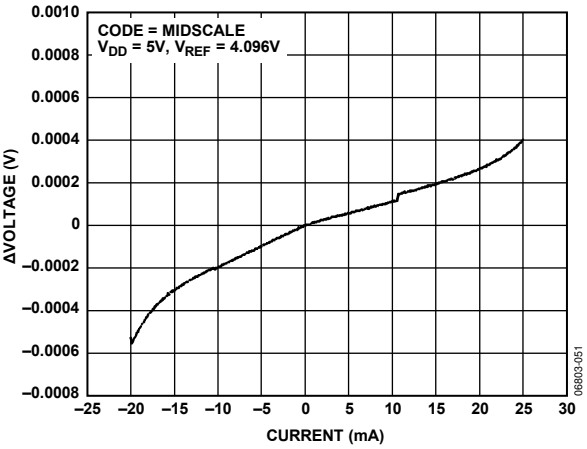


Figure 40. Typical Output Load Regulation

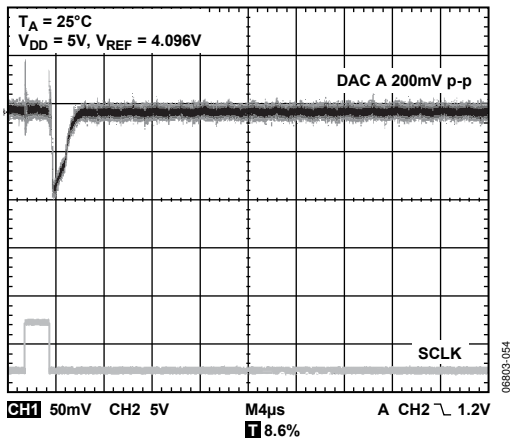


Figure 43. Glitch Upon Entering Power-Down (1 kΩ to GND) from Zero Scale, 5 kΩ/200 pF Load

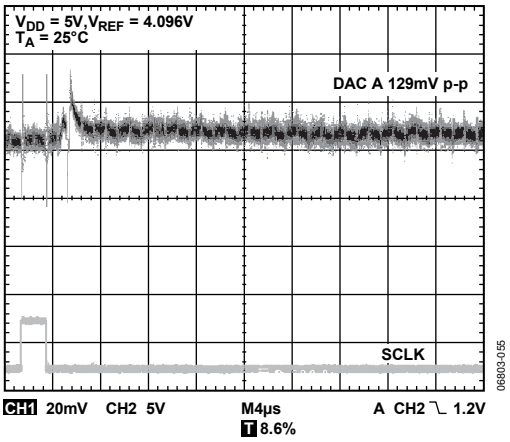


Figure 44. Glitch Upon Exiting Power-Down (1 kΩ to GND) to Zero Scale, No Load

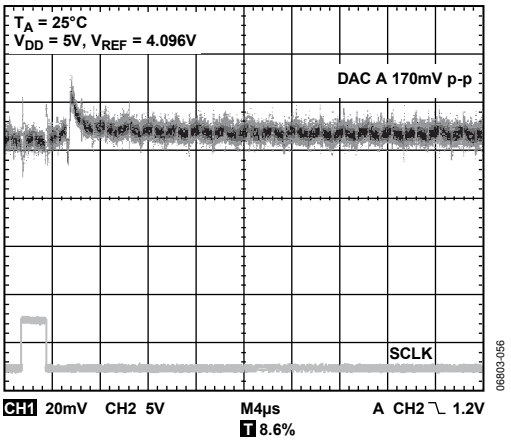


Figure 45. Glitch Upon Exiting Power-Down (1 kΩ to GND) to Zero Scale, 5 kΩ/200 pF Load

TERMINOLOGY

Relative Accuracy (INL)
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function. Figure 8, Figure 9, and Figure 10 show plots of typical INL vs. code.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Figure 11, Figure 12, and Figure 13 show plots of typical DNL vs. code.

Offset Error
Offset error is a measure of the difference between the actual V_{OUT} and the ideal V_{OUT}, expressed in millivolts in the linear region of the transfer function. Offset error is calculated using a reduced code range—AD5064/AD5064-1: Code 512 to Code 65,024; AD5044: Code 128 to Code 16,256; AD5024: Code 32 to Code 4064, with output unloaded. Offset error can be negative or positive and is expressed in millivolts.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range.

Offset Error Temperature Coefficient
Offset error temperature coefficient is a measure of the change in offset error with a change in temperature. It is expressed in microvolts per degree Celsius.

Gain Temperature Coefficient
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in parts per million of full-scale range per degree Celsius.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded into the DAC register. Ideally, the output should be V_{REF} − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range. Measured with $V_{REF} < V_{DD}$.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nanovolt-seconds and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 31.

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in decibels. V_{REF} is held at 2.5 V, and V_{DD} is varied by ±10%. Measured with $V_{REF} < V_{DD}$.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in microvolts.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in microvolts per milliamp.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, $\overline{\text{LDAC}}$ is high). It is expressed in decibels.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device, but it is measured when the DAC is not being written to ($\overline{\text{SYNC}}$ held high). It is specified in nanovolt-seconds and measured with one simultaneous data and clock pulse loaded to the DAC.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s or vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nanovolt-seconds.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s or vice versa) while keeping $\overline{\text{LDAC}}$ high, and then pulsing $\overline{\text{LDAC}}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nanovolt-seconds.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s or vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nanovolt-seconds.

Multiplying Bandwidth
The multiplying bandwidth is a measure of the finite bandwidth of the amplifiers within the DAC. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth, expressed in kilohertz, is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
Total harmonic distortion is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in decibels.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5024/AD5044/AD5064/AD5064-1 are single 12-/14-/16-bit, serial input, voltage output DACs with an individual reference pin. The AD5064-1 model (see the Ordering Guide) is a 16-bit, serial input, voltage output DAC that is identical to other AD5064 models but with a single reference pin for all DACs. The devices operate from supply voltages of 4.5 V to 5.5 V. Data is written to the AD5024/AD5044/AD5064/AD5064-1 in a 32-bit word format via a 3-wire serial interface. The AD5024/AD5044/AD5064/AD5064-1 incorporate a power-on reset circuit that ensures that the DAC output powers up to a known output state. The devices also have a software power-down mode that reduces the typical current consumption to typically 400 nA.

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N} \right)$$

where:
D is the decimal equivalent of the binary code that is loaded to the DAC register (0 to 65,535 for the 16-bit AD5064).
N is the DAC resolution.

DAC ARCHITECTURE

The DAC architecture of the AD5064 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 46. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either GND or the V_{REF} buffer output. The remaining 12 bits of the data-word drive the S0 to S11 switches of a 12-bit voltage mode R-2R ladder network.

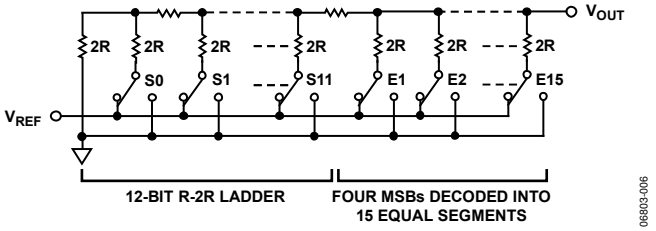


Figure 46. DAC Ladder Structure

REFERENCE BUFFER

The AD5024/AD5044/AD5064/AD5064-1 operate with an external reference. For most models, each DAC has a dedicated voltage reference pin. The AD5064-1 model has a single voltage reference pin for all DACs. The reference input pin has an input range of 2.2 V to V_{DD}. This input voltage is then buffered internally to provide a reference for the DAC core.

OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. The amplifier is capable of driving a load of 5 kΩ in parallel with 200 pF to GND. The slew rate is 1.5 V/μs with a ¼ to ¾ scale settling time of 5.8 μs.

SERIAL INTERFACE

The AD5024/AD5044/AD5064/AD5064-1 have a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most DSPs. See Figure 4 for a timing diagram of a typical write sequence. The AD5064-1 model contains an SDO pin to allow the user to daisy-chain multiple devices together (see the Daisy-Chaining section).

SHIFT REGISTER

The AD5024/AD5044/AD5064/AD5064-1 shift register is 32 bits wide. The first four bits are don't cares. The next four bits are the command bits, C3 to C0 (see Table 8), followed by the 4-bit DAC address bits, A3 to A0 (see Table 9), and finally the bit data-word. The data-word comprises 12-bit, 14-bit, or 16-bit input code, followed by eight, six, or four don't care bits for the AD5024, AD5044, and AD5064/AD5064-1, respectively (see Figure 47, Figure 48, and Figure 49). These data bits are transferred to the DAC register on the 32nd falling edge of SCLK. Commands can be executed on individually selected DAC channels or on all DACs.

Table 8. Command Definitions

Command				
C3	C2	C1	C0	Description
0	0	0	0	Write to Input Register n
0	0	0	1	Update DAC Register n
0	0	1	0	Write to Input Register n, update all (software $\overline{LDAC}$)
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Load clear code register
0	1	1	0	Load $\overline{LDAC}$ register
0	1	1	1	Reset (power-on reset)
1	0	0	0	Set up DCEN register[1] (daisy-chain enable)
1	0	0	1	Reserved
1	1	1	1	Reserved

[1] Available in the AD5064-1 14-lead TSSOP only.

Table 9. Address Commands

Address (n)				
A3	A2	A1	A0	Selected DAC Channel
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
1	1	1	1	All DACs

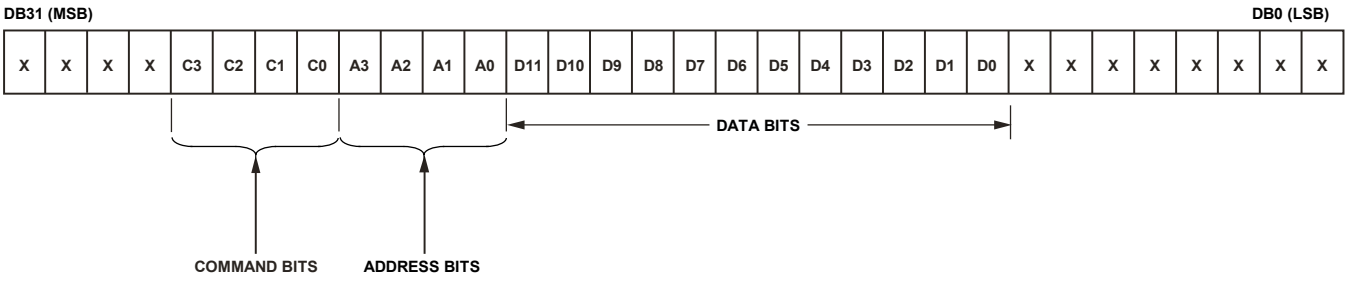


Figure 47. AD5024 Shift Register Content

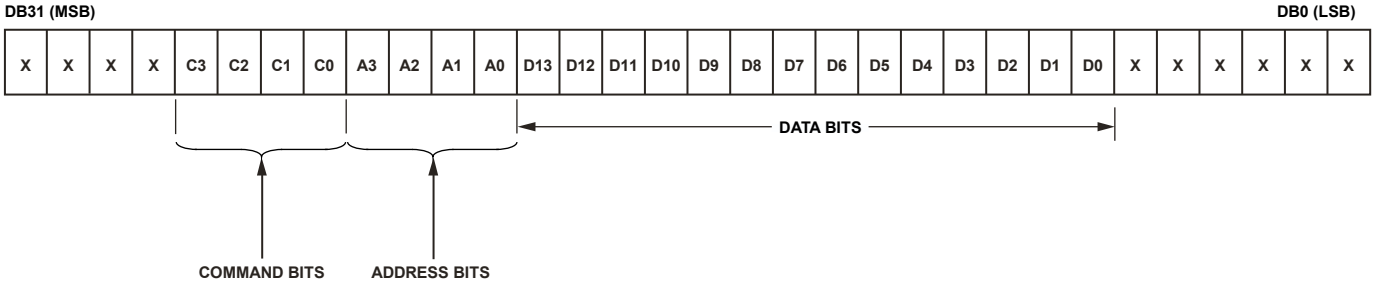


Figure 48. AD5044 Shift Register Content

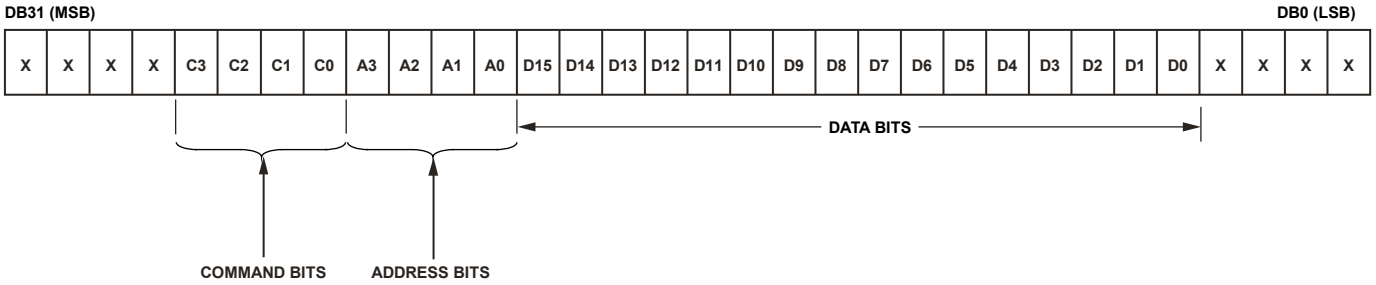


Figure 49. AD5064/AD5064-1 Shift Register Content

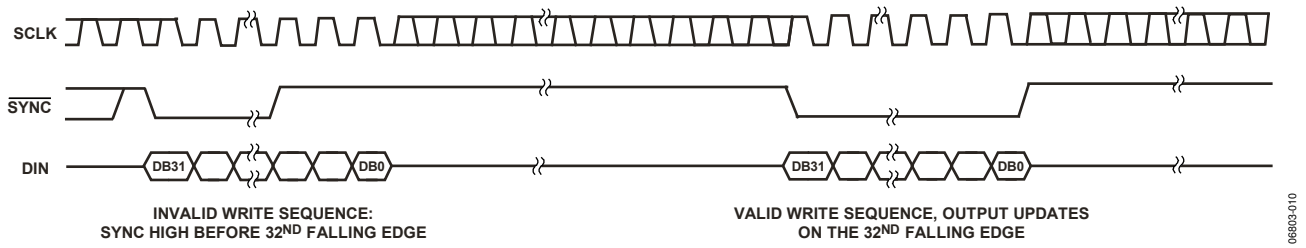


Figure 50. $\overline{SYNC}$ Interrupt Facility

MODES OF OPERATION

There are three main modes of operation: standalone mode where a single device is used, daisy-chain mode for a system that contains several DACs, and power-down mode when the supply current falls to 0.4 µA at 5 V.

Standalone Mode

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line is clocked into the 32-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the AD5024/AD5044/AD5064/AD5064-1 compatible with high speed DSPs. On the 32nd falling clock edge, the last data bit is clocked in and the programmed function is executed, that is, an $\overline{\text{LDAC}}$-dependent change in DAC register contents and/or a change in the mode of operation. At this stage, the $\overline{\text{SYNC}}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 3 µs (single channel, see Table 4, t_8 parameter) before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. $\overline{\text{SYNC}}$ should be idled at rails between write sequences for even lower power operation of the device.

$\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 32 falling edges of SCLK, and the DAC is updated on the 32nd falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 32nd falling edge, this acts as an interrupt to the write sequence. The write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 50).

Daisy-Chaining

For systems that contain several DACs the SDO pin can be used to daisy-chain several devices together and provide serial readback.

The daisy-chain mode is enabled through a software executable daisy-chain enable (DCEN) command. Command 1000 is reserved for this DCEN function (see Table 8). The daisy-chain mode is enabled by setting Bit DB1 in the DCEN register. The default setting is standalone mode, where DB1 = 0.

Table 10 shows how the state of the bit corresponds to the mode of operation of the device.

Table 10. DCEN (Daisy-Chain Enable) Register

DB1	DB0	Description
0	X	Standalone mode (default)
1	X	DCEN mode

The SCLK is continuously applied to the shift register when $\overline{\text{SYNC}}$ is low. If more than 32 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the DIN input on the next DAC in the chain, a daisy-chain interface is constructed. Each DAC in the system requires 32 clock pulses; therefore, the total number of clock cycles must equal 32N, where N is the total number of devices that are updated. If $\overline{\text{SYNC}}$ is taken high at a clock that is not a multiple of 32, it is considered an invalid frame and the data is discarded.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This prevents any further data from being clocked into the shift register.

In daisy-chain mode, the $\overline{\text{LDAC}}$ pin cannot be tied permanently low. The $\overline{\text{LDAC}}$ pin must be used in asynchronous $\overline{\text{LDAC}}$ update mode, as shown in Figure 5. The $\overline{\text{LDAC}}$ pin must be brought high after pulsing. This allows all DAC outputs to simultaneously update.

The serial clock can be continuous or a gated clock. A continuous SCLK source can be used only if $\overline{\text{SYNC}}$ can be held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data.

Table 11. 32-Bit Shift Register Contents for Daisy-Chain Enable

MSB											LSB
DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB2	DB1	DB0
X	1	0	0	0	X	X	X	X	X	1/0	X
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)				Don't cares	DCEN register	

POWER-ON RESET

The AD5024/AD5044/AD5064/AD5064-1 contain a power-on reset circuit that initializes the registers to their default values and controls the output voltage during power-up. By connecting the POR pin low, the AD5024/AD5044/AD5064/AD5064-1 output powers up to zero scale. Note that this is outside the linear region of the DAC; by connecting the POR pin high, the AD5024/AD5044/AD5064/AD5064-1 output powers up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0111 is designated for this reset function (see Table 8). Any events on $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ during power-on reset are ignored. The power-on reset circuit is triggered when V_{DD} passes 2.6 V approximately and takes 50 µs to complete. No writes to the AD5024/AD5044/AD5064/AD5064-1 should take place during this time.

To prevent unintended operation during power-up, control the digital input signals ($\overline{\text{SYNC}}$, SCLK, DIN, $\overline{\text{LDAC}}$, and $\overline{\text{CLR}}$) while the power supply is ramping. Control these signals by using pull-up resistors connected to V_{DD} or GND. For applications that do not require the hardware $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ functions, the $\overline{\text{LDAC}}$ pin and the $\overline{\text{CLR}}$ pin can be tied directly to GND. For applications with a slow V_{DD} ramp time (for example, more than 2 ms to 3 ms), it is recommended that a software reset command is written when the power supplies have reached their final value.

POWER-DOWN MODES

The AD5024/AD5044/AD5064/AD5064-1 contain three separate power-down modes. Command 0100 is designated for the power-down function (see Table 8). These power-down modes are software-programmable by setting two bits, Bit DB9 and Bit DB8, in the shift register. Table 12 shows how the state of the bits corresponds to the mode of operation of the device.

Table 12. Modes of Operation

DB9	DB8	Operating Mode
0	0	Normal operation
		Power-down modes:
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-state

Any or all DACs (DAC D to DAC A) can be powered down to the selected mode by setting the corresponding four bits (DB3, DB2, DB1, DB0) to 1. See Table 13 for the contents of the shift register during power-down/power-up operation.

When both Bit DB9 and Bit D8 in the shift register are set to 0, the device works normally with its normal power consumption of 4 mA at 5 V. However, for the three power-down modes, the supply current falls to 0.4 µA at 5 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while the device is in power-down mode. There are three different power-down options. The output is connected internally to GND through either a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 51.

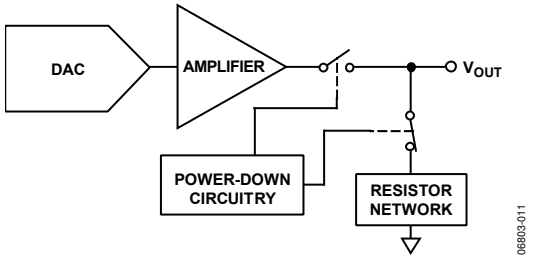


Figure 51. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The DAC register can be updated while the device is in power-down mode. The time to exit power-down is typically 4.5 µs for V_{DD} = 5 V (see Figure 30).

Table 13. 32-Bit Shift Register Contents for Power-Up/Power-Down Function

MSB																LSB
DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB10	DB9	DB8	DB7 to DB4	DB3	DB2	DB1	DB0
X	0	1	0	0	X	X	X	X	X	PD1	PD0	X	DAC D	DAC C	DAC B	DAC A
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)—don't cares				Don't cares	Power-down mode		Don't cares	Power-down/power-up channel selection—set bit to 1 to select			

CLEAR CODE REGISTER

The AD5024/AD5044/AD5064/AD5064-1 have a hardware $\overline{CLR}$ pin that is an asynchronous clear input. The $\overline{CLR}$ input is falling edge sensitive. Bringing the $\overline{CLR}$ line low clears the contents of the input register and the DAC registers to the data contained in the user-configurable $\overline{CLR}$ register and sets the analog outputs accordingly (see Table 14). This function can be used in system calibration or reset to load zero scale, midscale, or full scale to all channels together. Note that zero scale and full scale are outside the linear region of the DAC. These clear code values are user-programmable by setting two bits, Bit DB1 and Bit DB0, in the shift register (see Table 14). The default setting clears the outputs to 0 V. Command 0101 is designated for loading the clear code register (see Table 8).

Table 14. Clear Code Register

DB1 (CR1)	DB0 (CR0)	Clears to Code
0	0	0x0000
0	1	0x8000
1	0	0xFFFF
1	1	No operation

The device exits clear code mode on the 32nd falling edge of the next write to the device. If hardware $\overline{CLR}$ pin is activated during a write sequence, the write is aborted.

The $\overline{CLR}$ pulse activation time, which is the falling edge of $\overline{CLR}$ to when the output starts to change, is typically 10.6 µs. See Table 16 for contents of the shift register while loading the clear code register.

$\overline{LDAC}$ FUNCTION

Hardware $\overline{LDAC}$ Pin

The outputs of all DACs can be updated simultaneously using the hardware $\overline{LDAC}$ pin, as shown in Figure 4. $\overline{LDAC}$ can be permanently low or pulsed. There are two methods of using the hardware $\overline{LDAC}$ pin, synchronously and asynchronously.

Synchronous $\overline{LDAC}$: After new data is read, the DAC registers are updated on the falling edge of the 32nd SCLK pulse, provided $\overline{LDAC}$ is held low.

Asynchronous $\overline{LDAC}$: The outputs are not updated at the same time that the input registers are written to. When $\overline{LDAC}$ is pulsed low, the DAC registers are updated with the contents of the input registers.

Software $\overline{LDAC}$ Function

Alternatively, the outputs of all DACs can be updated simultaneously or individually using the software $\overline{LDAC}$ function by writing to Input Register n and updating all DAC registers. Command 0010 is reserved for this software $\overline{LDAC}$ function. Writing to the DAC using Command 0110 loads the 4-bit $\overline{LDAC}$ register (DB3 to DB0). The default for each channel is 0; that is, the $\overline{LDAC}$ pin works normally. Setting the bits to 1 updates the DAC channel regardless of the state of the hardware $\overline{LDAC}$ pin, so that it effectively sees the hardware $\overline{LDAC}$ pin as being tied low (see Table 15 for the $\overline{LDAC}$ register mode of operation.) This flexibility is useful in applications where the user wants to simultaneously update select channels while the remainder of the channels are synchronously updating.

Table 15. $\overline{LDAC}$ Overwrite Definition

Load $\overline{LDAC}$ Register		
$\overline{LDAC}$ Bits (DB3 to DB0)	$\overline{LDAC}$ Pin	$\overline{LDAC}$ Operation
0	1 or 0	Determined by the $\overline{LDAC}$ pin.
1	X[1]	DAC channels update, overrides the $\overline{LDAC}$ pin. DAC channels see $\overline{LDAC}$ as 0.

[1] X = don't care.

The $\overline{LDAC}$ register gives the user extra flexibility and control over the hardware $\overline{LDAC}$ pin (see Table 17). Setting the $\overline{LDAC}$ bits (DB0 to DB3) to 0 for a DAC channel means that the update of this channel is controlled by the hardware $\overline{LDAC}$ pin.

Table 16. 32-Bit Shift Register Contents for Clear Code Function

MSB											LSB
DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB2	DB1	DB0
X	0	1	0	1	X	X	X	X	X	1/0	1/0
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)				Don't cares	Clear code register (CR1 to CR0)	

Table 17. 32-Bit Shift Register Contents for $\overline{LDAC}$ Overwrite Function

MSB													LSB
DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB4	DB3	DB2	DB1	DB0
X	0	1	1	0	X	X	X	X	X	DAC D	DAC C	DAC B	DAC A
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)—don't cares				Don't cares	Setting $\overline{LDAC}$ bits to 1 overrides $\overline{LDAC}$ pin			

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board (PCB) containing the AD5024/AD5044/AD5064/AD5064-1 should have separate analog and digital sections. If the AD5024/AD5044/AD5064/AD5064-1 are in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5024/AD5044/AD5064/AD5064-1.

The power supply to the AD5024/AD5044/AD5064/AD5064-1 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be as physically close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor have low effective series resistance (ESR) and low effective series inductance (ESI), such as is typical of common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals, if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

MICROPROCESSOR INTERFACING

AD5024/AD5044/AD5064/AD5064-1 to Blackfin ADSP-BF527 Interface

Figure 52 shows a serial interface between the AD5024/AD5044/AD5064/AD5064-1 and the Blackfin® ADSP-BF527 microprocessor. The ADSP-BF527 processor incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5024/AD5044/AD5064/AD5064-1, the setup for the interface is as follows: DT0PRI drives the DIN pin of the AD5024/AD5044/AD5064/AD5064-1, and TSCLK0 drives the SCLK of the devices. The $\overline{\text{SYNC}}$ pin is driven from TFS0.

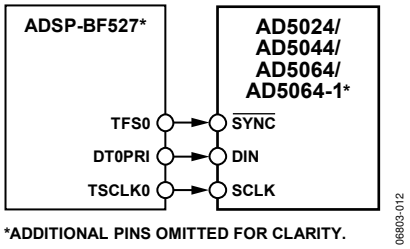


Figure 52. AD5024/AD5044/AD5064/AD5064-1 to Blackfin ADSP-BF527 Interface

AD5024/AD5044/AD5064/AD5064-1 to 68HC11/68L11 Interface

Figure 53 shows a serial interface between the AD5024/AD5044/AD5064/AD5064-1 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5024/AD5044/AD5064/AD5064-1, and the MOSI output drives the serial data line of the DAC.

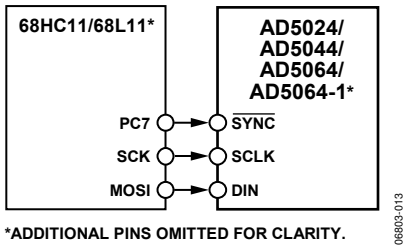


Figure 53. AD5024/AD5044/AD5064/AD5064-1 to 68HC11/68L11 Interface

The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: The 68HC11/68L11 is configured with its CPOL bit as 0, and its CPHA bit as 1. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 is configured as described previously, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5024/AD5044/AD5064, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.

AD5024/AD5044/AD5064/AD5064-1 to 80C51/80L51 Interface

Figure 54 shows a serial interface between the AD5024/AD5044/AD5064/AD5064-1 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TxD of the 80C51/80L51 drives SCLK of the AD5024/AD5044/AD5064/AD5064-1, and RxD drives the serial data line of the device. The $\overline{\text{SYNC}}$ signal is again derived from a bit-programmable pin on the port. In this case, Port Line P3.3 is used. When data is to be transmitted to the AD5024/AD5044/AD5064/AD5064-1, P3.3 is taken low. The 80C51/80L51 transmit data in 8-bit bytes only; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 output the serial data in a format that has the LSB first. The AD5024/AD5044/AD5064/AD5064-1 must receive data with the MSB first. The 80C51/80L51 transmit routine should take this into account.

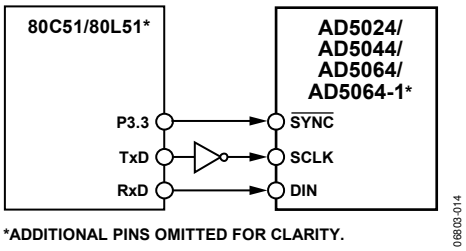


Figure 54. AD5024/AD5044/AD5064/AD5064-1 to 80C512/80L51 Interface

AD5024/AD5044/AD5064/AD5064-1 to MICROWIRE Interface

Figure 55 shows an interface between the AD5024/AD5044/AD5064/AD5064-1 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5024/AD5044/AD5064/AD5064-1 on the rising edge of the SCLK.

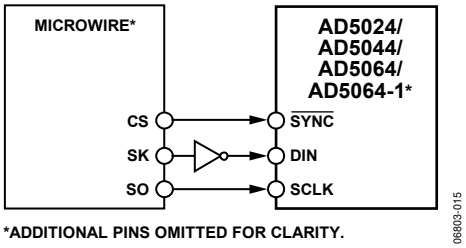


Figure 55. AD5024/AD5044/AD5064/AD5064-1 to MICROWIRE Interface