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Quad Channel, 128-/256-Position, I²C/SPI, Nonvolatile Digital Potentiometer

Data Sheet

AD5124/AD5144/AD5144A

FEATURES

10 kΩ and 100 kΩ resistance options
Resistor tolerance: 8% maximum
Wiper current: ±6 mA
Low temperature coefficient: 35 ppm/°C
Wide bandwidth: 3 MHz
Fast start-up time < 75 µs
Linear gain setting mode
Single- and dual-supply operation
Independent logic supply: 1.8 V to 5.5 V
Wide operating temperature: −40°C to +125°C
4 mm × 4 mm package option
4 kV ESD protection

APPLICATIONS

Portable electronics level adjustment
LCD panel brightness and contrast controls
Programmable filters, delays, and time constants
Programmable power supplies

FUNCTIONAL BLOCK DIAGRAM

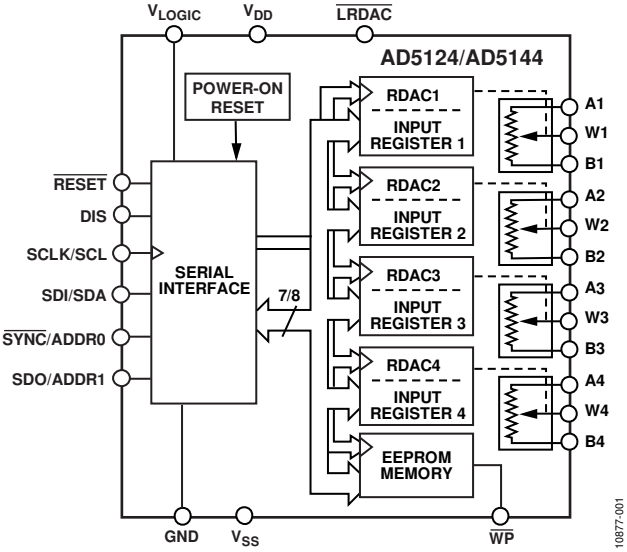

Figure 1. AD5124/AD5144 24-Lead LFCSP

GENERAL DESCRIPTION

The AD5124/AD5144/AD5144A potentiometers provide a nonvolatile solution for 128-/256-position adjustment applications, offering guaranteed low resistor tolerance errors of ±8% and up to ±6 mA current density in the Ax, Bx, and Wx pins.

The low resistor tolerance and low nominal temperature coefficient simplify open-loop applications as well as applications requiring tolerance matching.

The linear gain setting mode allows independent programming of the resistance between the digital potentiometer terminals, through the R_{AW} and R_{WB} string resistors, allowing very accurate resistor matching.

The high bandwidth and low total harmonic distortion (THD) ensure optimal performance for ac signals, making these devices suitable for filter design.

The low wiper resistance of only 40 Ω at the ends of the resistor array allow for pin-to-pin connection.

The wiper values can be set through an SPI-/I²C-compatible digital interface that is also used to read back the wiper register and EEPROM contents.

The AD5124/AD5144/AD5144A are available in a compact, 24-lead, 4 mm × 4 mm LFCSP and a 20-lead TSSOP. The parts are guaranteed to operate over the extended industrial temperature range of −40°C to +125°C.

Table 1. Family Models

Model	Channel	Position	Interface	Package
AD5123[1]	Quad	128	I²C	LFCSP
AD5124	Quad	128	SPI/I²C	LFCSP
AD5124	Quad	128	SPI	TSSOP
AD5143[1]	Quad	256	I²C	LFCSP
AD5144	Quad	256	SPI/I²C	LFCSP
AD5144	Quad	256	SPI	TSSOP
AD5144A	Quad	256	I²C	TSSOP
AD5122	Dual	128	SPI	LFCSP/TSSOP
AD5122A	Dual	128	I²C	LFCSP/TSSOP
AD5142	Dual	256	SPI	LFCSP/TSSOP
AD5142A	Dual	256	I²C	LFCSP/TSSOP
AD5121	Single	128	SPI/I²C	LFCSP
AD5141	Single	256	SPI/I²C	LFCSP

[1] Two potentiometers and two rheostats.

Rev. A Document Feedback

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Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

12/12—Rev. 0 to Rev. A

Changes to Table 12 and Table 13 ... 25

10/12—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAMS—TSSOP

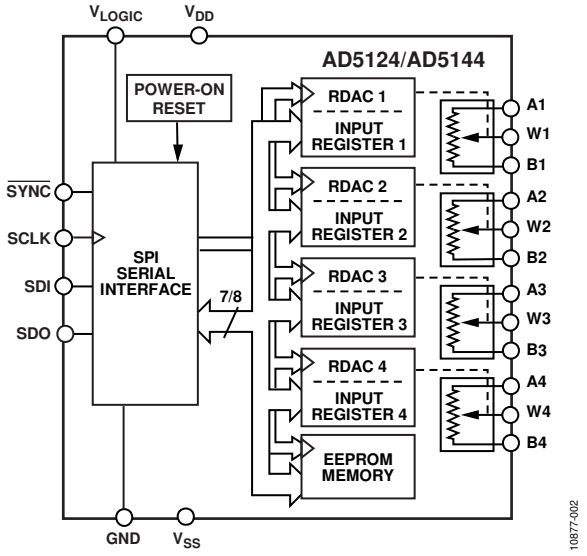

Figure 2. AD5124/AD5144 20-Lead TSSOP

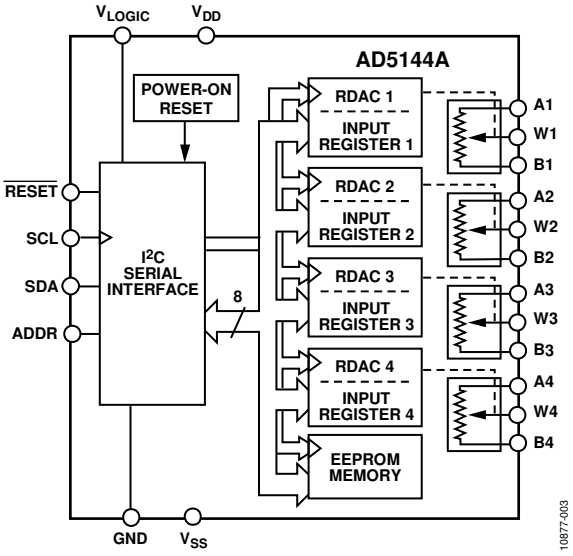

Figure 3. AD5144A 20-Lead TSSOP

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—AD5124

V_{DD} = 2.3 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.25 V to 2.75 V, V_{SS} = −2.25 V to −2.75 V; V_{LOGIC} = 1.8 V to 5.5 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (ALL RDACs)						
Resolution	N		7			Bits
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} = 10 kΩ				
		V_{DD} ≥ 2.7 V	−1	±0.1	+1	LSB
		V_{DD} < 2.7 V	−2.5	±1	+2.5	LSB
		R_{AB} = 100 kΩ				
		V_{DD} ≥ 2.7 V	−0.5	±0.1	+0.5	LSB
		V_{DD} < 2.7 V	−1	±0.25	+1	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−0.5	±0.1	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8	±1	+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance[3]	R_W	Code = zero scale				
		R_{AB} = 10 kΩ		55	125	Ω
		R_{AB} = 100 kΩ		130	400	Ω
Bottom Scale or Top Scale	R_{BS} or R_{TS}					
		R_{AB} = 10 kΩ		40	80	Ω
		R_{AB} = 100 kΩ		60	230	Ω
Nominal Resistance Match	R_{AB1}/R_{AB2}	Code = 0xFF	−1	±0.2	+1	%
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (ALL RDACs)						
Integral Nonlinearity[4]	INL					
		R_{AB} = 10 kΩ	−0.5	±0.1	+0.5	LSB
		R_{AB} = 100 kΩ	−0.25	±0.1	+0.25	LSB
Differential Nonlinearity[4]	DNL		−0.25	±0.1	+0.25	LSB
Full-Scale Error	V_{WFSE}					
		R_{AB} = 10 kΩ	−1.5	−0.1		LSB
		R_{AB} = 100 kΩ	−0.5	±0.1	+0.5	LSB
Zero-Scale Error	V_{WZSE}					
		R_{AB} = 10 kΩ		1	1.5	LSB
		R_{AB} = 100 kΩ		0.25	0.5	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±5		ppm/°C

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
RESISTOR TERMINALS						
Maximum Continuous Current	I_A, I_B, and I_W					
		R_{AB} = 10 kΩ	−6		+6	mA
		R_{AB} = 100 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[3]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale				
		R_{AB} = 10 kΩ		25		pF
		R_{AB} = 100 kΩ		12		pF
Capacitance W[3]	C_W	f = 1 MHz, measured to GND, code = half scale				
		R_{AB} = 10 kΩ		12		pF
		R_{AB} = 100 kΩ		5		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}	V_{LOGIC} = 1.8 V to 2.3 V	0.8 × V_{LOGIC}			V
		V_{LOGIC} = 2.3 V to 5.5 V	0.7 × V_{LOGIC}			V
Low	V_{INL}				0.2 × V_{LOGIC}	V
Input Hysteresis[3]	V_{HYST}		0.1 × V_{LOGIC}			V
Input Current[3]	I_{IN}				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
DIGITAL OUTPUTS						
Output High Voltage[3]	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to V_{LOGIC}		V_{LOGIC}		V
Output Low Voltage[3]	V_{OL}	I_{SINK} = 3 mA			0.4	V
		I_{SINK} = 6 mA, V_{LOGIC} > 2.3 V			0.6	V
Three-State Leakage Current			−1		+1	µA
Three-State Output Capacitance				2		pF
POWER SUPPLIES						
Single-Supply Power Range		V_{SS} = GND	2.3		5.5	V
Dual-Supply Power Range			±2.25		±2.75	V
Logic Supply Range		Single supply, V_{SS} = GND	1.8		V_{DD}	V
		Dual supply, V_{SS} < GND	2.25		V_{DD}	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND				
		V_{DD} = 5.5 V		0.7	5.5	µA
		V_{DD} = 2.3 V		400		nA
Negative Supply Current	I_{SS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND	−5.5	−0.7		µA
EEPROM Store Current[3, 6]	$I_{DD\_EEPROM\_STORE}$	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		2		mA
EEPROM Read Current[3, 7]	$I_{DD\_EEPROM\_READ}$	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		320		µA
Logic Supply Current	I_{LOGIC}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		1	120	nA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		3.5		µW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS} = V_{DD}$ ± 10%, code = full scale		−66	−60	dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[9]						
Bandwidth	BW	−3 dB				
		R_{AB} = 10 kΩ		3		MHz
		R_{AB} = 100 kΩ		0.43		MHz
Total Harmonic Distortion	THD	V_{DD}/V_{SS} = ±2.5 V, V_A = 1 V rms, V_B = 0 V, f = 1 kHz				
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 100 kΩ		−90		dB
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 10 kHz				
		R_{AB} = 10 kΩ		7		nV/√Hz
		R_{AB} = 100 kΩ		20		nV/√Hz
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, from zero scale to full scale, ±0.5 LSB error band				
		R_{AB} = 10 kΩ		2		µs
		R_{AB} = 100 kΩ		12		µs
Crosstalk (C_{W1}/C_{W2})	C_T	R_{AB} = 10 kΩ		10		nV-sec
		R_{AB} = 100 kΩ		25		nV-sec
Analog Crosstalk	C_{TA}			−90		dB
Endurance[10]		T_A = 25°C		1		Mcycles
			100			kcycles
Data Retention[11]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] Resistor integral nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to $(0.7 \times V_{DD})/R_{AB}$.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[6] Different from operating current; supply current for EEPROM program lasts approximately 30 ms.
[7] Different from operating current; supply current for EEPROM read lasts approximately 20 µs.
[8] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{LOGIC} \times V_{LOGIC})$.
[9] All dynamic characteristics use V_{DD}/V_{SS} = ±2.5 V, and V_{LOGIC} = 2.5 V.
[10] Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117 and measured at −40°C to +125°C.
[11] Retention lifetime equivalent at junction temperature (T_J) = 125°C per JEDEC Standard 22, Method A117. Retention lifetime, based on an activation energy of 1 eV, derates with junction temperature in the Flash/EE memory.

ELECTRICAL CHARACTERISTICS—AD5144 AND AD5144A

V_{DD} = 2.3 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.25 V to 2.75 V, V_{SS} = −2.25 V to −2.75 V; V_{LOGIC} = 1.8 V to 5.5 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (ALL RDACs)						
Resolution	N		8			Bits
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} = 10 kΩ				
		V_{DD} ≥ 2.7 V	−2	±0.2	+2	LSB
		V_{DD} < 2.7 V	−5	±1.5	+5	LSB
		R_{AB} = 100 kΩ				
		V_{DD} ≥ 2.7 V	−1	±0.1	+1	LSB
		V_{DD} < 2.7 V	−2	±0.5	+2	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−0.5	±0.2	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8	±1	+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance[3]	R_W	Code = zero scale				
		R_{AB} = 10 kΩ		55	125	Ω
		R_{AB} = 100 kΩ		130	400	Ω
Bottom Scale or Top Scale	R_{BS} or R_{TS}					
		R_{AB} = 10 kΩ		40	80	Ω
		R_{AB} = 100 kΩ		60	230	Ω
Nominal Resistance Match	R_{AB1}/R_{AB2}	Code = 0xFF	−1	±0.2	+1	%
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (ALL RDACs)						
Integral Nonlinearity[4]	INL					
		R_{AB} = 10 kΩ	−1	±0.2	+1	LSB
		R_{AB} = 100 kΩ	−0.5	±0.1	+0.5	LSB
Differential Nonlinearity[4]	DNL		−0.5	±0.2	+0.5	LSB
Full-Scale Error	V_{WFSE}					
		R_{AB} = 10 kΩ	−2.5	−0.1		LSB
		R_{AB} = 100 kΩ	−1	±0.2	+1	LSB
Zero-Scale Error	V_{WZSE}					
		R_{AB} = 10 kΩ		1.2	3	LSB
		R_{AB} = 100 kΩ		0.5	1	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±5		ppm/°C

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
RESISTOR TERMINALS						
Maximum Continuous Current	I_A, I_B, and I_W					
		R_{AB} = 10 kΩ	−6		+6	mA
		R_{AB} = 100 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[3]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale				
		R_{AB} = 10 kΩ		25		pF
		R_{AB} = 100 kΩ		12		pF
Capacitance W[3]	C_W	f = 1 MHz, measured to GND, code = half scale				
		R_{AB} = 10 kΩ		12		pF
		R_{AB} = 100 kΩ		5		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}	V_{LOGIC} = 1.8 V to 2.3 V	0.8 × V_{LOGIC}			V
		V_{LOGIC} = 2.3 V to 5.5 V	0.7 × V_{LOGIC}			V
Low	V_{INL}				0.2 × V_{LOGIC}	V
Input Hysteresis[3]	V_{HYST}		0.1 × V_{LOGIC}			V
Input Current[3]	I_{IN}				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
DIGITAL OUTPUTS						
Output High Voltage[3]	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to V_{LOGIC}		V_{LOGIC}		V
Output Low Voltage[3]	V_{OL}	I_{SINK} = 3 mA			0.4	V
		I_{SINK} = 6 mA, V_{LOGIC} > 2.3 V			0.6	V
Three-State Leakage Current			−1		+1	µA
Three-State Output Capacitance				2		pF
POWER SUPPLIES						
Single-Supply Power Range		V_{SS} = GND	2.3		5.5	V
Dual-Supply Power Range			±2.25		±2.75	V
Logic Supply Range		Single supply, V_{SS} = GND	1.8		V_{DD}	V
		Dual supply, V_{SS} < GND	2.25		V_{DD}	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND				
		V_{DD} = 5.5 V		0.7	5.5	µA
		V_{DD} = 2.3 V		400		nA
Negative Supply Current	I_{SS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND	−5.5	−0.7		µA
EEPROM Store Current[3, 6]	$I_{DD\_EEPROM\_STORE}$	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		2		mA
EEPROM Read Current[3, 7]	$I_{DD\_EEPROM\_READ}$	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		320		µA
Logic Supply Current	I_{LOGIC}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		1	120	nA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		3.5		µW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS} = V_{DD}$ ± 10%, code = full scale		−66	−60	dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[9]						
Bandwidth	BW	−3 dB				
		R_{AB} = 10 kΩ		3		MHz
		R_{AB} = 100 kΩ		0.43		MHz
Total Harmonic Distortion	THD	V_{DD}/V_{SS} = ±2.5 V, V_A = 1 V rms, V_B = 0 V, f = 1 kHz				
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 100 kΩ		−90		dB
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 10 kHz				
		R_{AB} = 10 kΩ		7		nV/√Hz
		R_{AB} = 100 kΩ		20		nV/√Hz
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, from zero scale to full scale, ±0.5 LSB error band				
		R_{AB} = 10 kΩ		2		µs
		R_{AB} = 100 kΩ		12		µs
Crosstalk (C_{W1}/C_{W2})	C_T	R_{AB} = 10 kΩ		10		nV-sec
		R_{AB} = 100 kΩ		25		nV-sec
Analog Crosstalk	C_{TA}			−90		dB
Endurance[10]		T_A = 25°C		1		Mcycles
			100			kcycles
Data Retention[11]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] Resistor integral nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to $(0.7 \times V_{DD})/R_{AB}$.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[6] Different from operating current; supply current for EEPROM program lasts approximately 30 ms.
[7] Different from operating current; supply current for EEPROM read lasts approximately 20 µs.
[8] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{LOGIC} \times V_{LOGIC})$.
[9] All dynamic characteristics use V_{DD}/V_{SS} = ±2.5 V, and V_{LOGIC} = 2.5 V.
[10] Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117 and measured at −40°C to +125°C.
[11] Retention lifetime equivalent at junction temperature (T_J) = 125°C per JEDEC Standard 22, Method A117. Retention lifetime, based on an activation energy of 1 eV, derates with junction temperature in the Flash/EE memory.

INTERFACE TIMING SPECIFICATIONS

V_{LOGIC} = 1.8 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4. SPI Interface

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit	Description
t_1	V_{LOGIC} > 1.8 V	20			ns	SCLK cycle time
	V_{LOGIC} = 1.8 V	30			ns	
t_2	V_{LOGIC} > 1.8 V	10			ns	SCLK high time
	V_{LOGIC} = 1.8 V	15			ns	
t_3	V_{LOGIC} > 1.8 V	10			ns	SCLK low time
	V_{LOGIC} = 1.8 V	15			ns	
t_4		10			ns	$\overline{SYNC}$-to-SCLK falling edge setup time
t_5		5			ns	Data setup time
t_6		5			ns	Data hold time
t_7		10			ns	$\overline{SYNC}$ rising edge to next SCLK fall ignored
t_8[2]		20			ns	Minimum $\overline{SYNC}$ high time
t_9[3]			50		ns	SCLK rising edge to SDO valid
t_{10}				500	ns	$\overline{SYNC}$ rising edge to SDO pin disable

[1] All input signals are specified with $t_r = t_f$ = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[2] Refer to $t_{EEPROM\_PROGRAM}$ and $t_{EEPROM\_READBACK}$ for memory commands operations (see Table 6).
[3] R_{PULL_UP} = 2.2 kΩ to V_{DD} with a capacitance load of 168 pF.

Table 5. I²C Interface

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit	Description
f_{SCL}[2]	Standard mode			100	kHz	Serial clock frequency
	Fast mode			400	kHz	
t_1	Standard mode	4.0			µs	SCL high time, t_{HIGH}
	Fast mode	0.6			µs	
t_2	Standard mode	4.7			µs	SCL low time, t_{LOW}
	Fast mode	1.3			µs	
t_3	Standard mode	250			ns	Data setup time, $t_{SU;\,DAT}$
	Fast mode	100			ns	
t_4	Standard mode	0		3.45	µs	Data hold time, $t_{HD;\,DAT}$
	Fast mode	0		0.9	µs	
t_5	Standard mode	4.7			µs	Setup time for a repeated start condition, $t_{SU;\,STA}$
	Fast mode	0.6			µs	
t_6	Standard mode	4			µs	Hold time (repeated) for a start condition, $t_{HD;\,STA}$
	Fast mode	0.6			µs	
t_7	Standard mode	4.7			µs	Bus free time between a stop and a start condition, t_{BUF}
	Fast mode	1.3			µs	
t_8	Standard mode	4			µs	Setup time for a stop condition, $t_{SU;\,STO}$
	Fast mode	0.6			µs	
t_9	Standard mode			1000	ns	Rise time of SDA signal, t_{RDA}
	Fast mode	20 + 0.1 C_L		300	ns	
t_{10}	Standard mode			300	ns	Fall time of SDA signal, t_{FDA}
	Fast mode	20 + 0.1 C_L		300	ns	
t_{11}	Standard mode			1000	ns	Rise time of SCL signal, t_{RCL}
	Fast mode	20 + 0.1 C_L		300	ns	
t_{11A}	Standard mode			1000	ns	Rise time of SCL signal after a repeated start condition and after an acknowledge bit, t_{RCL1} (not shown in Figure 5)
	Fast mode	20 + 0.1 C_L		300	ns	

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit	Description
t_{12}	Standard mode			300	ns	Fall time of SCL signal, t_{FCL}
	Fast mode	20 + 0.1 C_L		300	ns	
t_{SP}[3]	Fast mode	0		50	ns	Pulse width of suppressed spike

[1] Maximum bus capacitance is limited to 400 pF.
[2] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate; however, it has a negative effect on the EMC behavior of the part.
[3] Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns for fast mode.

Table 6. Control Pins

Parameter	Min	Typ	Max	Unit	Description
t_1	1			µs	End command to $\overline{\text{LRDAC}}$ falling edge
t_2	50			ns	Minimum $\overline{\text{LRDAC}}$ low time
t_3	0.1		10	µs	$\overline{\text{RESET}}$ low time
$t_{EEPROM\_PROGRAM}$[1]		15	50	ms	Memory program time (not shown in Figure 8)
$t_{EEPROM\_READBACK}$		7	30	µs	Memory readback time (not shown in Figure 8)
t_{POWER_UP}[2]			75	µs	Start-up time (not shown in Figure 8)
t_{RESET}		30		µs	Reset EEPROM restore time (not shown in Figure 8)

[1] EEPROM program time depends on the temperature and EEPROM write cycles. Higher timing is expected at lower temperatures and higher write cycles.
[2] Maximum time after $V_{DD} - V_{SS}$ is equal to 2.3 V.

SHIFT REGISTER AND TIMING DIAGRAMS

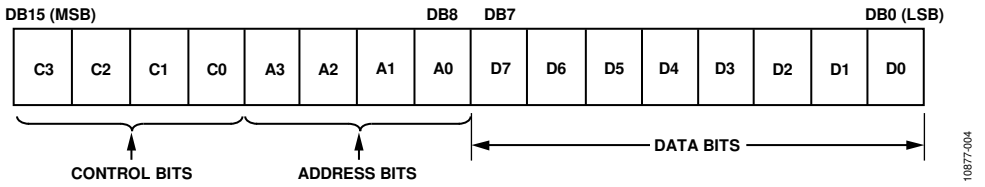

Figure 4. Input Shift Register Contents

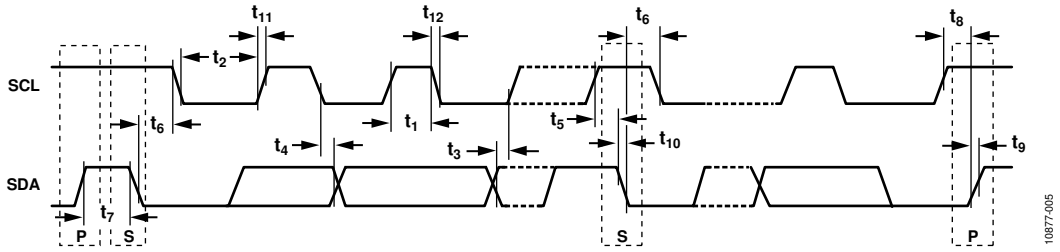

Figure 5. I²C Serial Interface Timing Diagram (Typical Write Sequence)

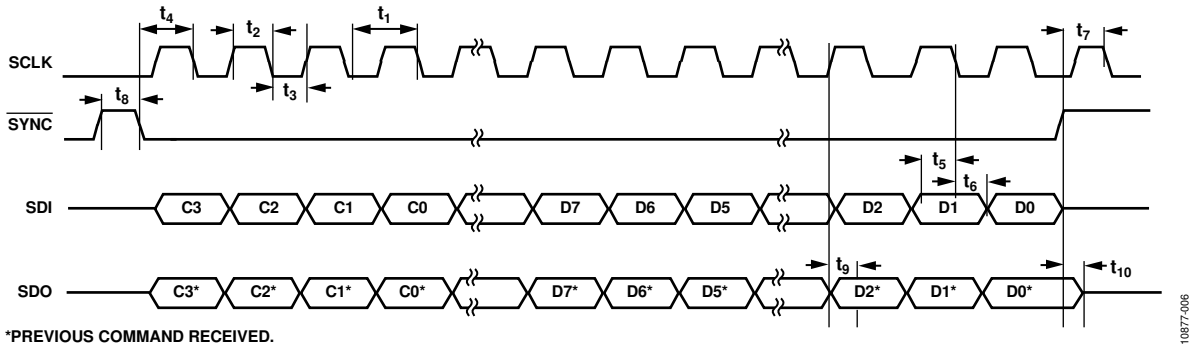

Figure 6. SPI Serial Interface Timing Diagram, CPOL = 0, CPHA = 1

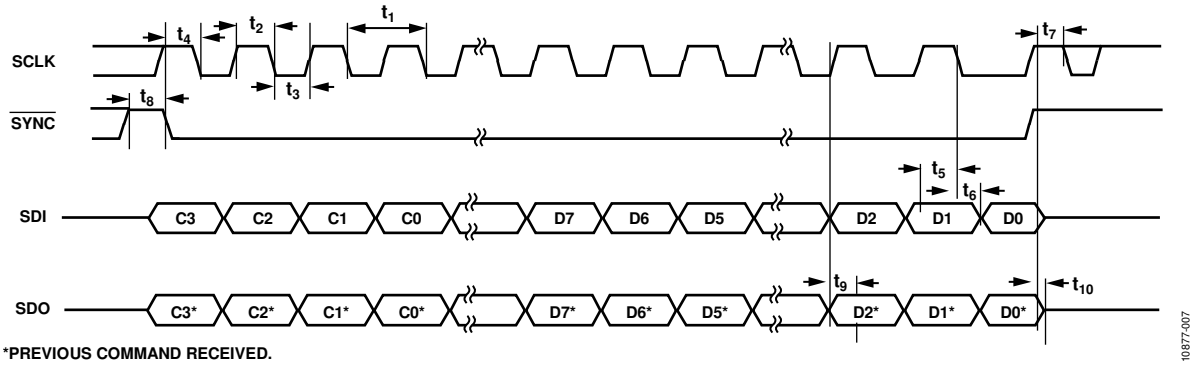

Figure 7. SPI Serial Interface Timing Diagram, CPOL = 1, CPHA = 0

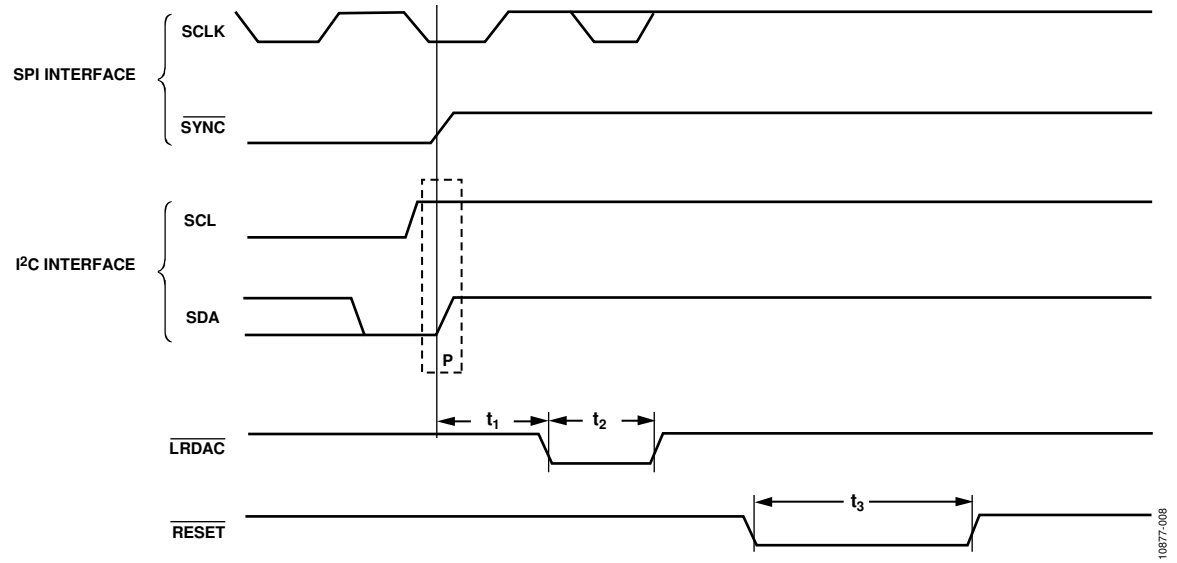

Figure 8. Control Pins Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
V_{SS} to GND	+0.3 V to −7.0 V
V_{DD} to V_{SS}	7 V
V_{LOGIC} to GND	−0.3 V to V_{DD} + 0.3 V or +7.0 V (whichever is less)
V_A, V_W, V_B to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V
I_A, I_W, I_B	
Pulsed[1]	
Frequency > 10 kHz	
R_{AW} = 10 kΩ	±6 mA/d^2[2]
R_{AW} = 100 kΩ	±1.5 mA/d^2
Frequency ≤ 10 kHz	
R_{AW} = 10 kΩ	±6 mA/$\sqrt{d^2}$
R_{AW} = 100 kΩ	±1.5 mA/$\sqrt{d^2}$
Digital Inputs	−0.3 V to V_{LOGIC} + 0.3 V or +7 V (whichever is less)
Operating Temperature Range, T_A[3]	−40°C to +125°C
Maximum Junction Temperature, T_J Maximum	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	(T_J max − T_A)/θ_{JA}
ESD[4]	4 kV
FICDM	1.5 kV

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] d = pulse duty factor.
[3] Includes programming of EEPROM memory.
[4] Human body model (HBM) classification.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is defined by the JEDEC JESD51 standard, and the value is dependent on the test board and test environment.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead LFCSP	35[1]	3	°C/W
20-Lead TSSOP	143[1]	45	°C/W

[1] JEDEC 2S2P test board, still air (0 m/sec airflow).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

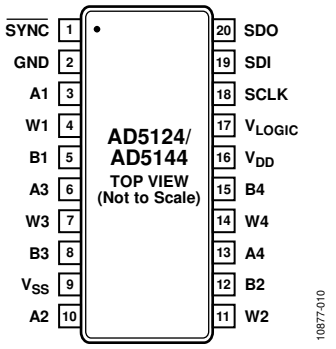

Figure 9. 20-Lead TSSOP, SPI Interface Pin Configuration (AD5124/AD5144)

Table 9. 20-Lead TSSOP, SPI Interface Pin Function Descriptions (AD5124/AD5144)

Pin No.	Mnemonic	Description
1	$\overline{\text{SYNC}}$	Synchronization Data Input, Active Low. When $\overline{\text{SYNC}}$ returns high, data is loaded into the input shift register.
2	GND	Ground Pin, Logic Ground Reference.
3	A1	Terminal A of RDAC1. $V_{SS} \le V_A \le V_{DD}$.
4	W1	Wiper Terminal of RDAC1. $V_{SS} \le V_W \le V_{DD}$.
5	B1	Terminal B of RDAC1. $V_{SS} \le V_B \le V_{DD}$.
6	A3	Terminal A of RDAC3. $V_{SS} \le V_A \le V_{DD}$.
7	W3	Wiper Terminal of RDAC3. $V_{SS} \le V_W \le V_{DD}$.
8	B3	Terminal B of RDAC3. $V_{SS} \le V_B \le V_{DD}$.
9	V_{SS}	Negative Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
10	A2	Terminal A of RDAC2. $V_{SS} \le V_A \le V_{DD}$.
11	W2	Wiper Terminal of RDAC2. $V_{SS} \le V_W \le V_{DD}$.
12	B2	Terminal B of RDAC2. $V_{SS} \le V_B \le V_{DD}$.
13	A4	Terminal A of RDAC4. $V_{SS} \le V_A \le V_{DD}$.
14	W4	Wiper Terminal of RDAC4. $V_{SS} \le V_W \le V_{DD}$.
15	B4	Terminal B of RDAC4. $V_{SS} \le V_B \le V_{DD}$.
16	V_{DD}	Positive Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
17	V_{LOGIC}	Logic Power Supply; 1.8 V to V_{DD}. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
18	SCLK	Serial Clock Line. Data is clocked in at the logic low transition.
19	SDI	Serial Data Input.
20	SDO	Serial Data Output. This is an open-drain output pin, and it needs an external pull-up resistor.

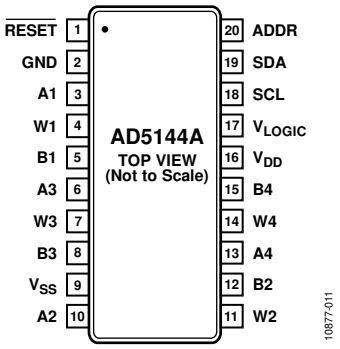

Figure 10. 20-Lead TSSOP, I²C Interface Pin Configuration (AD5144A)

Table 10. 20-Lead TSSOP, I²C Interface Pin Function Descriptions (AD5144A)

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Hardware Reset Pin. Refresh the RDAC registers from EEPROM. $\overline{\text{RESET}}$ is activated at the logic low. If this pin is not used, tie $\overline{\text{RESET}}$ to V_{LOGIC}.
2	GND	Ground Pin, Logic Ground Reference.
3	A1	Terminal A of RDAC1. $V_{SS} \le V_A \le V_{DD}$.
4	W1	Wiper Terminal of RDAC1. $V_{SS} \le V_W \le V_{DD}$.
5	B1	Terminal B of RDAC1. $V_{SS} \le V_B \le V_{DD}$.
6	A3	Terminal A of RDAC3. $V_{SS} \le V_A \le V_{DD}$.
7	W3	Wiper Terminal of RDAC3. $V_{SS} \le V_W \le V_{DD}$.
8	B3	Terminal B of RDAC3. $V_{SS} \le V_B \le V_{DD}$.
9	V_{SS}	Negative Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
10	A2	Terminal A of RDAC2. $V_{SS} \le V_A \le V_{DD}$.
11	W2	Wiper Terminal of RDAC2. $V_{SS} \le V_W \le V_{DD}$.
12	B2	Terminal B of RDAC2. $V_{SS} \le V_B \le V_{DD}$.
13	A4	Terminal A of RDAC4. $V_{SS} \le V_A \le V_{DD}$.
14	W4	Wiper Terminal of RDAC4. $V_{SS} \le V_W \le V_{DD}$.
15	B4	Terminal B of RDAC4. $V_{SS} \le V_B \le V_{DD}$.
16	V_{DD}	Positive Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
17	V_{LOGIC}	Logic Power Supply; 1.8 V to V_{DD}. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
18	SCL	Serial Clock Line. Data is clocked in at the logic low transition.
19	SDA	Serial Data Input/Output.
20	ADDR	Programmable Address for Multiple Package Decoding.

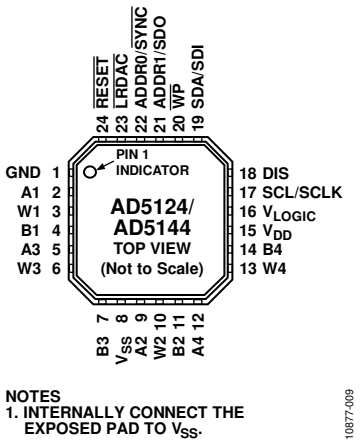

Figure 11. 24-Lead LFCSP Pin Configuration (AD5124/AD5144)

Table 11. 24-Lead LFCSP Pin Function Descriptions (AD5124/AD5144)

Pin No.	Mnemonic	Description
1	GND	Ground Pin, Logic Ground Reference.
2	A1	Terminal A of RDAC1. $V_{SS} \le V_A \le V_{DD}$.
3	W1	Wiper Terminal of RDAC1. $V_{SS} \le V_W \le V_{DD}$.
4	B1	Terminal B of RDAC1. $V_{SS} \le V_B \le V_{DD}$.
5	A3	Terminal A of RDAC3. $V_{SS} \le V_A \le V_{DD}$.
6	W3	Wiper Terminal of RDAC3. $V_{SS} \le V_W \le V_{DD}$.
7	B3	Terminal B of RDAC3. $V_{SS} \le V_B \le V_{DD}$.
8	V_{SS}	Negative Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
9	A2	Terminal A of RDAC2. $V_{SS} \le V_A \le V_{DD}$.
10	W2	Wiper Terminal of RDAC2. $V_{SS} \le V_W \le V_{DD}$.
11	B2	Terminal B of RDAC2. $V_{SS} \le V_B \le V_{DD}$.
12	A4	Terminal A of RDAC4. $V_{SS} \le V_A \le V_{DD}$.
13	W4	Wiper Terminal of RDAC4. $V_{SS} \le V_W \le V_{DD}$.
14	B4	Terminal B of RDAC4. $V_{SS} \le V_B \le V_{DD}$.
15	V_{DD}	Positive Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
16	V_{LOGIC}	Logic Power Supply; 1.8 V to V_{DD}. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
17	SCL/SCLK	I^2C Serial Clock Line (SCL). Data is clocked in at the logic low transition. SPI Serial Clock Line (SCLK). Data is clocked in at the logic low transition.
18	DIS	Digital Interface Select (SPI/I^2C Select). SPI when DIS = 0 (GND), and I^2C when DIS = 1 (V_{LOGIC}). This pin cannot be left floating.
19	SDA/SDI	Serial Data Input/Output (SDA), When DIS = 1. Serial Data Input (SDI), When DIS = 0.
20	$\overline{WP}$	Optional Write Protect. This pin prevents any changes to the present RDAC and EEPROM content, except when reloading the content of the EEPROM into the RDAC register. $\overline{WP}$ is activated at logic low. If this pin is not used, tie $\overline{WP}$ to V_{LOGIC}.
21	ADDR1/SDO	Programmable Address (ADDR1) for Multiple Package Decoding, When DIS = 1. Serial Data Output (SDO). Open-drain output, needs an external pull-up resistor, when DIS = 0.
22	ADDR0/$\overline{SYNC}$	Programmable Address (ADDR0) for Multiple Package Decoding, When DIS = 1. Synchronization Data Input, When DIS = 0. This pin is active low. When $\overline{SYNC}$ returns high, data is loaded into the input shift register.
23	$\overline{LRDAC}$	Load RDAC. Transfers the contents of the input registers to their respective RDAC registers when their associated input registers were previously loaded using Command 2 (see Table 20). This allows simultaneous update of all RDAC registers. $\overline{LRDAC}$ is activated at the high-to-low transition. If not used, tie $\overline{LRDAC}$ to V_{LOGIC}.
24	$\overline{RESET}$	Hardware Reset Pin. Refresh the RDAC registers from EEPROM. $\overline{RESET}$ is activated at the logic low. If not used, tie $\overline{RESET}$ to V_{LOGIC}.
	EPAD	Internally Connect the Exposed Pad to V_{SS}.

TYPICAL PERFORMANCE CHARACTERISTICS

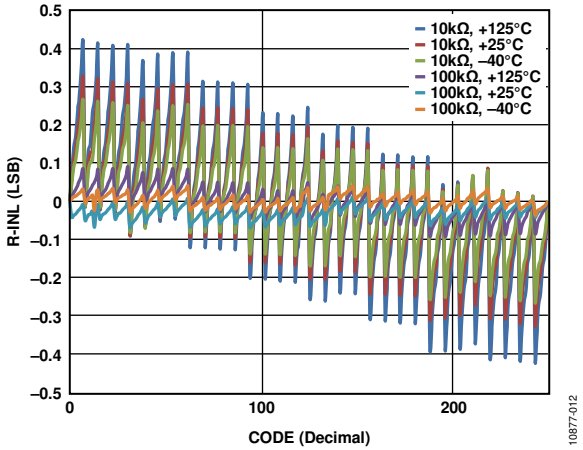

Figure 12. R-INL vs. Code (AD5144/AD5144A)

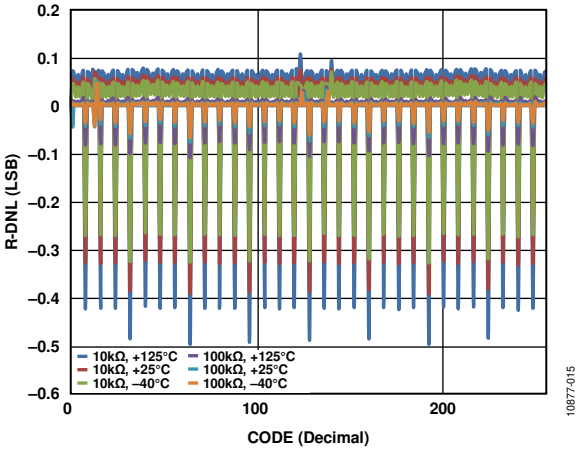

Figure 15. R-DNL vs. Code (AD5144/AD5144A)

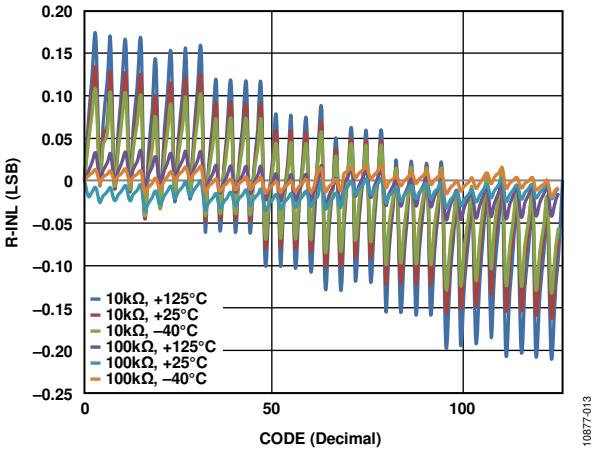

Figure 13. R-INL vs. Code (AD5124)

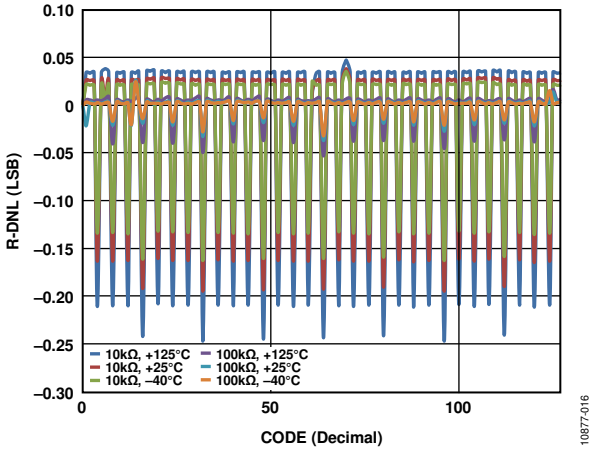

Figure 16. R-DNL vs. Code (AD5124)

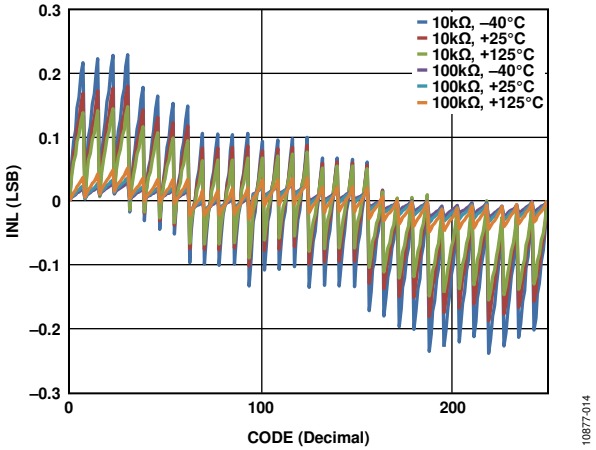

Figure 14. INL vs. Code (AD5144/AD5144A)

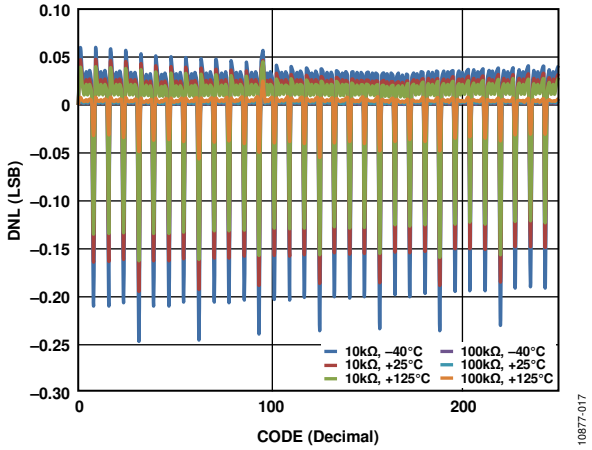

Figure 17. DNL vs. Code (AD5144/AD5144A)

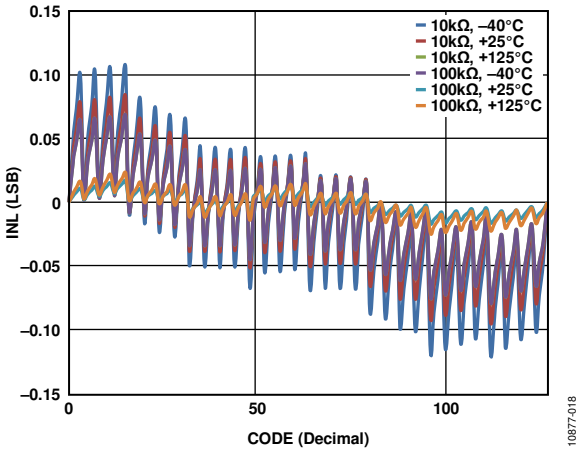

Figure 18. INL vs. Code (AD5124)

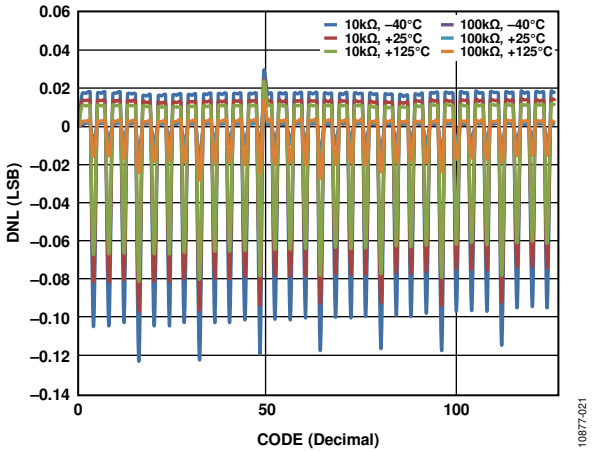

Figure 21. DNL vs. Code (AD5124)

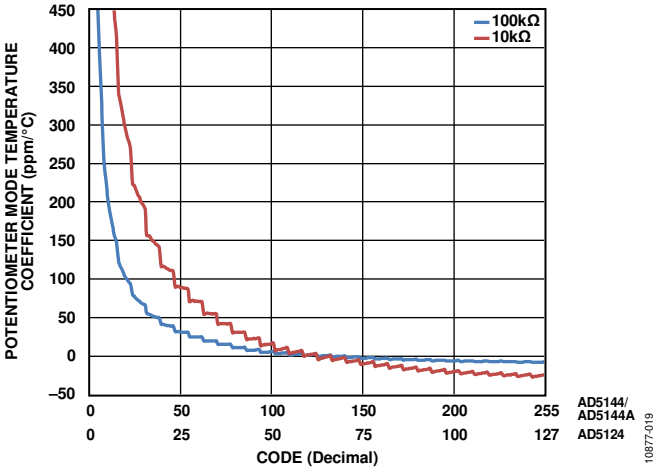

Figure 19. Potentiometer Mode Temperature Coefficient ($(\Delta V_W/V_W)/\Delta T \times 10^6$) vs. Code

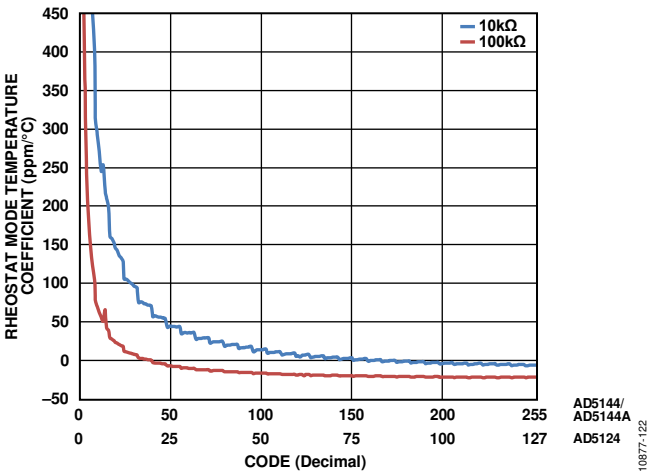

Figure 22. Rheostat Mode Temperature Coefficient ($(\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$) vs. Code

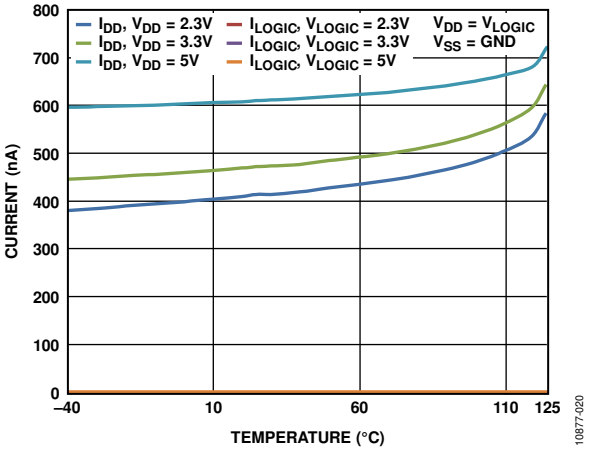

Figure 20. Supply Current vs. Temperature

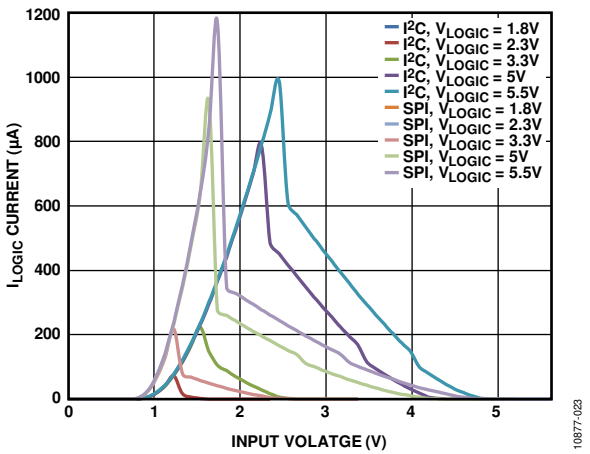

Figure 23. I_{LOGIC} Current vs. Digital Input Voltage

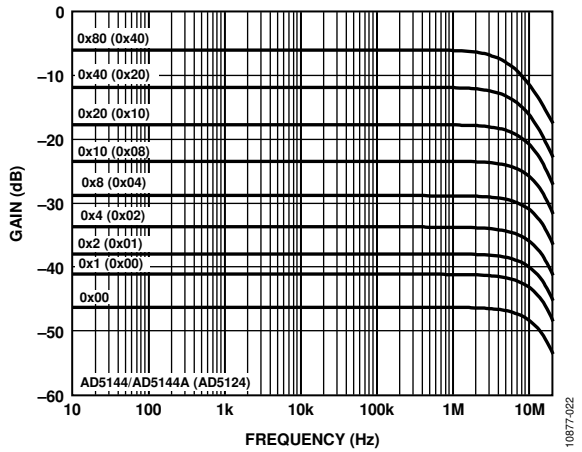

Figure 24. 10 kΩ Gain vs. Frequency vs. Code

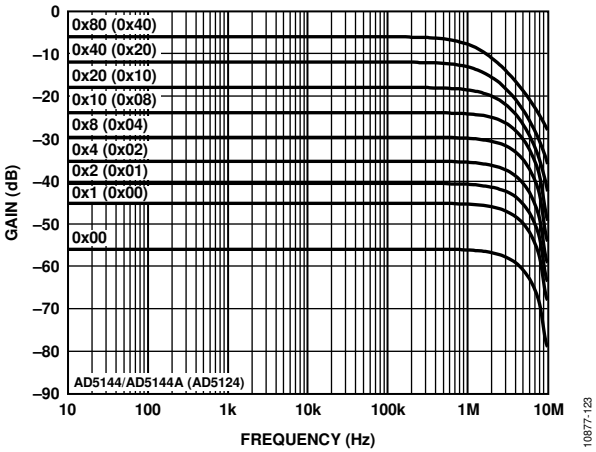

Figure 27. 100 kΩ Gain vs. Frequency vs. Code

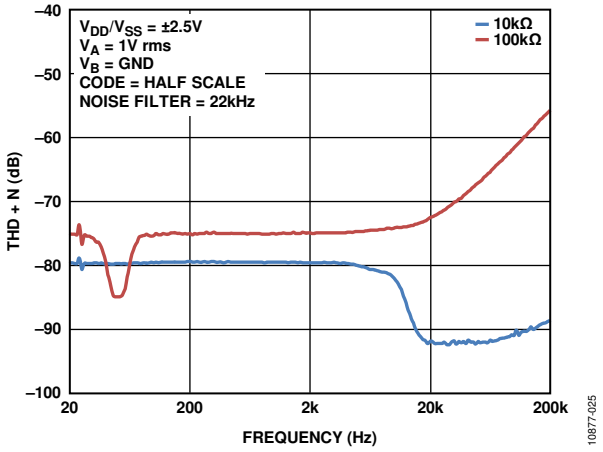

Figure 25. Total Harmonic Distortion Plus Noise (THD + N) vs. Frequency

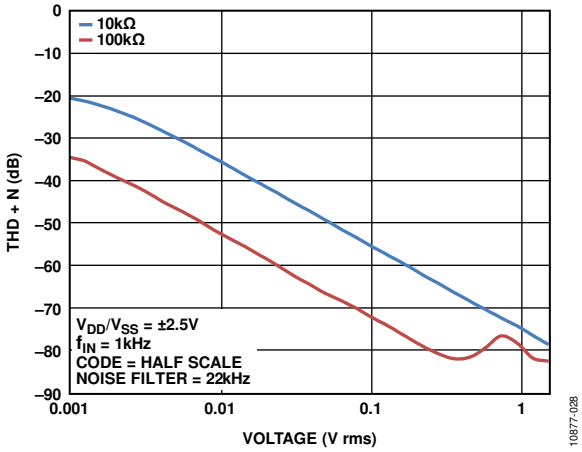

Figure 28. Total Harmonic Distortion Plus Noise (THD + N) vs. Amplitude

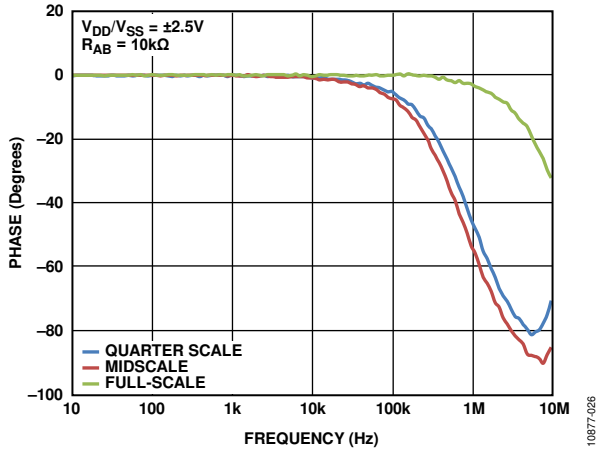

Figure 26. Normalized Phase Flatness vs. Frequency, R_{AB} = 10 kΩ

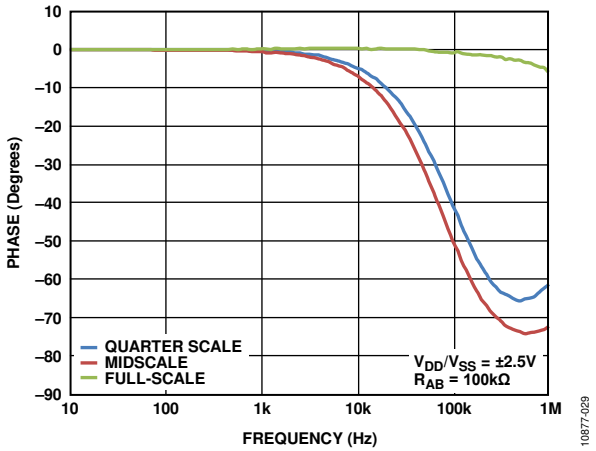

Figure 29. Normalized Phase Flatness vs. Frequency, R_{AB} = 100 kΩ

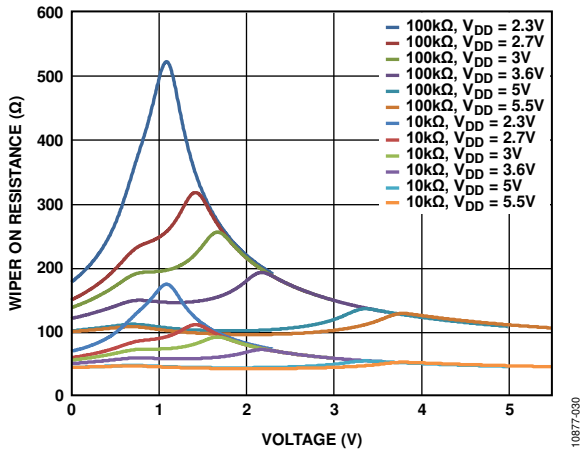

Figure 30. Incremental Wiper On Resistance vs. Positive Power Supply (V_{DD})

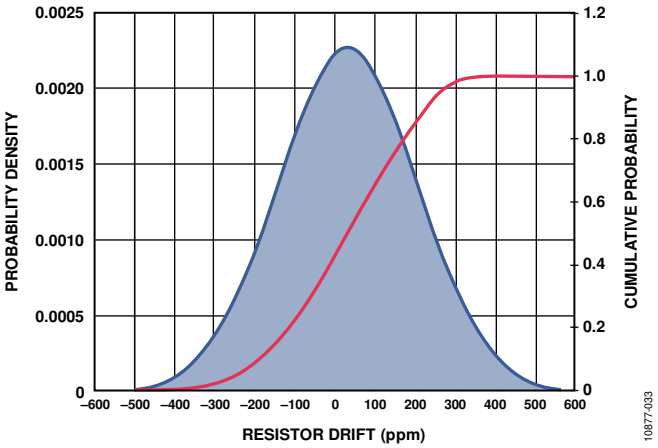

Figure 33. Resistor Lifetime Drift

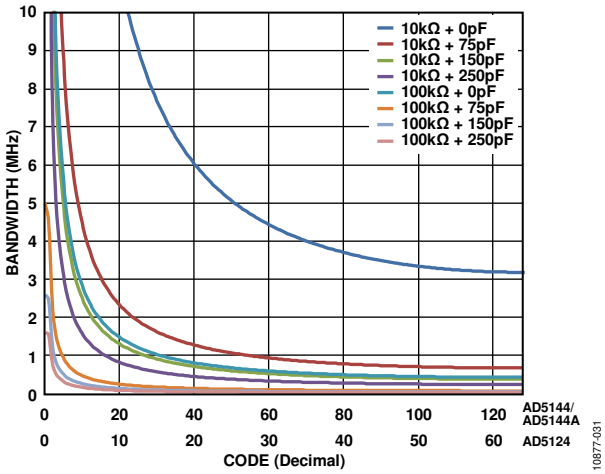

Figure 31. Maximum Bandwidth vs. Code vs. Net Capacitance

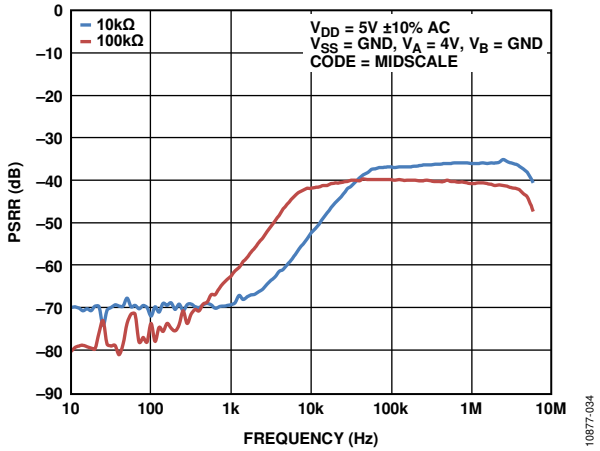

Figure 34. Power Supply Rejection Ratio (PSRR) vs. Frequency

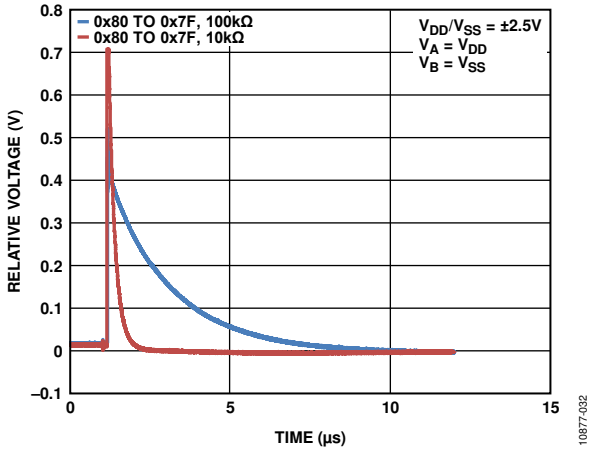

Figure 32. Maximum Transition Glitch

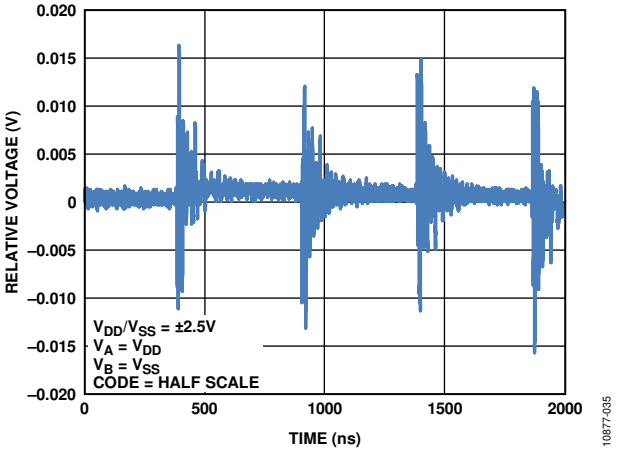

Figure 35. Digital Feedthrough

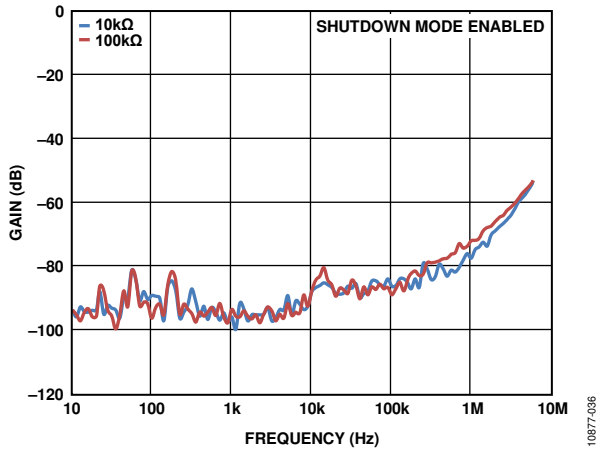

Figure 36. Shutdown Isolation vs. Frequency

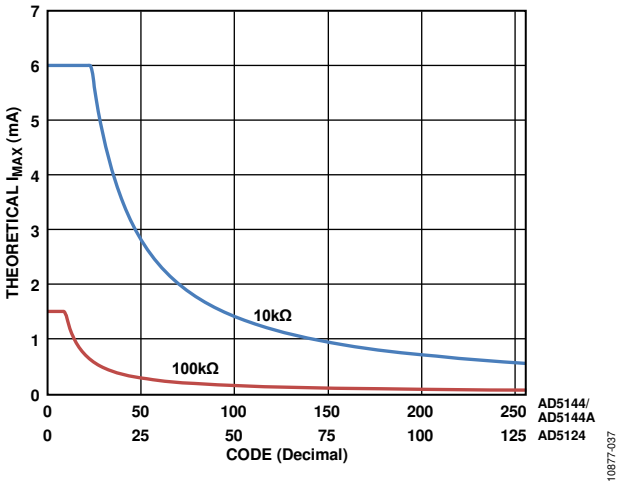

Figure 37. Theoretical Maximum Current vs. Code

TEST CIRCUITS

Figure 38 to Figure 42 define the test conditions used in the Specifications section.

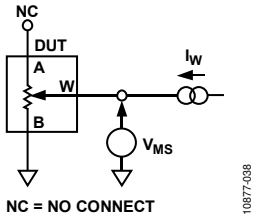

Figure 38. Resistor Integral Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

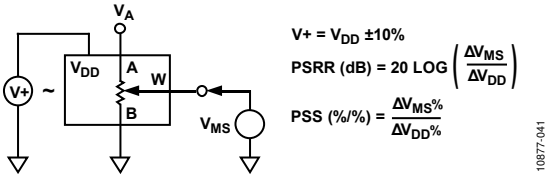

Figure 41. Power Supply Sensitivity and Power Supply Rejection Ratio (PSS and PSRR)

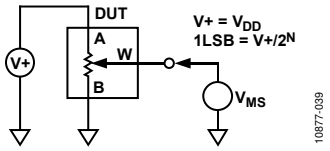

Figure 39. Potentiometer Divider Nonlinearity Error (INL, DNL)

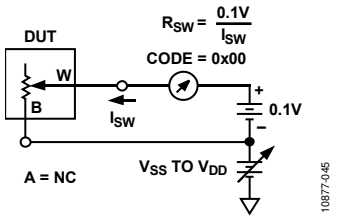

Figure 42. Incremental On Resistance

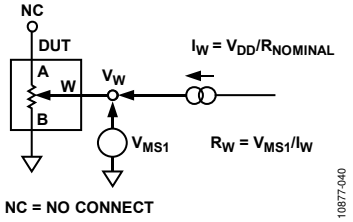

Figure 40. Wiper Resistance

THEORY OF OPERATION

The AD5124/AD5144/AD5144A digital programmable potentiometers are designed to operate as true variable resistors for analog signals within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The resistor wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register that allows unlimited changes of resistance settings. A secondary register (the input register) can be used to preload the RDAC register data.

The RDAC register can be programmed with any position setting using the I²C or SPI interface (depending on the model). When a desirable wiper position is found, this value can be stored in the EEPROM memory. Thereafter, the wiper position is always restored to that position for subsequent power-ups. The storing of the EEPROM data takes approximately 15 ms; during this time, the device is locked and does not acknowledge any new command, preventing any changes from taking place.

RDAC REGISTER AND EEPROM

The RDAC register directly controls the position of the digital potentiometer wiper. For example, when the RDAC register is loaded with 0x80 (AD5144/AD5144A, 256 taps), the wiper is connected to half scale of the variable resistor. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed.

It is possible to both write to and read from the RDAC register using the digital interface (see Table 14).

The contents of the RDAC register can be stored to the EEPROM using Command 9 (see Table 14). Thereafter, the RDAC register always sets at that position for any future on-off-on power supply sequence. It is possible to read back data saved into the EEPROM with Command 3 (see Table 14).

Alternatively, the EEPROM can be written to independently using Command 11 (see Table 20).

INPUT SHIFT REGISTER

For the AD5124/AD5144/AD5144A, the input shift register is 16 bits wide, as shown in Figure 4. The 16-bit word consists of four control bits, followed by four address bits and by eight data bits.

If the AD5124 RDAC or EEPROM registers are read from or written to, the lowest data bit (Bit 0) is ignored.

Data is loaded MSB first (Bit 15). The four control bits determine the function of the software command, as listed in Table 14 and Table 20.

SERIAL DATA DIGITAL INTERFACE SELECTION, DIS

The AD5124/AD5144 LFSCP provides the flexibility of a selectable interface. When the digital interface select (DIS) pin is tied low, the SPI mode is engaged. When the DIS pin is tied high, the I²C mode is engaged.

SPI SERIAL DATA INTERFACE

The AD5124/AD5144 contain a 4-wire, SPI-compatible digital interface (SDI, $\overline{\text{SYNC}}$, SDO, and SCLK). The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. The $\overline{\text{SYNC}}$ pin must be held low until the complete data-word is loaded from the SDI pin. Data is loaded in at the SCLK falling edge transition, as shown in Figure 6. When $\overline{\text{SYNC}}$ returns high, the serial data-word is decoded according to the instructions in Table 20.

To minimize power consumption in the digital input buffers when the part is enabled, operate all serial interface pins close to the V_{LOGIC} supply rails.

$\overline{\text{SYNC}}$ Interruption

In a standalone write sequence for the AD5124/AD5144, the $\overline{\text{SYNC}}$ line is kept low for 16 falling edges of SCLK, and the instruction is decoded when $\overline{\text{SYNC}}$ is pulled high. However, if the $\overline{\text{SYNC}}$ line is kept low for less than 16 falling edges of SCLK, the input shift register content is ignored, and the write sequence is considered invalid.

SDO Pin

The serial data output pin (SDO) serves two purposes: to read back the contents of the control, EEPROM, RDAC, and input registers using Command 3 (see Table 14 and Table 20), and to connect the AD5124/AD5144 in daisy-chain mode.

The SDO pin contains an internal open-drain output that needs an external pull-up resistor. The SDO pin is enabled when $\overline{\text{SYNC}}$ is pulled low, and the data is clocked out of SDO on the rising edge of SCLK, as shown in Figure 6 and Figure 7.

Daisy-Chain Connection

Daisy chaining minimizes the number of port pins required from the controlling IC. As shown in Figure 43, the SDO pin of one package must be tied to the SDI pin of the next package. The clock period may need to be increased because of the propagation delay of the line between subsequent devices. When two AD5124/AD5144 devices are daisy chained, 32 bits of data are required. The first 16 bits are assigned to U2, and the second 16 bits are assigned to U1, as shown in Figure 44. Keep the $\overline{\text{SYNC}}$ pin low until all 32 bits are clocked into their respective serial registers. The $\overline{\text{SYNC}}$ pin is then pulled high to complete the operation.

To prevent data from mislocking (for example, due to noise) the part includes an internal counter, if the SCLK falling edges count is not a multiple of 8, the part ignores the command. A valid clock count is 16, 24, 32, 40, and so on. The counter resets when $\overline{\text{SYNC}}$ returns high.

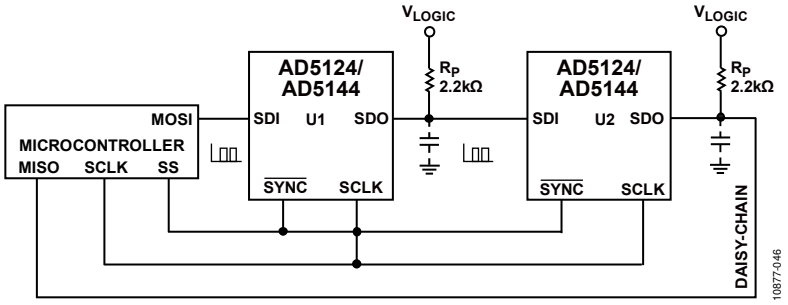

Figure 43. Daisy-Chain Configuration

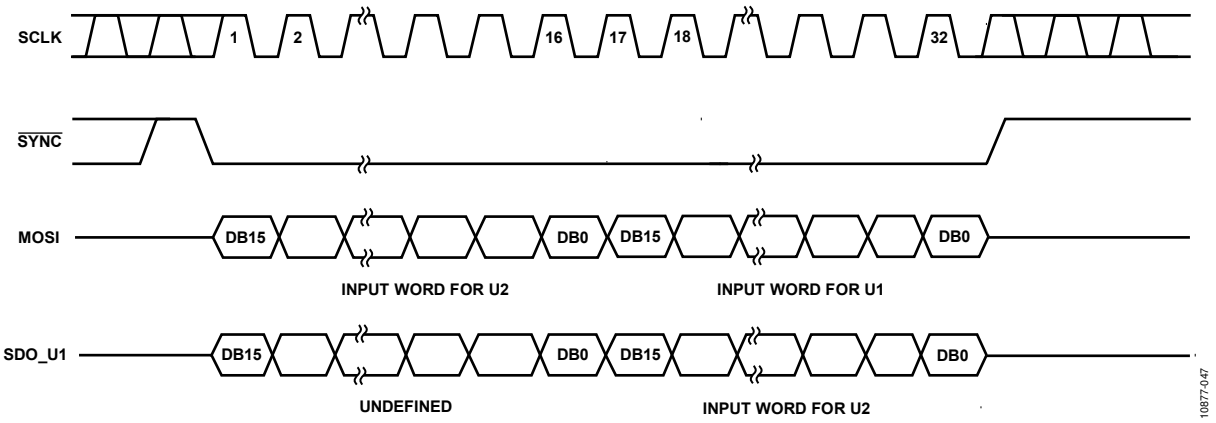

Figure 44. Daisy-Chain Diagram

I²C SERIAL DATA INTERFACE

The AD5144/AD5144A have 2-wire, I²C-compatible serial interfaces. These devices can be connected to an I²C bus as a slave device, under the control of a master device. See Figure 5 for a timing diagram of a typical write sequence.

The AD5144/AD5144A support standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing.

The 2-wire serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address and an R/$\overline{W}$ bit. The slave device corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is called the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its shift register.
   If the R/$\overline{W}$ bit is set high, the master reads from the slave device. However, if the R/$\overline{W}$ bit is set low, the master writes to the slave device.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read from or written to, a stop condition is established. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the tenth clock pulse, and then high again during the tenth clock pulse to establish a stop condition.

I²C ADDRESS

The AD5144/AD5144A each have two different device address options available (see Table 12 and Table 13).

Table 12. 20-Lead TSSOP Device Address Selection

ADDR	7-Bit I²C Device Address
V_{LOGIC}	0101000
No connect[1]	0101010
GND	0101011

[1] Not available in bipolar mode (V_{SS} < 0 V) or in low voltage mode (V_{LOGIC} = 1.8 V).

Table 13. 24-Lead LFCSP Device Address Selection

ADDR0 Pin	ADDR1 Pin	7-Bit I²C Device Address
V_{LOGIC}	V_{LOGIC}	0100000
No connect[1]	V_{LOGIC}	0100010
GND	V_{LOGIC}	0100011
V_{LOGIC}	No connect[1]	0101000
No connect[1]	No connect[1]	0101010
GND	No connect[1]	0101011
V_{LOGIC}	GND	0101100
No connect[1]	GND	0101110
GND	GND	0101111

[1] Not available in bipolar mode (V_{SS} < 0 V) or in low voltage mode (V_{LOGIC} = 1.8 V).