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### FEATURES

- 256-position, 4-channel
- End-to-end resistance 20 k $\Omega$ , 50 k $\Omega$ , 200 k $\Omega$
- Pin-selectable SPI<sup>®</sup>- or I<sup>2</sup>C<sup>®</sup>-compatible interface
- Power-on preset to midscale
- Two package address decode pins AD0 and AD1
- Rheostat mode temperature coefficient 30 ppm/ $^{\circ}$ C
- Voltage divider temperature coefficient 5 ppm/ $^{\circ}$ C
- Wide operating temperature range  $-40^{\circ}$ C to  $+125^{\circ}$ C
- 10 V to 15 V single supply;  $\pm 5$  V dual supply

### APPLICATIONS

- Mechanical potentiometer replacement
- Optical network adjustment
- Instrumentation: gain, offset adjustment
- Stereo channel audio level control
- Automotive electronics adjustment
- Programmable power supply
- Programmable filters, delays, time constants
- Line impedance matching
- Low resolution DAC/trimmer replacement
- Base station power amp biasing
- Sensor calibration

### GENERAL DESCRIPTION

The AD5263 is the industry's first quad-channel, 256-position, digital potentiometer<sup>1</sup> with a selectable digital interface. This device performs the same electronic adjustment function as mechanical potentiometers or variable resistors, with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

Each channel of the AD5263 offers a completely programmable value of resistance between the A terminal and the wiper or between the B terminal and the wiper. The fixed A-to-B terminal resistance of 20 k $\Omega$ , 50 k $\Omega$ , or 200 k $\Omega$  has a nominal temperature coefficient of  $\pm 30$  ppm/ $^{\circ}$ C and a  $\pm 1\%$  channel-to-channel matching tolerance. Another key feature of this part is the ability to operate from  $+4.5$  V to  $+15$  V, or at  $\pm 5$  V.

### FUNCTIONAL BLOCK DIAGRAM

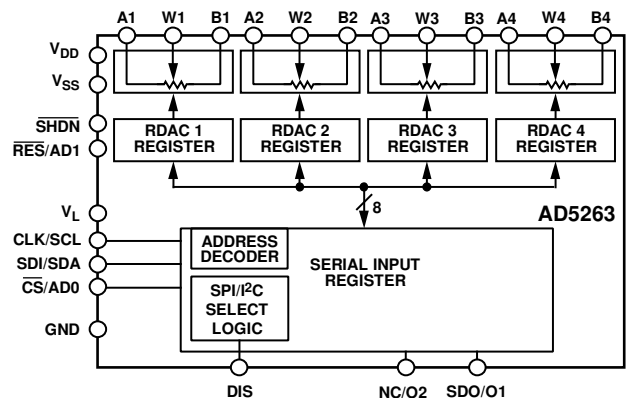


Figure 1.

Wiper position programming presets to midscale upon power-on. Once powered, the VR wiper position is programmed by either the 3-wire SPI or 2-wire I<sup>2</sup>C-compatible interface. In the I<sup>2</sup>C mode, additional programmable logic outputs enable users to drive digital loads, logic gates, and analog switches in their systems.

The AD5263 is available in a narrow body, 24-lead TSSOP. All parts are guaranteed to operate over the automotive temperature range of  $-40^{\circ}$ C to  $+125^{\circ}$ C.

For single- or dual-channel applications, refer to the AD5260/AD5280 or AD5262/AD5282 data sheets.

<sup>1</sup>The terms digital potentiometer, VR, and RDAC are used interchangeably.

# AD5263\* PRODUCT PAGE QUICK LINKS

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD5263 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-1291: Digital Potentiometers: Frequently Asked Questions
- AN-580: Programmable Oscillator Uses Digital Potentiometers
- AN-582: Resolution Enhancements of Digital Potentiometers with Multiple Devices
- AN-686: Implementing an I<sup>2</sup>C<sup>®</sup> Reset

### Data Sheet

- AD5263: Quad, 15 V, 256-Position, Digital Potentiometer with Pin-Selectable SPI/I<sup>2</sup>C Data Sheet

## DESIGN RESOURCES

- AD5263 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD5263 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

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## ELECTRICAL CHARACTERISTICS—20 k $\Omega$ , 50 k $\Omega$ , 200 k $\Omega$ VERSIONS

$V_{DD} = +5\text{ V}$ ,  $V_{SS} = -5\text{ V}$ ,  $V_L = +5\text{ V}$ ,  $V_A = +V_{DD}$ ,  $V_B = 0\text{ V}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>DC CHARACTERISTICS—RHEOSTAT MODE</b>						
Resistor Differential NL <sup>2</sup>	R-DNL	Specifications apply to all VRs $R_{WB}$ , $V_A = \text{NC}$	-1	$\pm 1/4$	+1	LSB
Resistor Nonlinearity <sup>2</sup>	R-INL	$R_{WB}$ , $V_A = \text{NC}$	-1	$\pm 1/2$	+1	LSB
Nominal Resistor Tolerance <sup>3</sup>	$\Delta R_{AB}$	$T_A = 25^\circ\text{C}$	-30		+30	%
Resistance Mode Temperature Coefficient	$\Delta R_{WB}/\Delta T$			30		ppm/ $^\circ\text{C}$
	$\Delta R_{WA}/\Delta T$			30		ppm/ $^\circ\text{C}$
Wiper Resistance	$R_W$	$I_W = 1\text{ V}/R_{AB}$		60	150	$\Omega$
<b>DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE</b>						
Resolution	N	Specifications apply to all VRs			8	Bits
Differential Nonlinearity <sup>4</sup>	DNL		-1	$\pm 1/4$	+1	LSB
Integral Nonlinearity <sup>4</sup>	INL		-1	$\pm 1/2$	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x80		5		ppm/ $^\circ\text{C}$
Full-Scale Error	$V_{WFSE}$	Code = 0xFF	-2	-1	+0	LSB
Zero-Scale Error	$V_{WZSE}$	Code = 0x00	0	+1	+2	LSB
<b>RESISTOR TERMINALS</b>						
Voltage Range <sup>5</sup>	$V_{A,B,W}$		$V_{SS}$		$V_{DD}$	V
Capacitance <sup>6</sup> Ax, Bx	$C_{A,B}$	$f = 1\text{ MHz}$ , measured to GND, Code = 0x80		25		pF
Capacitance <sup>6</sup> Wx	$C_W$	$f = 1\text{ MHz}$ , measured to GND, Code = 0x80		55		pF
Common-Mode Leakage	$I_{CM}$	$V_A = V_B = V_{DD}/2$		1		nA
Shutdown Current <sup>7</sup>	$I_{SHDN}$			0.02	5	$\mu\text{A}$
<b>DIGITAL INPUTS</b>						
Input Logic High	$V_{IH}$		2.4			V
Input Logic Low	$V_{IL}$				0.8	V
Input Logic High (SDA and SCL)	$V_{IH}$	$V_{SS} = 0\text{ V}$	$0.7 \times V_L$		$V_L + 0.5$	V
Input Logic Low (SDA and SCL)	$V_{IL}$	$V_{SS} = 0\text{ V}$	-0.5		$0.3 \times V_L$	V
Input Current	$I_{IL}$	$V_{IN} = 0\text{ V}$ or $+5\text{ V}$			$\pm 1$	$\mu\text{A}$
Input Capacitance <sup>6</sup>	$C_{IL}$			5		pF
<b>DIGITAL OUTPUTS</b>						
SDA	$V_{OL}$	$I_{SINK} = 3\text{ mA}$			0.4	V
	$V_{OL}$	$I_{SINK} = 6\text{ mA}$			0.6	V
O1, O2	$V_{OH}$	$I_{SOURCE} = 40\text{ }\mu\text{A}$	4			V
O1, O2	$V_{OL}$	$I_{SINK} = 1.6\text{ mA}$			0.4	V
SDO	$V_{OH}$	$R_L = 2.2\text{ k}\Omega$ to $V_{DD}$	$V_{DD} - 0.1$			V
SDO	$V_{OL}$	$I_{SINK} = 3\text{ mA}$			0.4	V
Three-State Leakage Current	$I_{OZ}$	$V_{IN} = 0\text{ V}$ or $+5\text{ V}$			$\pm 1$	$\mu\text{A}$
Output Capacitance <sup>6</sup>	$C_{OZ}$			3	8	pF

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>POWER SUPPLIES</b>						
Logic Supply <sup>8</sup>	$V_L$		2.7		5.5	V
Power Single-Supply Range	$V_{DD\ RANGE}$	$V_{SS} = 0\ V$	4.5		16.5	V
Power Dual-Supply Range	$V_{DD/SS\ RANGE}$		$\pm 4.5$		$\pm 7.5$	V
Logic Supply Current <sup>9</sup>	$I_L$	$V_L = +5\ V$		25	60	$\mu A$
Positive Supply Current	$I_{DD}$	$V_{IH} = +5\ V$ or $V_{IL} = 0\ V$			1	$\mu A$
Negative Supply Current	$I_{SS}$	$V_{SS} = -5\ V$			1	$\mu A$
Power Dissipation <sup>10</sup>	$P_{DISS}$	$V_{IH} = +5\ V$ or $V_{IL} = 0\ V$ , $V_{DD} = +5\ V$ , $V_{SS} = -5\ V$			0.6	mW
Power Supply Sensitivity	PSS	$\Delta V_{DD} = +5\ V \pm 10\%$		0.002	0.01	%/%
<b>DYNAMIC CHARACTERISTICS<sup>6, 11</sup></b>						
Bandwidth (3 dB)	BW	$R_{AB} = 20\ k\Omega/50\ k\Omega/200\ k\Omega$		300/150/35		kHz
Total Harmonic Distortion	$THD_W$	$V_A = 1\ V\ rms$ , $V_B = 0\ V$ , $f = 1\ kHz$ , $R_{AB} = 20\ k\Omega$		0.05		%
$V_W$ Settling Time <sup>12</sup>	$t_S$	$V_A = 10\ V$ , $V_B = 0\ V$ , $\pm 1\ LSB$ error band		2		$\mu s$
Resistor Noise Voltage	$e_{N\_WB}$	$R_{WB} = 10\ k\Omega$ , $f = 1\ kHz$ , $R_S = 0$		9		$nV/\sqrt{Hz}$

<sup>1</sup>Typicals represent average readings at +25°C and  $V_{DD} = +5\ V$ ,  $V_{SS} = -5\ V$ .

<sup>2</sup>Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.  $I_W = V_{DD}/R$  for both  $V_{DD} = +5\ V$  and  $V_{SS} = -5\ V$ .

<sup>3</sup> $V_{AB} = V_{DD}$ , Wiper ( $V_W$ ) = no connect.

<sup>4</sup>INL and DNL are measured at  $V_W$  with the RDAC configured as a potentiometer divider similar to a voltage output DAC.  $V_A = V_{DD}$  and  $V_B = 0\ V$ . DNL specification limits of  $\pm 1\ LSB$  maximum are guaranteed monotonic operating conditions.

<sup>5</sup>The A, B, and W resistor terminals have no limitations on polarity with respect to each other.

<sup>6</sup>Guaranteed by design and not subject to production test.

<sup>7</sup>Measured at the Ax terminals. All Ax terminals are open-circuited in shutdown mode.

<sup>8</sup> $V_L$  is limited to  $V_{DD}$  or 5.5 V, whichever is less.

<sup>9</sup>Worst-case supply current consumed when all logic-input levels set at 2.4 V, standard characteristic of CMOS logic.

<sup>10</sup> $P_{DISS}$  is calculated from  $I_{DD} \times V_{DD}$ . CMOS logic level inputs result in minimum power dissipation.

<sup>11</sup>All dynamic characteristics use  $V_{DD} = +5\ V$ ,  $V_{SS} = -5\ V$ ,  $V_L = +5\ V$ .

<sup>12</sup>Settling time depends on value of  $V_{DD}$ ,  $R_L$ , and  $C_L$ .

## TIMING CHARACTERISTICS—20 k $\Omega$ , 50 k $\Omega$ , 200 k $\Omega$ VERSIONS

$V_{DD} = +5\text{ V}$ ,  $V_{SS} = -5\text{ V}$ ,  $V_L = +5\text{ V}$ ,  $V_A = +V_{DD}$ ,  $V_B = 0\text{ V}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>SPI INTERFACE TIMING CHARACTERISTICS</b>						
Clock Frequency	$f_{\text{CLK}}$	Specifications apply to all parts <sup>2,3</sup>			25	MHz
Input Clock Pulse Width	$t_{\text{CH}}, t_{\text{CL}}$	Clock level high or low	20			ns
Data Setup Time	$t_{\text{DS}}$		10			ns
Data Hold Time	$t_{\text{DH}}$		10			ns
$\overline{\text{CS}}$ Setup Time	$t_{\text{CSS}}$		15			ns
$\overline{\text{CS}}$ High Pulse Width	$t_{\text{CSW}}$		20			ns
CLK Fall to $\overline{\text{CS}}$ Fall Hold Time	$t_{\text{CSH0}}$		0			ns
CLK Fall to $\overline{\text{CS}}$ Rise Hold Time	$t_{\text{CSH1}}$		0			ns
$\overline{\text{CS}}$ Rise to Clock Rise Setup	$t_{\text{CS1}}$		10			ns
Reset Pulse Width	$t_{\text{RS}}$		5			ns
<b>I<sup>2</sup>C INTERFACE TIMING CHARACTERISTICS</b>						
SCL Clock Frequency	$f_{\text{SCL}}$	Specifications apply to all parts <sup>2,3</sup>			400	kHz
$t_{\text{BUF}}$ Bus Free Time Between Stop and Start	$t_1$	After this period, the first clock pulse is generated.	1.3			$\mu\text{s}$
$t_{\text{HD,STA}}$ Hold Time (Repeated Start)	$t_2$		0.6			$\mu\text{s}$
$t_{\text{LOW}}$ Low Period of SCL Clock	$t_3$		1.3			$\mu\text{s}$
$t_{\text{HIGH}}$ High Period of SCL Clock	$t_4$		0.6		50	$\mu\text{s}$
$t_{\text{SU,STA}}$ Setup Time for Start Condition	$t_5$		0.6			$\mu\text{s}$
$t_{\text{HD,DAT}}$ Data Hold Time	$t_6$				0.9	$\mu\text{s}$
$t_{\text{SU,DAT}}$ Data Setup Time	$t_7$		100			ns
$t_{\text{F}}$ Fall Time of Both SDA and SCL Signals	$t_8$				300	ns
$t_{\text{R}}$ Rise Time of Both SDA and SCL Signals	$t_9$				300	ns
$t_{\text{SU,STO}}$ Setup Time for Stop Condition	$t_{10}$			0.6		$\mu\text{s}$

<sup>1</sup> Typical values represent average readings at  $+25^\circ\text{C}$  and  $V_{DD} = +5\text{ V}$ ,  $V_{SS} = -5\text{ V}$ .

<sup>2</sup> Guaranteed by design and not subject to production test.

<sup>3</sup> See timing diagrams for location of measured values. All input control voltages are specified with  $t_{\text{R}} = t_{\text{F}} = 2\text{ ns}$  (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using  $V_L = 5\text{ V}$ .

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Value
$V_{DD}$ to GND	-0.3 V to +16.5 V
$V_{SS}$ to GND	-7.5 V to 0 V
$V_{DD}$ to $V_{SS}$	+16.5 V
$V_L$ to GND	-0.3 V to +6.5 V
$V_A, V_B, V_W$ to GND	$V_{SS}$ to $V_{DD}$
Terminal Current, Ax to Bx, Ax to Wx, Bx to Wx	
Pulsed <sup>1</sup>	±20 mA
Continuous	±3 mA
Digital Inputs and Output Voltage to GND	-0.3 V to +7 V
Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature ( $T_{JMAX}$ )	150°C
Storage Temperature Range	-65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Thermal Resistance <sup>2</sup> $\theta_{JA}$	
TSSOP-24	143°C/W

<sup>1</sup> Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

<sup>2</sup> Package power dissipation:  $(T_{JMAX} - T_A)/\theta_{JA}$ .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

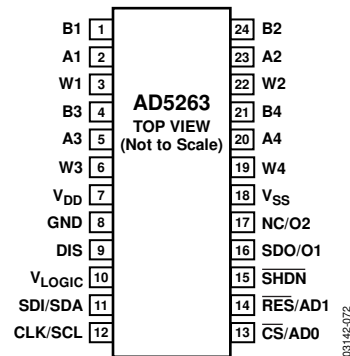


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin	Name	Description
1	B1	Resistor Terminal B1.
2	A1	Resistor Terminal A1 (ADDR = 00).
3	W1	Wiper Terminal W1.
4	B3	Resistor Terminal B3.
5	A3	Resistor Terminal A3.
6	W3	Wiper Terminal W3 (ADDR = 10).
7	V <sub>DD</sub>	Positive Power Supply, specified for +5 V to +15 V operation.
8	GND	Ground.
9	DIS	Digital Interface Select (SPI/I <sup>2</sup> C Select). SPI when DIS = 0, I <sup>2</sup> C when DIS = 1
10	V <sub>LOGIC</sub>	2.7 V to 5.5 V Logic Supply Voltage. The logic supply voltage should always be less than or equal to V <sub>DD</sub> . In addition, logic levels must be limited to the logic supply voltage regardless of V <sub>DD</sub> .
11	SDI/SDA	SDI = 3-Wire Serial Data Input. SDA = 2-Wire Serial Data Input/Output.
12	CLK/SCL	Serial Clock Input.
13	CS/AD0	Chip Select in SPI Mode. Device Address Bit 0 in I <sup>2</sup> C Mode.
14	RES/AD1	RESET in SPI Mode. Device Address Bit 1 in I <sup>2</sup> C Mode.
15	SHDN	Shutdown. Shorts wiper to Terminal B, opens Terminal A. Tie to +5 V supply if not used. Do not tie to V <sub>DD</sub> if V <sub>DD</sub> > 5 V.
16	SDO/O1	Serial Data Output in SPI Mode. Open-drain transistor requires pull-up resistor. Digital Output O1 in I <sup>2</sup> C Mode. Can be used to drive external logic.
17	NC/O2	No Connection in SPI Mode. Digital Output O2 in I <sup>2</sup> C Mode. Can be used to drive external logic.
18	V <sub>SS</sub>	Negative Power Supply. Specified for operation from 0 V to -5 V.
19	W4	Wiper Terminal W4 (ADDR = 11).
20	A4	Resistor Terminal A4.
21	B4	Resistor Terminal B4.
22	W2	Wiper Terminal W2 (ADDR = 01).
23	A2	Resistor Terminal A2.
24	B2	Resistor Terminal B2.

# TYPICAL PERFORMANCE CHARACTERISTICS

$R_{AB} = 20\text{ k}\Omega$ , unless otherwise noted.

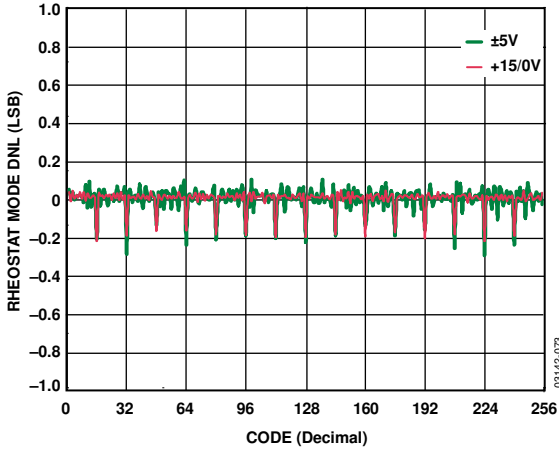


Figure 3. R-DNL vs. Code vs. Supply Voltage

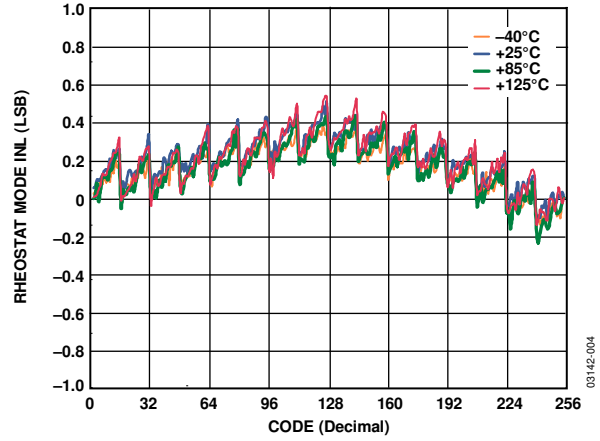


Figure 6. R-INL vs. Code;  $V_{DD} = \pm 5\text{ V}$

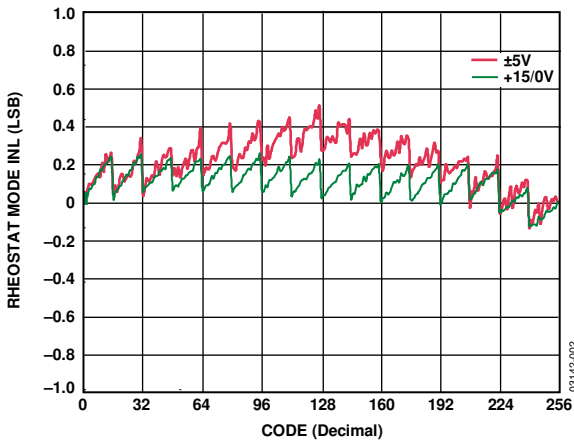


Figure 4. R-INL vs. Code vs. Supply Voltage

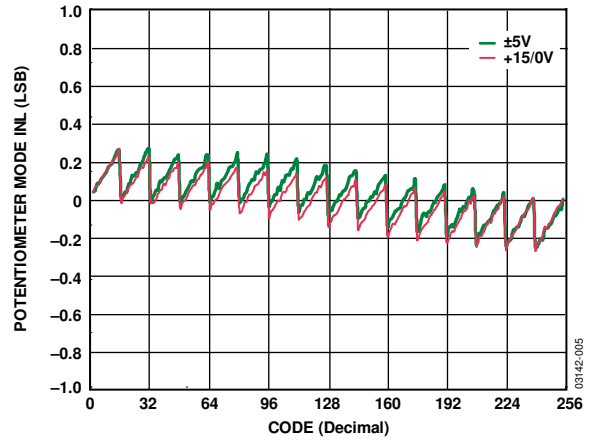


Figure 7. INL vs. Code vs. Supply Voltage

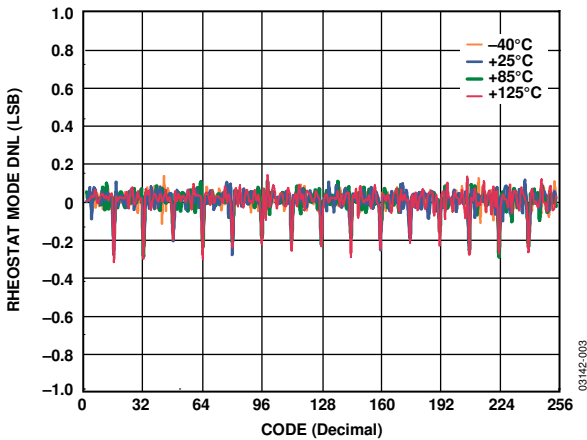


Figure 5. R-DNL vs. Code;  $V_{DD} = \pm 5\text{ V}$

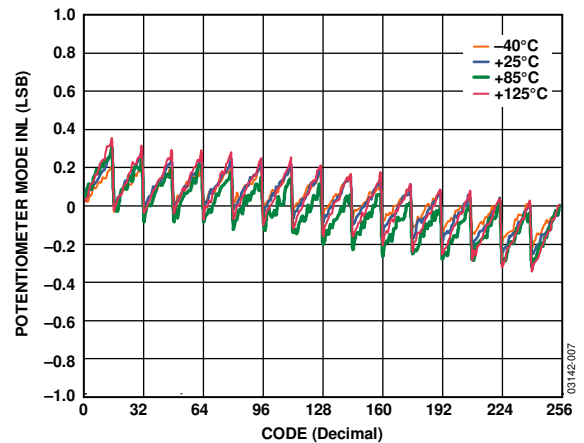


Figure 8. INL vs. Code vs. Supply Voltage

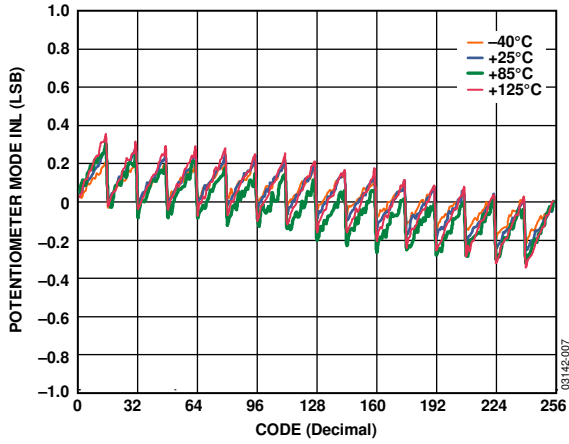


Figure 9. INL vs. Code;  $V_{DD} = \pm 5 V$

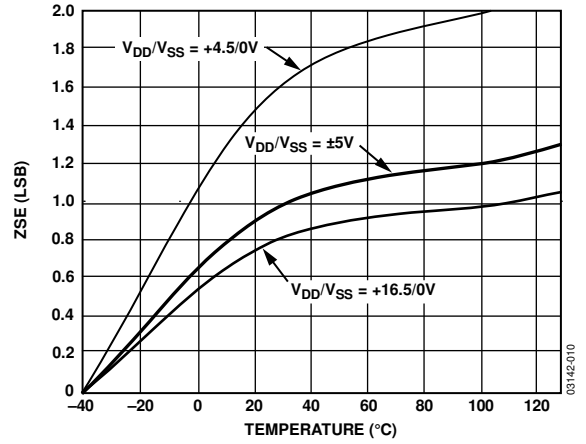


Figure 12. Zero-Scale Error vs. Temperature

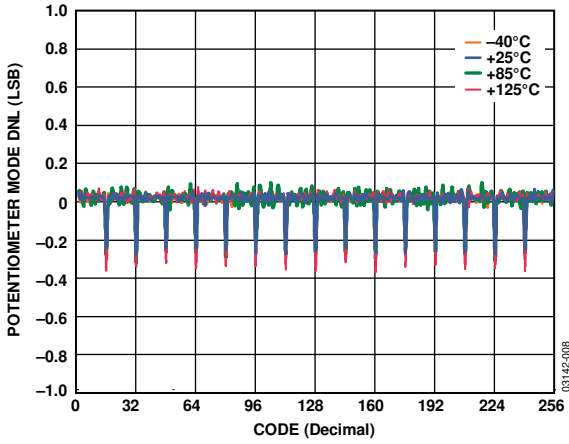


Figure 10. DNL vs. Code;  $V_{DD} = \pm 5 V$

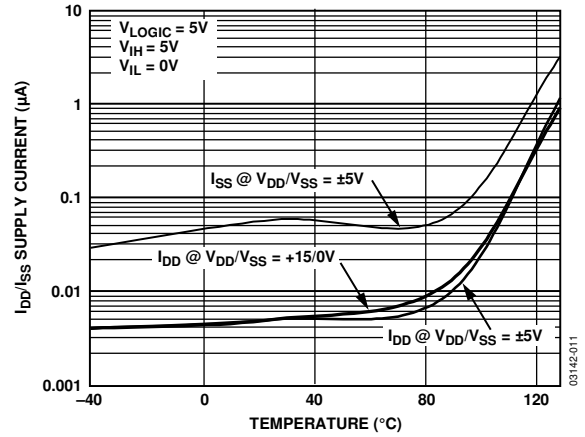


Figure 13. Supply Current vs. Temperature

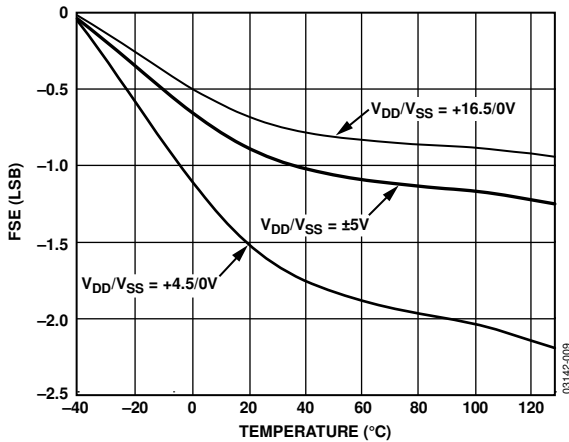


Figure 11. Full-Scale Error vs. Temperature

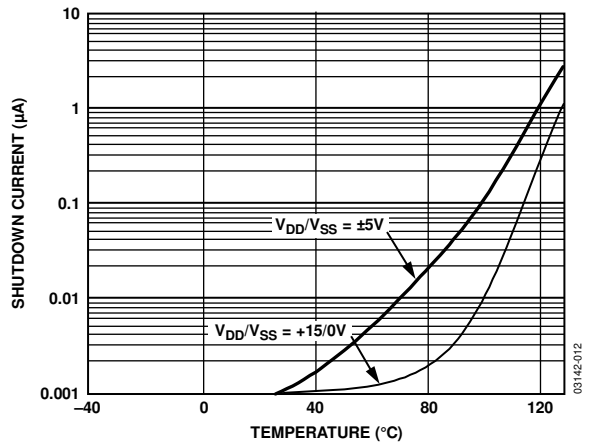


Figure 14. Shutdown Current vs. Temperature

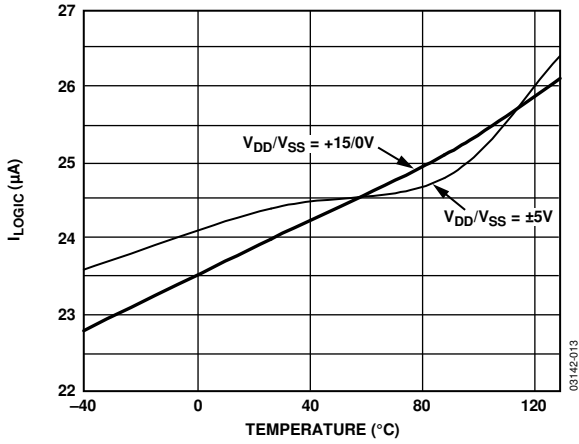


Figure 15.  $I_{LOGIC}$  vs. Temperature

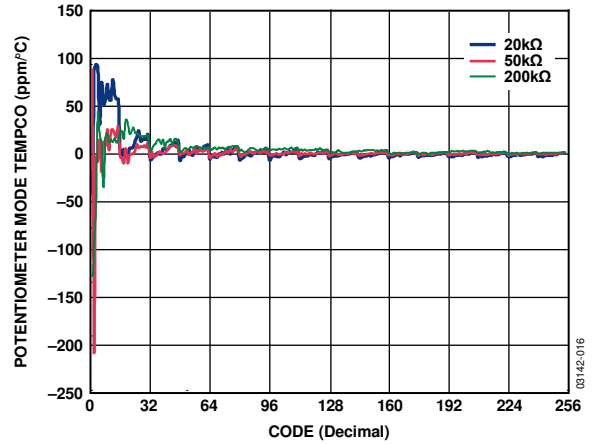


Figure 18. Potentiometer Mode Tempco  $\Delta R_{WB}/\Delta T$  vs. Code

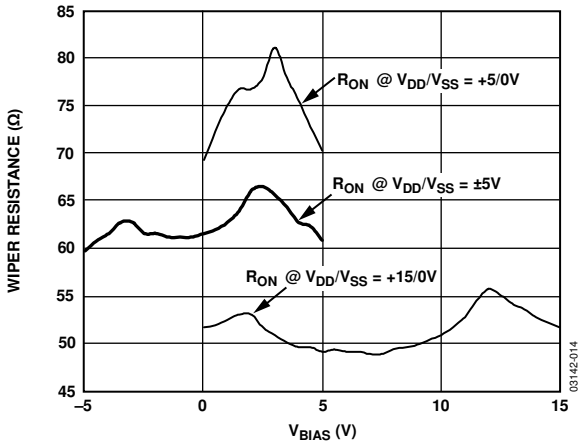


Figure 16. Wiper On-Resistance vs. Bias Voltage

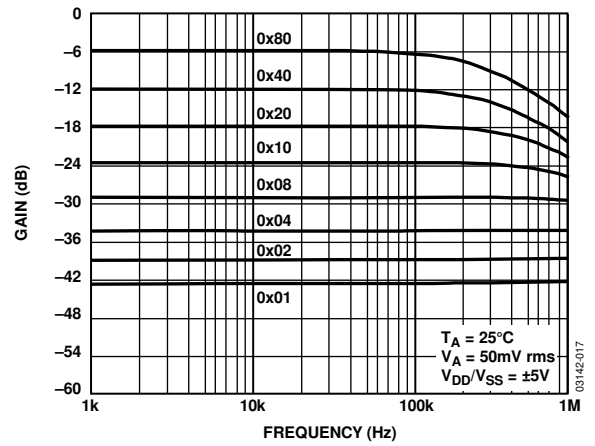


Figure 19. Gain vs. Frequency vs. Code;  $R_{AB} = 20\text{ k}\Omega$

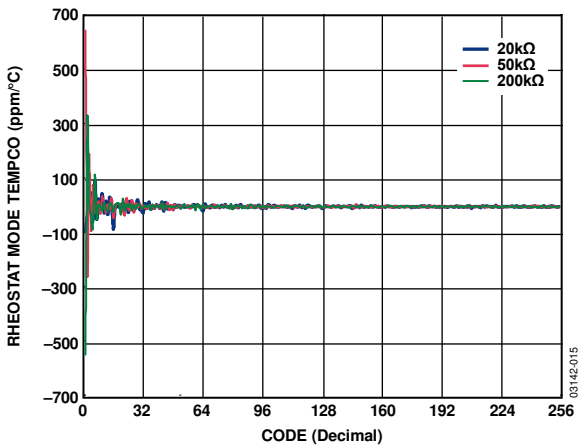


Figure 17. Rheostat Mode Tempco  $\Delta R_{WB}/\Delta T$  vs. Code

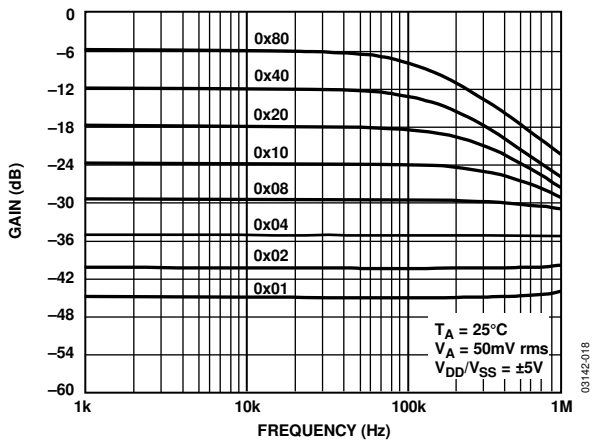


Figure 20. Gain vs. Frequency vs. Code;  $R_{AB} = 50\text{ k}\Omega$

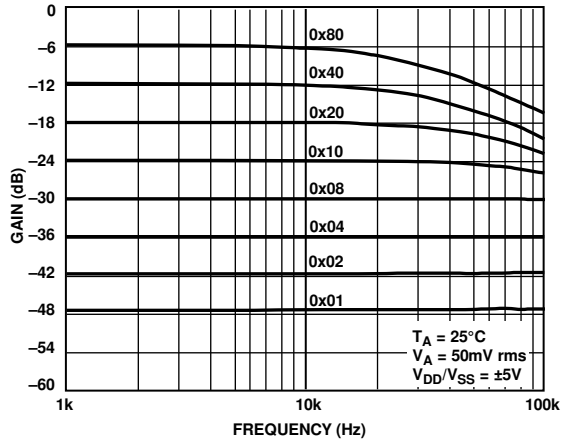


Figure 21. Gain vs. Frequency vs. Code;  $R_{AB} = 200\text{ k}\Omega$

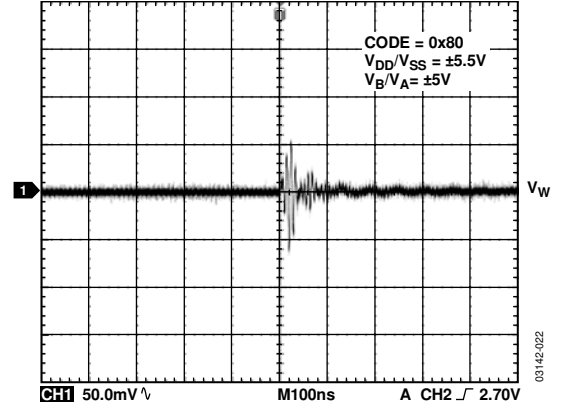


Figure 24. Digital Feedthrough

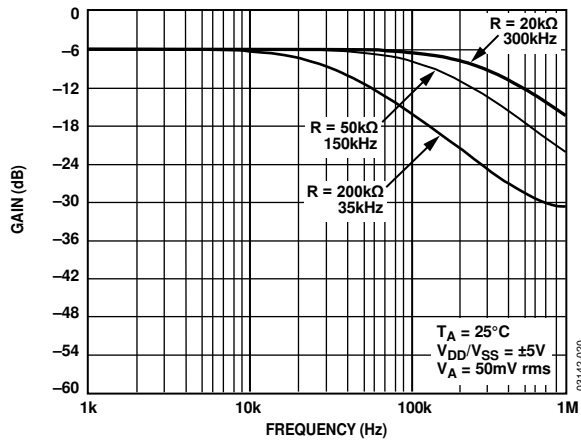


Figure 22. Gain vs. Frequency at -3 dB Bandwidth

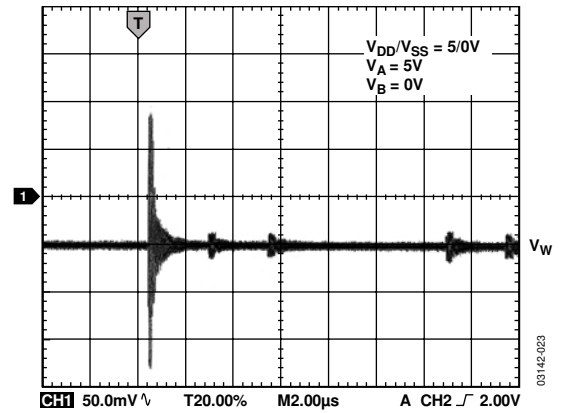


Figure 25. Midscale Glitch; Code 0x80 to 0x7F (4.7 nF Capacitor Used from Wiper to Ground)

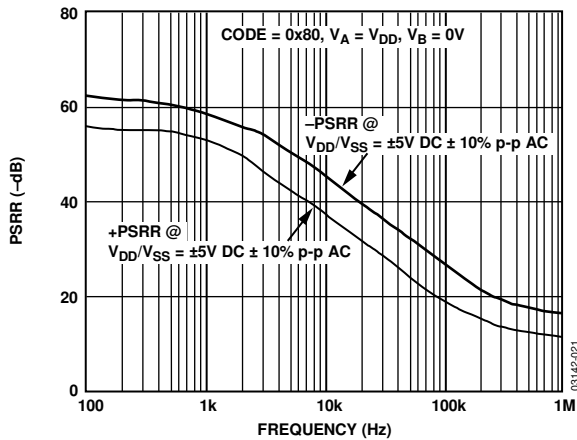


Figure 23. PSRR vs. Frequency

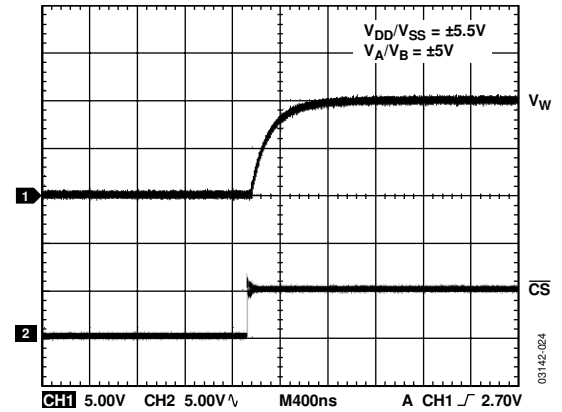


Figure 26. Large Signal Settling Time; Code 0x00 to 0xFF

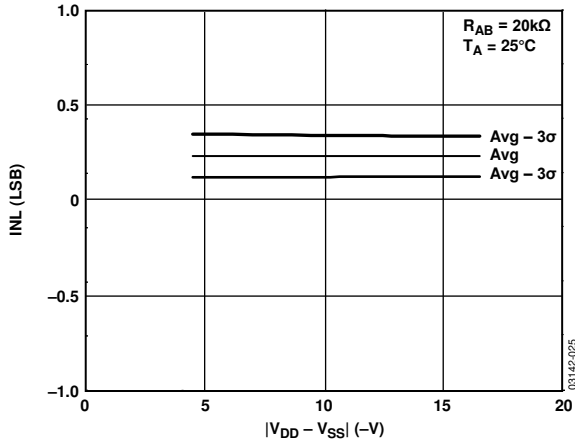


Figure 27. INL vs. Supply Voltage

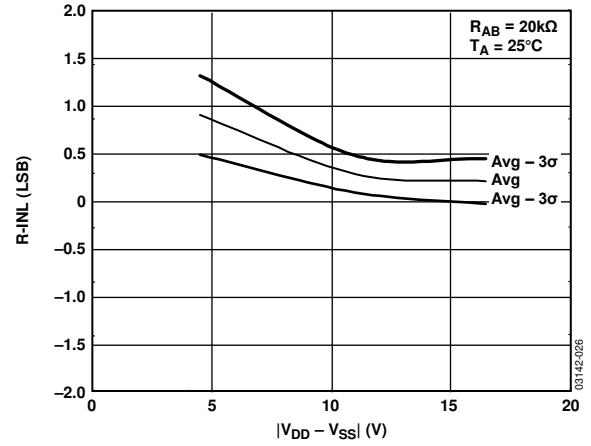


Figure 28. R-INL vs. Supply Voltage

### TEST CIRCUITS

Figure 29 to Figure 39 define the test conditions used in the Electrical Characteristics—20 KΩ, 50 KΩ, 200 KΩ Versions section and the Timing Characteristics—20 KΩ, 50 KΩ, 200 KΩ Versions.

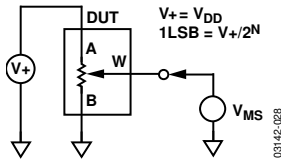


Figure 29. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

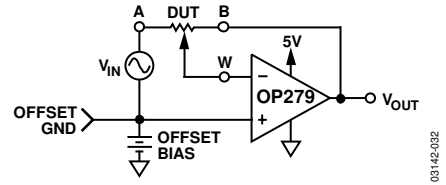


Figure 33. Test Circuit for Inverting Gain

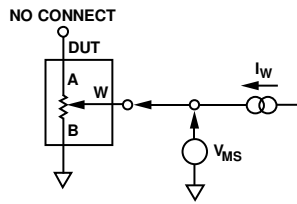


Figure 30. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

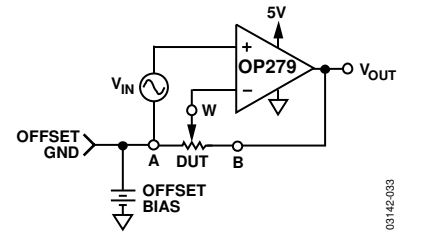


Figure 34. Test Circuit for Noninverting Gain

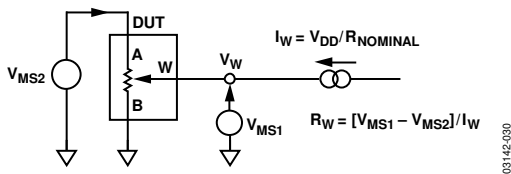


Figure 31. Test Circuit for Wiper Resistance

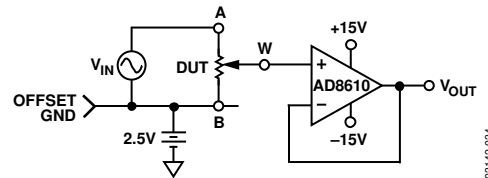


Figure 35. Test Circuit for Gain vs. Frequency

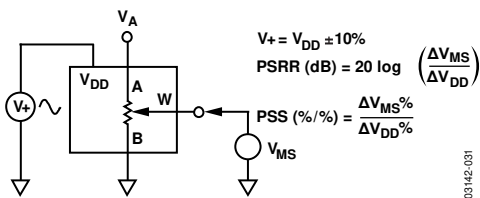


Figure 32. Test Circuit for Power Supply Sensitivity (PSS, PSRR)

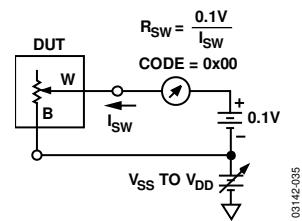


Figure 36. Test Circuit for Incremental On Resistance

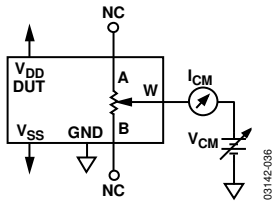


Figure 37. Test Circuit for Common-Mode Leakage Current

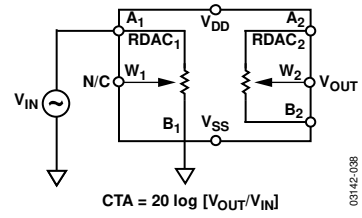


Figure 39. Test Circuit for Analog Crosstalk

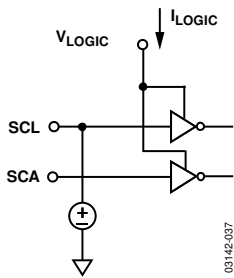


Figure 38. Test Circuit for  $V_{LOGIC}$  Current vs. Digital Input Voltage



# SPI-COMPATIBLE DIGITAL INTERFACE (DIS = 0)

## SERIAL DATA-WORD FORMAT

MSB		Data						LSB	
Addr		B7	B6	B5	B4	B3	B2	B1	B0
B9	B8	D7	D6	D5	D4	D3	D2	D1	D0
A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
2 <sup>9</sup>		2 <sup>7</sup>							2 <sup>0</sup>

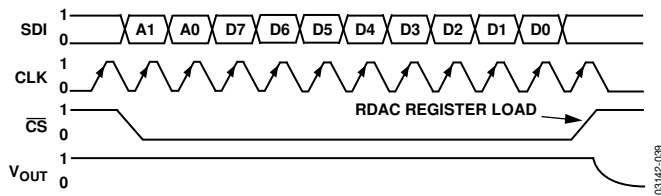


Figure 40. AD5263 Timing Diagram ( $V_A = 5\text{ V}$ ,  $V_B = 0\text{ V}$ ,  $V_W = V_{OUT}$ )

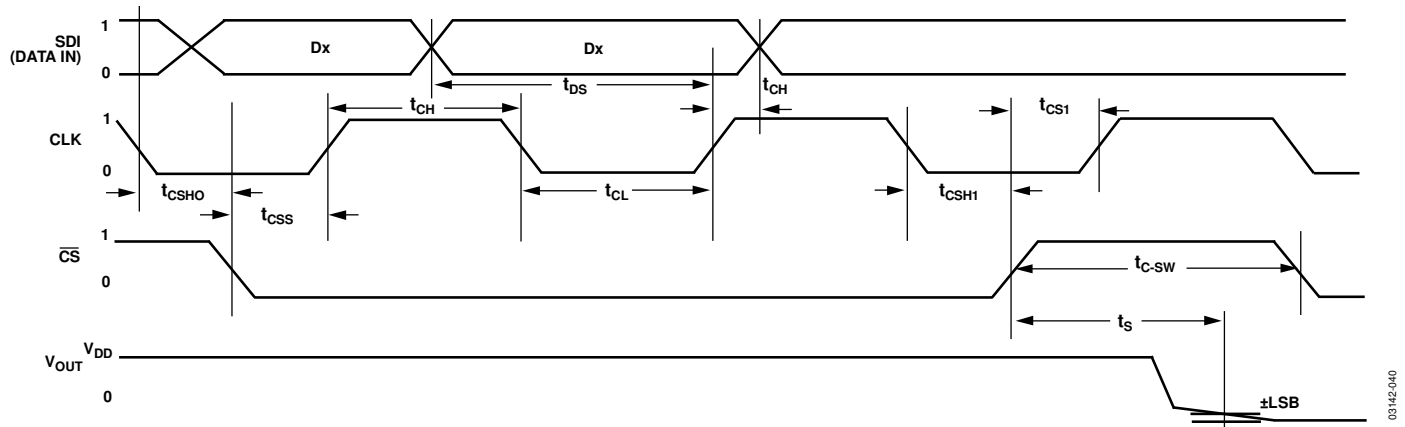


Figure 41. Detailed SPI Timing Diagram ( $V_A = 5\text{ V}$ ,  $V_B = 0\text{ V}$ ,  $V_W = V_{OUT}$ )

## I<sup>2</sup>C-COMPATIBLE DIGITAL INTERFACE (DIS = 1)

The word format maps in this section use the following abbreviations.

Abbreviation	Description
S	Start condition.
P	Stop condition.
A	Acknowledge.
AD1, AD0	I <sup>2</sup> C device address bits. Must match with the logic states at Pin AD1 and Pin AD0. Refer to Figure 49.
A1, A0	RDAC channel select.
RS	Software reset wiper (A1, A0) to midscale position.
SD	Shutdown active high; ties wiper (A1, A0) to Terminal B, opens Terminal A, RDAC register contents are not disturbed. To exit shutdown, the command SD = 0 must be executed for each RDAC (A1, A0).
O1, O2	Data to digital output pins, Pin O1 and Pin O2 in I <sup>2</sup> C mode, used to drive external logic. The logic high level is determined by V <sub>L</sub> and the logic low level is GND.
$\bar{W}$	Write = 0.
R	Read = 1.
D7, D6, D5, D4, D3, D2, D1, D0	Data bits.
X	Don't care.

### I<sup>2</sup>C WRITE MODE DATA-WORD FORMAT

S	0	1	0	1	1	AD1	AD0	$\bar{W}$	A	X	A1	A0	RS	SD	O1	O2	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
Slave Address Byte									Instruction Byte									Data Byte										

### I<sup>2</sup>C READ MODE DATA-WORD FORMAT

S	0	1	0	1	1	AD1	AD0	R	A	D7	D8	D5	D4	D3	D2	D1	D0	A	P
Slave Address Byte									Data Byte										

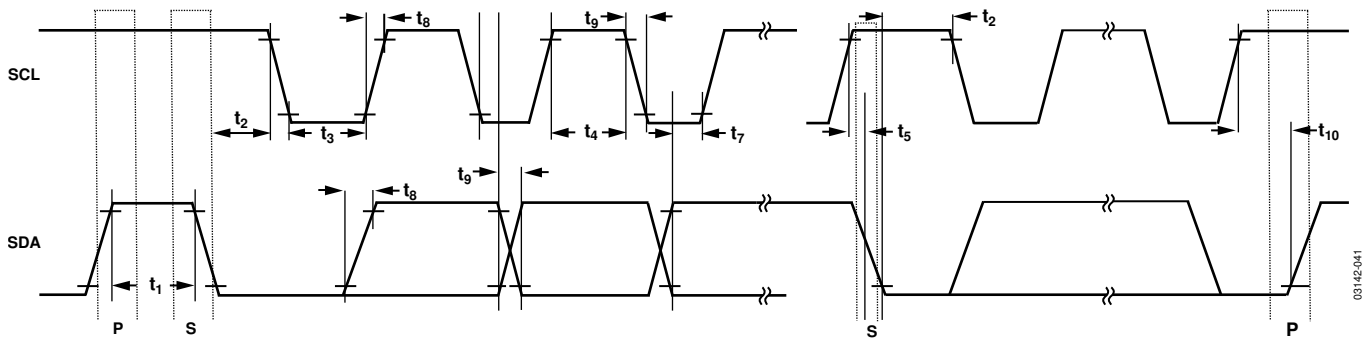


Figure 42. Detailed I<sup>2</sup>C Timing Diagram

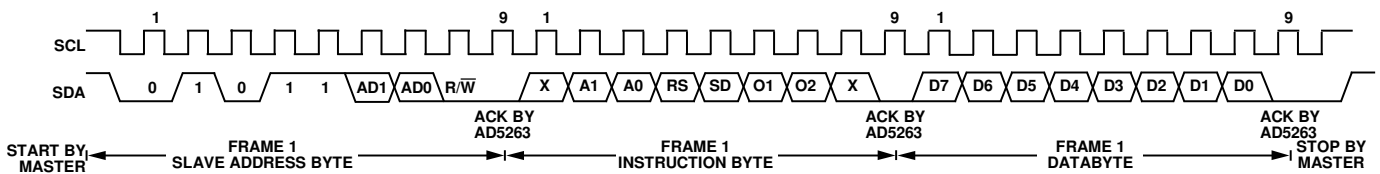


Figure 43. Writing to the RDAC Register

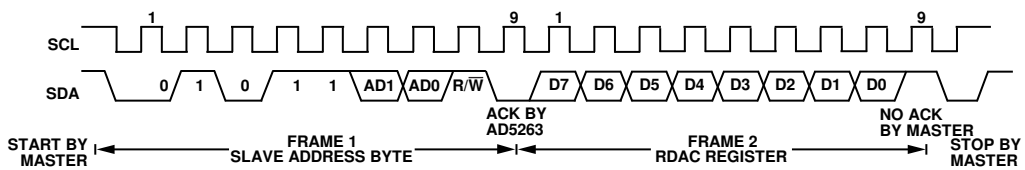


Figure 44. Reading Data from a Previously Selected RDAC Register in Write Mode

## OPERATION

The AD5263 is a quad-channel, 256-position, digitally controlled, variable resistor (VR) device.

To program the VR settings, refer to the SPI-Compatible Digital Interface (DIS = 0) section and the I2C-Compatible Digital Interface (DIS = 1) section. The part has an internal power-on preset that places the wiper at midscale during power-on, simplifying the fault condition recovery at power-up. In addition, the shutdown (SHDN) pin of AD5263 places the RDAC in an almost zero-power consumption state where Terminal A is open circuited and the wiper W is connected to Terminal B, resulting in only leakage current consumption in the VR structure. During shutdown, the VR latch settings are maintained or new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting is applied to the RDAC.

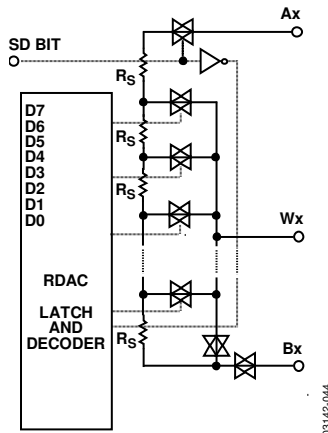


Figure 45. AD5263 Equivalent RDAC Circuit

## PROGRAMMING THE VARIABLE RESISTOR

### Rheostat Operation

The nominal resistance of the RDAC between Terminal A and Terminal B is available in 20 kΩ, 50 kΩ, and 200 kΩ. The final two or three digits of the part number determine the nominal resistance value, for example, 20 kΩ = 20; 50 kΩ = 50; 200 kΩ = 200. The nominal resistance ( $R_{AB}$ ) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assuming a 20 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Because there is a 60 Ω wiper contact resistance, such a connection yields a minimum of  $2 \times 60 \Omega$  resistance between the W and B terminals. The second connection is the first tap point, and corresponds to 198 Ω ( $R_{WB} = R_{AB}/256 + R_W = 78 \Omega + 2 \times 60 \Omega$ ) for Data 0x01. The third connection is the next tap point representing 276 Ω ( $R_{WB} = 78 \Omega \times 2 + 2 \times 60 \Omega$ ) for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 20,042 Ω

( $R_{AB} - 1 \text{ LSB} + 2 \times R_W$ ). Figure 45 shows a simplified diagram of the equivalent RDAC circuit, where the last resistor string is not accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

The general equation determining the digitally programmed output resistance between the W and B terminals is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \quad (1)$$

where:

$D$  is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.

$R_{AB}$  is the end-to-end resistance.

$R_W$  is the wiper resistance contributed by the on-resistance of one internal switch.

In summary, if  $R_{AB} = 20 \text{ k}\Omega$  and the A terminal is open circuited, the RDAC latch codes in Table 5 result in the corresponding output resistance,  $R_{WB}$ .

Table 5. Codes and Corresponding  $R_{WB}$  Resistances

D (Dec)	$R_{WB}$ (Ω)	Output State
255	20,042	Full-scale ( $R_{AB} - 1 \text{ LSB} + 2 \times R_W$ )
128	10,120	Midscale
1	198	1 LSB + $2 \times R_W$
0	120	Zero-scale (wiper contact resistance)

Note that in the zero-scale condition a finite wiper resistance of 120 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the W wiper and Terminal A also produces a digitally controlled complementary resistance,  $R_{WA}$ . When these terminals are used, the B terminal can be opened. Setting the resistance value for  $R_{WA}$  starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \quad (2)$$

For  $R_{AB} = 20 \text{ k}\Omega$  and the B terminal is open circuited, the RDAC latch codes in Table 6 result in the corresponding output resistance  $R_{WA}$ .

Table 6. Codes and Corresponding  $R_{WA}$  Resistances

D (Dec)	$R_{WA}$ (Ω)	Output State
255	198	Full scale
128	10,120	Midscale
1	20,042	1 LSB + $2 \times R_W$
0	20,120	Zero scale

The typical distribution of the end-to-end resistance  $R_{AB}$  from channel to channel matches within  $\pm 1\%$ . Device-to-device matching is process-lot dependent, and it is possible to have  $\pm 30\%$  variation. Because the resistance element is processed in thin film technology, the change in  $R_{AB}$  with temperature has a very low temperature coefficient of 30 ppm/°C.

### PROGRAMMING THE POTENTIOMETER DIVIDER VOLTAGE OUTPUT OPERATION

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage from Terminal A and Terminal B. Unlike the polarity from  $V_{DD}$  to  $V_{SS}$ , which must be positive, the voltage across A to B, W to A, and W to B can be at either polarity, if  $V_{SS}$  is powered by a negative supply.

If the effect of the wiper resistance for approximation is ignored, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage from the wiper to B, starting at 0 V up to 1 LSB below 5 V. Each LSB step of voltage is equal to the voltage applied across Terminal A to Terminal B divided by the 256 positions of the potentiometer divider. Because the AD5263 can be powered by dual supplies, the general equation defining the output voltage  $V_W$  with respect to ground for any valid input voltages applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256-D}{256}V_B \quad (3)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistances  $R_{WA}$  and  $R_{WB}$ , and not their absolute values; therefore, the temperature drift reduces to 5 ppm/°C.

### PIN-SELECTABLE DIGITAL INTERFACE

The AD5263 provides the flexibility of a selectable interface. When the digital interface select (DIS) pin is tied low, the SPI mode is engaged. When the DIS pin is tied high to the  $V_L$  supply, the I<sup>2</sup>C mode is engaged.

### SPI-COMPATIBLE 3-WIRE SERIAL BUS (DIS = 0)

The AD5263 contains a 3-wire SPI-compatible digital interface (SDI,  $\overline{CS}$ , and CLK). The 10-bit serial word must be loaded with address bits A1 and A0, followed by the data byte, MSB first. The format of the word is shown in the Serial Data-Word Format section and bit map.

The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. When  $\overline{CS}$  is low, the clock loads data into the serial register on each positive clock edge (see Figure 40).

Table 7. AD5263 Address Decode Table

A1	A0	Latch Loaded
0	0	RDAC 1
0	1	RDAC 2
1	0	RDAC 3
1	1	RDAC 4

The data setup and data hold times in the specification table determine the valid timing requirements. The AD5263 uses a 10-bit serial input data register word that is transferred to the internal RDAC register when the  $\overline{CS}$  line returns to logic high. Note that only the last 10 bits that are clocked into the register are latched into the decoder. As  $\overline{CS}$  goes high, it activates the address decoder and updates the corresponding channel according to Table 7.

During shutdown ( $\overline{SHDN}$ ), the serial data output (SDO) pin is forced to logic high in order to avoid power dissipation in the external pull-up resistor. For an equivalent SDO output circuit schematic, see Figure 46.

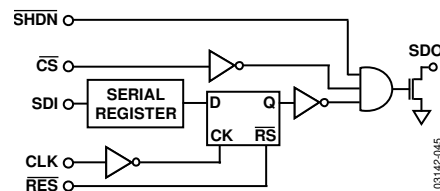


Figure 46. Detailed SDO Output Schematic of the AD5263

During reset ( $\overline{RES}$ ), the wiper is set to midscale. Note that unlike  $\overline{SHDN}$ , when the part is taken out of reset, the wiper remains at midscale and does not revert to its pre-reset setting.

### Daisy-Chain Operation

The serial data output (SDO) pin contains an open-drain N-channel FET. This output requires a pull-up resistor in order to transfer data to the SDI pin of the next package. This allows for daisy-chaining several RDACs from a single processor serial data line. The pull-up resistor termination voltage can be greater than the  $V_{DD}$  supply voltage. It is recommended to increase the clock period when using a pull-up resistor to the SDI pin of the following device because capacitive loading at the daisy-chain node (SDO to SDI) between devices may induce time delay to subsequent devices. Users should be aware of this potential problem to achieve data transfer successfully (see Figure 47). If two AD5263s are daisy-chained, a total of 20 bits of data is required. The first 10 bits, complying with the format shown in the Serial Data-Word Format section and bit map, go to U2 and the second 10 bits, with the same format, go to U1.  $\overline{CS}$  should be kept low until all 20 bits are clocked into their respective serial registers. After this,  $\overline{CS}$  is pulled high to complete the operation and load the RDAC latch. Data appears on SDO on the negative edge of the clock, thus making it available to the input of the daisy-chained device on the rising edge of the next clock.

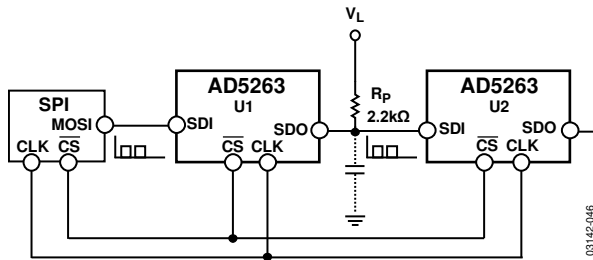


Figure 47. Daisy-Chain Configuration

### I<sup>2</sup>C-COMPATIBLE 2-WIRE SERIAL BUS (DIS = 1)

In the I<sup>2</sup>C-compatible mode, the RDACs are connected to the bus as slave devices.

Referring to the bit maps in the I<sup>2</sup>C-Compatible Digital Interface (DIS = 1) section, the first byte of the AD5263 is a slave address byte, consisting of a 7-bit slave address and a R/W bit. The five MSBs are 01011 and the following two bits are determined by the state of the AD0 and AD1 pins of the device. AD0 and AD1 allow the user to place up to four of the I<sup>2</sup>C-compatible devices on one bus.

The 2-wire I<sup>2</sup>C serial bus protocol operates as follows.

- The master initiates a data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 43). The following byte is the slave address byte, which consists of the 7-bit slave address followed by an R/W bit. This R/W bit determines whether data will be read from or written to the slave device.
 

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/W bit is high, the master reads from the slave device. If the R/W bit is low, the master writes to the slave device.
- In write mode, the second byte is the instruction byte. The first bit (MSB) of the instruction byte is a don't care. The following two bits, labeled A1 and A0, are the RDAC subaddress select bits.

The fourth MSB (RS) is the midscale reset. A logic high on this bit moves the wiper of the selected channel to the center tap where  $R_{WA} = R_{WB}$ . This feature effectively writes over the contents of the register, so that when taken out of reset mode, the RDAC remains at midscale.

The fifth MSB (SD) is the shutdown bit. A logic high causes the selected channel to open circuit at Terminal A while shorting the wiper to Terminal B. This operation yields almost  $0\ \Omega$  in rheostat mode or  $0\ V$  in potentiometer mode. This SD bit serves the same function as the SHDN pin except that the SHDN pin reacts to active low. In addition, the SHDN pin affects all channels, as opposed to the SD bit, which affects only the channel being written to. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting is applied to the RDAC.

The next two bits are O2 and O1. They are extra programmable logic outputs that can be used to drive other digital loads, logic gates, LED drivers, analog switches, etc.

The LSB is a don't care bit (see the bit map in the I<sup>2</sup>C Write Mode Data-Word Format section).

After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 43).

- In read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference with the write mode, where there are eight data bits followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 44).

Note that the channel of interest is the one that was previously selected in write mode. In cases where users need to read the RDAC values of both channels, they must program the first channel in write mode and then change to read mode to read the first channel value. After that, they must change back to write mode with the second channel selected and read the second channel value in read mode again. It is not necessary for users to issue the Frame 3 data byte in the write mode for subsequent readback operation. Refer to Figure 44 for the programming format.

- After all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a stop condition (see Figure 43). In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the tenth clock pulse, which goes high to establish a stop condition (see Figure 44).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in the write mode, the RDAC output updates on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

### ADDITIONAL PROGRAMMABLE LOGIC OUTPUT

The AD5263 features additional programmable logic outputs, O1 and O2, which can be used to drive a digital load, analog switches, and logic gates. O1 and O2 default to Logic 0. The voltage level can swing from GND to  $V_L$ . The logic states of O1 and O2 can be programmed in Frame 2 under write mode (see Figure 43). These logic outputs have adequate current driving capability to sink/source milliamperes of load.

Users can also activate O1 and O2 in three different ways without affecting the wiper settings. They may do the following:

- Start, slave address byte, acknowledge, instruction byte with O1 and O2 specified, acknowledge, Stop.
- Complete the write cycle with stop, then start, slave address byte, acknowledge, instruction byte with O1 and O2 specified, acknowledge, stop.

- Do not complete the write cycle by not issuing the stop, then start, slave address byte, acknowledge, instruction byte with O1 and O2 specified, acknowledge, stop.

### SELF-CONTAINED SHUTDOWN FUNCTION

Shutdown can be activated by strobing the  $\overline{\text{SHDN}}$  pin or programming the SD bit in the write mode instruction byte. In addition, shutdown can even be implemented with the device's digital output, as shown in Figure 48. In this configuration, the device is shut down during power-up, but users are allowed to program the device. Thus, when O1 is programmed high, the device exits from the shutdown mode and responds to the new setting. This self-contained shutdown function allows absolute shutdown during power-up, which is crucial in hazardous environments, without adding extra components.

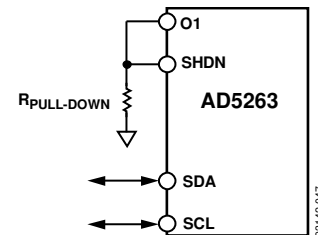


Figure 48. Shutdown by Internal Logic Output

If the shutdown function is enabled by using the SD bit, see the I<sup>2</sup>C Write Mode Data-Word Format section. Table 8 and Table 9 show the sequences that can place any channel in an undesirable shutdown state.

Table 8. Direct Sequence

Command Sequence	RDAC Shutdown
Write RDAC 1, SHDN RDAC 2	RDAC1 and RDAC2
Write RDAC 2, SHDN RDAC 1	RDAC1 and RDAC2
Write RDAC 3, SHDN RDAC 4	RDAC3 and RDAC4
Write RDAC 4, SHDN RDAC 3	RDAC3 and RDAC4

To overcome the issue, employ the following sequence, as an example for the first case:

- Start, slave address byte, acknowledge, instruction byte (write RDAC1), acknowledge, data byte, acknowledge, stop.
- Start, slave address byte, acknowledge, instruction byte (write RDAC1), acknowledge, stop.
- Start, slave address byte, acknowledge, instruction byte (SHDN RDAC2), acknowledge, data byte, acknowledge, stop.

Table 9. Indirect Sequence

Command Sequence	RDAC Shutdown
Write RDAC 1, SHDN RDAC 1, SHDN RDAC 4	RDAC1, RDAC3, and RDAC4
Write RDAC 3, SHDN RDAC 3, SHDN RDAC 2	RDAC1, RDAC2, and RDAC3

To overcome this issue, swap the SHDN order command, for example, write RDAC 1, SHDN RDAC 4, and then SHDN RDAC 1.

**MULTIPLE DEVICES ON ONE BUS**

Figure 49 shows four AD5263 devices on the same serial bus. Each has a different slave address because the states of their AD0 and AD1 pins are different. This allows each RDAC within each device to be written to or read from independently. The master device output bus line drivers are open-drain, pull-downs in a fully I<sup>2</sup>C-compatible interface.

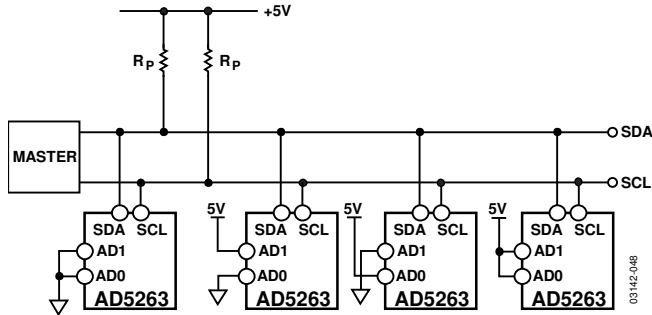


Figure 49. Multiple AD5263 Devices on One I<sup>2</sup>C Bus

**LEVEL SHIFT FOR NEGATIVE VOLTAGE OPERATION**

The digital potentiometer is popular in laser diode driver and certain telecommunication equipment level-setting applications. These applications are sometimes operated between ground and some negative supply voltage so that the systems can be biased at round to avoid large bypass capacitors that may significantly impede the ac performance. Like most digital potentiometers, the AD5263 can be configured with a negative supply (see Figure 50).

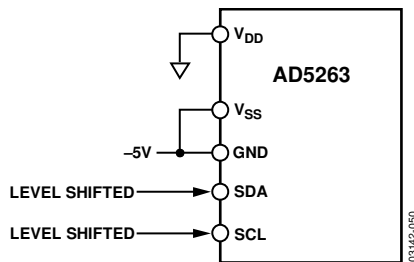


Figure 50. Biased at Negative Voltage

However, the digital inputs must also be level shifted to allow proper operation because the ground is referenced to the negative potential. As a result, Figure 51 shows one implementation with a couple of transistors and a few resistors. When V<sub>IN</sub> is high, Q1 is turned on and its emitter is clamped at one threshold above ground. This threshold appears at the base of Q2, which causes Q2 to turn off. In this state, V<sub>OUT</sub> approaches -5 V. When V<sub>IN</sub> is low, Q1 is turned off and the base of Q2 is pulled low, which in turn causes Q2 to turn on. In this state, V<sub>OUT</sub> approaches 0 V. Beware that proper time shifting is also needed for successful communication with the device.

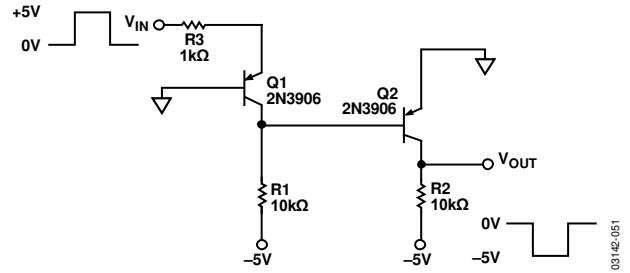


Figure 51. Level Shift for Bipolar Potential Operation

**ESD PROTECTION**

All digital inputs are protected with a series input resistor and parallel Zener ESD structures shown in Figure 52 and Figure 53. This protection applies to digital input pins SDA/SDA, CLK/SCL, CS/AD0, RES/AD1, and SHDN.

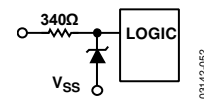


Figure 52. ESD Protection of Digital Pins

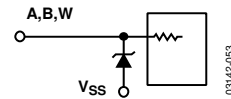


Figure 53. ESD Protection of Resistor Terminals

**TERMINAL VOLTAGE OPERATING RANGE**

The AD5263 positive V<sub>DD</sub> and negative V<sub>SS</sub> power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on the A, B, and W terminals that exceed V<sub>DD</sub> or V<sub>SS</sub> are clamped by the internal forward-biased diodes shown in Figure 54.

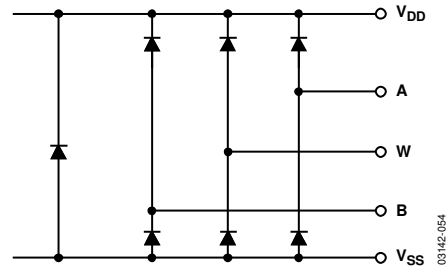


Figure 54. Maximum Terminal Voltages Set by V<sub>DD</sub> and V<sub>SS</sub>

**POWER-UP SEQUENCE**

Because the ESD protection diodes limit the voltage compliance at the A, B, and W terminals (see Figure 54), it is important to power V<sub>DD</sub> and V<sub>SS</sub> before applying any voltage to the A, B, and W terminals; otherwise, the diodes are forward biased such that V<sub>DD</sub> and V<sub>SS</sub> are powered unintentionally and may affect the rest of the circuit. The ideal power-up sequence is in the following order: GND, V<sub>DD</sub>, V<sub>SS</sub>, V<sub>L</sub>, digital inputs, and V<sub>A/B/W</sub>. The relative order of powering V<sub>A</sub>, V<sub>B</sub>, V<sub>W</sub>, and digital inputs is not important as long as they are powered after V<sub>DD</sub> and V<sub>SS</sub>.

**V<sub>LOGIC</sub> POWER SUPPLY**

The AD5263 is capable of operating at high voltages beyond the internal logic levels, which are limited to operation at 5 V. As a result, V<sub>L</sub> always needs to be tied to a separate 2.7 V to 5.5 V source to ensure proper digital signal levels. Logic levels must be limited to V<sub>L</sub>, regardless of V<sub>DD</sub>. In addition, V<sub>L</sub> should always be less than or equal to V<sub>DD</sub>.

**LAYOUT AND POWER SUPPLY BYPASSING**

It is a good practice to employ compact, minimum-lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 μF to 0.1 μF ceramic disc or chip capacitors. Low ESR 1 μF to 10 μF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 55). Notice the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

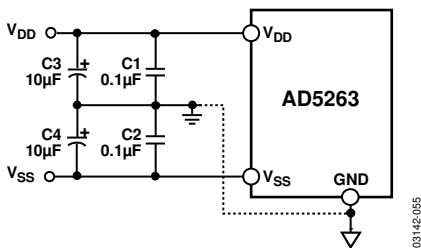


Figure 55. Power Supply Bypassing

**RDAC CIRCUIT SIMULATION MODEL**

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the RDACs. Configured as a potentiometer divider, the -3 dB bandwidth of the AD5263 (20 kΩ resistor) measures 300 kHz at half scale. Figure 22 provides the large signal BODE plot characteristics of the three available resistor versions: 20 kΩ, 50 kΩ, and 200 kΩ. A parasitic simulation model is shown in Figure 56. The following code provides a macro model net list for the 20 kΩ RDAC.

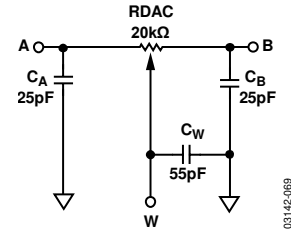


Figure 56. RDAC Circuit Simulation Model for RDAC = 20 kΩ

**Listing 1. Macro Model Net List for RDAC**

```
.PARAM D=256, RDAC=20E3
*
.SUBCKT DPOT (A,W,B)
*
CA      A      0      25E-12
RWA     A      W      {(1-D/256)*RDAC+60}
CW      W      0      55E-12
RWB     W      B      {D/256*RDAC+60}
CB      B      0      25E-12
*
.ENDS DPOT
```



## APPLICATIONS INFORMATION

### BIPOLAR DC OR AC OPERATION FROM DUAL SUPPLIES

The AD5263 can be operated from dual supplies, enabling control of ground referenced ac signals or bipolar operation. The ac signal, as high as  $V_{DD}/V_{SS}$ , can be applied directly across Terminal A to Terminal B, with the output taken from Terminal W.

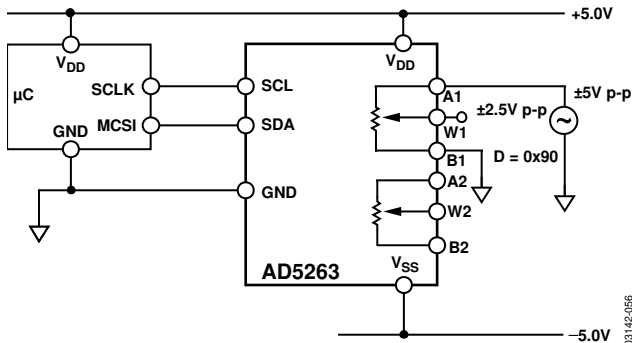


Figure 57. Bipolar Operation from Dual Supplies

### GAIN CONTROL COMPENSATION

A digital potentiometer is commonly used in gain control such as the noninverting gain amplifier shown in Figure 58.

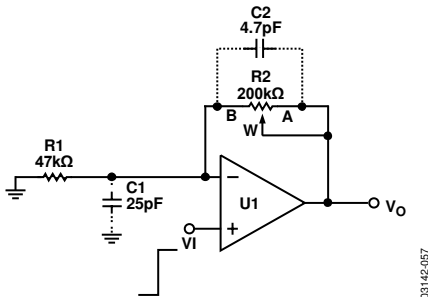


Figure 58. Typical Noninverting Gain Amplifier

Notice the RDAC B terminal parasitic capacitance is connected to the op amp noninverting node. It introduces a zero for the  $1/\beta_o$  term with +20 dB/dec, whereas a typical op amp GBP has -20 dB/dec characteristics. A large R2 and finite C1 can cause this zero's frequency to fall well below the crossover frequency. Thus, the rate of closure becomes 40 dB/dec and the system has 0° phase margin at the crossover frequency. The output may ring or oscillate if the input is a rectangular pulse or step function. Similarly, it is also likely to ring when switching between two gain values, because this is equivalent to a step change at the input.

Depending on the op amp GBP, reducing the feedback resistor may extend the zero's frequency far enough to overcome the problem. A better approach is to include a compensation capacitor C2 to cancel the effect caused by C1. Optimum compensation occurs when  $R1 \times C1 = R2 \times C2$ . This is not an option, because of the variation of R2. As a result, one may use the relationship described and scale C2 as if R2 is at its maximum value. Doing so may overcompensate and compromise the performance slightly when R2 is set at low values. However, it avoids the gain peaking, ringing, or oscillation in the worst case. For critical applications, C2 should be found empirically to suit the need. In general, C2 in the range of a few pF to no more than a few tenths of pF is usually adequate for the compensation.

Similarly, there are W and A terminal capacitances connected to the output (not shown); fortunately, their effect at this node is less significant and the compensation can be disregarded in most cases.

### PROGRAMMABLE VOLTAGE REFERENCE

For voltage divider mode operation (Figure 59), it is common to buffer the output of the digital potentiometer unless the load is much larger than  $R_{WB}$ . Not only does the buffer serve the purpose of impedance conversion, but it also allows a heavier load to be driven.

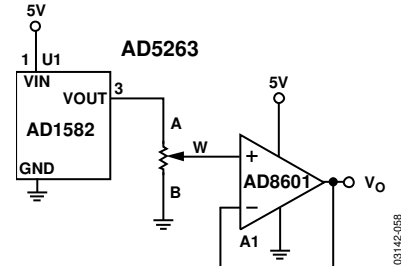


Figure 59. Programmable Voltage Reference

**8-BIT BIPOLAR DAC**

Figure 60 shows a low cost, 8-bit, bipolar DAC. It offers the same number of adjustable steps, but not the precision as compared to conventional DACs. The linearity and temperature coefficient, especially at low values codes, are skewed by the effects of the digital potentiometer wiper resistance. The output of this circuit is

$$V_O = \left( \frac{2D}{256} - 1 \right) \times V_{REF} \quad (4)$$

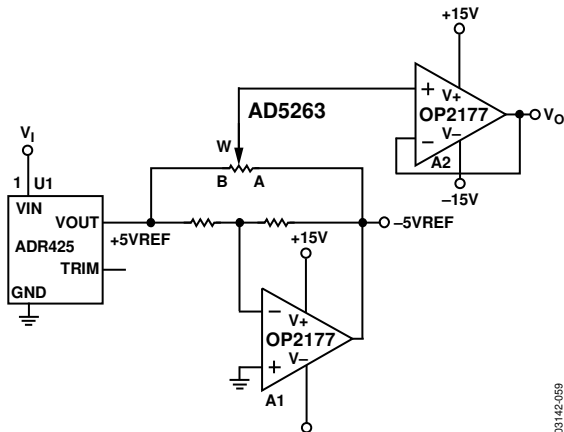


Figure 60. 8-Bit Bipolar DAC

**BIPOLAR PROGRAMMABLE GAIN AMPLIFIER**

For applications requiring bipolar gain, Figure 61 shows one implementation similar to the previous circuit. The digital potentiometer U1 sets the adjustment range. The wiper voltage at W2 can therefore be programmed between  $V_I$  and  $-KV_I$  at a given U2 setting. Configuring A2 in the noninverting mode allows linear gain and attenuation. The transfer function is

$$\frac{V_O}{V_I} = \left( 1 + \frac{R2}{R1} \right) \times \left( \frac{D2}{256} \times (1+K) - K \right) \quad (5)$$

where  $K$  is the ratio of  $R_{WB1}/R_{WA1}$  set by U1.

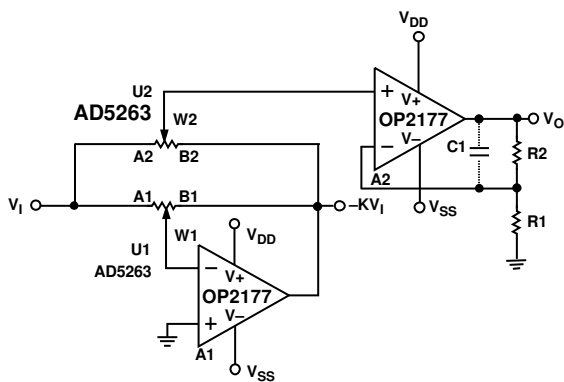


Figure 61. Bipolar Programmable Gain Amplifier

Similar to the previous example, in the simpler (and much more usual) case where  $K = 1$ , a single channel is used and U1 is replaced by a matched pair of resistors to apply  $V_I$  and  $-V_I$  at the ends of the digital potentiometer. The relationship becomes

$$V_O = \left( 1 + \frac{R2}{R1} \right) \times \left( \frac{2 \times D2}{256} - 1 \right) \times V_I \quad (6)$$

If R2 is large, a compensation capacitor of a few pF may be needed to avoid any gain peaking.

Table 10 shows the result of adjusting D, with A2 configured with unity gain, gain of 2, and gain of 10. The result is a bipolar amplifier with linearly programmable gain and 256-step resolution.

Table 10. Result of Bipolar Gain Amplifier

D	R1 = ∞, R2 = 0	R1 = R2	R2 = 9 × R1
0	-1	-2	-10
64	-0.5	-1	-5
128	0	0	0
192	0.5	1	5
255	0.968	1.937	9.680

**PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT**

For applications that require high current adjustment, such as a laser diode driver or tunable laser, a boosted voltage source can be considered. See Figure 62.

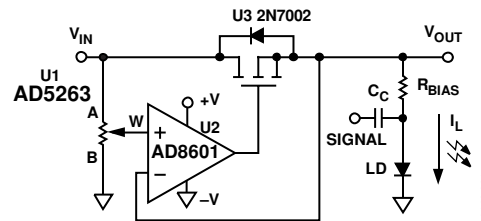


Figure 62. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces the  $V_{OUT}$  to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-channel FET, N1. N1 power handling must be adequate to dissipate power equal to  $(V_{IN} - V_{OUT}) \times I_L$ . This circuit can source a maximum of 100 mA with a 5 V supply. For precision applications, a voltage reference such as ADR421 or ADR03 can be applied at the A terminal of the digital potentiometer.