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## FEATURES

- Single-channel, 256-/1024-position resolution
- 20 k $\Omega$ , 50 k $\Omega$ , and 100 k $\Omega$  nominal resistance
- Maximum  $\pm 1\%$  nominal resistor tolerance error (resistor performance mode)
- 20-times programmable wiper memory
- Rheostat mode temperature coefficient: 35 ppm/ $^{\circ}\text{C}$
- Voltage divider temperature coefficient: 5 ppm/ $^{\circ}\text{C}$
- +9 V to +33 V single-supply operation
- $\pm 9$  V to  $\pm 16.5$  V dual-supply operation
- SPI-compatible serial interface
- Wiper setting readback
- Power-on refreshed from 20-TP memory

## APPLICATIONS

- Mechanical potentiometer replacement
- Instrumentation: gain and offset adjustment
- Programmable voltage-to-current conversion
- Programmable filters, delays, and time constants
- Programmable power supply
- Low resolution DAC replacement
- Sensor calibration

## GENERAL DESCRIPTION

The [AD5291](#) and [AD5292](#) are single-channel, 256-/1024-position digital potentiometers<sup>1</sup> that combine industry leading variable resistor performance with nonvolatile memory (NVM) in a compact package. These devices are capable of operating across a wide voltage range, supporting both dual supply operation at  $\pm 10.5$  V to  $\pm 16.5$  V and single supply operation at +21 V to +33 V, while ensuring less than 1% end-to-end resistor tolerance error and offering 20-time programmable (20-TP) memory.

The guaranteed industry leading low resistor tolerance error feature simplifies open-loop applications as well as precision calibration and tolerance matching applications.

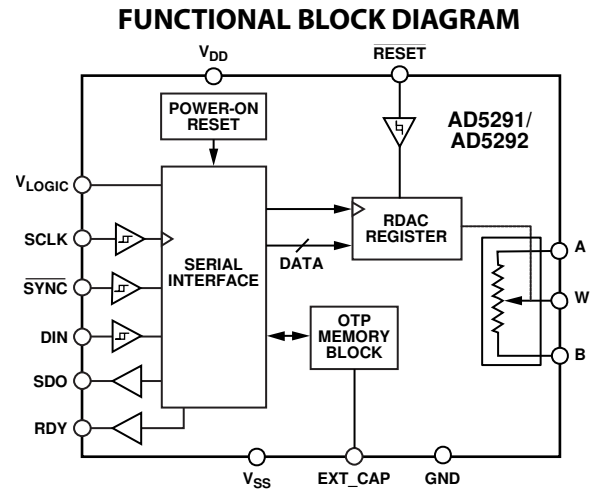


Figure 1.

The [AD5291](#) and [AD5292](#) device wiper settings are controllable through the SPI digital interface. Unlimited adjustments are allowed before programming the resistance value into the 20-TP memory. The [AD5291](#) and [AD5292](#) do not require any external voltage supply to facilitate fuse blow, and there are 20 opportunities for permanent programming. During 20-TP activation, a permanent blow fuse command freezes the wiper position (analogous to placing epoxy on a mechanical trimmer).

The [AD5291](#) and [AD5292](#) are available in a compact 14-lead TSSOP package. The part is guaranteed to operate over the extended industrial temperature range of  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ .

<sup>1</sup> The terms digital potentiometer and RDAC are used interchangeably.

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## REVISION HISTORY

### 12/14—Rev. D to Rev. E

Changes to Shift Register Section and Table 11 ..... 22

### 9/10—Rev. C to Rev. D

Changes to SDO Pin and Daisy-Chain Operation Section..... 25

### 3/10—Rev. B to Rev. C

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### 3/10—Rev. A to Rev. B

Changes to Data Sheet Title ..... 1

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### 12/09—Rev. 0 to Rev. A

Added 50 k $\Omega$  and 100 k $\Omega$  specifications..... Universal

Changes to Features Section .....

Changes to Table 1.....

Changes to Table 2.....

Added Table 3 .....

Changes to Table 4.....

Changes to Table 5.....

Added Table 6 .....

Change to Table 7 .....

Changes to Absolute Maximum Rating Section .....

Changes Table 9 .....

Changes to Typical Performance Characteristics Section .....

Changes to Ordering Guide .....

### 4/09—Revision 0: Initial Version

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—AD5291

$V_{DD} = 21\text{ V to }33\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ;  $V_{DD} = 10.5\text{ V to }16.5\text{ V}$ ,  $V_{SS} = -10.5\text{ V to }-16.5\text{ V}$ ;  $V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_A = V_{DD}$ ,  $V_B = V_{SS}$ ,  
 $-40^\circ\text{C} < T_A < +105^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N		8			Bits
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$R_{WB}$ , $V_A = \text{NC}$	-1		+1	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL		-1		+1	LSB
Nominal Resistor Tolerance (R-Perf Mode) <sup>3</sup>	$\Delta R_{AB}/R_{AB}$	See Table 2, Table 3	-1	$\pm 0.5$	+1	%
Nominal Resistor Tolerance (Normal Mode)	$\Delta R_{AB}/R_{AB}$			$\pm 7$		%
Resistance Temperature Coefficient <sup>4</sup>	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full-scale; See Figure 38		35		ppm/°C
Wiper Resistance	$R_W$	Code = zero scale		60	100	$\Omega$
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Resolution	N		8			Bits
Differential Nonlinearity <sup>5</sup>	DNL		-0.5		+0.5	LSB
Integral Nonlinearity <sup>5</sup>	INL		-0.5		+0.5	LSB
Voltage Divider Temperature Coefficient <sup>4</sup>	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half-scale; See Figure 41		1.5		ppm/°C
Full-Scale Error	$V_{WFSE}$	Code = full scale	-2		+0.25	LSB
Zero-Scale Error	$V_{WZSE}$	Code = zero scale	0		2	LSB
RESISTOR TERMINALS						
Terminal Voltage Range <sup>6</sup>	$V_A$ , $V_B$ , $V_W$		$V_{SS}$		$V_{DD}$	V
Capacitance A, Capacitance B <sup>4</sup>	$C_A$ , $C_B$	$f = 1\text{ MHz}$ , measured to GND, code = half-scale		85		pF
Capacitance W <sup>4</sup>	$C_W$	$f = 1\text{ MHz}$ , measured to GND, code = half-scale		65		pF
Common-Mode Leakage Current <sup>4</sup>	$I_{CM}$	$V_A = V_B = V_W$		$\pm 1$		nA
DIGITAL INPUTS						
Input Logic High <sup>4</sup>	$V_{IH}$	JEDEC compliant $V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$	2.0			V
Input Logic Low <sup>4</sup>	$V_{IL}$	$V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$			0.8	V
Input Current	$I_{IL}$	$V_{IN} = 0\text{ V or }V_{LOGIC}$			$\pm 1$	$\mu\text{A}$
Input Capacitance <sup>4</sup>	$C_{IL}$			5		pF
DIGITAL OUTPUTS (SDO and RDY)						
Output High Voltage <sup>4</sup>	$V_{OH}$	$R_{PULL\_UP} = 2.2\text{ k}\Omega$ to $V_{LOGIC}$	$V_{LOGIC} - 0.4$			V
Output Low Voltage <sup>4</sup>	$V_{OL}$	$R_{PULL\_UP} = 2.2\text{ k}\Omega$ to $V_{LOGIC}$			GND + 0.4 V	V
Three-State Leakage Current			-1		+1	$\mu\text{A}$
Output Capacitance <sup>4</sup>	$C_{OL}$			5		pF
POWER SUPPLIES						
Single-Supply Power Range	$V_{DD}$	$V_{SS} = 0\text{ V}$	9		33	V
Dual-Supply Power Range	$V_{DD}/V_{SS}$		$\pm 9$		$\pm 16.5$	V
Positive Supply Current	$I_{DD}$	$V_{DD}/V_{SS} = \pm 16.5\text{ V}$		0.1	2	$\mu\text{A}$
Negative Supply Current	$I_{SS}$	$V_{DD}/V_{SS} = \pm 16.5\text{ V}$	-2	-0.1		$\mu\text{A}$
Logic Supply Range	$V_{LOGIC}$		2.7		5.5	V
Logic Supply Current	$I_{LOGIC}$	$V_{LOGIC} = 5\text{ V}$ ; $V_{IH} = 5\text{ V or }V_{IL} = \text{GND}$		1	10	$\mu\text{A}$
OTP Store Current <sup>4,7</sup>	$I_{LOGIC\_PROG}$	$V_{IH} = 5\text{ V or }V_{IL} = \text{GND}$		25		mA
OTP Read Current <sup>4,8</sup>	$I_{LOGIC\_FUSE\_READ}$	$V_{IH} = 5\text{ V or }V_{IL} = \text{GND}$		25		mA
Power Dissipation <sup>9</sup>	$P_{DISS}$	$V_{IH} = 5\text{ V or }V_{IL} = \text{GND}$		8	110	$\mu\text{W}$
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS} = \pm 15\text{ V} \pm 10\%$ $R_{AB} = 20\text{ k}\Omega$ $R_{AB} = 50\text{ k}\Omega$ $R_{AB} = 100\text{ k}\Omega$		0.103 0.039 0.021		%/%

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
DYNAMIC CHARACTERISTICS <sup>5, 10</sup>						
Bandwidth	BW	−3 dB, code = half-scale R <sub>AB</sub> = 20 kΩ R <sub>AB</sub> = 50 kΩ R <sub>AB</sub> = 100 kΩ		520 210 105		kHz
Total Harmonic Distortion	THD <sub>w</sub>	V <sub>A</sub> = 1 V rms, V <sub>B</sub> = 0 V, f = 1 kHz R <sub>AB</sub> = 20 kΩ R <sub>AB</sub> = 50 kΩ R <sub>AB</sub> = 100 kΩ		−93 −101 −106		dB
V <sub>w</sub> Settling Time	t <sub>s</sub>	V <sub>A</sub> = 30 V, V <sub>B</sub> = 0 V, ±0.5 LSB error band, initial code = zero scale, board capacitance = 170 pF Code = full-scale, normal mode Code = full-scale, R-Perf mode Code = half-scale, normal mode R <sub>AB</sub> = 20 kΩ R <sub>AB</sub> = 50 kΩ R <sub>AB</sub> = 100 kΩ Code = half-scale, R-Perf mode R <sub>AB</sub> = 20 kΩ R <sub>AB</sub> = 50 kΩ R <sub>AB</sub> = 100 kΩ		750 2.5 2.5 7 14 5 9 16		ns μs μs μs
Resistor Noise Density	e <sub>N_WB</sub>	Code = half-scale, T <sub>A</sub> = 25°C, 0 kHz to 200 kHz R <sub>AB</sub> = 20 kΩ R <sub>AB</sub> = 50 kΩ R <sub>AB</sub> = 100 kΩ		10 18 27		nV/√Hz

<sup>1</sup> Typical values represent average readings at 25°C, V<sub>DD</sub> = 15 V, V<sub>SS</sub> = −15 V, and V<sub>LOGIC</sub> = 5 V.

<sup>2</sup> Resistor position nonlinearity error. R-INL is the deviation from an ideal value measured between the R<sub>WB</sub> at code 0x02 to code 0xFF or between R<sub>WA</sub> at code 0xFD to code 0x00. R-DNL measures the relative step change from ideal between successive tap positions. The specification is guaranteed in resistor performance mode, with a wiper current of 1 mA for V<sub>A</sub> < 12 V and 1.2 mA for V<sub>A</sub> ≥ 12 V.

<sup>3</sup> Resistor performance mode (see the Resistor Performance Mode section). The terms resistor performance mode and R-Perf mode are used interchangeably.

<sup>4</sup> Guaranteed by design and characterization, not subject to production test.

<sup>5</sup> INL and DNL are measured at V<sub>WB</sub> with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V<sub>A</sub> = V<sub>DD</sub> and V<sub>B</sub> = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

<sup>6</sup> Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.

<sup>7</sup> Different from operating current; supply current for fuse program lasts approximately 550 μs.

<sup>8</sup> Different from operating current; supply current for fuse read lasts approximately 550 μs.

<sup>9</sup> P<sub>DISS</sub> is calculated from (I<sub>DD</sub> × V<sub>DD</sub>) + (I<sub>SS</sub> × V<sub>SS</sub>) + (I<sub>LOGIC</sub> × V<sub>LOGIC</sub>).

<sup>10</sup> All dynamic characteristics use V<sub>DD</sub> = 15 V, V<sub>SS</sub> = −15 V, and V<sub>LOGIC</sub> = 5 V.

## RESISTOR PERFORMANCE MODE CODE RANGE

Table 2.

Resistor Tolerance per Code	R <sub>AB</sub> = 20 kΩ							
	V <sub>DD</sub> − V <sub>SS</sub>   = 30 V to 33 V		V <sub>DD</sub> − V <sub>SS</sub>   = 26 V to 30 V		V <sub>DD</sub> − V <sub>SS</sub>   = 22 V to 26 V		V <sub>DD</sub> − V <sub>SS</sub>   = 21 V to 22 V	
	R <sub>WB</sub>	R <sub>WA</sub>	R <sub>WB</sub>	R <sub>WA</sub>	R <sub>WB</sub>	R <sub>WA</sub>	R <sub>WB</sub>	R <sub>WA</sub>
1% R-Tolerance	From 0x5A to 0xFF	From 0x00 to 0xA5	From 0x7D to 0xFF	From 0x00 to 0x82	From 0x7D to 0xFF	From 0x00 to 0x82	N/A	N/A
2% R-Tolerance	From 0x23 to 0xFF	From 0x00 to 0xDC	From 0x2D to 0xFF	From 0x00 to 0xD2	From 0x23 to 0xFF	From 0x00 to 0xDC	From 0x23 to 0xFF	From 0x00 to 0xDC
3% R-Tolerance	From 0x1E to 0xFF	From 0x00 to 0xE1	From 0x19 to 0xFF	From 0x00 to 0xE6	From 0x17 to 0xFF	From 0x00 to 0xE8	From 0x17 to 0xFF	From 0x00 to 0xE8

Table 3.

Resistor Tolerance per Code	$R_{AB} = 50 \text{ k}\Omega$				$R_{AB} = 100 \text{ k}\Omega$			
	$ V_{DD} - V_{SS}  = 26 \text{ V to } 33 \text{ V}$		$ V_{DD} - V_{SS}  = 21 \text{ V to } 26 \text{ V}$		$ V_{DD} - V_{SS}  = 26 \text{ V to } 33 \text{ V}$		$ V_{DD} - V_{SS}  = 21 \text{ V to } 26 \text{ V}$	
	$R_{WB}$	$R_{WA}$	$R_{WB}$	$R_{WA}$	$R_{WB}$	$R_{WA}$	$R_{WB}$	$R_{WA}$
1% R-Tolerance	From 0x2A to 0xFF	From 0x00 to 0xD5	From 0x37 to 0xFF	From 0x00 to 0xC8	From 0x1E to 0xFF	From 0x00 to 0xE1	From 0x14 to 0xFF	From 0x00 to 0xEB
2% R-Tolerance	From 0x11 to 0xFF	From 0x00 to 0xEE	From 0x16 to 0xFF	From 0x00 to 0xE9	From 0x0A to 0xFF	From 0x00 to 0xF5	From 0x0A to 0xFF	From 0x00 to 0xF5
3% R-Tolerance	From 0x0A to 0xFF	From 0x00 to 0xF5	From 0x0D to 0xFF	From 0x00 to 0xF2	From 0x07 to 0xFF	From 0x00 to 0xF8	From 0x07 to 0xFF	From 0x00 to 0xF8

**ELECTRICAL CHARACTERISTICS—AD5292**

$V_{DD} = 21\text{ V to }33\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ;  $V_{DD} = 10.5\text{ V to }16.5\text{ V}$ ,  $V_{SS} = -10.5\text{ V to }-16.5\text{ V}$ ;  $V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_A = V_{DD}$ ,  $V_B = V_{SS}$ ,  
 $-40^\circ\text{C} < T_A < +105^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>DC CHARACTERISTICS—RHEOSTAT MODE</b>						
Resolution	N		10			Bits
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$R_{WB}$ , $V_A = NC$	-1		+1	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	$R_{AB} = 50\text{ k}\Omega$ , $100\text{ k}\Omega$	-2		+2	LSB
	R-INL	$R_{AB} = 20\text{ k}\Omega$ , $ V_{DD} - V_{SS}  = 26\text{ V to }33\text{ V}$	-2		+2	LSB
	R-INL	$R_{AB} = 20\text{ k}\Omega$ , $ V_{DD} - V_{SS}  = 21\text{ V to }26\text{ V}$	-3		+3	LSB
Nominal Resistor Tolerance (R-Perf Mode) <sup>3</sup>	$\Delta R_{AB}/R_{AB}$	See Table 5 and Table 6	-1	$\pm 0.5$	+1	%
Nominal Resistor Tolerance (Normal Mode) <sup>4</sup>	$\Delta R_{AB}/R_{AB}$			$\pm 7$		%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale; See Figure 38		35		ppm/ $^\circ\text{C}$
Wiper Resistance	$R_W$	Code = zero scale		60	100	$\Omega$
<b>DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE</b>						
Resolution	N		10			Bits
Differential Nonlinearity <sup>5</sup>	DNL		-1		+1	LSB
Integral Nonlinearity <sup>5</sup>	INL		-1.5		+1.5	LSB
Voltage Divider Temperature Coefficient <sup>4</sup>	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale; See Figure 41		5		ppm/ $^\circ\text{C}$
Full-Scale Error	$V_{WFSE}$	Code = full scale	-8		+1	LSB
Zero-Scale Error	$V_{WZSE}$	Code = zero scale	0		8	LSB
<b>RESISTOR TERMINALS</b>						
Terminal Voltage Range <sup>4</sup>	$V_A$ , $V_B$ , $V_W$		$V_{SS}$		$V_{DD}$	V
Capacitance A, Capacitance B <sup>6</sup>	$C_A$ , $C_B$	$f = 1\text{ MHz}$ , measured to GND, code = half scale		85		pF
Capacitance W <sup>5</sup>	$C_W$	$f = 1\text{ MHz}$ , measured to GND, code = half scale		65		pF
Common-Mode Leakage Current <sup>4</sup>	$I_{CM}$	$V_A = V_B = V_W$		$\pm 1$		nA
<b>DIGITAL INPUTS</b>						
Input Logic High <sup>4</sup>	$V_{IH}$	JEDEC compliant $V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$	2.0			V
Input Logic Low <sup>4</sup>	$V_{IL}$	$V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$			0.8	V
Input Current	$I_{IL}$	$V_{IN} = 0\text{ V or }V_{LOGIC}$			$\pm 1$	$\mu\text{A}$
Input Capacitance <sup>4</sup>	$C_{IL}$			5		pF
<b>DIGITAL OUTPUTS (SDO and RDY)</b>						
Output High Voltage <sup>4</sup>	$V_{OH}$	$R_{PULL\_UP} = 2.2\text{ k}\Omega$ to $V_{LOGIC}$	$V_{LOGIC} - 0.4$			V
Output Low Voltage <sup>4</sup>	$V_{OL}$	$R_{PULL\_UP} = 2.2\text{ k}\Omega$ to $V_{LOGIC}$			$GND + 0.4$	V
Three-State Leakage Current			-1		+1	$\mu\text{A}$
Output Capacitance <sup>4</sup>	$C_{OL}$			5		pF
<b>POWER SUPPLIES</b>						
Single-Supply Power Range	$V_{DD}$	$V_{SS} = 0\text{ V}$	9		33	V
Dual-Supply Power Range	$V_{DD}/V_{SS}$		$\pm 9$		$\pm 16.5$	V
Positive Supply Current	$I_{DD}$	$V_{DD}/V_{SS} = \pm 16.5\text{ V}$		0.1	2	$\mu\text{A}$
Negative Supply Current	$I_{SS}$	$V_{DD}/V_{SS} = \pm 16.5\text{ V}$	-2	-0.1		$\mu\text{A}$
Logic Supply Range	$V_{LOGIC}$		2.7		5.5	V
Logic Supply Current	$I_{LOGIC}$	$V_{LOGIC} = 5\text{ V}$ ; $V_{IH} = 5\text{ V or }V_{IL} = GND$		1	10	$\mu\text{A}$
OTP Store Current <sup>6,7</sup>	$I_{LOGIC\_PROG}$	$V_{IH} = 5\text{ V or }V_{IL} = GND$		25		mA
OTP Read Current <sup>6,8</sup>	$I_{LOGIC\_FUZE\_READ}$	$V_{IH} = 5\text{ V or }V_{IL} = GND$		25		mA
Power Dissipation <sup>9</sup>	$P_{DISS}$	$V_{IH} = 5\text{ V or }V_{IL} = GND$		8	110	$\mu\text{W}$
Power Supply Rejection Ratio <sup>6</sup>	PSSR	$\Delta V_{DD}/\Delta V_{SS} = \pm 15\text{ V} \pm 10\%$ $R_{AB} = 20\text{ k}\Omega$ $R_{AB} = 50\text{ k}\Omega$ $R_{AB} = 100\text{ k}\Omega$		0.103 0.039 0.021		%/%

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
DYNAMIC CHARACTERISTICS <sup>5, 10</sup>						
Bandwidth	BW	–3 dB R <sub>AB</sub> = 20 kΩ R <sub>AB</sub> = 50 kΩ R <sub>AB</sub> = 100 kΩ		520 210 105		kHz
Total Harmonic Distortion	THD <sub>W</sub>	V <sub>A</sub> = 1 V rms, V <sub>B</sub> = 0 V, f = 1 kHz R <sub>AB</sub> = 20 kΩ R <sub>AB</sub> = 50 kΩ R <sub>AB</sub> = 100 kΩ		–93 –101 –106		dB
V <sub>W</sub> Settling Time	t <sub>S</sub>	V <sub>A</sub> = 30 V, V <sub>B</sub> = 0 V, ±0.5 LSB error band, initial code = zero scale, board capacitance = 170 pF Code = full-scale, normal mode Code = full-scale, R-Perf mode Code = half-scale, normal mode R <sub>AB</sub> = 20 kΩ R <sub>AB</sub> = 50 kΩ R <sub>AB</sub> = 100 kΩ Code = half-scale, R-Perf mode R <sub>AB</sub> = 20 kΩ R <sub>AB</sub> = 50 kΩ R <sub>AB</sub> = 100 kΩ		750 2.5 2.5 7 14 5 9 16		ns μs μs μs
Resistor Noise Density	e <sub>N, WB</sub>	Code = half-scale, T <sub>A</sub> = 25°C, 0 kHz to 200 kHz R <sub>AB</sub> = 20 kΩ R <sub>AB</sub> = 50 kΩ R <sub>AB</sub> = 100 kΩ		10 18 27		nV/√Hz

<sup>1</sup> Typical values represent average readings at 25°C, V<sub>DD</sub> = 15 V, V<sub>SS</sub> = –15 V, and V<sub>LOGIC</sub> = 5 V.

<sup>2</sup> Resistor position nonlinearity error. R-INL is the deviation from an ideal value measured between the R<sub>WB</sub> at code 0x00B to code 0x3FF or between R<sub>WA</sub> at code 0x3F3 to code 0x000. R-DNL measures the relative step change from ideal between successive tap positions. The specification is guaranteed in resistor performance mode, with a wiper current of 1 mA for V<sub>A</sub> < 12 V and 1.2 mA for V<sub>A</sub> ≥ 12 V.

<sup>3</sup> Resistor performance mode (see the Resistor Performance Mode section). The terms resistor performance mode and R-Perf mode are used interchangeably.

<sup>4</sup> Guaranteed by design and characterization, not subject to production test.

<sup>5</sup> INL and DNL are measured at V<sub>W</sub> with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V<sub>A</sub> = V<sub>DD</sub> and V<sub>B</sub> = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

<sup>6</sup> Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.

<sup>7</sup> Different from operating current; supply current for fuse program lasts approximately 550 μs.

<sup>8</sup> Different from operating current; supply current for fuse read lasts approximately 550 μs.

<sup>9</sup> P<sub>DISS</sub> is calculated from (I<sub>DD</sub> × V<sub>DD</sub>) + (I<sub>SS</sub> × V<sub>SS</sub>) + (I<sub>LOGIC</sub> × V<sub>LOGIC</sub>).

<sup>10</sup> All dynamic characteristics use V<sub>DD</sub> = 15 V, V<sub>SS</sub> = –15 V, and V<sub>LOGIC</sub> = 5 V.

## RESISTOR PERFORMANCE MODE CODE RANGE

Table 5.

Resistor Tolerance per Code	R <sub>AB</sub> = 20 kΩ							
	V <sub>DD</sub> – V <sub>SS</sub>   = 30 V to 33 V		V <sub>DD</sub> – V <sub>SS</sub>   = 26 V to 30 V		V <sub>DD</sub> – V <sub>SS</sub>   = 22 V to 26 V		V <sub>DD</sub> – V <sub>SS</sub>   = 21 V to 22 V	
	R <sub>WB</sub>	R <sub>WA</sub>	R <sub>WB</sub>	R <sub>WA</sub>	R <sub>WB</sub>	R <sub>WA</sub>	R <sub>WB</sub>	R <sub>WA</sub>
1% R-Tolerance	From 0x15E to 0x3FF	From 0x000 to 0x2A1	From 0x1F4 to 0x3FF	From 0x000 to 0x20B	From 0x1F4 to 0x3FF	From 0x000 to 0x20B	N/A	N/A
2% R-Tolerance	From 0x8C to 0x3FF	From 0x000 to 0x373	From 0xB4 to 0x3FF	From 0x000 to 0x34B	From 0xFA to 0x3FF	From 0x000 to 0x305	From 0xFA to 0x3FF	From 0x000 to 0x305
3% R-Tolerance	From 0x5A to 0x3FF	From 0x000 to 0x3A5	From 0x64 to 0x3FF	From 0x000 to 0x39B	From 0x78 to 0x3FF	From 0x000 to 0x387	From 0x78 to 0x3FF	From 0x000 to 0x387



Table 6.

Resistor Tolerance per Code	$R_{AB} = 50\text{ k}\Omega$				$R_{AB} = 100\text{ k}\Omega$			
	$ V_{DD} - V_{SS}  = 26\text{ V to }33\text{ V}$		$ V_{DD} - V_{SS}  = 21\text{ V to }26\text{ V}$		$ V_{DD} - V_{SS}  = 26\text{ V to }33\text{ V}$		$ V_{DD} - V_{SS}  = 21\text{ V to }26\text{ V}$	
	$R_{WB}$	$R_{WA}$	$R_{WB}$	$R_{WA}$	$R_{WB}$	$R_{WA}$	$R_{WB}$	$R_{WA}$
1% R-Tolerance	From 0x08C to 0x3FF	From 0x000 to 0x35F	From 0x0B4 to 0x3FF	From 0x000 to 0x31E	From 0x04B to 0x3FF	From 0x000 to 0x3B4	From 0x064 to 0x3FF	From 0x000 to 0x39B
2% R-Tolerance	From 0x03C to 0x3FF	From 0x000 to 0x3C3	From 0x050 to 0x3FF	From 0x000 to 0x3AF	From 0x028 to 0x3FF	From 0x000 to 0x3D7	From 0x028 to 0x3FF	From 0x000 to 0x3D7
3% R-Tolerance	From 0x028 to 0x3FF	From 0x000 to 0x3D7	From 0x032 to 0x3FF	From 0x000 to 0x3CD	From 0x019 to 0x3FF	From 0x000 to 0x3E6	From 0x019 to 0x3FF	From 0x000 to 0x3E6

## INTERFACE TIMING SPECIFICATIONS

$V_{DD}/V_{SS} = \pm 15\text{ V}$ ,  $V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$ ,  $-40^\circ\text{C} < T_A < +105^\circ\text{C}$ . All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 7.

Parameter	Limit <sup>1</sup>	Unit	Description
$t_1^2$	20	ns min	SCLK cycle time
$t_2$	10	ns min	SCLK high time
$t_3$	10	ns min	SCLK low time
$t_4$	10	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge setup time
$t_5$	5	ns min	Data setup time
$t_6$	5	ns min	Data hold time
$t_7$	1	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
$t_8$	400 <sup>3</sup>	ns min	Minimum $\overline{\text{SYNC}}$ high time
$t_9$	14	ns min	$\overline{\text{SYNC}}$ rising edge to next SCLK fall ignore
$t_{10}^4$	1	ns min	RDY rising edge to $\overline{\text{SYNC}}$ falling edge
$t_{11}^4$	40	ns max	$\overline{\text{SYNC}}$ rising edge to RDY fall time
$t_{12}^4$	2.4	$\mu\text{s max}$	RDY low time, RDAC register write command execute time (R-Perf mode)
$t_{12}^4$	410	ns max	RDY low time, RDAC register write command execute time (normal mode)
$t_{12}^4$	8	ms max	RDY low time, memory program execute time
$t_{12}^4$	1.5	ms min	Software/hardware reset
$t_{13}^4$	450	ns max	RDY low time, RDAC register readback execute time
$t_{13}^4$	1.3	ms max	RDY low time, memory readback execute time
$t_{14}^4$	450	ns max	SCLK rising edge to SDO valid
$t_{\text{RESET}}$	20	ns min	Minimum $\overline{\text{RESET}}$ pulse width (asynchronous)
$t_{\text{POWER-UP}}^5$	2	ms max	Power-on OTP restore time

<sup>1</sup> All input signals are specified with  $t_r = t_f = 1\text{ ns/V}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .

<sup>2</sup> Maximum SCLK frequency is 50 MHz.

<sup>3</sup> Refer to  $t_{12}$  and  $t_{13}$  for RDAC register and memory commands operations.

<sup>4</sup>  $R_{\text{PULL-UP}} = 2.2\text{ k}\Omega$  to  $V_{\text{LOGIC}}$ , with a capacitance load of 168 pF.

<sup>5</sup> Maximum time after  $V_{\text{LOGIC}}$  is equal to 2.5 V.

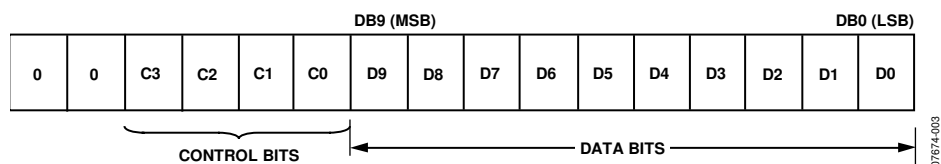


Figure 2. Shift Register Content

Timing Diagrams

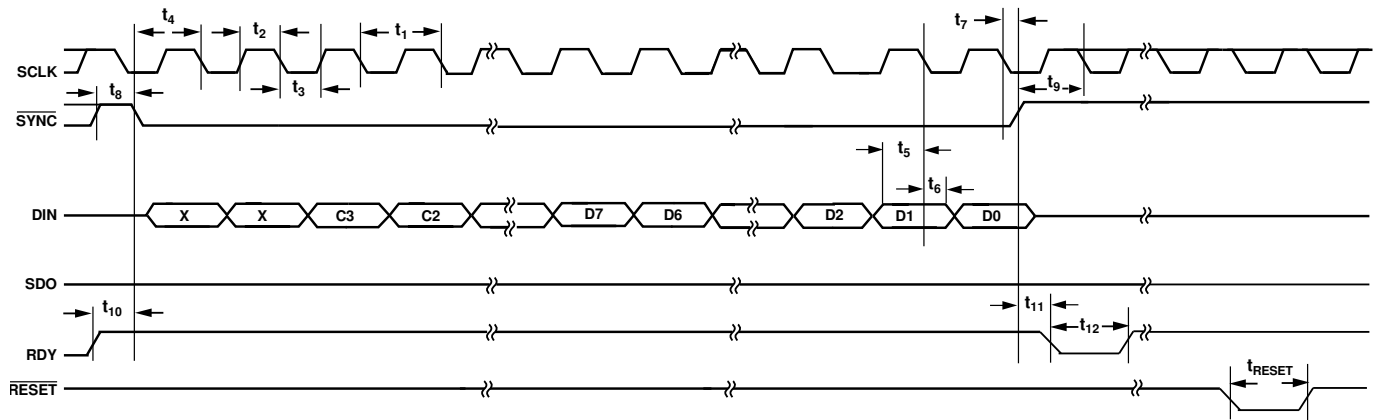


Figure 3. Write Timing Diagram, CPOL = 0, CPHA = 1

07674-004

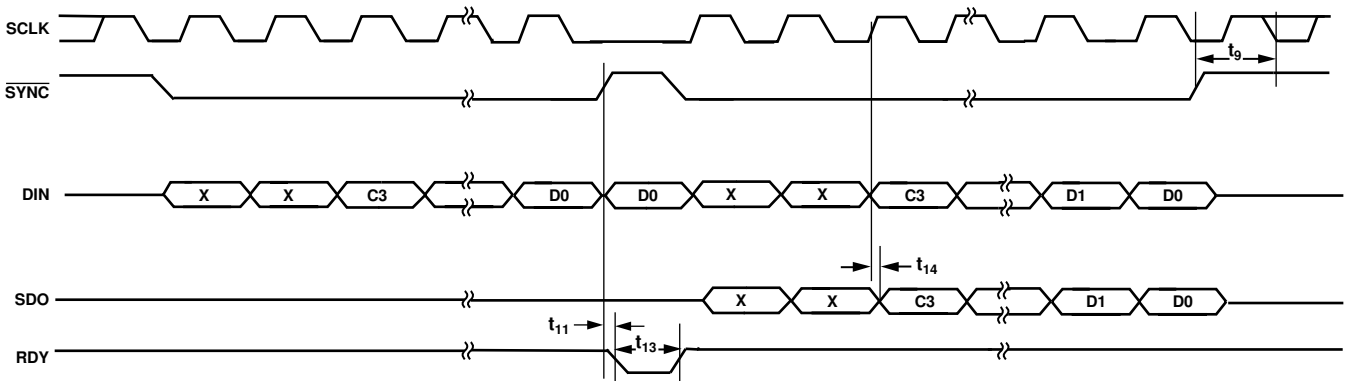


Figure 4. Read Timing Diagram, CPOL = 0, CPHA = 1

07674-005

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 8.

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +35 V
$V_{SS}$ to GND	+0.3 V to -25 V
$V_{LOGIC}$ to GND	-0.3 V to +7 V
$V_{DD}$ to $V_{SS}$	35 V
$V_A, V_B, V_W$ to GND	$V_{SS} - 0.3\text{ V}, V_{DD} + 0.3\text{ V}$
Digital Input and Output Voltage to GND	-0.3 V to $V_{LOGIC} + 0.3\text{ V}$
EXT_CAP Voltage to GND	-0.3 V to +7 V
$I_A, I_B, I_W$	
Continuous	
$R_{AB} = 20\text{ k}\Omega$	$\pm 3\text{ mA}$
$R_{AB} = 50\text{ k}\Omega, 100\text{ k}\Omega$	$\pm 2\text{ mA}$
Pulsed <sup>1</sup>	
Frequency > 10 kHz	$MCC^2/d^3$
Frequency $\leq 10\text{ kHz}$	$MCC^2/\sqrt{d^3}$
Operating Temperature Range <sup>4</sup>	-40°C to +105°C
Maximum Junction Temperature ( $T_J$ max)	150°C
Storage Temperature Range	-65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$

<sup>1</sup> Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

<sup>2</sup> Maximum continuous current

<sup>3</sup> Pulse duty factor.

<sup>4</sup> Includes programming of OTP memory.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### THERMAL RESISTANCE

$\theta_{JA}$  is defined by JEDEC specification JESD-51 and the value is dependent on the test board and test environment.

Table 9. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
14-Lead TSSOP	93 <sup>1</sup>	20	°C/W

<sup>1</sup> JEDEC 252P test board, still air (0 m/sec to 1 m/sec airflow).

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

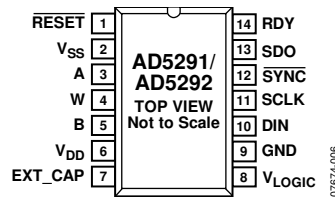


Figure 5. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RESET	Hardware Reset Pin. Refreshes the RDAC register with the contents of the 20-TP memory register. Factory default loads midscale until the first 20-TP wiper memory location is programmed. RESET is activated at the logic high transition. Tie RESET to V <sub>LOGIC</sub> if not used.
2	V <sub>SS</sub>	Negative Supply. Connect to 0 V for single-supply applications. This pin should be decoupled with 0.1 μF ceramic capacitors and 10 μF capacitors.
3	A	Terminal A of RDAC. $V_{SS} \leq V_A \leq V_{DD}$ .
4	W	Wiper Terminal of RDAC. $V_{SS} \leq V_W \leq V_{DD}$ .
5	B	Terminal B of RDAC. $V_{SS} \leq V_B \leq V_{DD}$ .
6	V <sub>DD</sub>	Positive Power Supply. This pin should be decoupled with 0.1 μF ceramic capacitors and 10 μF capacitors.
7	EXT_CAP	External Capacitor. Connect a 1 μF capacitor to EXT_CAP. This capacitor must have a voltage rating of ≥7 V.
8	V <sub>LOGIC</sub>	Logic Power Supply; 2.7 V to 5.5 V. This pin should be decoupled with 0.1 μF ceramic capacitors and 10 μF capacitors.
9	GND	Ground Pin, Logic Ground Reference.
10	DIN	Serial Data Input. The AD5291 and AD5292 have a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
11	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.
12	SYNC	Falling Edge Synchronization Signal. This is the frame synchronization signal for the input data. When SYNC goes low, it enables the shift register and data is transferred in on the falling edges of the following clocks. The selected register is updated on the rising edge of SYNC following the 16 <sup>th</sup> clock cycle. If SYNC is taken high before the 16 <sup>th</sup> clock cycle, the rising edge of SYNC acts as an interrupt, and the write sequence is ignored by the DAC.
13	SDO	Serial Data Output. This open-drain output requires an external pull-up resistor. SDO can be used to clock data from the shift register in daisy-chain mode or in readback mode.
14	RDY	Ready Pin. This active-high open-drain output identifies the completion of a write or read operation to or from the RDAC register or memory.

TYPICAL PERFORMANCE CHARACTERISTICS

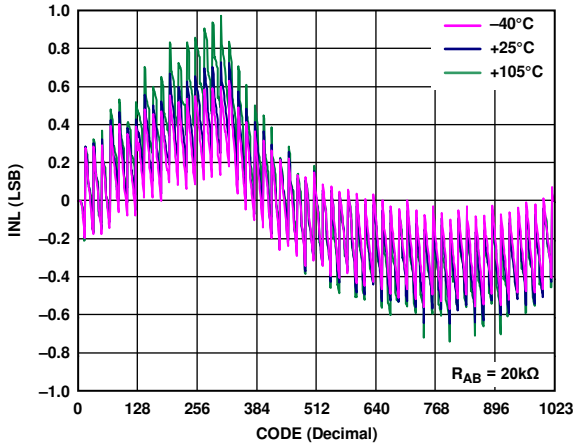


Figure 6. R-INL in R-Perf Mode vs. Code vs. Temperature (AD5292)

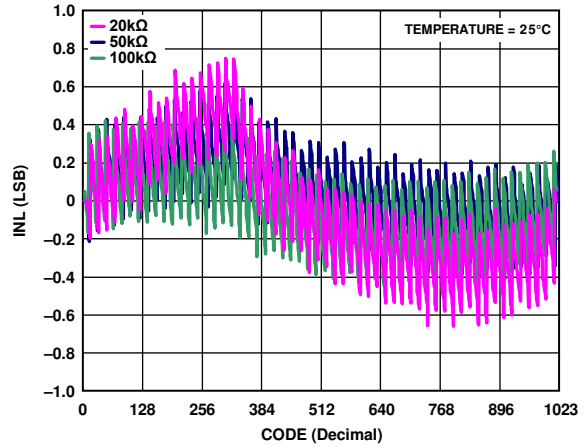


Figure 9. R-INL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5292)

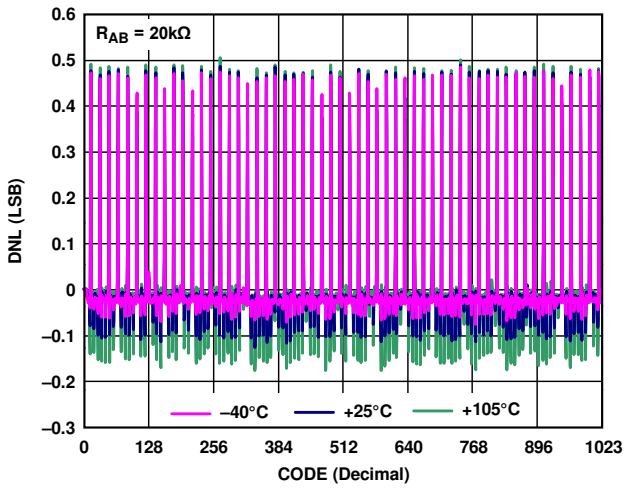


Figure 7. R-DNL in R-Perf Mode vs. Code vs. Temperature (AD5292)

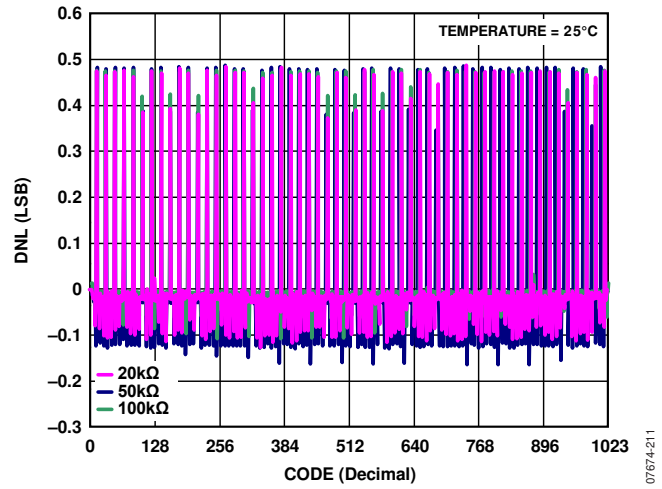


Figure 10. R-DNL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5292)

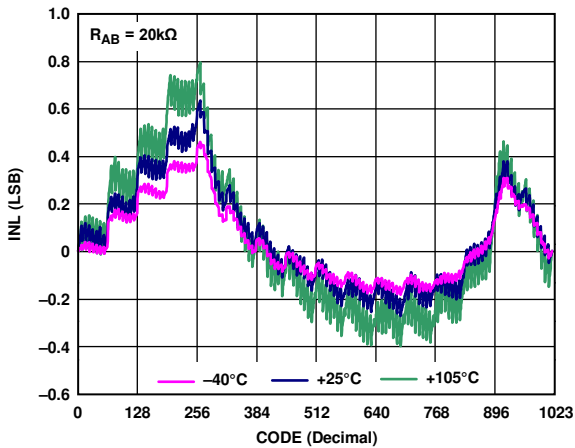


Figure 8. R-INL in Normal Mode vs. Code vs. Temperature (AD5292)

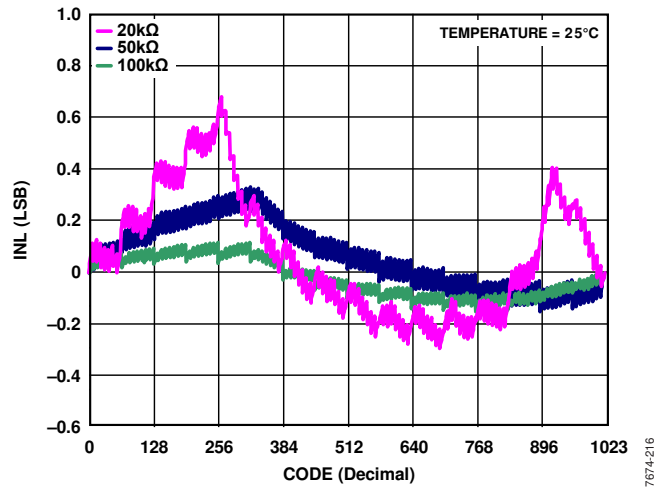


Figure 11. R-INL in Normal Mode vs. Code vs. Nominal Resistance (AD5292)

07674-108

07674-215

07674-007

07674-211

07674-010

07674-216

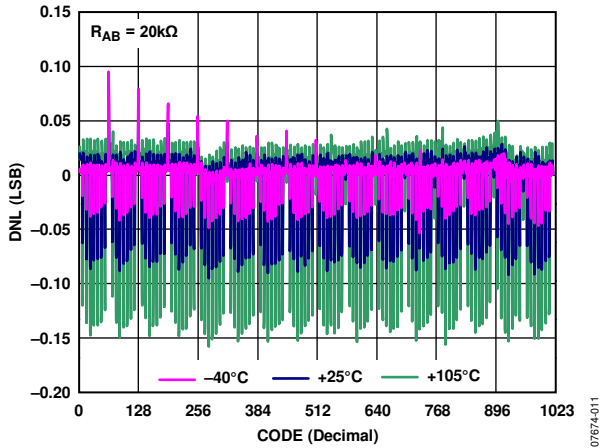


Figure 12. R-DNL in Normal Mode vs. Code vs. Temperature (AD5292)

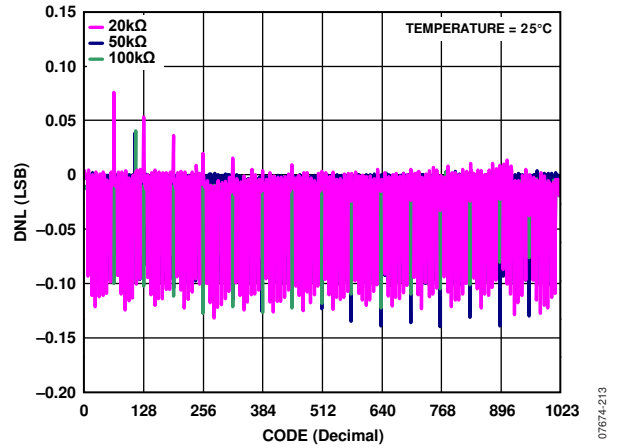


Figure 15. R-DNL in Normal Mode vs. Code vs. Nominal Resistance (AD5292)

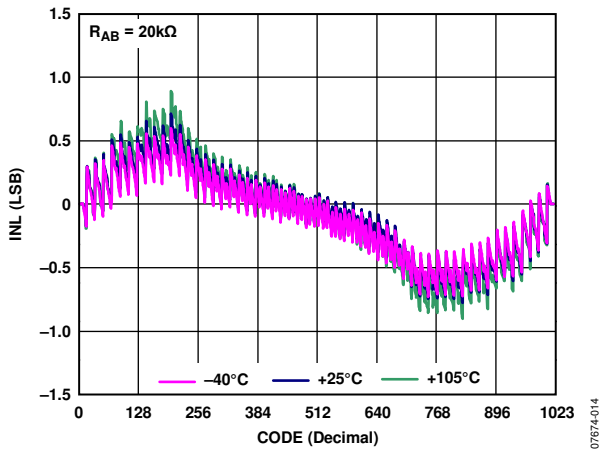


Figure 13. INL in R-Perf Mode vs. Code vs. Temperature (AD5292)

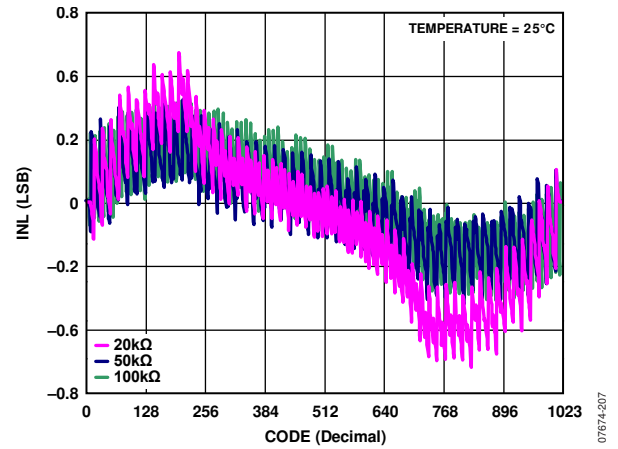


Figure 16. INL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5292)

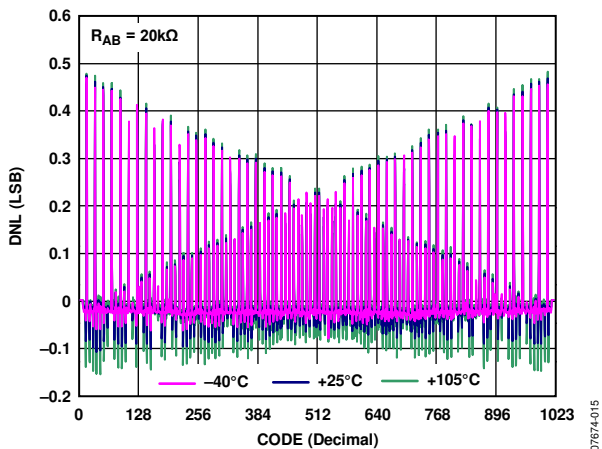


Figure 14. DNL in R-Perf Mode vs. Code vs. Temperature (AD5292)

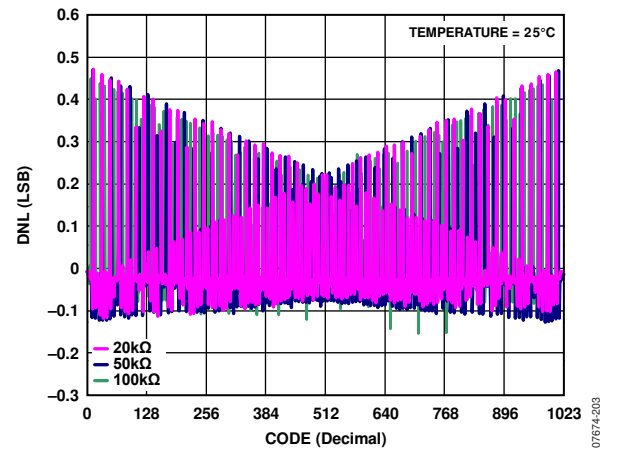


Figure 17. DNL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5292)

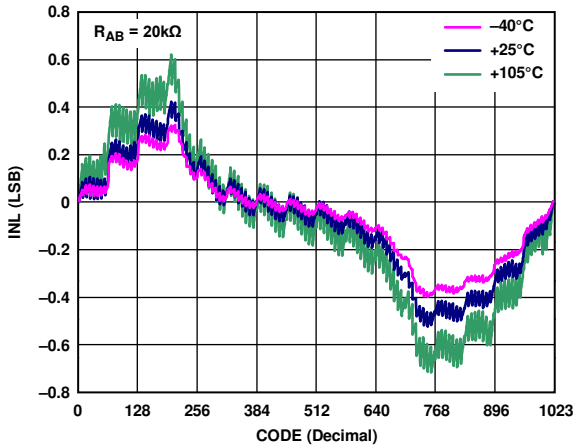


Figure 18. INL in Normal Mode vs. Code vs. Temperature (AD5292)

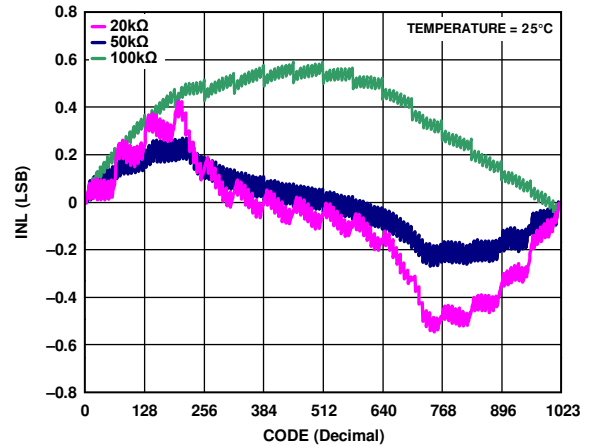


Figure 21. INL in Normal Mode vs. Code vs. Nominal Resistance (AD5292)

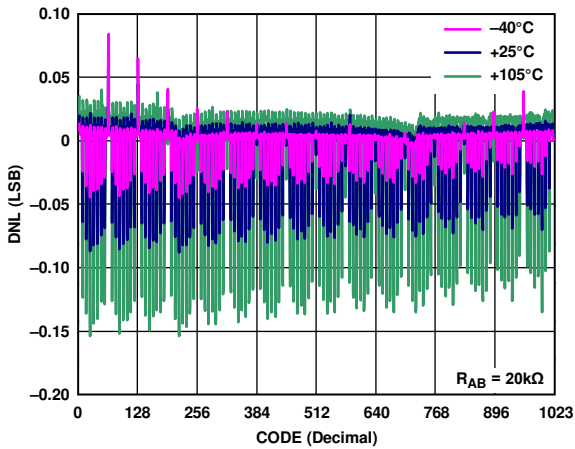


Figure 19. DNL in Normal Mode vs. Code vs. Temperature (AD5292)

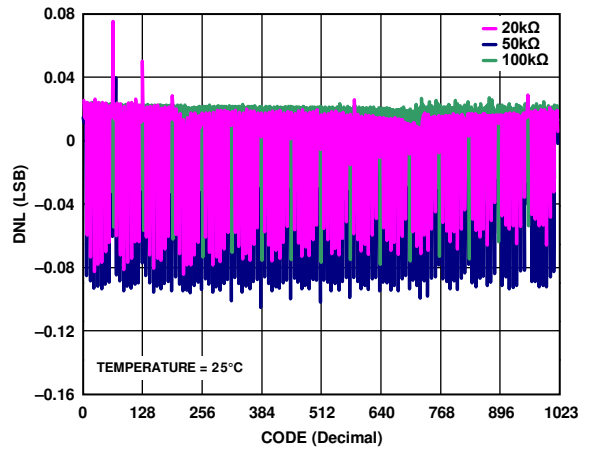


Figure 22. DNL in Normal Mode vs. Code vs. Nominal Resistance (AD5292)

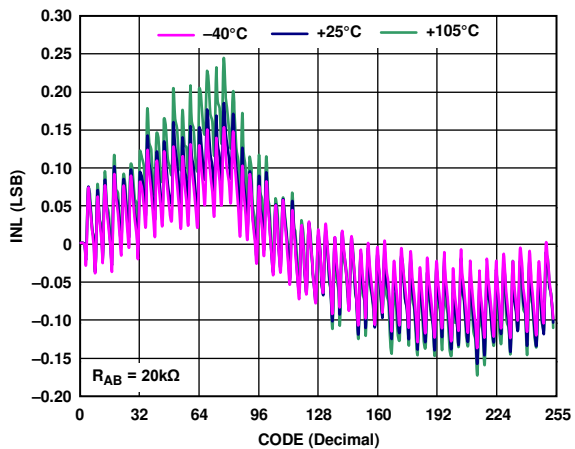


Figure 20. R-INL in R-Perf Mode vs. Code vs. Temperature (AD5292)

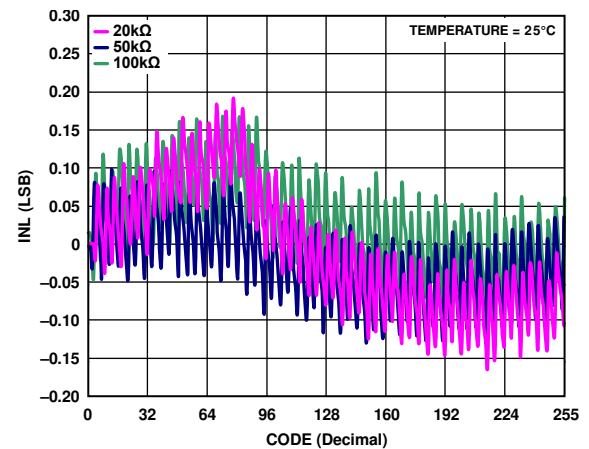


Figure 23. R-INL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5292)

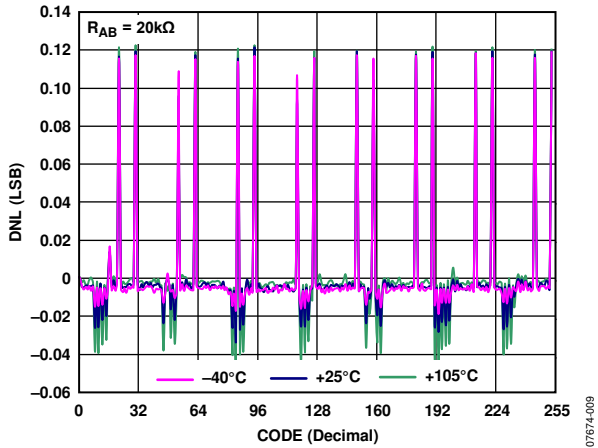


Figure 24. R-DNL in R-Perf Mode vs. Code vs. Temperature (AD5291)

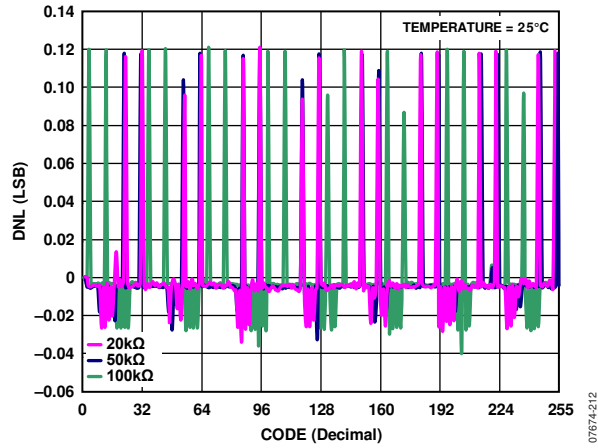


Figure 27. R-DNL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5291)

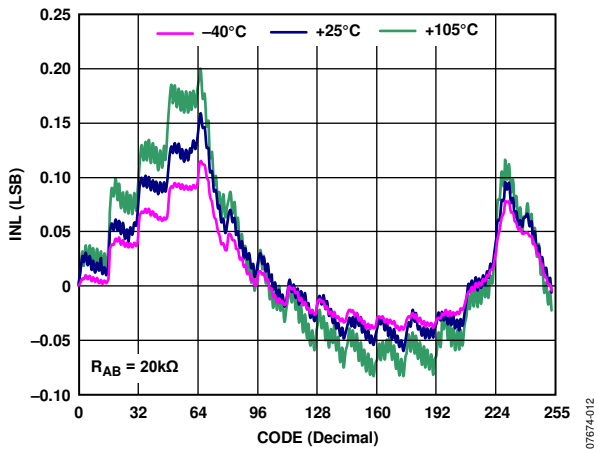


Figure 25. R-INL in Normal Mode vs. Code vs. Temperature (AD5291)

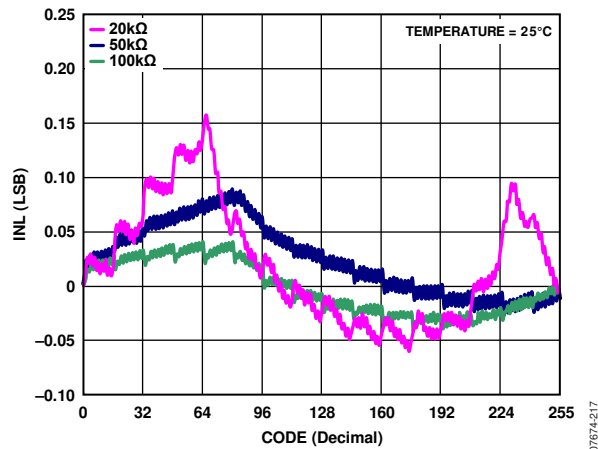


Figure 28. R-INL in Normal Mode vs. Code vs. Nominal Resistance (AD5291)

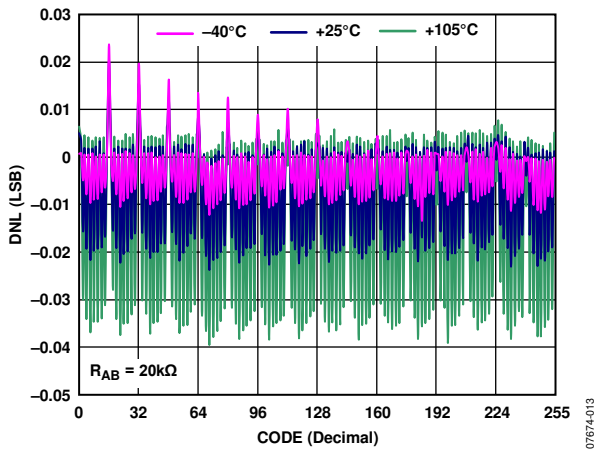


Figure 26. R-DNL in Normal Mode vs. Code vs. Temperature (AD5291)

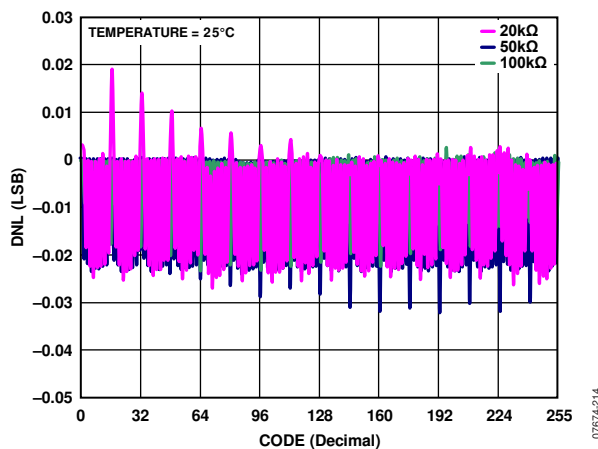
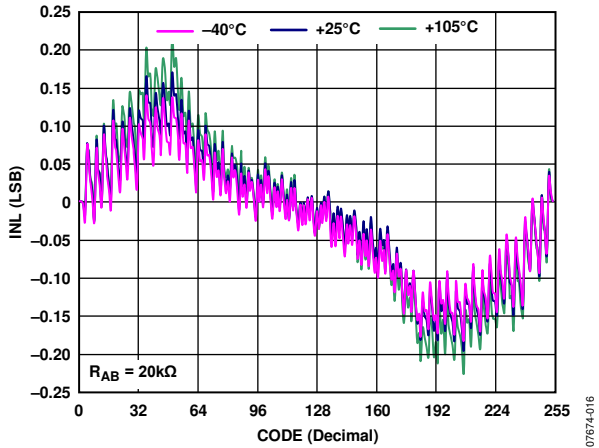


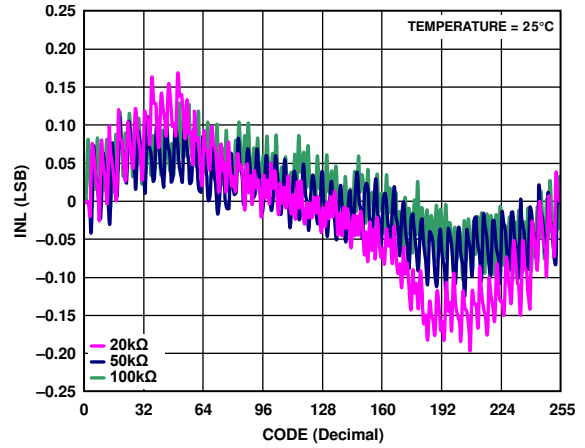
Figure 29. R-DNL in Normal Mode vs. Code vs. Nominal Resistance (AD5291)





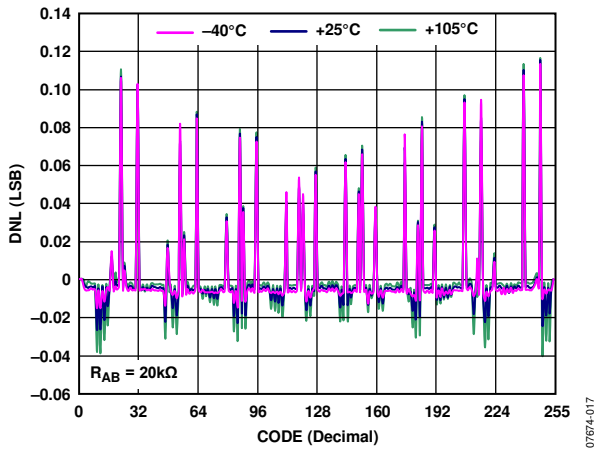
07674-016

Figure 30. INL in R-Perf Mode vs. Code vs. Temperature (AD5291)



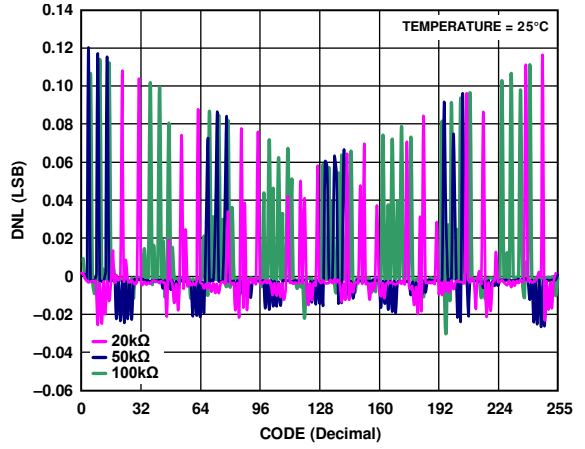
07674-208

Figure 33. INL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5291)



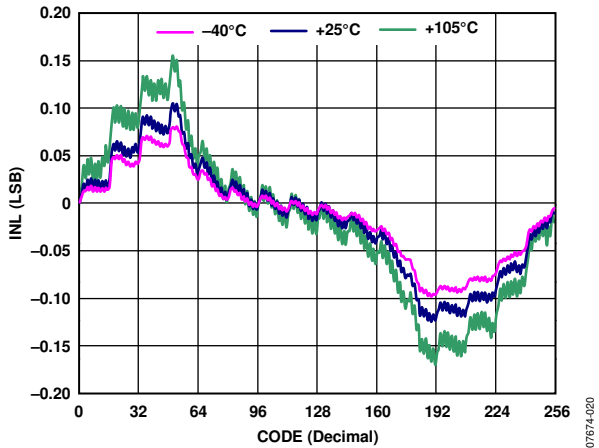
07674-017

Figure 31. DNL in R-Perf Mode vs. Code vs. Temperature (AD5291)



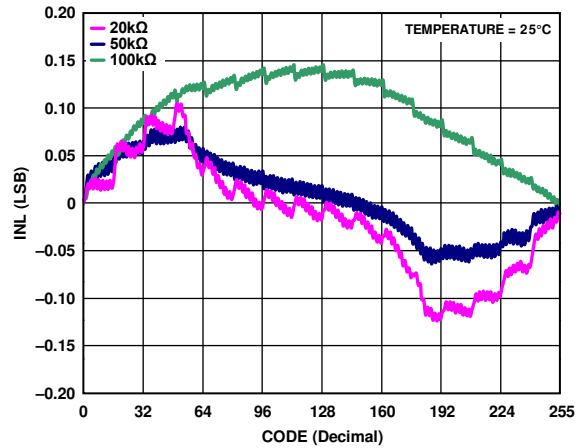
07674-204

Figure 34. DNL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5291)



07674-020

Figure 32. INL in Normal Mode vs. Code vs. Temperature (AD5291)



07674-210

Figure 35. INL in Normal Mode vs. Code vs. Nominal Resistance (AD5291)

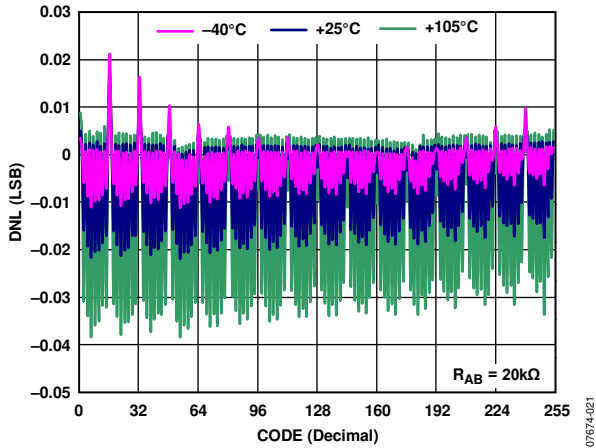


Figure 36. DNL in Normal Mode vs. Code vs. Temperature (AD5291)

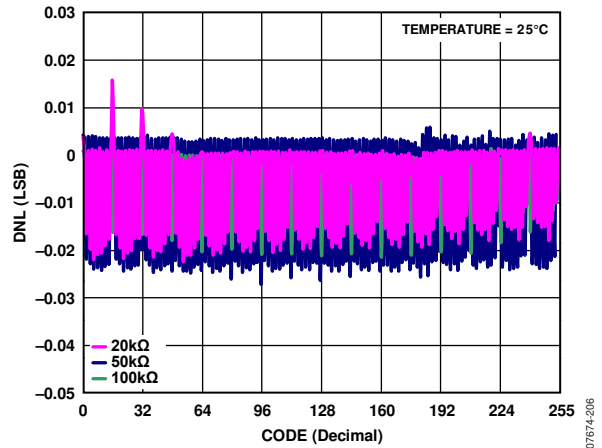


Figure 39. DNL in Normal Mode vs. Code vs. Temperature (AD5291)

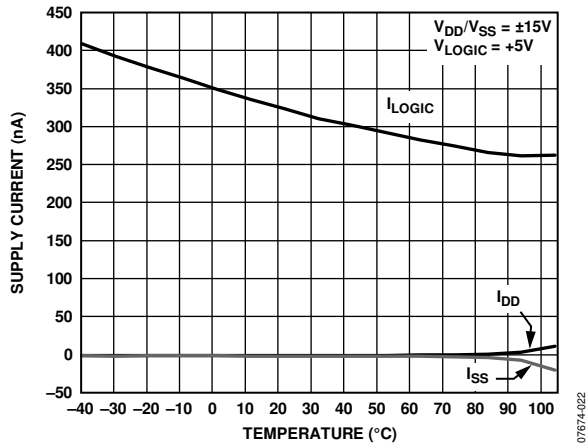


Figure 37. Supply Current ( $I_{DD}$ ,  $I_{SS}$ ,  $I_{LOGIC}$ ) vs. Temperature

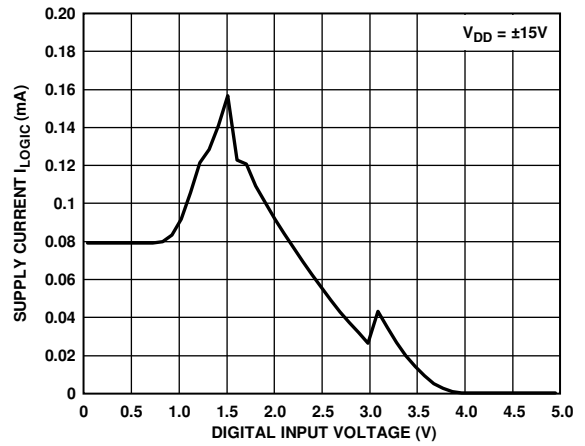


Figure 40. Supply Current  $I_{LOGIC}$  vs. Digital Input Voltage

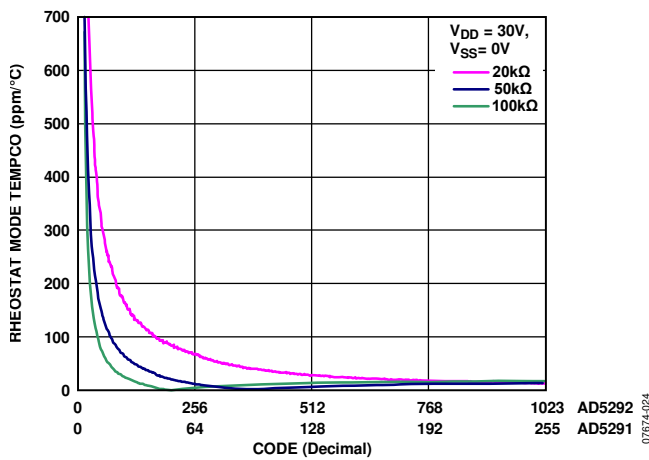


Figure 38. Rheostat Mode Tempco  $\Delta R_{WB}/\Delta T$  vs. Code

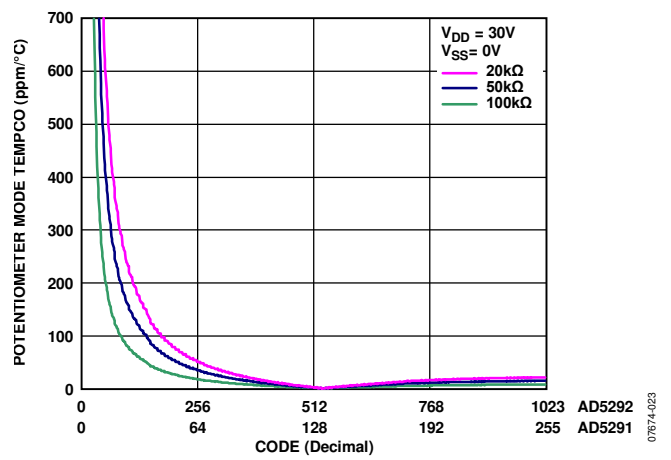


Figure 41. Potentiometer Mode Tempco  $\Delta R_{WB}/\Delta T$  vs. Code

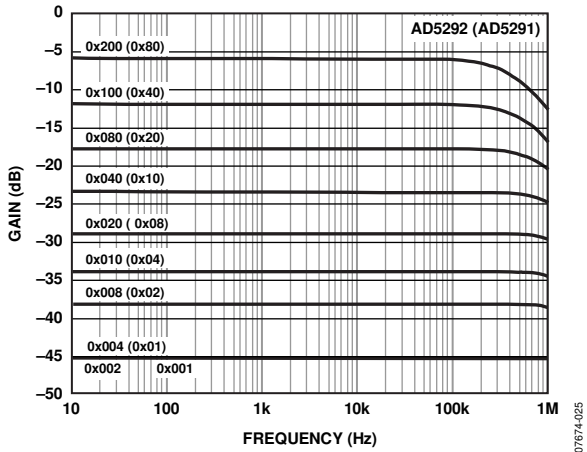


Figure 42. 20 kΩ Gain vs. Frequency vs. Code

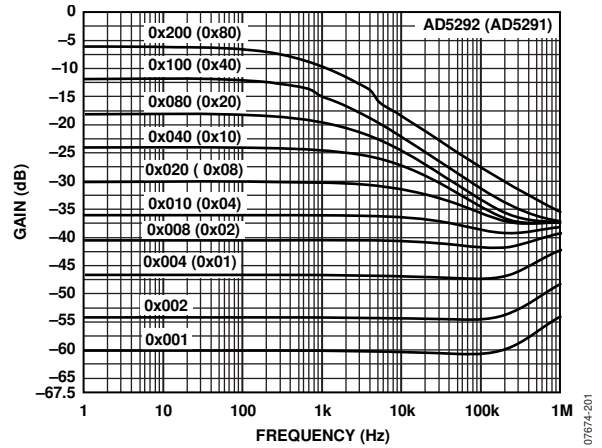


Figure 45. 100 kΩ Gain vs. Frequency vs. Code

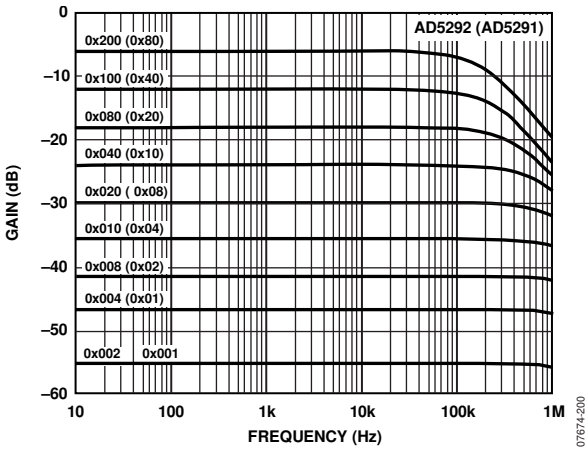


Figure 43. 50 kΩ Gain vs. Frequency vs. Code

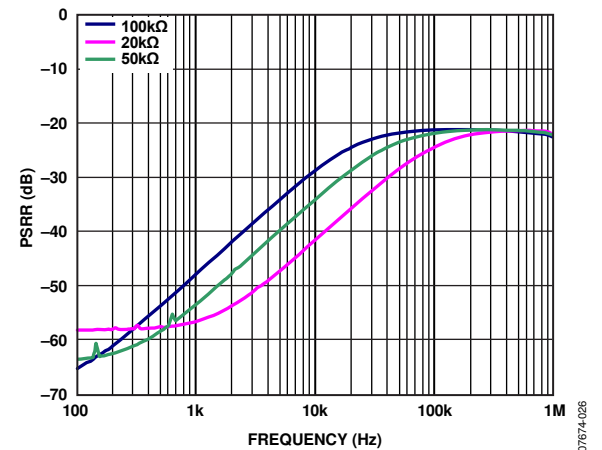


Figure 46. Power Supply Rejection Ratio vs. Frequency

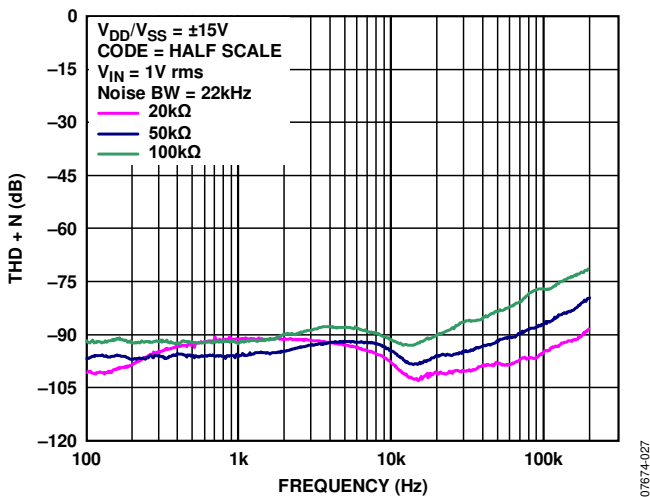


Figure 44. THD + Noise vs. Frequency

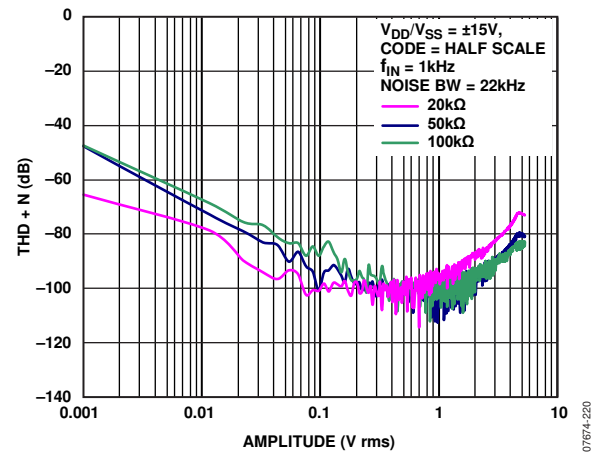


Figure 47. THD + Noise vs. Amplitude

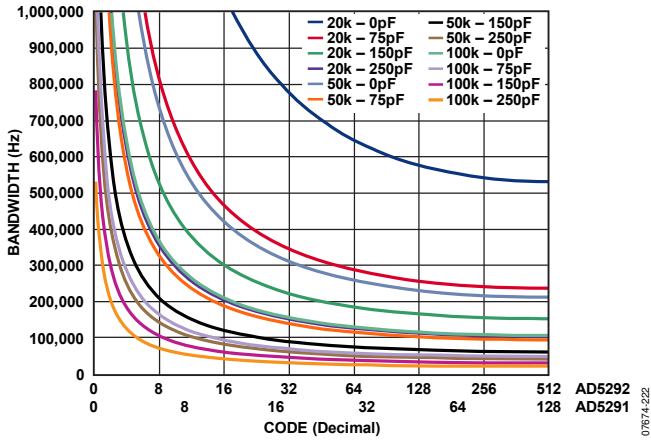


Figure 48. Bandwidth vs Code vs Net Capacitance

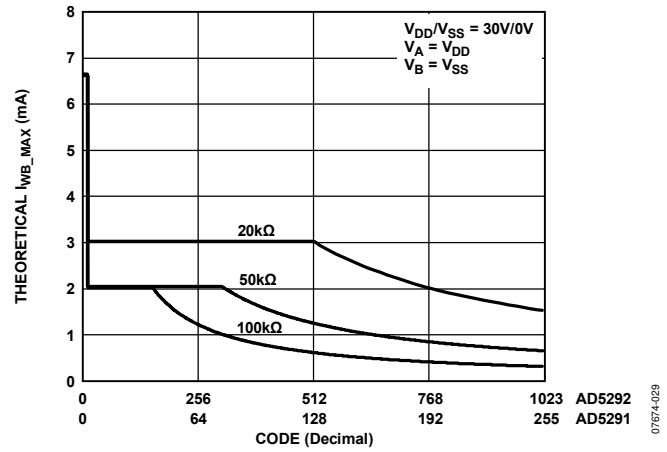


Figure 51. Theoretical Maximum Current vs. Code

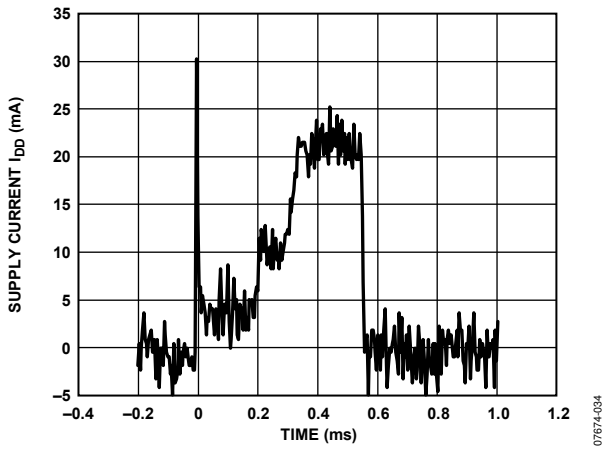


Figure 49.  $I_{DD}$  Waveform While Blowing/Reading Fuse

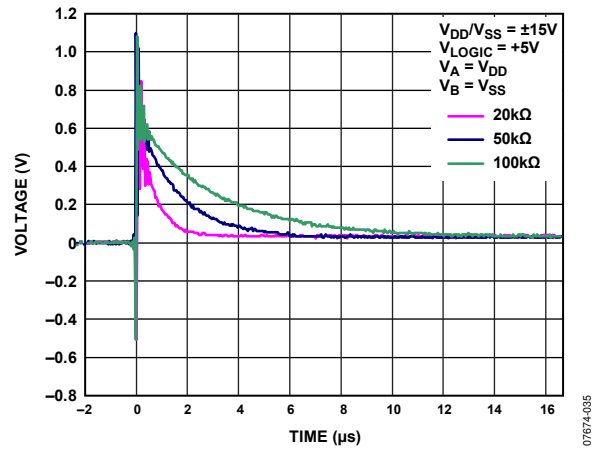


Figure 52. Maximum Transition Glitch

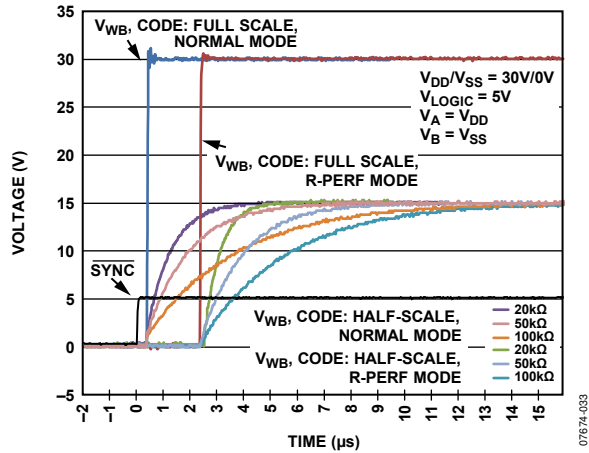


Figure 50. 20kΩ Large-Signal Settling Time from Code Zero Scale

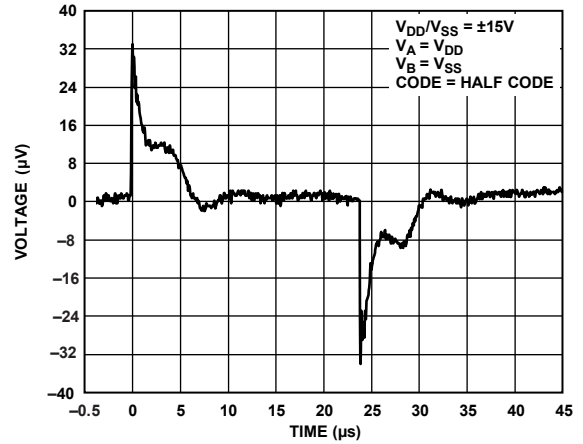


Figure 53. Digital Feedthrough

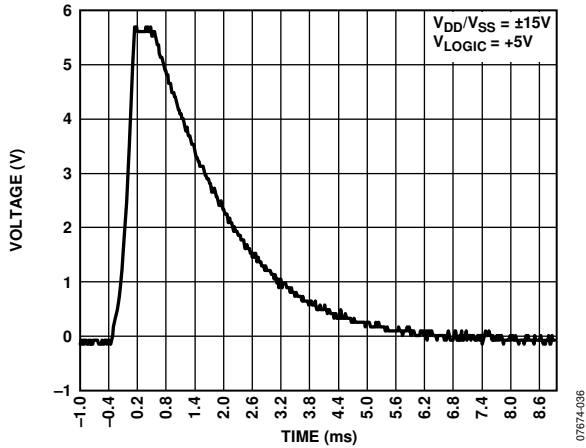


Figure 54.  $V_{EXT\_CAP}$  Waveform While Reading Fuse Or Calibration

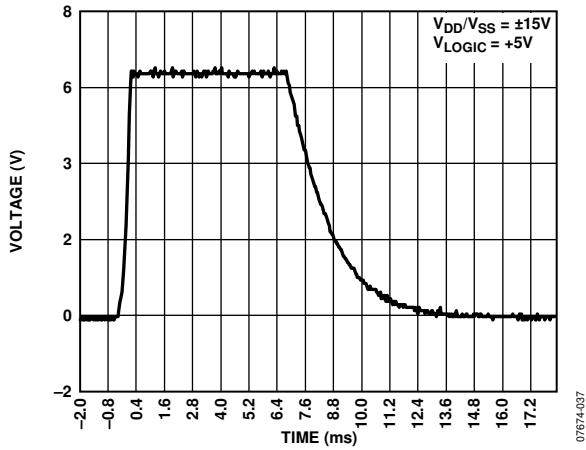


Figure 55.  $V_{EXT\_CAP}$  Waveform While Writing Fuse

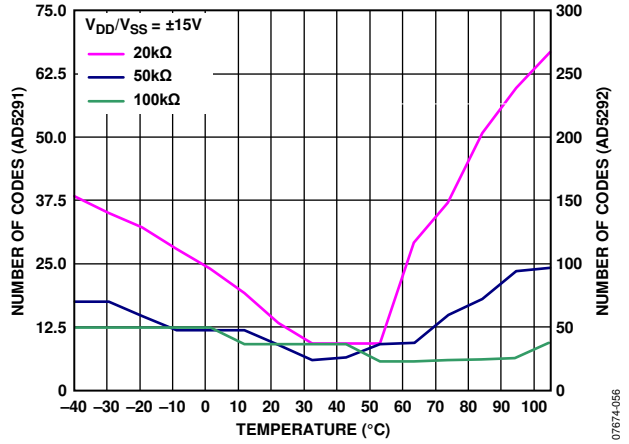


Figure 56. Code Range > 1% R-Tolerance Error vs. Temperature

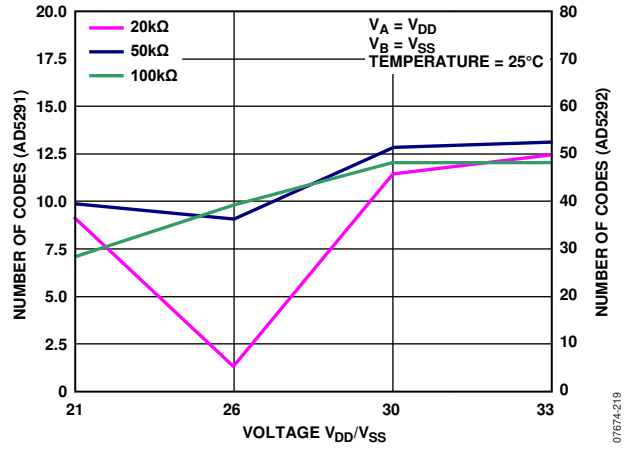


Figure 57. Code Range > 1% R-Tolerance Error vs. Voltage

### TEST CIRCUITS

Figure 58 to Figure 63 define the test conditions used in the Specifications section.

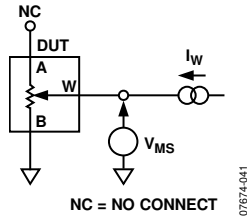


Figure 58. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

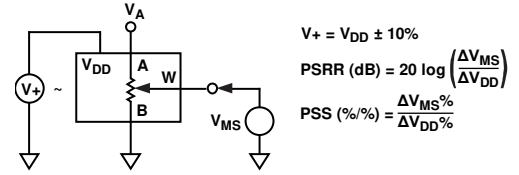


Figure 61. Power Supply Sensitivity (PSS, PSRR)

$$V_+ = V_{DD} \pm 10\%$$

$$PSRR \text{ (dB)} = 20 \log \left( \frac{\Delta V_{MS}}{\Delta V_{DD}} \right)$$

$$PSS \text{ (%/%) } = \frac{\Delta V_{MS}\%}{\Delta V_{DD}\%}$$

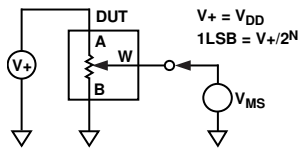


Figure 59. Potentiometer Divider Nonlinearity Error (INL, DNL)

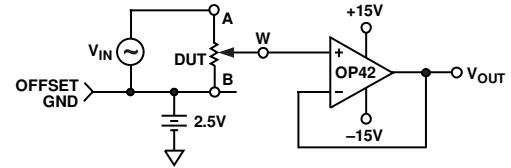


Figure 62. Gain vs. Frequency

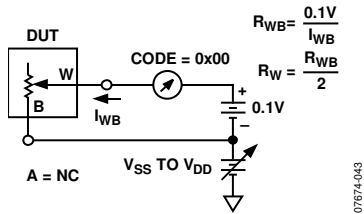


Figure 60. Wiper Resistance

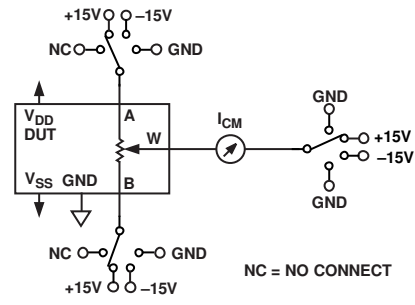


Figure 63. Common-Mode Leakage Current

## THEORY OF OPERATION

The [AD5291](#) and [AD5292](#) digital potentiometers are designed to operate as true variable resistors for analog signals that remain within the terminal voltage range of  $VSS < V_{TERM} < VDD$ . The patented  $\pm 1\%$  resistor tolerance feature helps to minimize the total RDAC resistance error, which reduces the overall system error by offering better absolute matching and improved open-loop performance. The digital potentiometer wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register, allowing as many value changes as necessary to place the potentiometer wiper in the correct position. The RDAC register can be programmed with any position setting using the standard SPI interface by loading the 16-bit data-word. Once a desirable position is found, this value can be stored in a 20-TP memory register. Thereafter, the wiper position is always restored to that position for subsequent power-up. The storing of 20-TP data takes approximately 6 ms; during this time, the shift register is locked, preventing any changes from taking place. The RDY pin identifies the completion of this 20-TP storage.

### SERIAL DATA INTERFACE

The [AD5291](#) and [AD5292](#) contain a serial interface ( $\overline{SYNC}$ , SCLK, DIN and SDO) that is compatible with SPI interface standards, as well as most DSPs. The part allows writing of data via the serial interface to every register.

### SHIFT REGISTER

The [AD5291](#) and [AD5292](#) shift register is 16 bits wide (see Figure 2). The 16-bit input word consists of two zeros, followed

by four control bits, and 10 RDAC data bits. For the [AD5291](#), the lower two RDAC data bits are don't cares if the RDAC register is read from or written to. Data is loaded MSB first (Bit DB15). The four control bits determine the function of the software command (see Table 11). Figure 3 shows a timing diagram of a typical [AD5291](#) and [AD5292](#) write sequence.

The write sequence begins by bringing the  $\overline{SYNC}$  line low. The  $\overline{SYNC}$  pin must be held low until the complete data-word is loaded from the DIN pin. When  $\overline{SYNC}$  returns high, the serial data-word is decoded according to the commands in Table 11. The command bits (Cx) control the operation of the digital potentiometer. The data bits (Dx) are the values that are loaded into the decoded register. The [AD5291](#) and [AD5292](#) have an internal counter that counts a multiple of 16 bits (a frame) for proper operation. For example, [AD5291](#) and [AD5292](#) work with a 32-bit word but does not work properly with a 31-bit or 33-bit word. The [AD5291](#) and [AD5292](#) do not require a continuous SCLK, when  $\overline{SYNC}$  is high, and all serial interface pins should be operated at close to the VLOGIC supply rails to minimize power consumption in the digital input buffers.

### RDAC REGISTER

The RDAC register directly controls the position of the digital potentiometer wiper. For example, when the RDAC register is loaded with all zeros, the wiper is connected to Terminal B of the variable resistor. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed.

Table 11. Command Operation Truth Table

Command	DB15	DB14	Command Bits[DB13:DB10]				Data Bits[DB9:DB0] <sup>1</sup>										Operation	
			C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	NOP command: do nothing.
1	0	0	0	0	0	1	D9	D8	D7	D6	D5	D4	D3	D2	D1 <sup>2</sup>	D0 <sup>2</sup>		Write contents of serial data to RDAC.
2	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	Read RDAC wiper setting from the SDO output in the next frame.
3	0	0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	Store wiper setting; store RDAC setting to 20-TP memory.
4	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	Reset: refresh RDAC with 20-TP stored value.
5	0	0	0	1	0	1	X	X	X	X	X	D4	D3	D2	D1	D0		Read contents of 20-TP memory, or status of 20-TP memory, from the SDO output in the next frame.
6	0	0	0	1	1	0	X	X	X	X	X	X	D3	D2	D1	D0		Write contents of serial data to control register.
7	0	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	Read control register from the SDO output in the next frame.
8	0	0	1	0	0	0	X	X	X	X	X	X	X	X	X	X	D0	Software shutdown. D0 = 0 (normal mode). D0 = 1 (device placed in shutdown mode).

<sup>1</sup> X = don't care.

<sup>2</sup> In the [AD5291](#), this bit is a don't care.

## 20-TP MEMORY

Once a desirable wiper position is found, the contents of the RDAC register can be saved into a 20-TP memory register (see Table 12). Thereafter, the wiper position is always set at that position for any future on-off-on power supply sequence. The AD5291 and AD5292 have an array of 20 one-time programmable (OTP) memory registers. When the desired word is programmed to 20-TP memory, the device automatically verifies that the program command was successful. The verification process includes margin testing. Bit C3 of the control register can be polled to verify that the fuse program command was successful. Programming data to 20-TP memory consumes approximately 25 mA for 550  $\mu$ s and takes approximately 8 ms to complete. During this time, the shift register is locked, preventing any changes from taking place. The RDY pin can be used to monitor the completion of the 20-TP memory program and verification. No change in supply voltage is required to program the 20-TP memory. However, a 1  $\mu$ F capacitor on the EXT\_CAP pin is required (see Figure 68). Prior to 20-TP activation, the AD5291 and AD5292 preset to midscale on power-up.

## WRITE PROTECTION

On power-up, the shift register write commands for both the RDAC register and the 20-TP memory register are disabled. The RDAC write protect bit, C1 of the control register (see Table 13 and Table 14), is set to 0 by default. This disables any change of the RDAC register content regardless of the software commands, except that the RDAC register can be refreshed from the 20-TP memory using the software reset command (Command 4) or through hardware by the  $\overline{\text{RESET}}$  pin. To enable programming of the variable resistor wiper position (programming the RDAC register), the write protect bit, C1 of the control register, must first be programmed. This is accomplished by loading the shift register with Command 6 (see Table 11). To enable programming of the 20-TP memory block bit, C0 of the control register (set to 0 by default) must first be set to 1.

**Table 12. Write and Read to RDAC and 20-TP Memory**

DIN	SDO	Action
0x1803	0xXXXX	Enable update of wiper position and 20-TP memory contents through digital interface.
0x0500	0x1803	Write 0x100 to the RDAC register; wiper moves to ¼ full-scale position.
0x0800	0x0500	Prepare data read from the RDAC register.
0x0C00	0x0100	Stores RDAC register content into 20-TP memory. The 16-bit word appears out of SDO, where the last 10 bits contain the contents of the RDAC register (0x100).
0x1C00	0x0C00	Prepare data read from the control register.
0x0000	0x000X	NOP Instruction 0 sends 16-bit word out of SDO, where the last four bits contain the contents of the control register. If Bit C3 = 1, the fuse program command is successful.

**Table 13. Control Register Bit Map<sup>1</sup>**

DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	X	X	X	X	C3	C2	C1	C0

<sup>1</sup> X = don't care.

**Table 14. Control Register Function**

Bit Name	Description
C0	20-TP program enable 0 = 20-TP program disabled (default) 1 = enable device for 20-TP program
C1	RDAC register write protect 0 = wiper position frozen to value in memory (default) <sup>1</sup> 1 = allow update of wiper position through digital Interface
C2	Calibration enable 0 = resistor performance mode enabled (default) 1 = normal mode enabled
C3	20-TP memory program success 0 = fuse program command unsuccessful (default) 1 = fuse program command successful

<sup>1</sup> Wiper position frozen to value last programmed in 20-TP memory. Wiper is frozen to midscale if 20-TP memory has not been previously programmed.



## BASIC OPERATION

The basic mode of setting the variable resistor wiper position (programming the RDAC register) is accomplished by loading the shift register with Command 1 (see Table 11) and the desired wiper position data. When the desired wiper position is determined, the user can load the shift register with Command 3 (see Table 11), which stores the wiper position data in the 20-TP memory register. After 6 ms, the wiper position is permanently stored in the 20-TP memory. The RDY pin can be used to monitor the completion of this 20-TP program. Table 12 provides a programming example, listing the sequence of serial data input (DIN) words with the serial data output appearing at the SDO pin in hexadecimal format.

## 20-TP READBACK AND SPARE MEMORY STATUS

It is possible to read back the contents of any of the 20-TP memory registers through SDO by using Command 5 (see Table 11). The lower five LSB bits (D0 to D4) of the data byte select which memory location is to be read back (see Table 16). Data from the selected memory location are clocked out of the SDO pin during the next SPI operation, where the last 10 bits contain the contents of the specified memory location.

It is also possible to calculate the address of the most recently programmed memory location by reading back the contents of

read-only Memory Address 0x14 and Memory Address 0x15 using Command 5. The data bytes read back from Memory Address 0x014 and Memory Address 0x015 are thermometer encoded versions of the address of the last programmed memory location.

For the example outlined in Table 15, the address of the last programmed location is calculated as

$$\begin{aligned} (\text{Number of Bits} = 1 \text{ in Memory Address } 0x14) + (\text{Number} \\ \text{of Bits} = 1 \text{ in Memory Address } 0x15) - 1 = 10 + 8 - 1 = 17 \\ (0x10) \end{aligned}$$

If no memory location has been programmed, then the address generated is -1.

## SHUTDOWN MODE

The AD5291 and AD5292 can be placed in shutdown mode by executing the software shutdown command, Command 8 (see Table 11), and setting the LSB, D0, to 1. This feature places the RDAC in a special state in which Terminal A is open-circuited, and Wiper W is connected to Terminal B. The contents of the RDAC register are unchanged by entering shutdown mode. However, all commands listed in Table 11 are supported while in shutdown mode. Execute Command 8 (see Table 11), and set the LSB, D0, to 0 to exit shutdown mode.

Table 15. Example 20-TP Memory Readback

DIN	SDO	Action
0x1414	0xXXXX	Prepares data read from Memory Address 0x14.
0x1415	0x03FF	Prepares data read from Memory Address 0x15. Sends 16-bit word out of SDO, where the last 10 bits contain the contents of Memory Address 0x14.
0x0000	0x00FF	NOP Command 0 sends 16-bit word out of SDO, where last 10-bits contain the contents of Memory Address 0x15.
0x1410	0x0000	Prepares data read from memory location 0x10.
0x0000	0xXXXX	NOP Instruction 0 sends 16-bit word out of SDO, where the last 10 bits contain the contents of Memory Address 0x10 (17).

Table 16. Memory Map of Command 5

Data Bits[DB9:DB0] <sup>1</sup>										Register Contents
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	X	0	0	0	0	0	1 <sup>st</sup> programmed wiper location (0x00)
X	X	X	X	X	0	0	0	0	1	2 <sup>nd</sup> programmed wiper location (0x01)
X	X	X	X	X	0	0	0	1	0	3 <sup>rd</sup> programmed wiper location (0x02)
X	X	X	X	X	0	0	0	1	1	4 <sup>th</sup> programmed wiper location (0x03)
X	X	X	X	X	0	0	1	0	0	5 <sup>th</sup> programmed wiper location (0x04)
...	...	...	...	...	...	...	...	...	...	...
X	X	X	X	X	0	1	0	0	1	10 <sup>th</sup> programmed wiper location (0x09)
X	X	X	X	X	0	1	1	1	0	15 <sup>th</sup> programmed wiper location (0x0E)
X	X	X	X	X	1	0	0	1	1	20 <sup>th</sup> programmed wiper location (0x13)
X	X	X	X	X	1	0	1	0	0	Programmed memory status (thermometer encoded) <sup>2</sup> (0x14)
X	X	X	X	X	1	0	1	0	1	Programmed memory status (thermometer encoded) <sup>2</sup> (0x15)

<sup>1</sup> X = don't care.

<sup>2</sup> Allows the user to calculate the remaining spare memory locations.

**RESISTOR PERFORMANCE MODE**

This mode activates a new, patented 1% end-to-end resistor tolerance that ensures a  $\pm 1\%$  resistor tolerance on each code, that is, code = half scale,  $R_{WB} = 10\text{ k}\Omega \pm 100\ \Omega$ . See Table 2 (AD5291) or Table 5 (AD5292) to check which codes achieve  $\pm 1\%$  resistor tolerance. The resistor performance mode is activated by programming Bit C2 of the control register (see Table 13 and Table 14). The typical settling time is shown in Figure 50.

**RESET**

A low-to-high transition of the hardware  $\overline{\text{RESET}}$  pin loads the RDAC register with the contents of the most recently programmed 20-TP memory location. The AD5291 and AD5292 can also be reset through software by executing Command 4 (see Table 11). If no 20-TP memory location is programmed, then the RDAC register loads with midscale upon reset. The control register is restored with default bits; see Table 14.

**SDO PIN AND DAISY-CHAIN OPERATION**

The serial data output pin (SDO) serves two purposes: it can be used to read the contents of the wiper setting, 50-TP values and control register using Command 2, Command 5 and Command 7, respectively (see Table 11) or the SDO pin can be used in daisy-chain mode. Data is clocked out of SDO on the rising edge of SCLK. The SDO pin contains an open-drain N-channel FET that requires a pull-up resistor if this pin is used. To place the pin in high impedance and minimize the power dissipation when the pin is used, the 0x8001 data word followed by Command 0 should be sent to the part. Table 17 provides a sample listing for the sequence of the serial data input (DIN). Daisy chaining minimizes the number of port pins required from the controlling IC. As shown in Figure 64, users need to tie the SDO pin of one package to the DIN pin of the next package. Users may need to increase the clock period, because the pull-up resistor and the capacitive loading at the SDO-to-DIN interface may require additional time delay between subsequent devices.

When two AD5291 and AD5292 devices are daisy-chained, 32 bits of data are required. The first 16 bits go to U2, and the second 16 bits go to U1. Hold the  $\overline{\text{SYNC}}$  pin low until all 32 bits are clocked into their respective shift registers. The  $\overline{\text{SYNC}}$  pin is then pulled high to complete the operation.

Keep the  $\overline{\text{SYNC}}$  pin low until all 32 bits are clocked into their respective serial registers. The  $\overline{\text{SYNC}}$  pin is then pulled high to complete the operation.

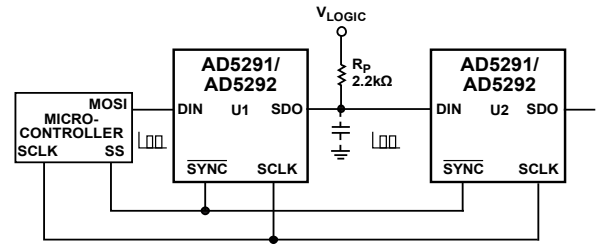


Figure 64. Daisy-Chain Configuration Using SDO

**RDAC ARCHITECTURE**

To achieve optimum performance, Analog Devices has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5291 and AD5292 employ a three-stage segmentation approach, as shown in Figure 65. The AD5291 and AD5292 wiper switches are designed with the transmission gate CMOS topology and with the gate voltages derived from  $V_{DD}$  and  $V_{SS}$ .

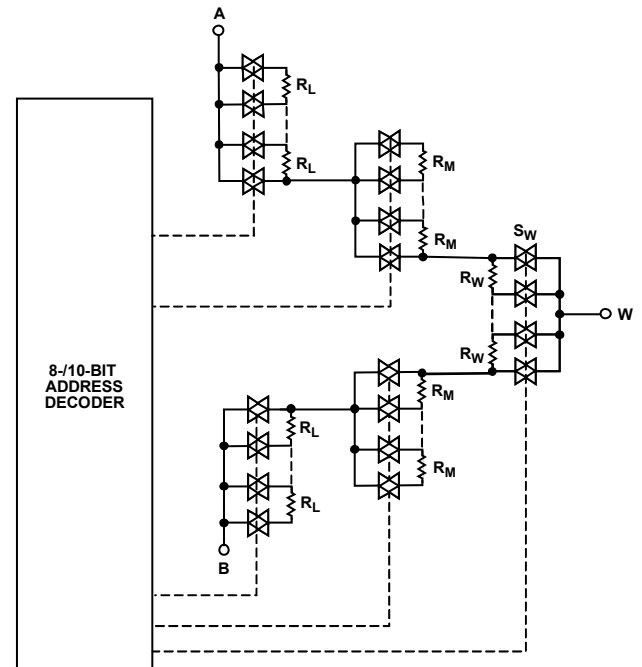


Figure 65. Simplified RDAC Circuit

**Table 17. Minimize Power Dissipation at SDO Pin**

DIN	SDO <sup>1</sup>	Action
0xXXXX	0xXXXX	Last user command sent to the digipot
0x8001	0xXXXX	Prepares the SDO pin to be placed in high impedance mode
0x0000	High impedance	The SDO pin is placed in high impedance

<sup>1</sup> X is don't care.