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Single Channel, 12-/16-Bit, Serial Input, Current Source and Voltage Output DACs, HART Connectivity

Data Sheet

AD5412/AD5422

FEATURES

- 12-/16-bit resolution and monotonicity
- Current output ranges: 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA
- ±0.01% FSR typical total unadjusted error (TUE)
- ±3 ppm FSR/°C output drift
- Voltage output ranges: 0 V to 5 V, 0 V to 10 V, ±5 V, or ±10 V
  - 10% overrange
  - ±0.01% FSR typical TUE
  - ±2 ppm FSR/°C output drift
- Flexible serial digital interface
- On-chip output fault detection
- On-chip reference: 10 ppm/°C maximum
- Optional regulated DV_{CC} output
- Asynchronous clear function
- Power supply range
  - AV_{DD}: 10.8 V to 40 V
  - AV_{SS}: −26.4 V to −3 V/0 V
- Current loop compliance voltage: AV_{DD} – 2.5 V
- Temperature range: −40°C to +105°C
- TSSOP and LFCSP packages

APPLICATIONS

- Process controls
- Actuator controls
- PLC
- HART network connectivity (LFCSP package only)

GENERAL DESCRIPTION

The AD5412/AD5422 are low cost, precision, fully integrated 12-/16-bit digital-to-analog converters (DAC) offering a programmable current source and programmable voltage output designed to meet the requirements of industrial process control applications.

The output current range is programmable at 4 mA to 20 mA, 0 mA to 20 mA, or an overrange function of 0 mA to 24 mA.

The LFCSP version of this product has a CAP2 pin so that the HART signals can be coupled onto the current output of the AD5412/AD5422.

Voltage output is provided from a separate pin that can be configured to provide 0 V to 5 V, 0 V to 10 V, ±5 V, or ±10 V output ranges; an overrange of 10% is available on all ranges.

Analog outputs are short and open-circuit protected and can drive capacitive loads of 1 µF.

The device operates with an AV_{DD} power supply range from 10.8 V to 40 V. Current loop compliance voltage is 0 V to AV_{DD} − 2.5 V.

The flexible serial interface is SPI- and MICROWIRE™-compatible and can be operated in 3-wire mode to minimize the digital isolation required in isolated applications.

The device also includes a power-on-reset function, ensuring that the device powers up in a known state. The part also includes an asynchronous clear pin (CLEAR) that sets the outputs to zero-scale/midscale voltage output or the low end of the selected current range.

The total output error is typically ±0.01% in current mode and ±0.01% in voltage mode.

Table 1. Pin-Compatible Devices

Part No.	Description
AD5410	Single channel, 12-bit, serial input current source DAC
AD5420	Single channel, 16-bit, serial input current source DAC

COMPANION PRODUCTS

HART Modem: AD5700, AD5700-1

Rev. N

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Tel: 781.329.4700
Technical Support www.analog.com

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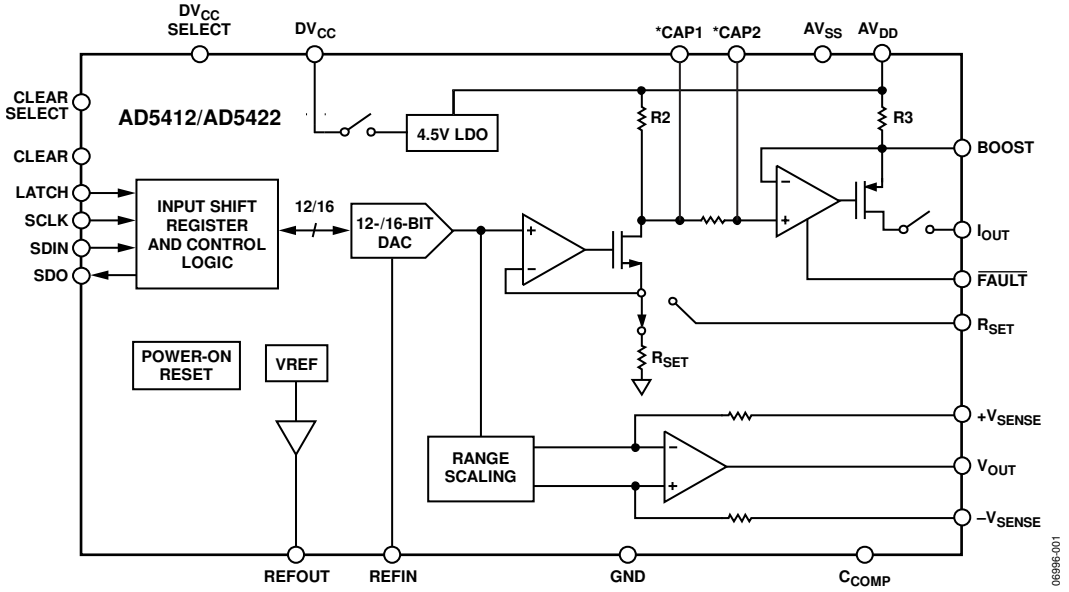
FUNCTIONAL BLOCK DIAGRAM



*PINS ONLY ON LFCSP OPTION.

Figure 1.

SPECIFICATIONS

AV_{DD} = 10.8 V to 26.4 V, AV_{SS} = −26.4 V to −3 V/0 V, AV_{DD} + |AV_{SS}| < 52.8 V, GND = 0 V, REFIN = 5 V external; DV_{CC} = 2.7 V to 5.5 V. V_{OUT}: R_{LOAD} = 1 kΩ, C_L = 200 pF, I_{OUT}: R_{LOAD} = 350 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE OUTPUT					
Output Voltage Ranges	0		5	V	
	0		10	V	
	−5		+5	V	
	−10		+10	V	
Accuracy					Output unloaded
Resolution	16			Bits	AD5422
	12			Bits	AD5412
Total Unadjusted Error (TUE)					
B Version	−0.1		+0.1	% FSR	
	−0.05	±0.01	+0.05	% FSR	T_A = 25°C
A Version	−0.3		+0.3	% FSR	T_A = −40°C to +85°C
	−0.1	±0.05	+0.1	% FSR	T_A = 25°C
Relative Accuracy (INL)[2]	−0.008		+0.008	% FSR	AD5422
	−0.032		+0.032	% FSR	AD5412
Differential Nonlinearity (DNL)	−1		+1	LSB	T_A = −40°C to +85°C, guaranteed monotonic
	−1		+1.3	LSB	Guaranteed monotonic
Bipolar Zero Error	−6		+6	mV	T_A = −40°C to +85°C, bipolar output range
	−9		+9	mV	Bipolar output range
	−1.5	±0.2	+1.5	mV	T_A = 25°C, bipolar output range
Bipolar Zero Error Temperature Coefficient (TC)[3]		±3		ppm FSR/°C	Bipolar output range
Zero-Scale Error	−5		+5	mV	T_A = −40°C to +85°C
	−8		+8	mV	
	−3.5	±0.3	+3.5	mV	T_A = 25°C
Zero-Scale Error TC[3]		±2		ppm FSR/°C	
Offset Error	−4		+4	mV	T_A = −40°C to +85°C, unipolar output range
	−6		+6	mV	Unipolar output range
	−1.5	±0.2	+1.5	mV	T_A = 25°C, unipolar output range
Offset Error TC[3]		±2		ppm FSR/°C	Unipolar output range
Gain Error	−0.07		+0.07	% FSR	
	−0.05	±0.004	+0.05	% FSR	T_A = 25°C
Gain Error TC[3]		±1		ppm FSR/°C	T_A = −40°C to +85°C
		±3		ppm FSR/°C	
Full-Scale Error	−0.07		+0.07	% FSR	
	−0.05	±0.001	+0.05	% FSR	T_A = 25°C
Full-Scale Error TC[3]		±1		ppm FSR/°C	T_A = −40°C to +85°C
		±2		ppm FSR/°C	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS[3]					
Headroom		0.5	0.8	V	Output unloaded
Output Voltage Drift vs. Time		90		ppm FSR	Drift after 1000 hours, T_A = 125°C
Short-Circuit Current		20		mA	
Load	1			kΩ	
Capacitive Load Stability					T_A = 25°C
R_{LOAD} = ∞			20	nF	
R_{LOAD} = 1 kΩ			5	nF	
R_{LOAD} = ∞			1	µF	External compensation capacitor of 4 nF connected
DC Output Impedance		0.3		Ω	
Power-On Time		10		µs	
DC PSRR		90	130	µV/V	
		3	12	µV/V	Output unloaded
CURRENT OUTPUT					
Output Current Ranges	0		24	mA	
	0		20	mA	
	4		20	mA	
Accuracy (Internal R_{SET})					
Resolution	16			Bits	AD5422
	12			Bits	AD5412
TUE					
B Version	−0.3		+0.3	% FSR	
	−0.13	±0.08	+0.13	% FSR	T_A = 25°C
A Version	−0.5		+0.5	% FSR	T_A = −40°C to +85°C
	−0.3	±0.15	+0.3	% FSR	T_A = 25°C
INL[4]	−0.024		+0.024	% FSR	AD5422
	−0.032		+0.032	% FSR	AD5412
DNL	−1		+1	LSB	T_A = −40°C to +85°C, guaranteed monotonic
	−1		+1.3	LSB	Guaranteed monotonic
Offset Error	−0.27		+0.27	% FSR	T_A = −40°C to +85°C
	−0.40		+0.40	% FSR	
	−0.12	±0.08	+0.12	% FSR	T_A = 25°C
Offset Error TC[3]		±16		ppm FSR/°C	T_A = −40°C to +85°C
		±28		ppm FSR/°C	
Gain Error	−0.18		+0.18	% FSR	T_A = −40°C to +85°C, AD5422
	−0.20		+0.20	% FSR	AD5422
	−0.03	±0.006	+0.03	% FSR	AD5422, T_A = 25°C
	−0.22		+0.22	% FSR	T_A = −40°C to +85°C, AD5412
	−0.24		+0.24	% FSR	AD5412
	−0.06	±0.006	+0.06	% FSR	AD5412, T_A = 25°C
Gain TC[3]		±10		ppm FSR/°C	T_A = −40°C to +85°C
		±21		ppm FSR/°C	
Full-Scale Error	−0.2		+0.2	% FSR	T_A = −40°C to +85°C
	−0.40		+0.40	% FSR	
	−0.1	±0.08	+0.1	% FSR	T_A = 25°C
Full-Scale TC[3]		±6		ppm FSR/°C	T_A = −40°C to +85°C
		±13		ppm FSR/°C	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Accuracy (External R_{SET})					
Resolution	16			Bits	AD5422
	12			Bits	AD5412
TUE					
B Version	−0.15		+0.15	% FSR	
	−0.06	±0.01	+0.06	% FSR	T_A = 25°C
A Version	−0.3		+0.3	% FSR	T_A = −40°C to +85°C
	−0.1	±0.02	+0.1	% FSR	T_A = 25°C
INL[4]	−0.012		+0.012	% FSR	AD5422
	−0.032		+0.032	% FSR	AD5412
DNL	−1		+1	LSB	T_A = −40°C to +85°C, guaranteed monotonic
	−1		+1.3	LSB	Guaranteed monotonic
Offset Error	−0.1		+0.1	% FSR	T_A = −40°C to +85°C
	−0.12		+0.12	% FSR	
	−0.03	±0.006	+0.03		T_A = 25°C
Offset Error TC[3]		±3		ppm FSR/°C	T_A = −40°C to +85°C
		±5		ppm FSR/°C	
Gain Error	−0.08		+0.08	% FSR	T_A = −40°C to +85°C
	−0.15		+0.15	% FSR	
	−0.05	±0.003	+0.05	% FSR	T_A = 25°C
Gain TC[3]		±4		ppm FSR/°C	
Full-Scale Error	−0.15		+0.15	% FSR	
	−0.06	±0.01	+0.06	% FSR	T_A = 25°C
Full-Scale Error TC[3]		±7		ppm FSR/°C	T_A = −40°C to +85°C
		±9		ppm FSR/°C	
OUTPUT CHARACTERISTICS[3]					
Current Loop Compliance Voltage	0		AV_{DD} − 2.5	V	
Output Current Drift vs. Time					Drift after 1000 hours, T_A = 125°C
		50		ppm FSR	Internal R_{SET}
		20		ppm FSR	External R_{SET}
Resistive Load			1200	Ω	
Inductive Load		50		mH	T_A = 25 °C
DC PSRR			1	µA/V	
Output Impedance		50		MΩ	
Output Current Leakage When Output Disabled		60		pA	
REFERENCE INPUT/OUTPUT					
Reference Input[3]					
Reference Input Voltage	4.95	5	5.05	V	For specified performance
DC Input Impedance	27	40		kΩ	
Reference Output					
Output Voltage	4.995	5	5.005		T_A = 25°C
Reference TC[3, 5]		1.8	10	ppm/°C	
Output Noise (0.1 Hz to 10 Hz)[3]		10		µV p-p	
Noise Spectral Density[3]		100		nV/√Hz	At 10 kHz
Output Voltage Drift vs. Time[3]		50		ppm	Drift after 1000 hours, T_A = 125°C
Capacitive Load[3]		600		nF	
Load Current[3]		5		mA	
Short-Circuit Current[3]		7		mA	
Load Regulation[3]		95		ppm/mA	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS[3]					JEDEC compliant
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current	−1		+1	µA	Per pin
Pin Capacitance		10		pF	Per pin
DIGITAL OUTPUTS[3]					
SDO					
Output Low Voltage, V_{OL}			0.4	V	Sinking 200 µA
Output High Voltage, V_{OH}	DV_{CC} − 0.5			V	Sourcing 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance		5		pF	
$\overline{FAULT}$					
Output Low Voltage, V_{OL}			0.4	V	10 kΩ pull-up resistor to DV_{CC}
Output Low Voltage, V_{OL}		0.6		V	At 2.5 mA
Output High Voltage, V_{OH}	3.6			V	10 kΩ pull-up resistor to DV_{CC}
POWER REQUIREMENTS					
AV_{DD}	10.8		40	V	
AV_{SS}	−26.4		0	V	
$\|AV_{SS}\| + AV_{DD}$	10.8		52.8	V	
DV_{CC}					
Input Voltage	2.7		5.5	V	Internal supply disabled
Output Voltage		4.5		V	DV_{CC}, which can be overdriven up to 5.5 V
Output Load Current[3]		5		mA	
Short-Circuit Current[3]		20		mA	
AI_{DD}					Outputs unloaded
		2.5	3	mA	Outputs disabled
		3.4	4	mA	Current output enabled
		3.9	4.4	mA	Voltage output enabled
AI_{SS}					Outputs unloaded
		0.24	0.3	mA	Outputs disabled
		0.5	0.6	mA	Current output enabled
		1.1	1.4	mA	Voltage output enabled
DI_{CC}			1	mA	$V_{IH} = DV_{CC}$, V_{IL} = GND
Power Dissipation		128		mW	AV_{DD} = 40 V, AV_{SS} = 0 V, outputs unloaded
		120		mW	AV_{DD} = +24 V, AV_{SS} = −24 V, outputs unloaded

[1] Temperature range: −40°C to +105°C; typical at +25°C.
[2] When the AD5412/AD5422 is powered with AV_{SS} = 0 V, INL for the 0 V to 5 V and 0 V to 10 V ranges is measured beginning from Code 256 for the AD5422 and Code 16 for the AD5412.
[3] Guaranteed by design and characterization; not production tested.
[4] For 0 mA to 20 mA and 0 mA to 24 mA ranges, INL is measured beginning from Code 256 for the AD5422 and Code 16 for the AD5412.
[5] The on-chip reference is production trimmed and tested at 25°C and 85°C. It is characterized from −40°C to +105°C.

AV_{DD} = 15 V to 26.4 V, AV_{SS} = −26.4 V to −3 V/0 V, AV_{DD} + |AV_{SS}| < 52.8 V, GND = 0 V, REFIN = 5 V external; DV_{CC} = 2.7 V to 5.5 V. V_{OUT}: R_{LOAD} = 1 kΩ, C_L = 200 pF, I_{OUT}: R_{LOAD} = 350 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Voltage over range enabled.

Table 3.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE OUTPUT					
Output Voltage Ranges	0		5.5	V	
	0		11	V	
	−5.5		+5.5	V	
	−11		+11	V	
Accuracy					Output unloaded
Resolution	16			Bits	AD5422
	12			Bits	AD5412
Total Unadjusted Error (TUE)					
B Version	−0.13		+0.13	% FSR	
	−0.10	±0.01	+0.10	% FSR	T_A = 25°C
Relative Accuracy (INL)[2]	−0.008		+0.008	% FSR	AD5422
	−0.032		+0.032	% FSR	AD5412
Differential Nonlinearity (DNL)	−1		+1.3	LSB	Guaranteed monotonic
Bipolar Zero Error	−9		+9	mV	Bipolar output range
Bipolar Zero Error Temperature Coefficient (TC)[3]		±3		ppm FSR/°C	Bipolar output range
Zero-Scale Error	−18		+18	mV	
Zero-Scale Error TC[3]		±2		ppm FSR/°C	
Offset Error	−6		+6	mV	Unipolar output range
Offset Error TC[3]		±2		ppm FSR/°C	Unipolar output range
Gain Error	−0.13		+0.13	% FSR	
Gain Error TC[3]		±3		ppm FSR/°C	
Full-Scale Error	−0.13		+0.13	% FSR	
Full-Scale Error TC[3]		±2		ppm FSR/°C	

[1] Temperature range: −40°C to +105°C; typical at +25°C.
[2] When the AD5412/AD5422 is powered with AV_{SS} = 0 V, INL for the 0 V to 5.5 V and 0 V to 11 V ranges is measured beginning from Code 256 for the AD5422 and Code 16 for the AD5412.
[3] Guaranteed by design and characterization; not production tested.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = 10.8 V to 26.4 V, AV_{SS} = −26.4 V to −3 V/0 V, AV_{DD} + |AV_{SS}| < 52.8 V, GND = 0 V, REFIN = +5 V external; DV_{CC} = 2.7 V to 5.5 V. V_{OUT}: R_{LOAD} = 1 kΩ, C_L = 200 pF, I_{OUT}: R_{LOAD} = 350 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Voltage Output					
Output Voltage Settling Time			25	µs	10 V step to ±0.03 % FSR
		32		µs	20 V step to ±0.03 % FSR
			18	µs	5 V step to ±0.03 % FSR
		8		µs	512 LSB step to ±0.03 % FSR (16-Bit LSB)
Slew Rate		0.8		V/µs	
Power-On Glitch Energy		10		nV-sec	
Digital-to-Analog Glitch Energy		10		nV-sec	
Glitch Impulse Peak Amplitude		20		mV	
Digital Feedthrough		1		nV-sec	
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.1		LSB p-p	16-bit LSB
Output Noise (100 kHz Bandwidth)		200		µV rms	
1/f Corner Frequency		1		kHz	
Output Noise Spectral Density		150		nV/√Hz	Measured at 10 kHz, midscale output, 10 V range
AC PSRR		−75		dB	200 mV 50 Hz/60 Hz sine wave superimposed on power supply voltage
Current Output					
Output Current Settling Time		10		µs	16 mA step to 0.1% FSR
		40		µs	16 mA step to 0.1% FSR, L = 1 mH
AC PSRR		−75		dB	200 mV 50 Hz/60 Hz sine wave superimposed on power supply voltage

[1] Guaranteed by characterization, not production tested.

TIMING CHARACTERISTICS

AV_{DD} = 10.8 V to 26.4 V, AV_{SS} = −26.4 V to −3 V/0 V, AV_{DD} + |AV_{SS}| < 52.8V, GND = 0 V, REFIN = +5 V external; DV_{CC} = 2.7 V to 5.5 V. V_{OUT}: R_{LOAD} = 1 kΩ, C_L = 200 pF, I_{OUT}: R_{LOAD} = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
WRITE MODE			
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK low time
t_3	13	ns min	SCLK high time
t_4	13	ns min	LATCH delay time
t_5	5	µs min	LATCH high time
t_6	5	ns min	Data setup time
t_7	5	ns min	Data hold time
t_8	40	ns min	LATCH low time
t_9	20	ns min	CLEAR pulse width
t_{10}	5	µs max	CLEAR activation time

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
READBACK MODE			
t_{11}	90	ns min	SCLK cycle time
t_{12}	40	ns min	SCLK low time
t_{13}	40	ns min	SCLK high time
t_{14}	13	ns min	LATCH delay time
t_{15}	40	ns min	LATCH high time
t_{16}	5	ns min	Data setup time
t_{17}	5	ns min	Data hold time
t_{18}	40	ns min	LATCH low time
t_{19}	35	ns max	Serial output delay time ($C_{L\ SDO}$[4] = 15 pF)
t_{20}	35	ns max	LATCH rising edge to SDO tristate ($C_{L\ SDO}$[4] = 15 pF)
DAISY-CHAIN MODE			
t_{21}	90	ns min	SCLK cycle time
t_{22}	40	ns min	SCLK low time
t_{23}	40	ns min	SCLK high time
t_{24}	13	ns min	LATCH delay time
t_{25}	40	ns min	LATCH high time
t_{26}	5	ns min	Data setup time
t_{27}	5	ns min	Data hold time
t_{28}	40	ns min	LATCH low time
t_{29}	35	ns max	Serial output delay time ($C_{L\ SDO}$[4] = 15 pF)

[1] Guaranteed by characterization; not production tested.
[2] All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, and Figure 4.
[4] $C_{L\ SDO}$ = capacitive load on SDO output.

Timing Diagrams

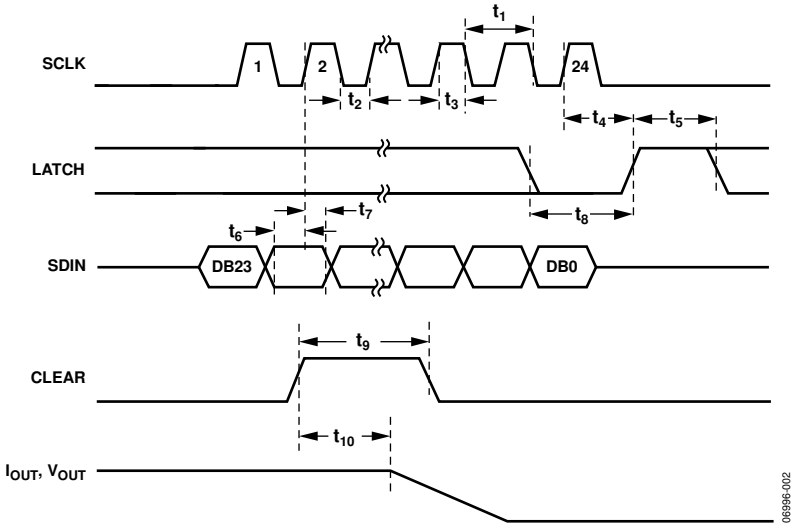


Figure 2. Write Mode Timing Diagram

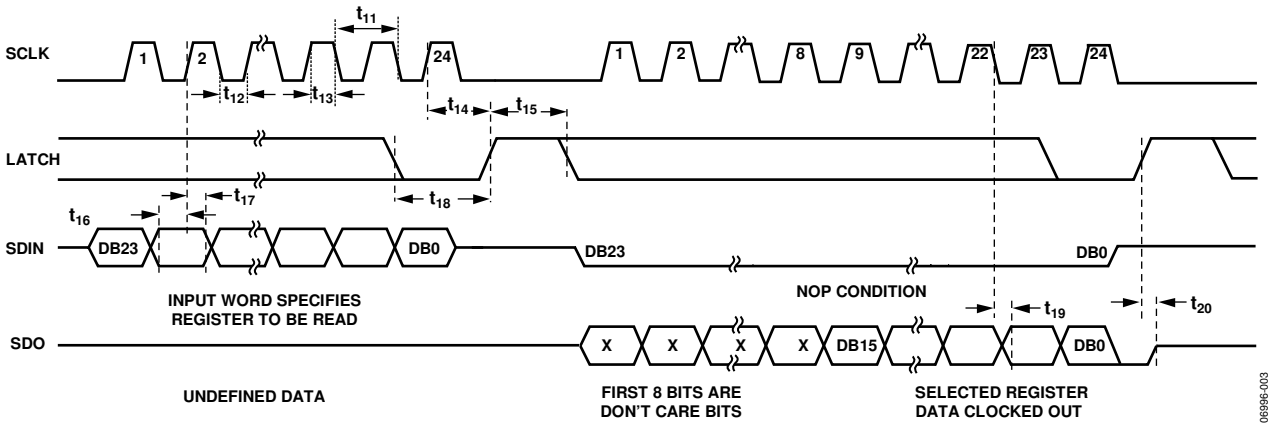


Figure 3. Readback Mode Timing Diagram

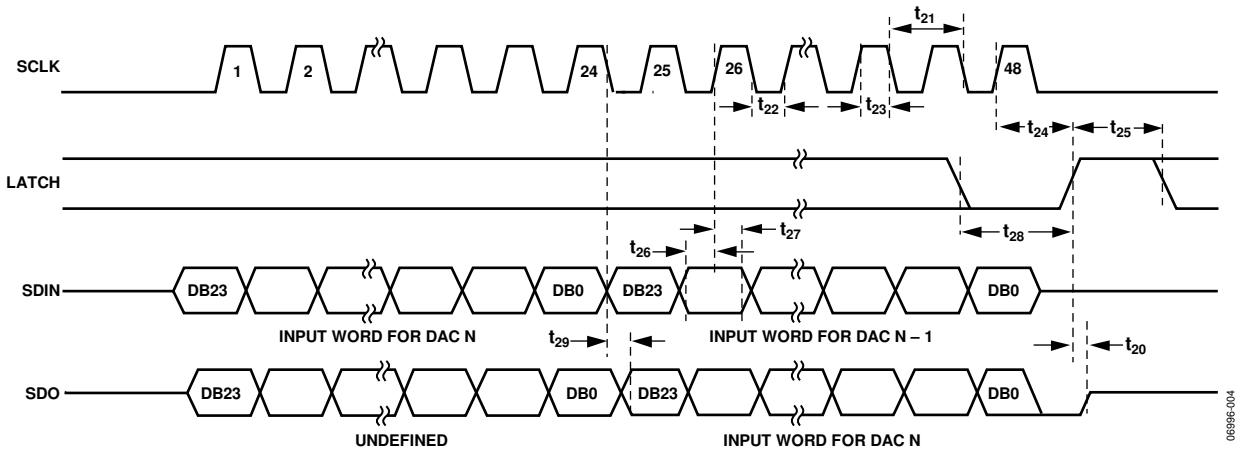


Figure 4. Daisy-Chain Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 80 mA do not cause SCR latch-up.

Table 6.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +48 V
AV_{SS} to GND	+0.3 V to −28 V
AV_{DD} to AV_{SS}	−0.3 V to +60 V
DV_{CC} to GND	−0.3 V to +7 V
Digital Inputs to GND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital Outputs to GND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
REFIN/REFOUT to GND	−0.3 V to +7 V
V_{OUT} to GND	AV_{SS} to AV_{DD}
I_{OUT} to GND	AV_{SS} to AV_{DD}
Operating Temperature Range (T_A)	
Industrial[1]	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
24-Lead TSSOP_EP Package	
θ_{JA} Thermal Impedance[2]	35°C/W
40-Lead LFCSP Package	
θ_{JA} Thermal Impedance[2]	33°C/W
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

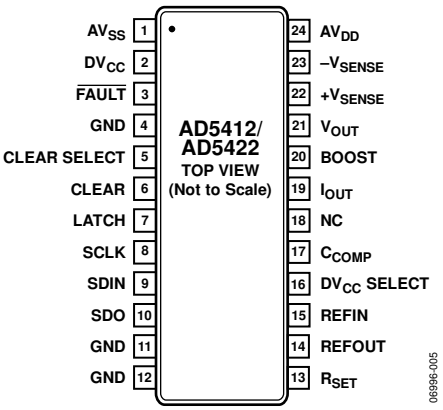
[1] Power dissipated on chip must be derated to keep the junction temperature below 125°C, assuming that the maximum power dissipation condition is sourcing 24 mA into GND from I_{OUT} with a 4 mA on-chip current.
[2] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with thermal vias. See JEDEC JESD51.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

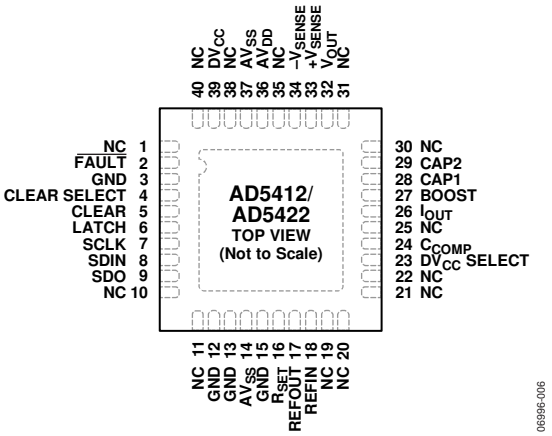
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT
2. THE PADDLE CAN BE CONNECTED TO 0V IF THE OUTPUT VOLTAGE RANGE IS UNIPOLAR. THE PADDLE CAN BE LEFT ELECTRICALLY UNCONNECTED PROVIDED THAT A SUPPLY CONNECTION IS MADE AT THE AV_{SS} PIN. IT IS RECOMMENDED THAT THE PADDLE BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE.

Figure 5. TSSOP Pin Configuration



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PADDLE CAN BE CONNECTED TO 0V IF THE OUTPUT VOLTAGE RANGE IS UNIPOLAR. THE EXPOSED PADDLE CAN BE LEFT ELECTRICALLY UNCONNECTED PROVIDED THAT A SUPPLY CONNECTION IS MADE AT THE AV_{SS} PIN. IT IS RECOMMENDED THAT THE PADDLE BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE.

Figure 6. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	14, 37	AV_{SS}	Negative Analog Supply Pin. Voltage ranges from −3 V to −24 V. This pin can be connected to 0 V if the output voltage range is unipolar.
2	39	DV_{CC}	Digital Supply Pin. Voltage ranges from 2.7 V to 5.5 V. This pin can also be configured as a 4.5 V LDO output by leaving the DV_{CC} SELECT pin floating.
3	2	$\overline{\text{FAULT}}$	Fault Alert. This pin is asserted low when an open circuit is detected in current mode or an overtemperature is detected. Open drain output must be connected to a pull-up resistor.
4, 12	3, 15	GND	These pins must be connected to 0 V.
18	1, 10, 11, 19, 20, 21, 22, 25, 30, 31, 35, 38, 40	NC	No Connection. Do not connect to these pins.
5	4	CLEAR SELECT	Selects the voltage output clear value, either zero-scale or midscale code (see Table 22).
6	5	CLEAR	Active High Input. Asserting this pin sets the current output to the bottom of the selected range or sets the voltage output to the user selected value (zero-scale or midscale).
7	6	LATCH	Positive Edge Sensitive Latch. A rising LATCH edge parallel loads the input shift register data into the DAC register, also updating the output.
8	7	SCLK	Serial Clock Input. Data is clocked into the shift register on the rising edge of SCLK. This operates at clock speeds of up to 30 MHz.
9	8	SDIN	Serial Data Input. Data must be valid on the rising edge of SCLK.
10	9	SDO	Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode. Data is valid on the rising edge of SCLK (see Figure 3 and Figure 4).
11	12, 13	GND	Ground Reference Pin.
13	16	R_{SET}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT} temperature drift performance. See the AD5412/AD5422 Features section.
14	17	REFOUT	Internal Reference Voltage Output. REFOUT = 5 V ± 5 mV.
15	18	REFIN	External Reference Voltage Input. Reference input range is 4 V to 5 V. REFIN = 5 V for a specified performance.

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
16	23	DV_{CC} SELECT	When connected to GND, this pin disables the internal supply, and an external supply must be connected to the DV_{CC} pin. Leave this pin unconnected to enable the internal supply. In this case, it is recommended to connect a 0.1 µF capacitor between DV_{CC} and GND. See the AD5412/AD5422 Features section.
17	24	C_{COMP}	Optional compensation capacitor connection for the voltage output buffer. Connecting a 4 nF capacitor between this pin and the V_{OUT} pin allows the voltage output to drive up to 1 µF. It should be noted that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
19	26	I_{OUT}	Current Output Pin.
20	27	BOOST	Optional External Transistor Connection. Connecting an external transistor reduces the power dissipated in the AD5412/AD5422. See the AD5412/AD5422 Features section.
N/A	28, 29	CAP1, CAP2	Connection for Optional Output Filtering Capacitor. See the AD5412/AD5422 Features section.
21	32	V_{OUT}	Buffered Analog Output Voltage. The output amplifier is capable of directly driving a 1 kΩ, 2000 pF load.
22	33	$+V_{SENSE}$	Sense connection for the positive voltage output load connection.
23	34	$-V_{SENSE}$	Sense connection for the negative voltage output load connection.
24	36	AV_{DD}	Positive Analog Supply Pin. Voltage ranges from 10.8 V to 60 V.
25 (EPAD)	41 (EPAD)	Exposed paddle	Negative Analog Supply Pin. Voltage ranges from –3 V to –24 V. This paddle can be connected to 0 V if the output voltage range is unipolar. The paddle can be left electrically unconnected provided that a supply connection is made at the AV_{SS} pin. It is recommended that the paddle be thermally connected to a copper plane for enhanced thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

GENERAL

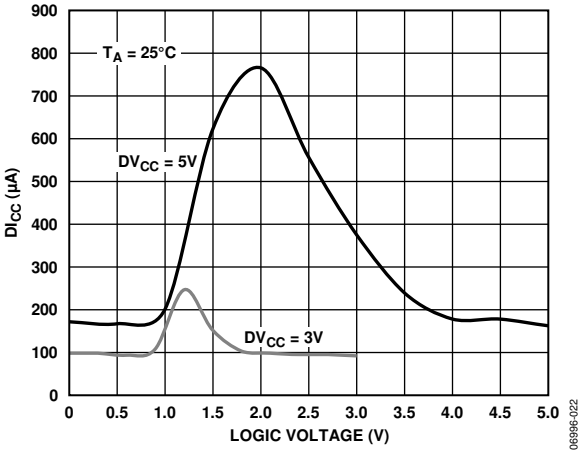


Figure 7. DI_{CC} vs. Logic Input Voltage

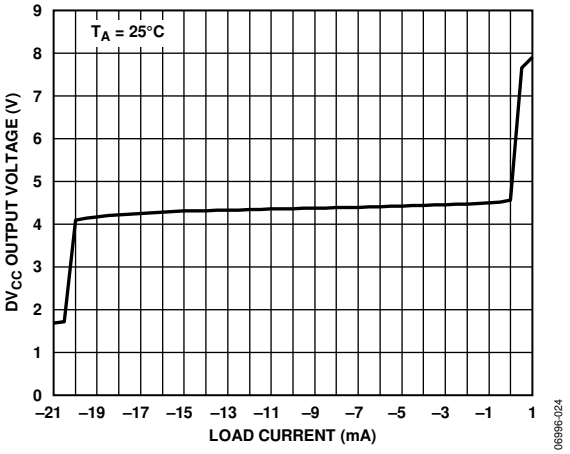


Figure 10. DV_{CC} Output Voltage vs. Load Current

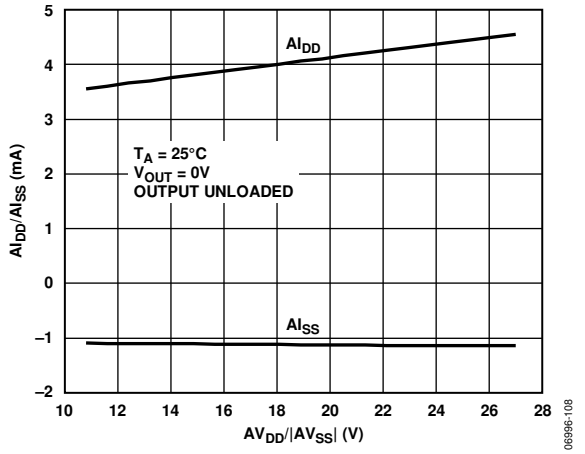


Figure 8. AI_{DD}/AI_{SS} vs. $AV_{DD}/|AV_{SS}|$

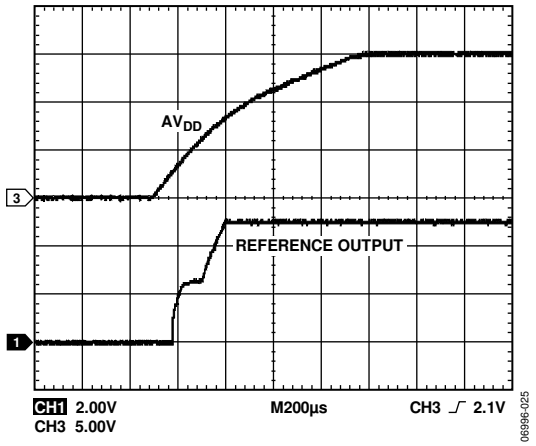


Figure 11. REFOUT Turn-on Transient

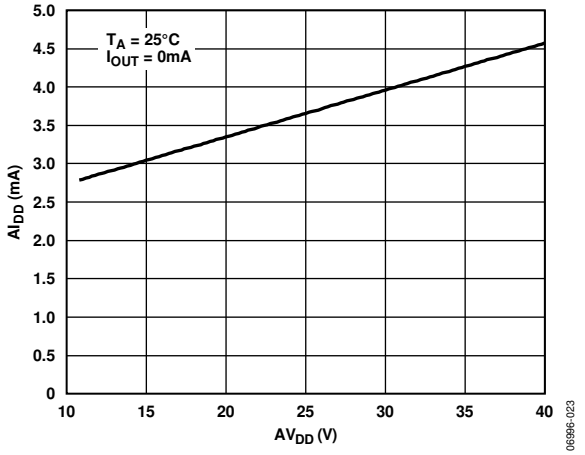


Figure 9. AI_{DD} vs. AV_{DD}

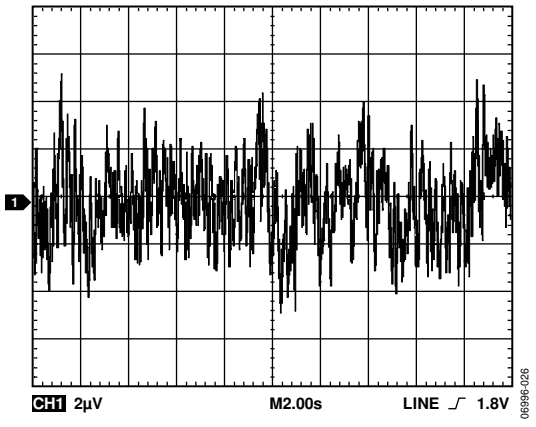


Figure 12. REFOUT Output Noise (0.1 Hz to 10 Hz Bandwidth)

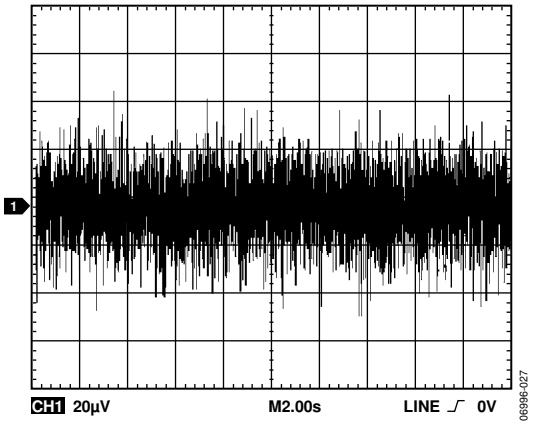


Figure 13. REFOUT Output Noise (100 kHz Bandwidth)

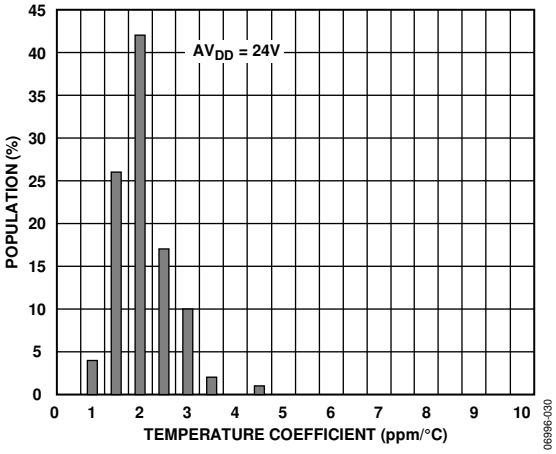


Figure 15. Reference Temperature Coefficient Histogram

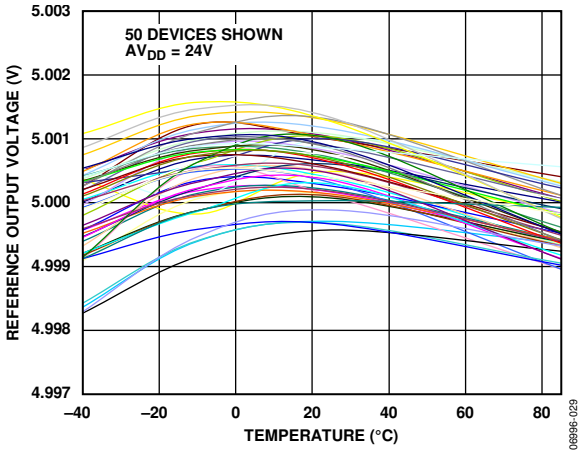


Figure 14. Reference Voltage vs. Temperature

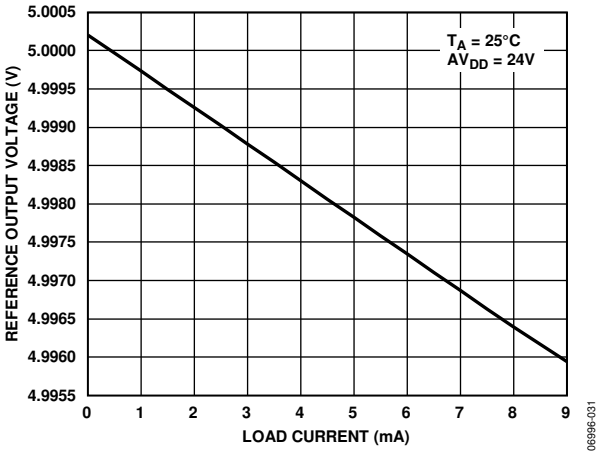


Figure 16. Reference Voltage vs. Load Current

VOLTAGE OUTPUT

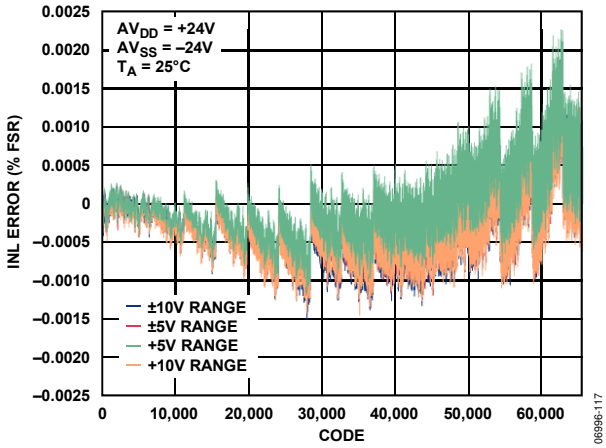


Figure 17. Integral Nonlinearity Error vs. DAC Code, Dual Supply

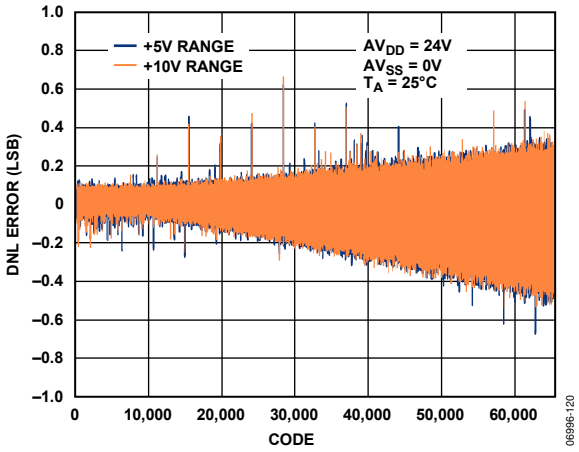


Figure 20. Differential Nonlinearity Error vs. DAC Code, Single Supply

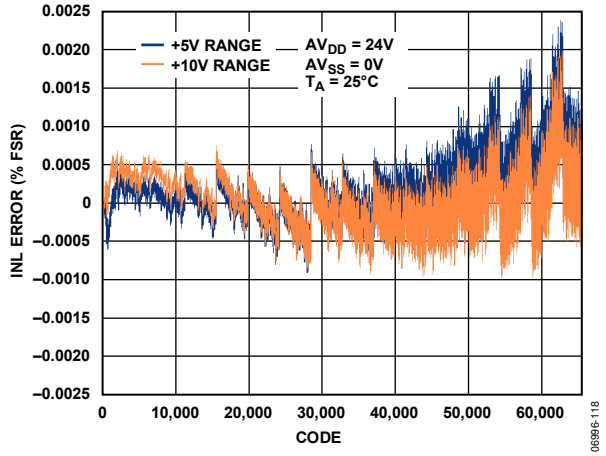


Figure 18. Integral Nonlinearity Error vs. DAC Code, Single Supply

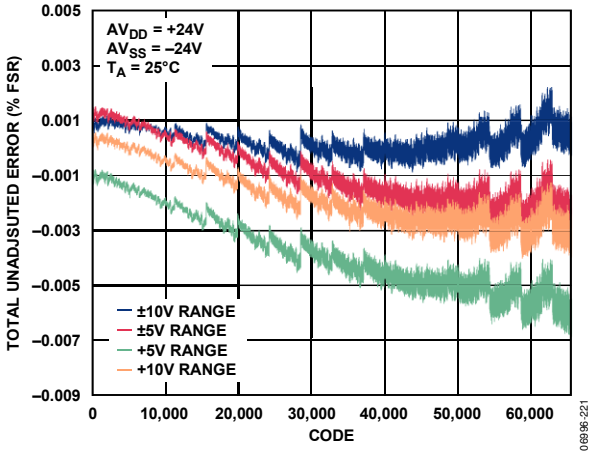


Figure 21. Total Unadjusted Error vs. DAC Code, Dual Supply

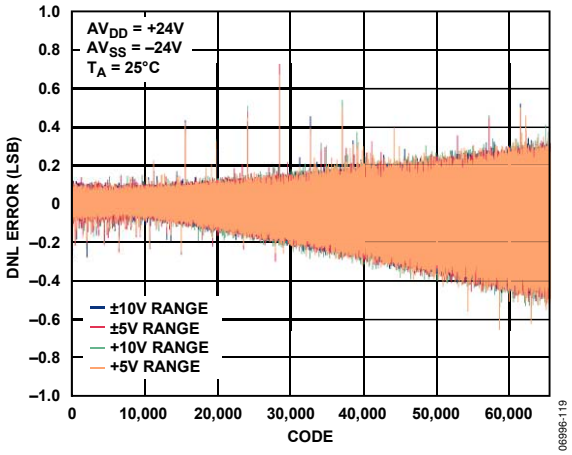


Figure 19. Differential Nonlinearity Error vs. DAC Code, Dual Supply

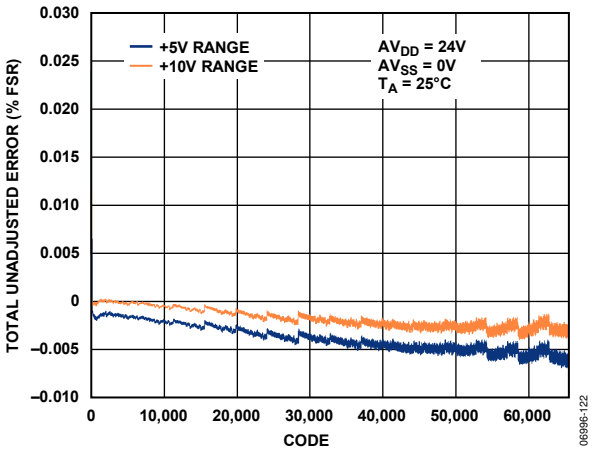


Figure 22. Total Unadjusted Error vs. DAC Code, Single Supply

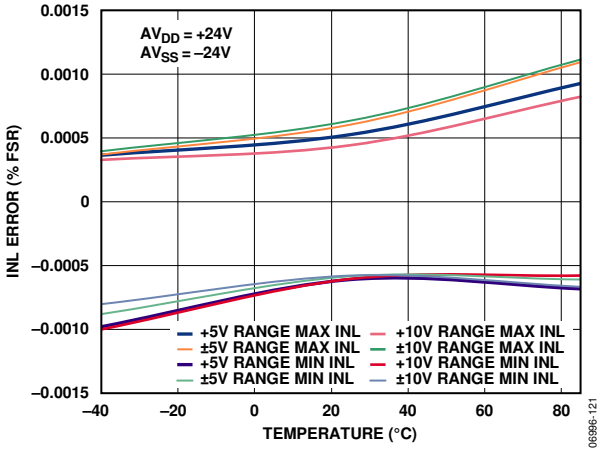


Figure 23. Integral Nonlinearity Error vs. Temperature

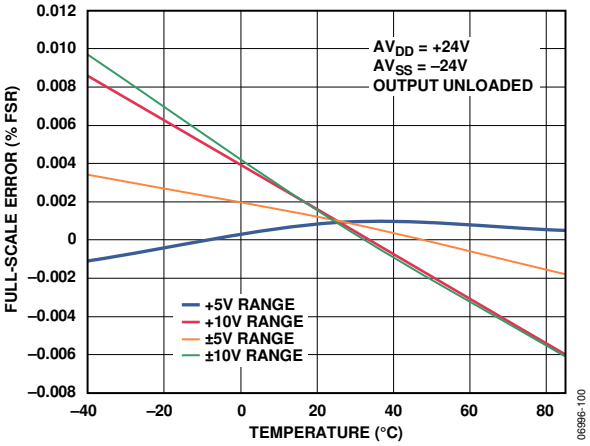


Figure 26. Full-Scale Error vs. Temperature

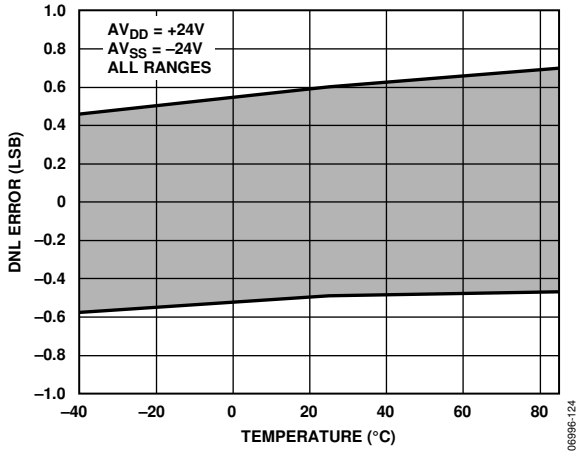


Figure 24. Differential Nonlinearity Error vs. Temperature

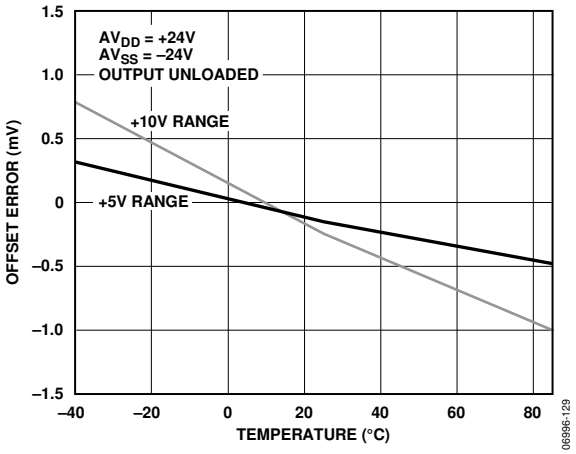


Figure 27. Offset Error vs. Temperature

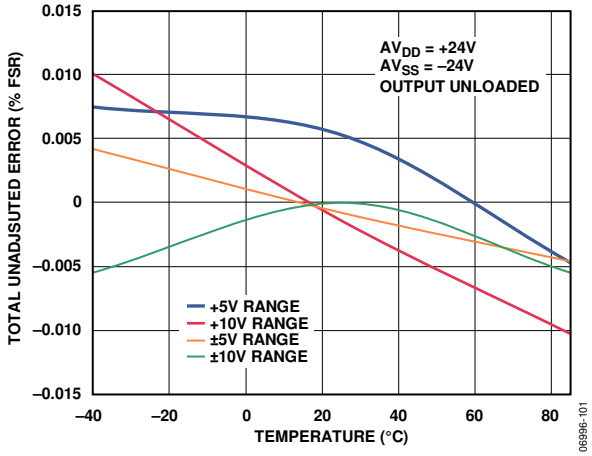


Figure 25. Total Unadjusted Error vs. Temperature

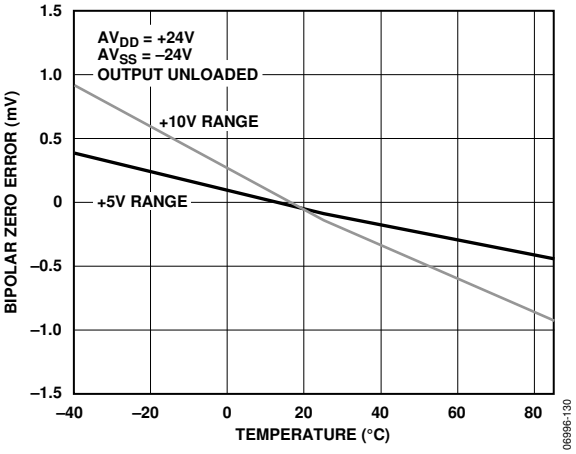


Figure 28. Bipolar Zero Error vs. Temperature

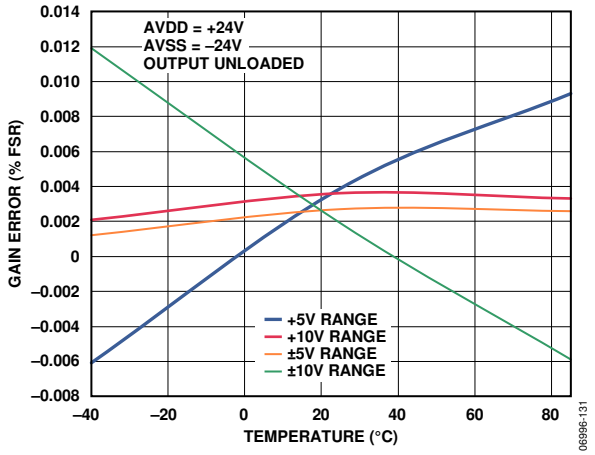


Figure 29. Gain Error vs. Temperature

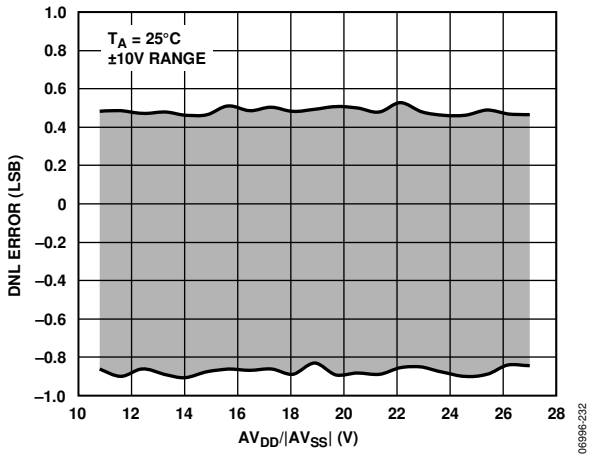


Figure 32. Differential Nonlinearity Error vs. $AV_{DD}/|AV_{SS}|$

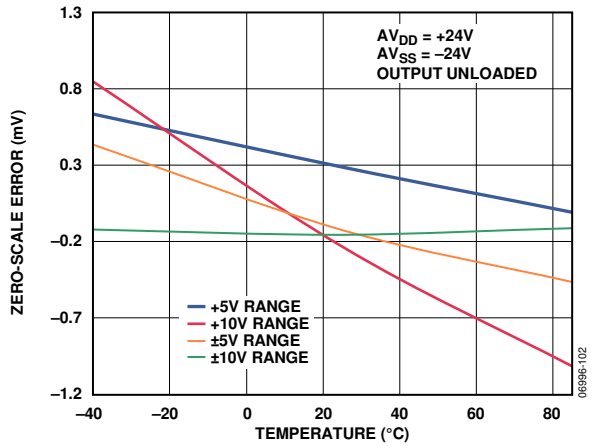


Figure 30. Zero-Scale Error vs. Temperature

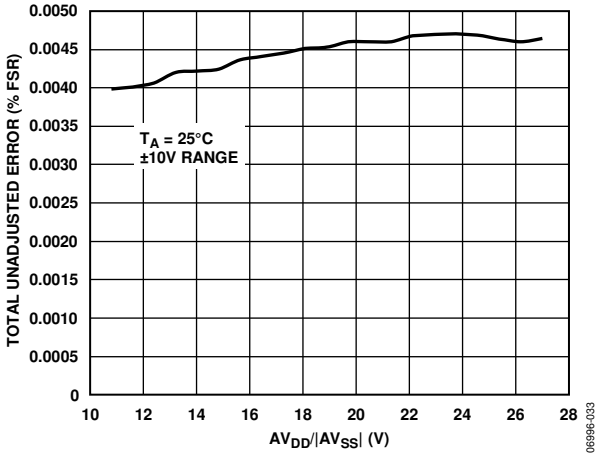


Figure 33. Total Unadjusted Error vs. $AV_{DD}/|AV_{SS}|$

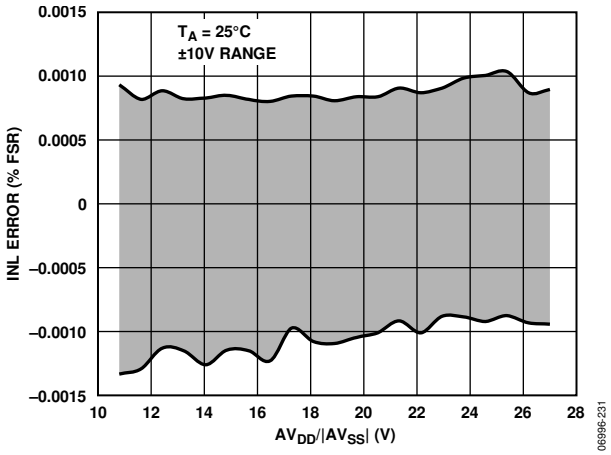


Figure 31. Integral Nonlinearity Error vs. $AV_{DD}/|AV_{SS}|$

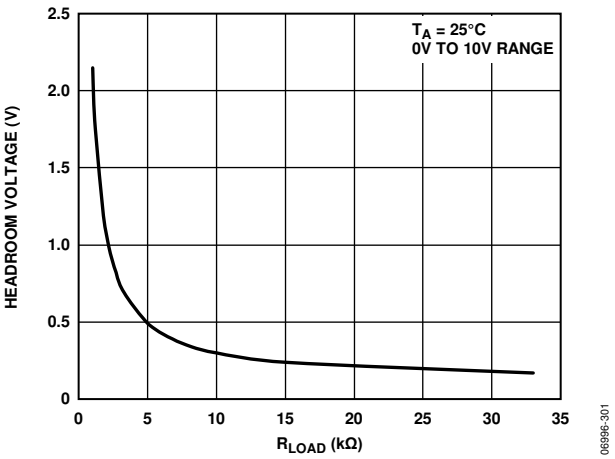


Figure 34. V_{OUT} Headroom

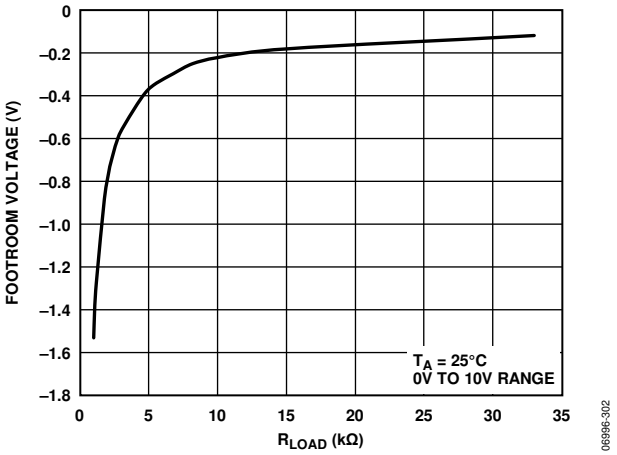


Figure 35. V_{OUT} Footroom

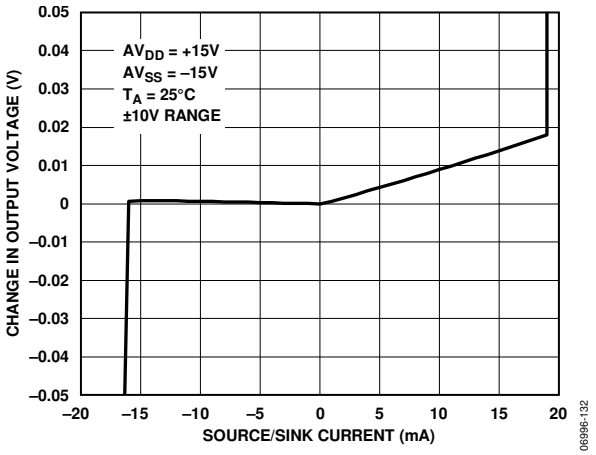


Figure 36. Source and Sink Capability of Output Amplifier, Full-Scale Code Loaded

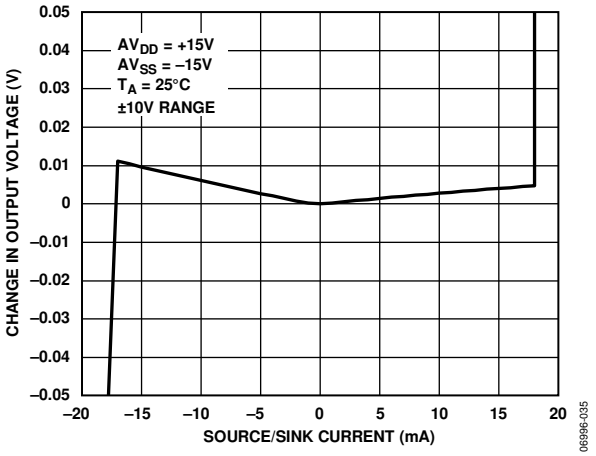


Figure 37. Source and Sink Capability of Output Amplifier, Zero-Scale Loaded

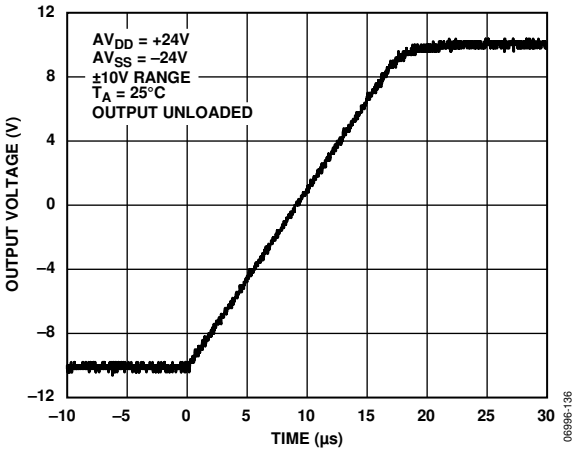


Figure 38. Full-Scale Positive Step

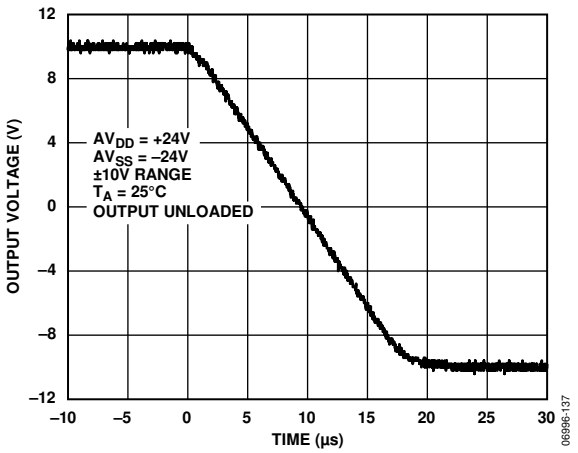


Figure 39. Full-Scale Negative Step

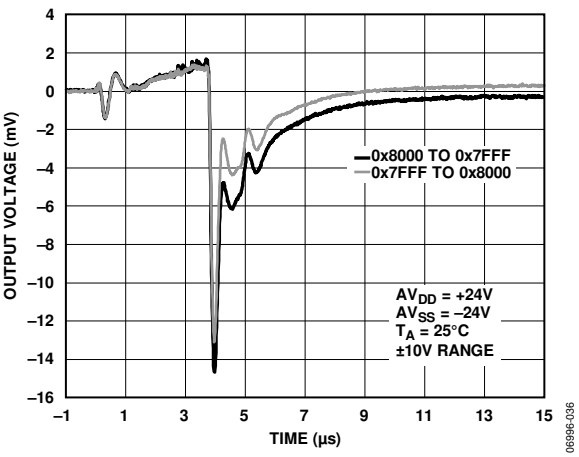


Figure 40. Digital-to-Analog Glitch

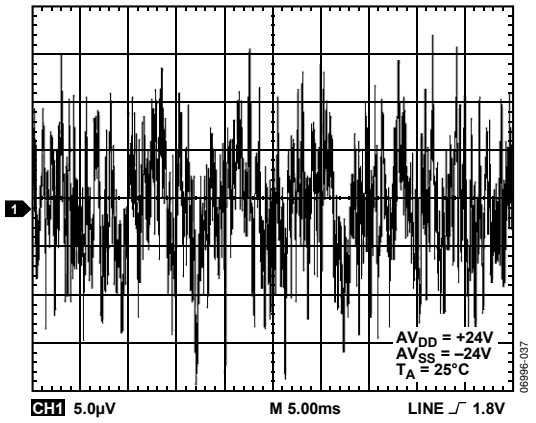


Figure 41. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

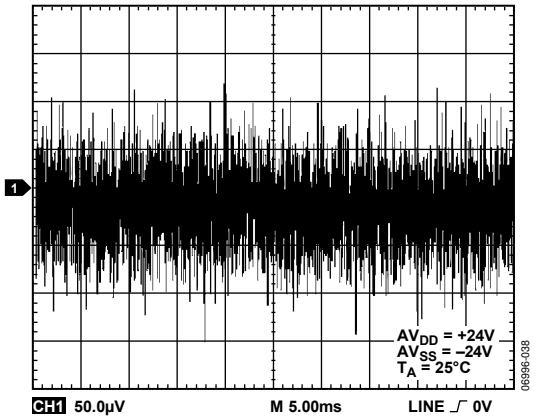


Figure 42. Peak-to-Peak Noise (100 kHz Bandwidth)

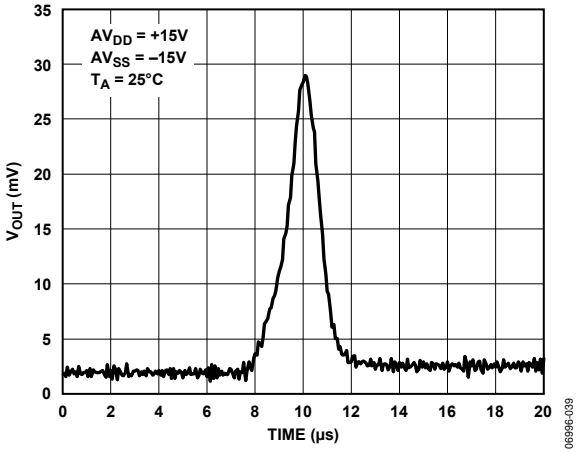


Figure 43. V_{OUT} vs. Time on Power-Up

CURRENT OUTPUT

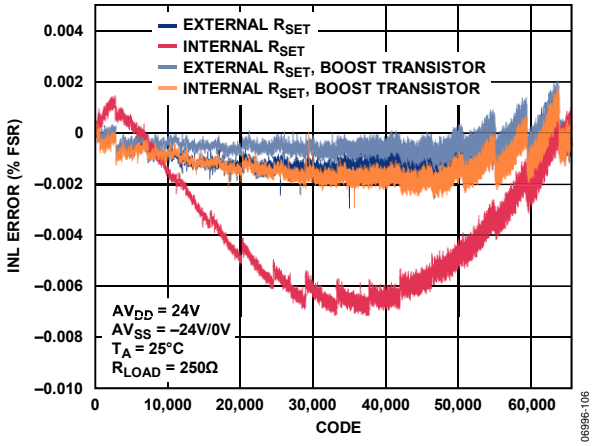


Figure 44. Integral Nonlinearity vs. Code

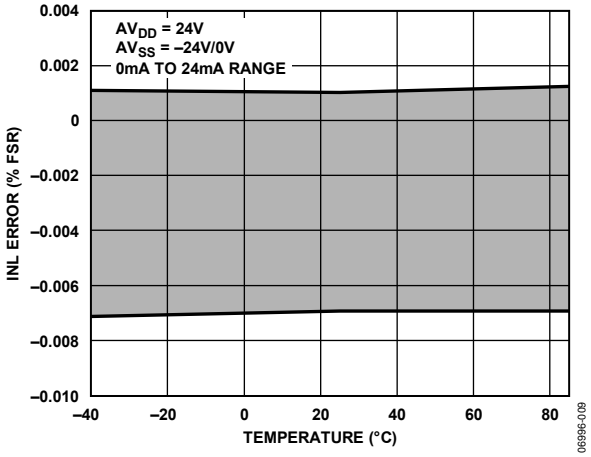


Figure 47. Integral Nonlinearity vs. Temperature, Internal R_{SET}

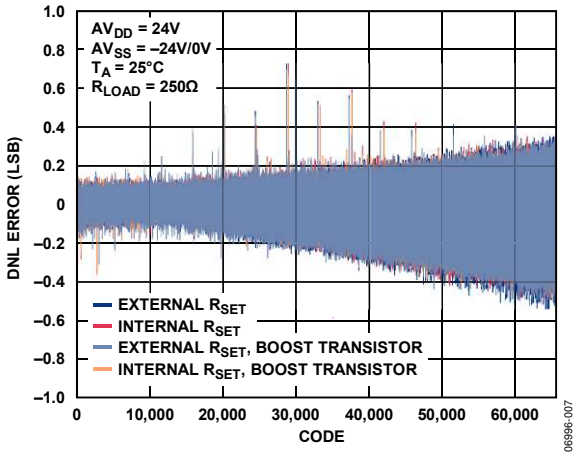


Figure 45. Differential Nonlinearity vs. Code

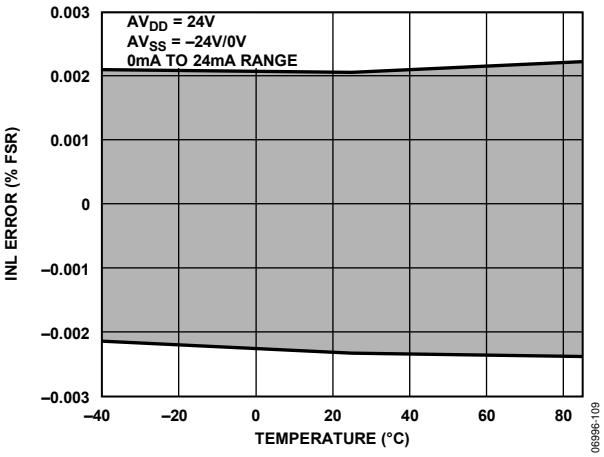


Figure 48. Integral Nonlinearity vs. Temperature, External R_{SET}

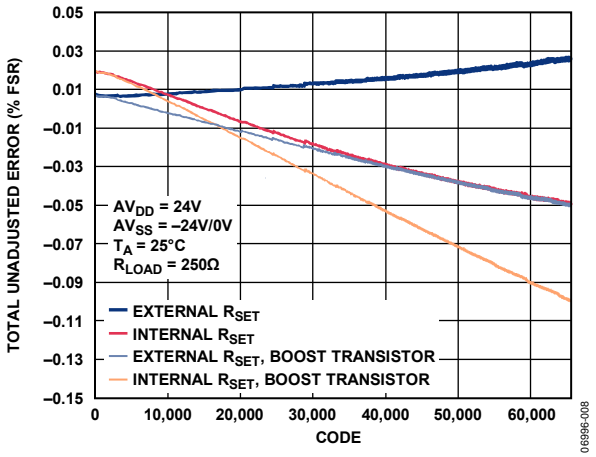


Figure 46. Total Unadjusted Error vs. Code

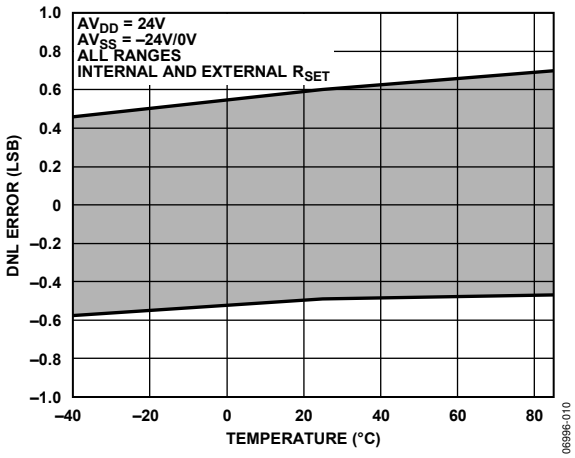


Figure 49. Differential Nonlinearity vs. Temperature

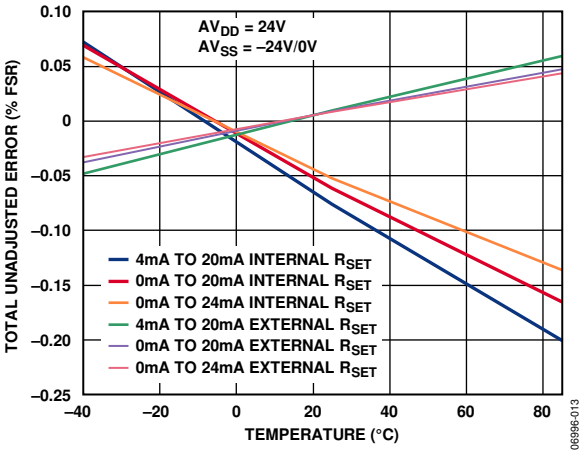


Figure 50. Total Unadjusted Error vs. Temperature

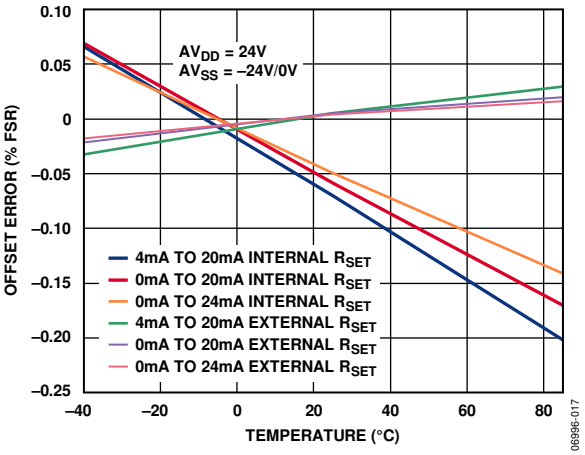


Figure 51. Offset Error vs. Temperature

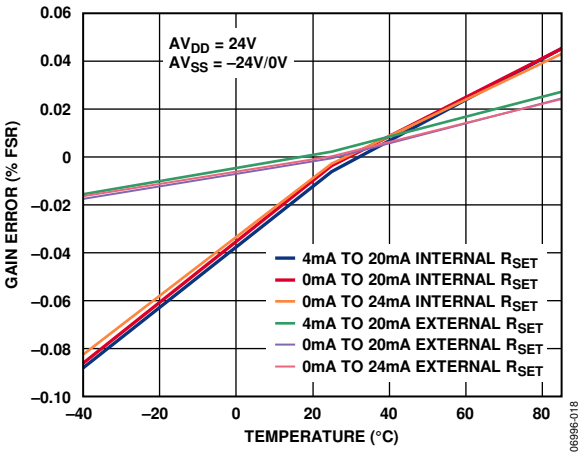


Figure 52. Gain Error vs. Temperature

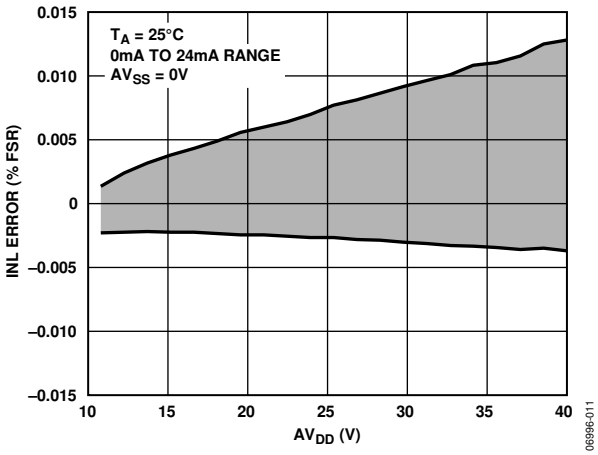


Figure 53. Integral Nonlinearity Error vs. AV_{DD}, External R_{SET}

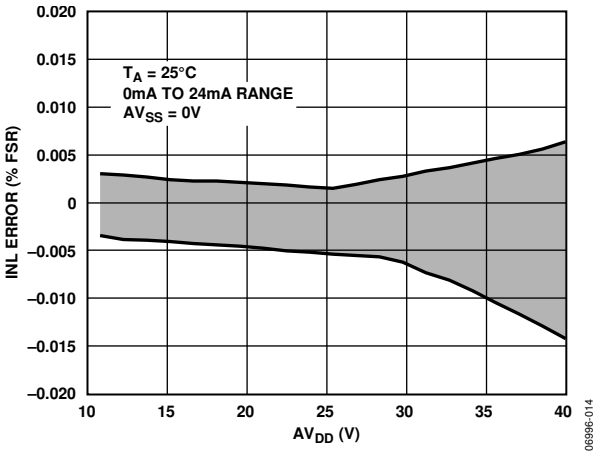


Figure 54. Integral Nonlinearity Error vs. AV_{DD}, Internal R_{SET}

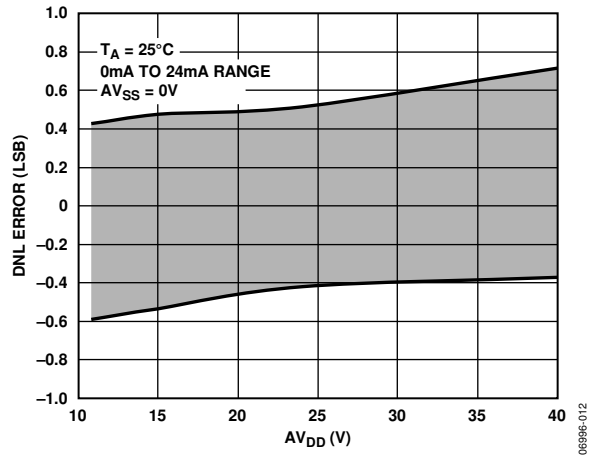


Figure 55. Differential Nonlinearity Error vs. AV_{DD}, External R_{SET}

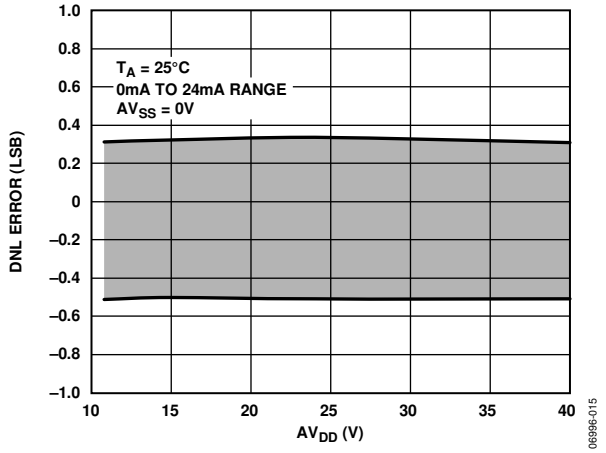


Figure 56. Differential Nonlinearity Error vs. AV_{DD}, Internal R_{SET}

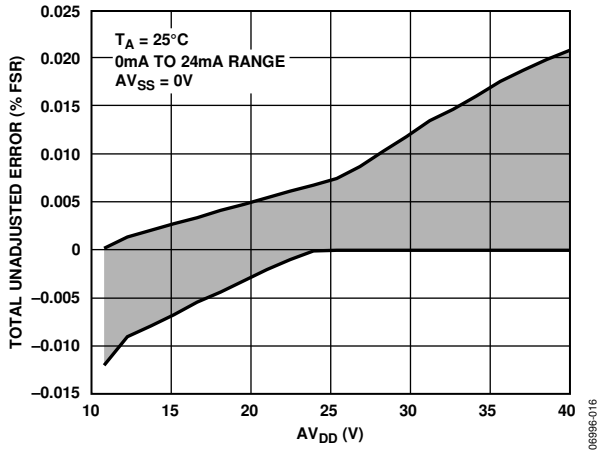


Figure 57. Total Unadjusted Error vs. AV_{DD}, External R_{SET}

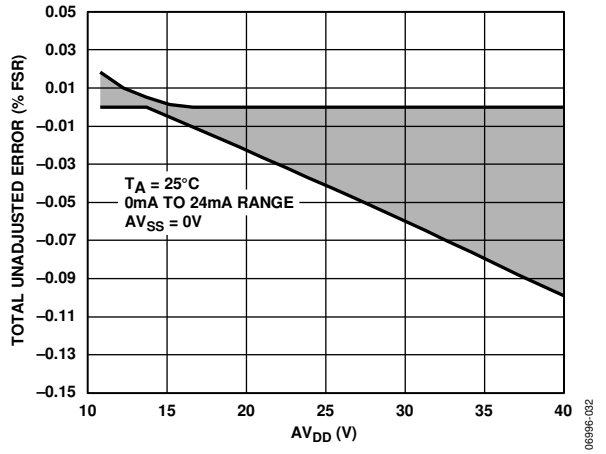


Figure 58. Total Unadjusted Error vs. AV_{DD}, Internal R_{SET}

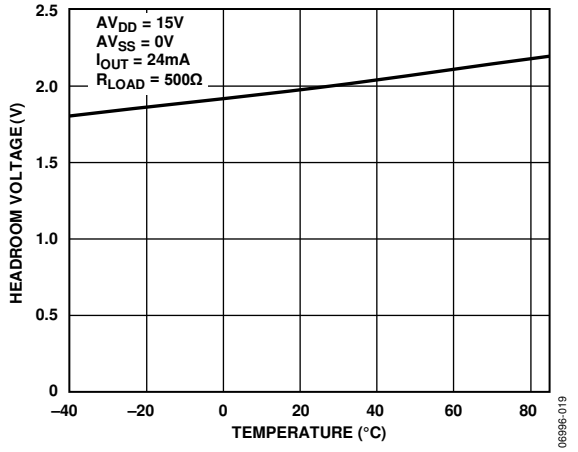


Figure 59. Compliance Voltage Headroom vs. Temperature

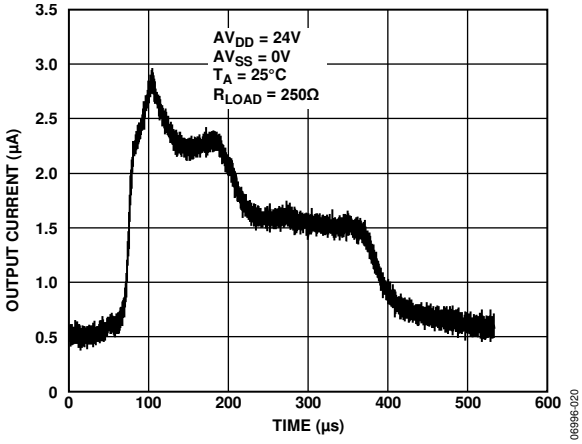


Figure 60. Output Current vs. Time on Power-Up

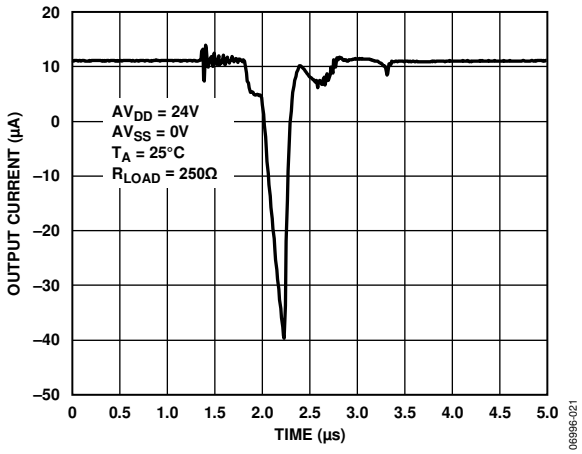


Figure 61. Output Current vs. Time on Output Enable