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Single-Channel, 12-/16-Bit, Serial Input, 4 mA to 20 mA, Current Source DAC, HART Connectivity

Data Sheet

AD5410/AD5420

FEATURES

- 12-/16-bit resolution and monotonicity
- Current output ranges: 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA
  - ±0.01% FSR typical total unadjusted error (TUE)
  - ±3 ppm/°C typical output drift
- Flexible serial digital interface
- On-chip output fault detection
- On-chip reference (10 ppm/°C maximum)
- Feedback/monitoring of output current
- Asynchronous clear function
- Power supply (AV_{DD}) range
  - 10.8 V to 40 V; AD5410AREZ/AD5420AREZ
  - 10.8 V to 60 V; AD5410ACPZ/AD5420ACPZ
- Output loop compliance to AV_{DD} − 2.5 V
- Temperature range: −40°C to +85°C
- 24-lead TSSOP and 40-lead LFCSP packages

APPLICATIONS

- Process control
- Actuator control
- PLC
- HART network connectivity

GENERAL DESCRIPTION

The AD5410/AD5420 are low cost, precision, fully integrated 12-/16-bit converters offering a programmable current source output designed to meet the requirements of industrial process control applications. The output current range is programmable at 4 mA to 20 mA, 0 mA to 20 mA, or an overrange function of 0 mA to 24 mA. The output is open-circuit protected. The device operates with a power supply (AVDD) range from 10.8 V to 60 V. Output loop compliance is 0 V to AV_{DD} − 2.5 V.

The flexible serial interface is SPI, MICROWIRE™, QSPI™, and DSP compatible and can be operated in 3-wire mode to minimize the digital isolation required in isolated applications.

The device also includes a power-on reset function, ensuring that the device powers up in a known state, and an asynchronous CLEAR pin that sets the output to the low end of the selected current range.

The total unadjusted error is typically ±0.01% FSR.

COMPANION PRODUCTS

HART Modem: AD5700, AD5700-1

FUNCTIONAL BLOCK DIAGRAM

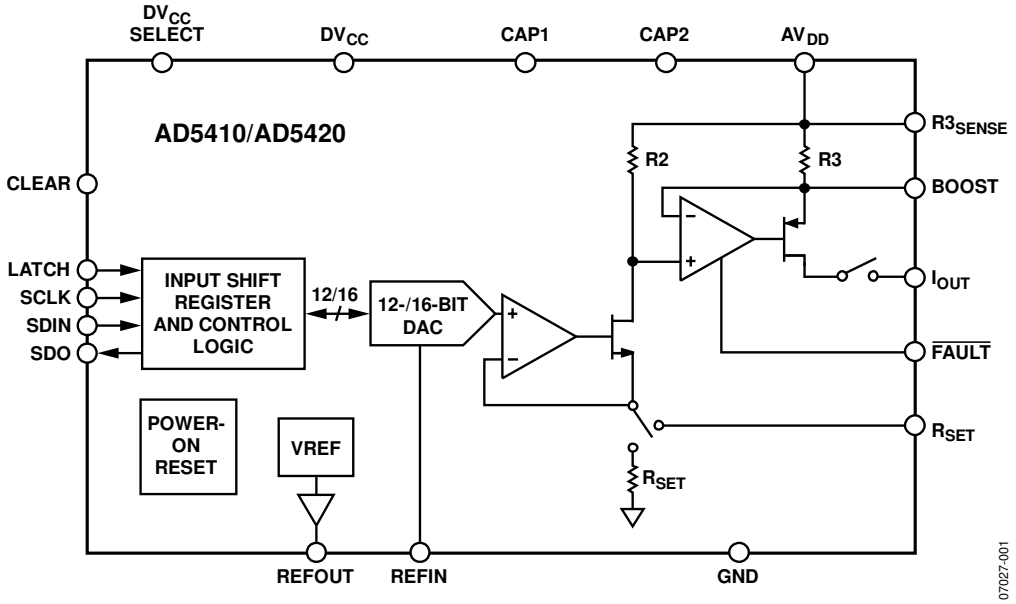

Figure 1.

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TABLE OF CONTENTS

REVISION HISTORY

4/2017—Rev. H to Rev. I

Changes to Table 4 8
Changes to Figure 5 and Figure 6 9

4/2015—Rev. G to Rev. H

Changes to Table 3 6
Changes to Table 5 9

10/2014—Rev. F to Rev. G

Changes to Power-On State Section 20

10/2013—Rev. E to Rev. F

Moved Revision History 3
Changes to Figure 51 27
Changes to Figure 55 29

3/2013—Rev. D to Rev. E

Changes to Table 4 7
Added Figure 40, Renumbered Sequentially 19
Changes to Table 10 20
Changes to Thermal and Supply Considerations Section and Table 21 27
Updated Outline Dimensions 29

5/2012—Rev. C to Rev. D

Reorganized Layout ..... Universal
Changes to Product Title 1
Added Companion Products Section; Changes to Features Section and Applications Section 1
Changes to Table 5 9
Change to Figure 8 11
Added HART Communication Section and Figure 41, Renumbered Sequentially 21
Changes to Industrial, HART Compatible Analog Output Application Section and Figure 54 27

11/2011—Rev. B to Rev. C

Changes to Table 10 18

2/2010—Rev. A to Rev. B

Changes to Figure 46 23

8/2009—Rev. 0 to Rev. A

Changes to Features and General Description 1
Changes to Table 1 3
Changes to Table 2 5
Changes to Introduction to Table 4 and to Table 4 7
Added Figure 6, Changes to Figure 5 and Table 5 8
Added Feedback/Monitoring of Output Current Section, Including Figure 45 to Figure 47; Renumbered Subsequent Figures 23
Changes to Thermal and Supply Considerations Section and Table 21 26
Updated Outline Dimensions 28
Changes to Ordering Guide 28

3/2009—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = 10.8 V to 26.4 V, GND = 0 V, REFIN = 5 V external; DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CURRENT RANGES	0		24	mA	
	0		20	mA	
	4		20	mA	
ACCURACY, INTERNAL R_{SET}					
Resolution	16			Bits	AD5420
	12			Bits	AD5410
Total Unadjusted Error (TUE)	−0.3		+0.3	% FSR	AD5420
	−0.13	±0.08	+0.13	% FSR	AD5420, T_A = 25°C
	−0.5		+0.5	% FSR	AD5410
	−0.3	±0.15	+0.3	% FSR	AD5410, T_A = 25°C
Relative Accuracy (INL)[2]	−0.024		+0.024	% FSR	AD5420
	−0.032		+0.032	% FSR	AD5410
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.27		+0.27	% FSR	
	−0.12	±0.08	+0.12	% FSR	T_A = 25°C
Offset Error Temperature Coefficient (TC)[3]		±16		ppm FSR/°C	
Gain Error	−0.18		+0.18	% FSR	AD5420
	−0.03	±0.006	+0.03	% FSR	AD5420, T_A = 25°C
	−0.22		+0.22		AD5410
	−0.06	±0.012	+0.06		AD5410, T_A = 25°C
Gain Error Temperature Coefficient (TC)[3]		±10		ppm FSR/°C	
Full-Scale Error	−0.2		+0.2	% FSR	
	−0.1	±0.08	+0.1	% FSR	T_A = 25°C
Full-Scale Error Temperature Coefficient (TC)[3]		±12		ppm FSR/°C	
ACCURACY, EXTERNAL R_{SET}					Assumes an ideal 15 kΩ resistor
Resolution	16			Bits	AD5420
	12			Bits	AD5410
Total Unadjusted Error (TUE)	−0.15		+0.15	% FSR	AD5420
	−0.06	±0.01	+0.06	% FSR	AD5420, T_A = 25°C
	−0.3		+0.3	% FSR	AD5410
	−0.1	±0.02	+0.1	% FSR	AD5410, T_A = 25°C
Relative Accuracy (INL)[2]	−0.012		+0.012	% FSR	AD5420
	−0.032		+0.032	% FSR	AD5410
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.1		+0.1	% FSR	
	−0.03	±0.006	+0.03	% FSR	T_A = 25°C
Offset Error Temperature Coefficient (TC)[3]		±3		ppm FSR/°C	
Gain Error	−0.08		+0.08	% FSR	
	−0.05	±0.003	+0.05	% FSR	T_A = 25°C
Gain Error Temperature Coefficient (TC)[3]		±4		ppm FSR/°C	
Full-Scale Error	−0.15		+0.15	% FSR	
	−0.06	±0.01	+0.06	% FSR	T_A = 25°C
Full-Scale Error Temperature Coefficient (TC)[3]		±7		ppm FSR/°C	
OUTPUT CHARACTERISTICS[3]					
Current Loop Compliance Voltage	0		AV_{DD} − 2.5	V	
Output Current Drift vs. Time		50		ppm FSR	Internal R_{SET}, drift after 1000 hours at 125°C
		20		ppm FSR	External R_{SET}, drift after 1000 hours at 125°C
Resistive Load			1200	Ω	
Inductive Load		50		mH	T_A = 25°C
DC Power Supply Rejection Ratio (PSRR)			1	µA/V	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Output Impedance		50		MΩ	
Output Current Leakage		60		pA	Output disabled
R3 Resistor Value	36	40	44	Ω	T_A = 25°C
R3 Resistor Temperature Coefficient (TC)		30		ppm/°C	
I_{BIAS} Current	399	444	489	µA	
I_{BIAS} Current Temperature Coefficient (TC)		30		ppm/°C	
REFERENCE INPUT/OUTPUT					
Reference Input[3]					
Reference Input Voltage	4.95	5	5.05	V	For specified performance
DC Input Impedance	25	30		kΩ	
Reference Output					
Output Voltage	4.995	5.000	5.005	V	T_A = 25°C
Reference TC[3, 4]		1.8	10	ppm/°C	
Output Noise (0.1 Hz to 10 Hz)[3]		18		µV p-p	
Noise Spectral Density[3]		100		nV/√Hz	At 10 kHz
Output Voltage Drift vs. Time[3]		50		ppm	Drift after 1000 hours, T_A = 125°C
Capacitive Load[3]		600		nF	
Load Current[3]		5		mA	
Short-Circuit Current[3]		7		mA	
Load Regulation[3]		95		ppm/mA	
DIGITAL INPUTS[3]					JEDEC compliant
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current	−1		+1	µA	Per pin
Pin Capacitance		10		pF	Per pin
DIGITAL OUTPUTS[3]					
SDO					
Output Low Voltage, V_{OL}			0.4	V	Sinking 200 µA
Output High Voltage, V_{OH}	DV_{CC} − 0.5			V	Sourcing 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance		5		pF	
$\overline{FAULT}$					
Output Low Voltage, V_{OL}			0.4	V	10 kΩ pull-up resistor to DV_{CC}
Output Low Voltage, V_{OL}		0.6		V	2.5 mA load current
Output High Voltage, V_{OH}	3.6			V	10 kΩ pull-up resistor to DV_{CC}
POWER REQUIREMENTS					
AV_{DD}	10.8		40	V	TSSOP package
	10.8		60	V	LFCSP package
DV_{CC}					
Input Voltage	2.7		5.5	V	Internal supply disabled
Output Voltage		4.5		V	DV_{CC} can be overdriven up to 5.5 V
Output Load Current[3]		5		mA	
Short-Circuit Current[3]		20		mA	
AI_{DD}			3	mA	Output disabled
			4	mA	Output enabled
DI_{CC}			1	mA	$V_{IH} = DV_{CC}$, V_{IL} = GND
Power Dissipation		144		mW	AV_{DD} = 40 V, I_{OUT} = 0 mA
		50		mW	AV_{DD} = 15 V, I_{OUT} = 0 mA

[1] Temperature range: −40°C to +85°C; typical at +25°C.
[2] For 0 mA to 20 mA and 0 mA to 24 mA ranges, INL is measured from Code 256 for the AD5420 and Code 16 for the AD5410.
[3] Guaranteed by design and characterization but not production tested.
[4] The on-chip reference is production trimmed and tested at 25°C and 85°C. It is characterized from −40°C to +85°C.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = 10.8 V to 26.4 V, GND = 0 V, REFIN = 5 V external; DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Output Current Settling Time[2]		10		µs	16 mA step, to 0.1% FSR
		40		µs	16 mA step, to 0.1% FSR, L = 1 mH
AC PSRR		−75		dB	200 mV, 50 Hz/60 Hz sine wave superimposed on power supply voltage

[1] Guaranteed by design and characterization; not production tested.
[2] Digital slew rate control feature disabled and CAP1 = CAP2 = open circuit.

TIMING CHARACTERISTICS

AV_{DD} = 10.8 V to 26.4 V, GND = 0 V, REFIN = 5 V external; DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
WRITE MODE			
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK low time
t_3	13	ns min	SCLK high time
t_4	13	ns min	LATCH delay time
t_5	5	µs min	LATCH high time
t_6	5	ns min	Data setup time
t_7	5	ns min	Data hold time
t_8	40	ns min	LATCH low time
t_9	20	ns min	CLEAR pulse width
t_{10}	5	µs max	CLEAR activation time
READBACK MODE			
t_{11}	90	ns min	SCLK cycle time
t_{12}	40	ns min	SCLK low time
t_{13}	40	ns min	SCLK high time
t_{14}	13	ns min	LATCH delay time
t_{15}	40	ns min	LATCH high time
t_{16}	5	ns min	Data setup time
t_{17}	5	ns min	Data hold time
t_{18}	40	ns min	LATCH low time
t_{19}	35	ns max	Serial output delay time ($C_{L\ SDO}$ = 50 pF)[4]
t_{20}	35	ns max	LATCH rising edge to SDO tristate
DAISY-CHAIN MODE			
t_{21}	90	ns min	SCLK cycle time
t_{22}	40	ns min	SCLK low time
t_{23}	40	ns min	SCLK high time
t_{24}	13	ns min	LATCH delay time
t_{25}	40	ns min	LATCH high time
t_{26}	5	ns min	Data setup time
t_{27}	5	ns min	Data hold time
t_{28}	40	ns min	LATCH low time
t_{29}	35	ns max	Serial output delay time ($C_{L\ SDO}$ = 50 pF)[4]

[1] Guaranteed by characterization but not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, and Figure 4.
[4] C_{LSDO} = capacitive load on SDO output.

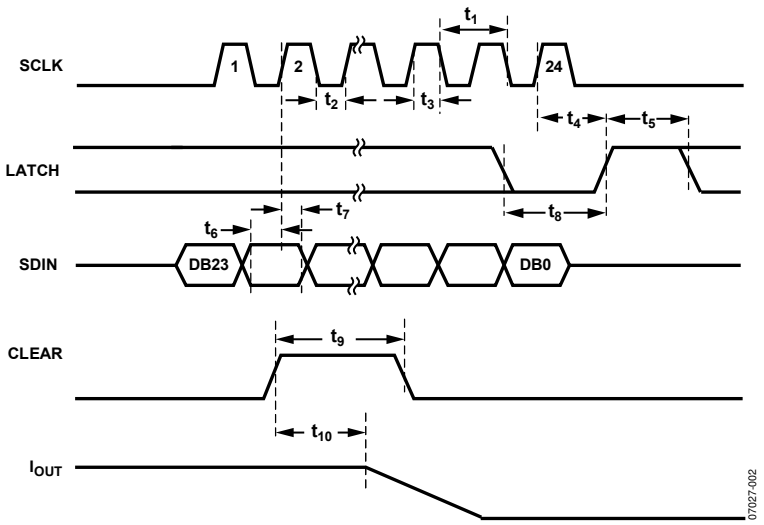


Figure 2. Write Mode Timing Diagram

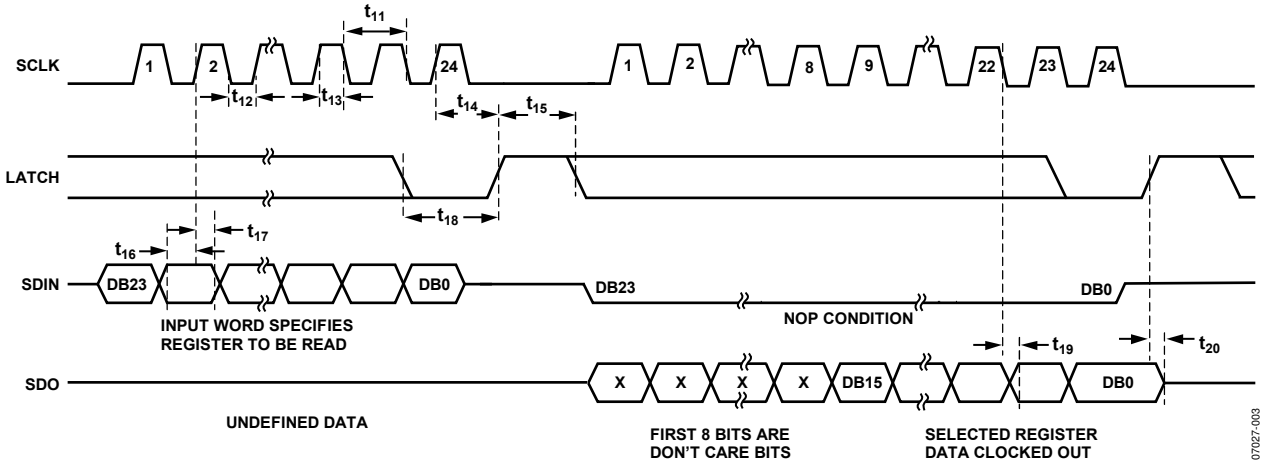


Figure 3. Readback Mode Timing Diagram

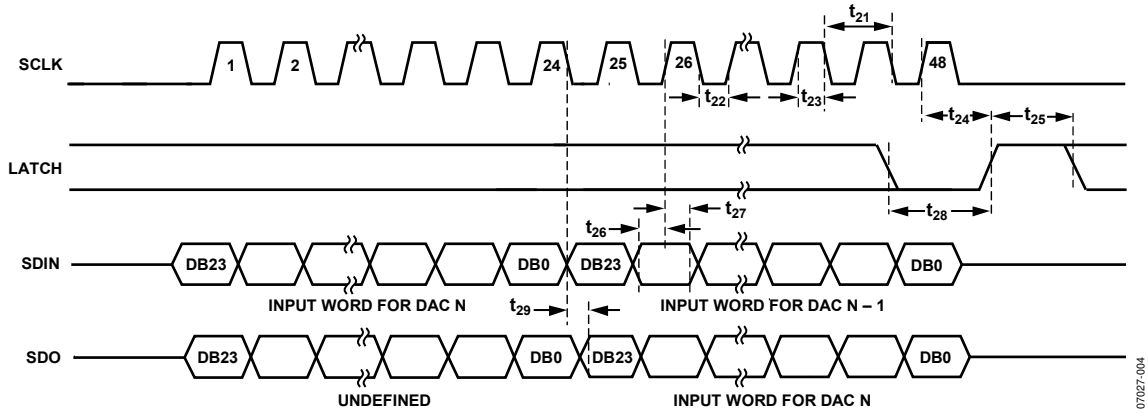


Figure 4. Daisy-Chain Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 80 mA do not cause SCR latch-up.

Table 4.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +60 V
DV_{CC} to GND	−0.3 V to +7 V
Digital Inputs to GND	−0.3 V to DV_{CC} + 0.3 V or +7 V (whichever is less)
Digital Outputs to GND	−0.3 V to DV_{CC} + 0.3 V or +7 V (whichever is less)
REFIN, REFOUT to GND	−0.3 V to +7 V
I_{OUT} to GND	−0.3 V to AV_{DD}
Operating Temperature Range	
Industrial	−40°C to +85°C[1]
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
24-Lead TSSOP_EP Package	
Thermal Impedance, θ_{JA}	35°C/W[2]
Thermal Impedance, θ_{JC}	9°C/W
40-Lead LFCSP Package	
Thermal Impedance, θ_{JA}	33°C/W[2]
Thermal Impedance, θ_{JC}	4°C/W
Power Dissipation	(T_J max − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

[1] Power dissipated on chip must be derated to keep junction temperature below 125°C. The assumption is that the maximum power dissipation condition is sourcing 24 mA into ground from AV_{DD} with a 4 mA on-chip current.

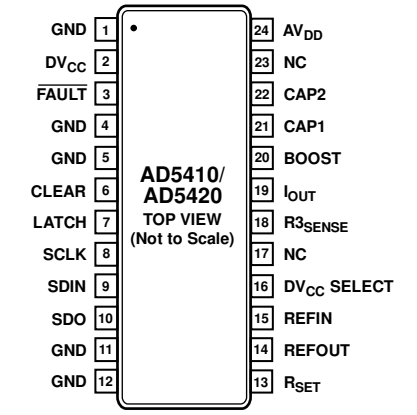
[2] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with thermal vias. Ref: JEDEC JESD51 documents.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

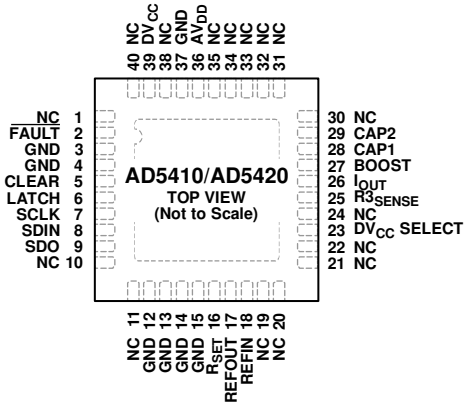
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD MUST BE CONNECTED TO THE GROUND REFERENCE.

07027-005

Figure 5. TSSOP Pin Configuration



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD MUST BE CONNECTED TO THE GROUND REFERENCE.

07027-053

Figure 6. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Description
1, 4, 5, 12	3, 4, 14, 15, 37	GND	These pins must be connected to ground.
2	39	DV_{CC}	Digital Supply Pin. Voltage ranges from 2.7 V to 5.5 V.
3	2	$\overline{FAULT}$	Fault Alert. This pin is asserted low when an open circuit is detected between I_{OUT} and GND or an overtemperature is detected. The $\overline{FAULT}$ pin is an open-drain output and must be connected to DV_{CC} through a pull-up resistor (typically 10 kΩ).
6	5	CLEAR	Active High Input. Asserting this pin sets the output current to the zero-scale value, which is either 0 mA or 4 mA, depending on the output range programmed, that is, 0 mA to 20 mA, 0 mA to 24 mA, or 4 mA to 20 mA.
7	6	LATCH	Positive Edge Sensitive Latch. A rising edge parallel loads the input shift register data into the relevant register. In the case of the data register, the output current is also updated.
8	7	SCLK	Serial Clock Input. Data is clocked into the input shift register on the rising edge of SCLK. This operates at clock speeds of up to 30 MHz.
9	8	SDIN	Serial Data Input. Data must be valid on the rising edge of SCLK.
10	9	SDO	Serial Data Output. This pin is used to clock data from the device in daisy-chain or readback mode. Data is clocked out on the falling edge of SCLK. See Figure 3 and Figure 4.
11	12, 13	GND	Ground Reference Pin.
13	16	R_{SET}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the overall performance of the device. See the Specifications and AD5410/AD5420 Features sections.
14	17	REFOUT	Internal Reference Voltage Output. V_{REFOUT} = 5 V ± 5 mV at T_A = 25°C. Typical temperature drift is 1.8 ppm/°C.
15	18	REFIN	External Reference Voltage Input. V_{REFIN} = 5 V ± 50 mV for specified performance.
16	23	DV_{CC} SELECT	This pin, when connected to GND, disables the internal supply, and an external supply must be connected to the DV_{CC} pin. Leave this pin unconnected to enable the internal supply. In this case, it is recommended to connect a 0.1 µF capacitor between DV_{CC} and GND. See the AD5410/AD5420 Features section.
17, 23	1, 10, 11, 19, 20, 21, 22, 24, 30, 31, 32, 33, 34, 35, 38, 40	NC	Do not connect to these pins.

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Description
18	25	$R3_{SENSE}$	The voltage measured between this pin and the BOOST pin is directly proportional to the output current and can be used as a monitor/feedback feature. This should be used as a voltage sense output only; current should not be sourced from this pin. See the AD5410/AD5420 Features section.
19	26	I_{OUT}	Current Output Pin.
20	27	BOOST	Optional External Transistor Connection. Connecting an external transistor reduces the power dissipated in the AD5410/AD5420. See the AD5410/AD5420 Features section.
21	28	CAP1	Connection for Optional Output Filtering Capacitor. See the AD5410/AD5420 Features section.
22	29	CAP2	Connection for Optional Output Filtering Capacitor. See the AD5410/AD5420 Features section. Also HART Input Connection, see Device Features Section.
24	36	AV_{DD}	Positive Analog Supply Pin. Voltage ranges from 10.8 V to 40 V.
25 (EPAD)	41 (EPAD)	Exposed pad	The exposed pad must be connected to the ground reference.

TYPICAL PERFORMANCE CHARACTERISTICS

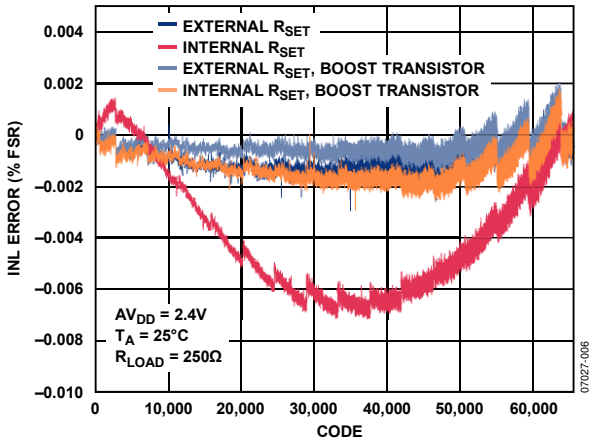


Figure 7. Integral Nonlinearity Error vs. Code

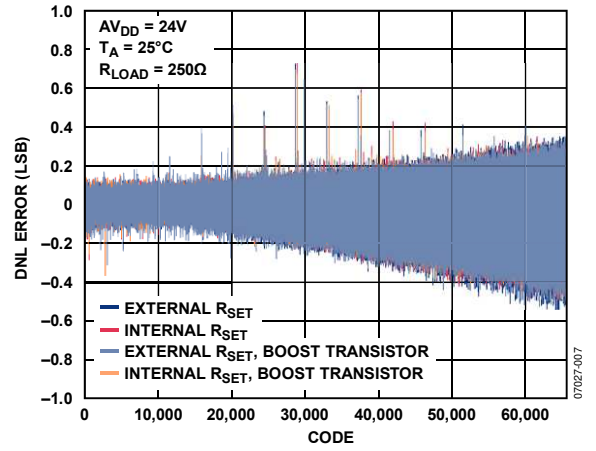


Figure 8. Differential Nonlinearity Error vs. Code

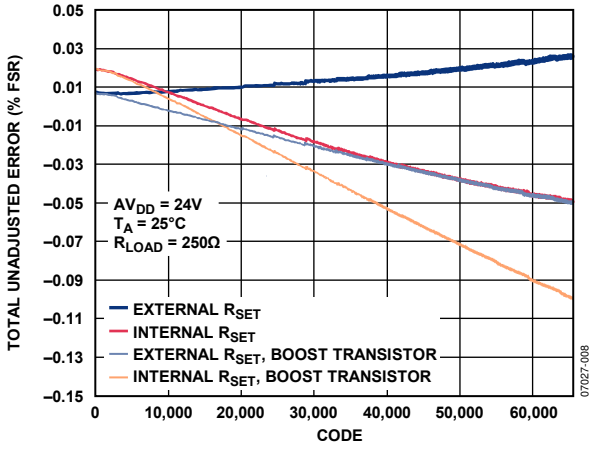


Figure 9. Total Unadjusted Error vs. Code

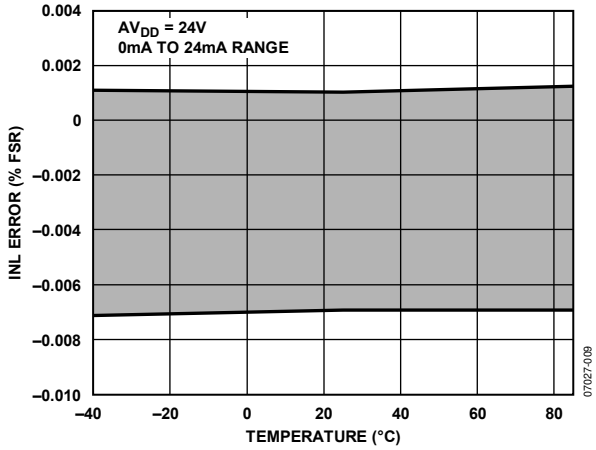


Figure 10. Integral Nonlinearity Error vs. Temperature, Internal R_{SET}

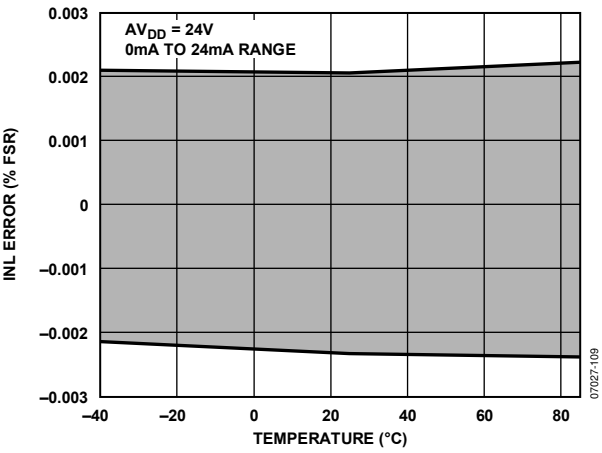


Figure 11. Integral Nonlinearity Error vs. Temperature, External R_{SET}

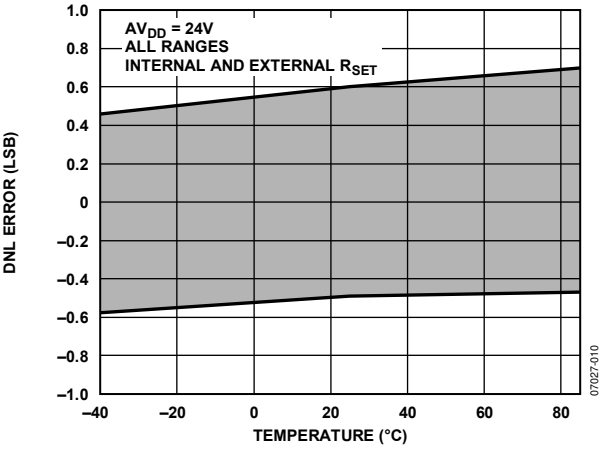


Figure 12. Differential Nonlinearity Error vs. Temperature

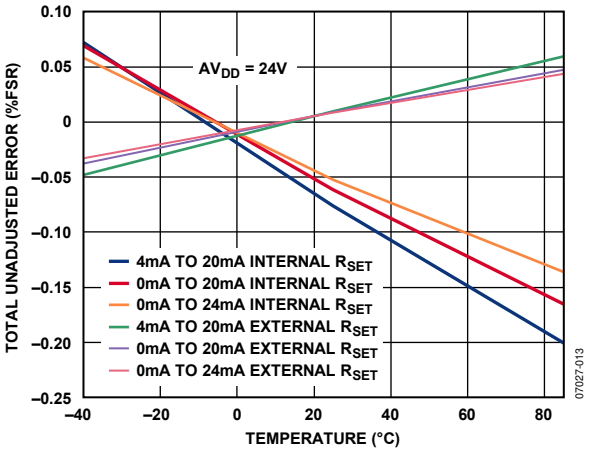


Figure 13. Total Unadjusted Error vs. Temperature

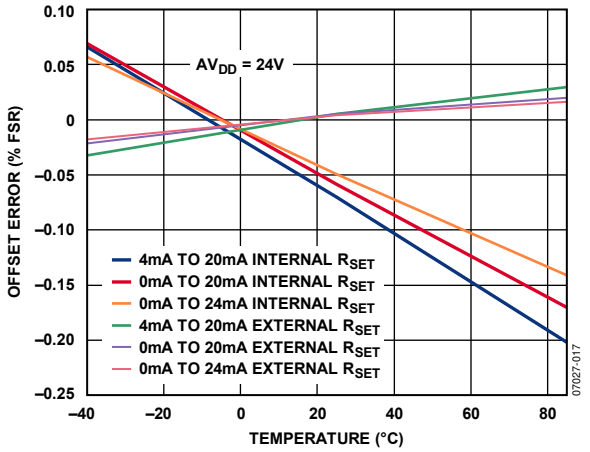


Figure 14. Offset Error vs. Temperature

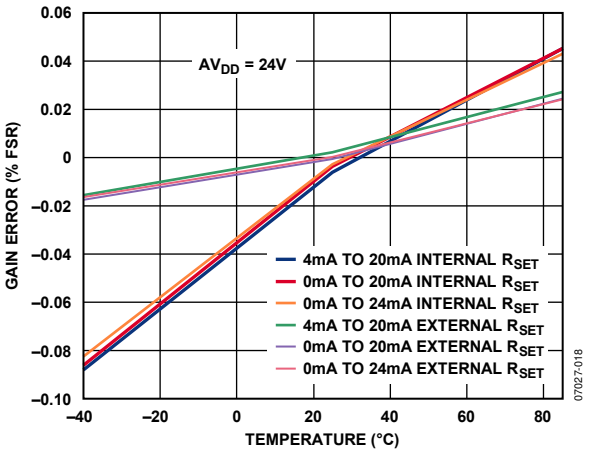


Figure 15. Gain Error vs. Temperature

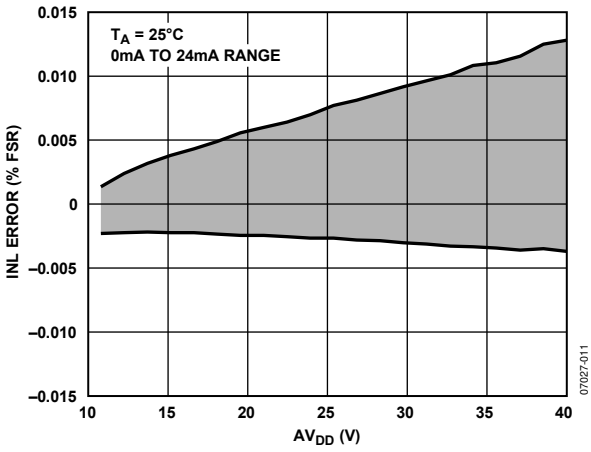


Figure 16. Integral Nonlinearity Error vs. AV_{DD}, External R_{SET}

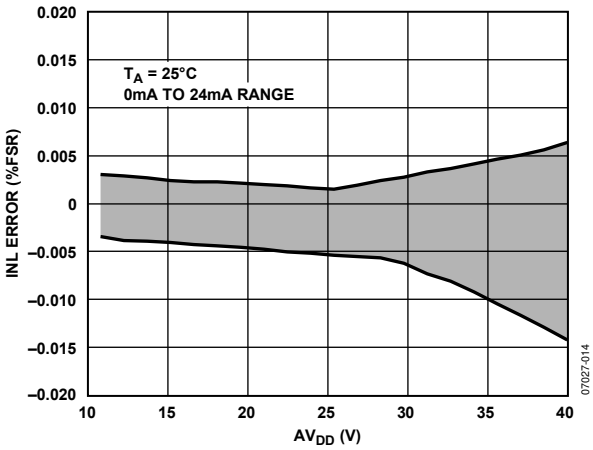


Figure 17. Integral Nonlinearity Error vs. AV_{DD}, Internal R_{SET}

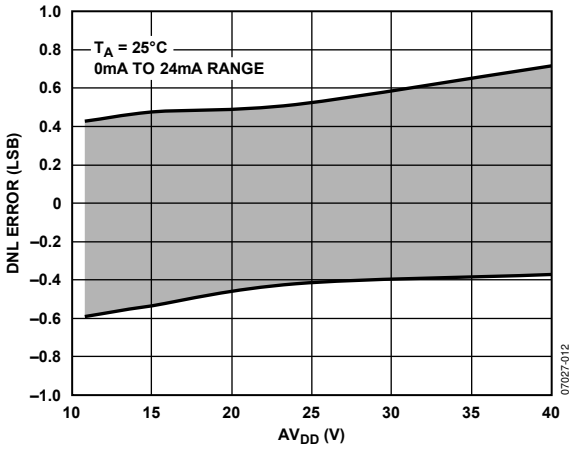


Figure 18. Differential Nonlinearity Error vs. AV_{DD}, External R_{SET}

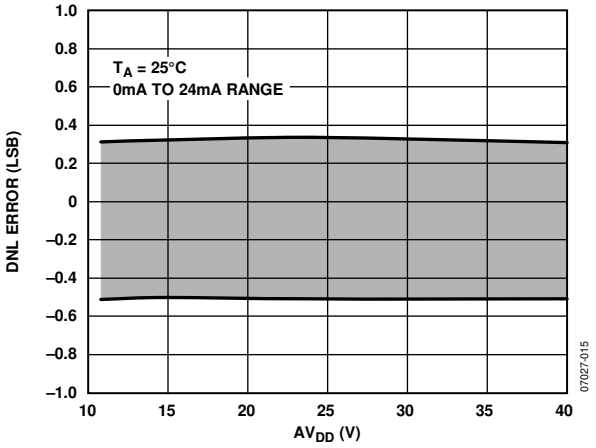


Figure 19. Differential Nonlinearity Error vs. AV_{DD}, Internal R_{SET}

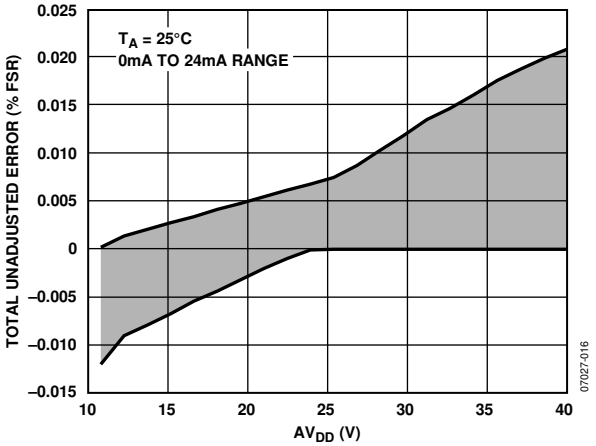


Figure 20. Total Unadjusted Error vs. AV_{DD}, External R_{SET}

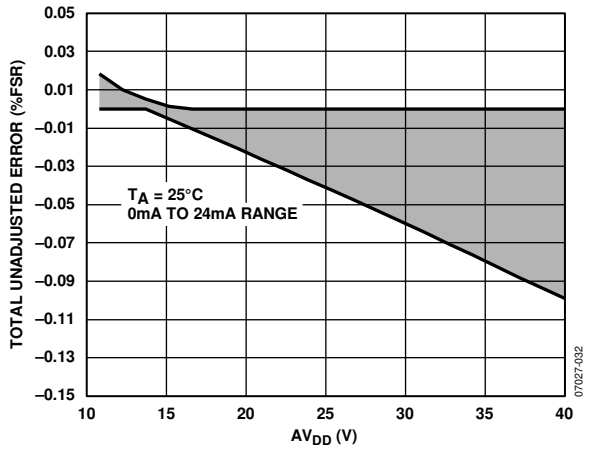


Figure 21. Total Unadjusted Error vs. AV_{DD}, Internal R_{SET}

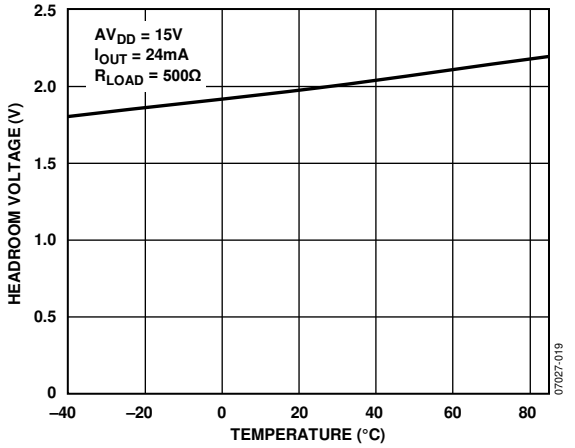


Figure 22. Compliance Voltage Headroom vs. Temperature

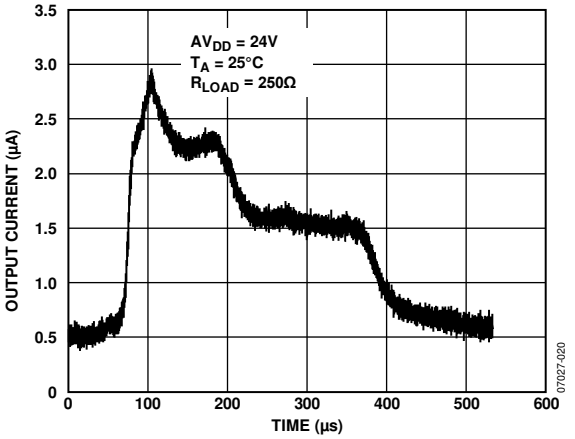


Figure 23. Output Current vs. Time on Power-Up

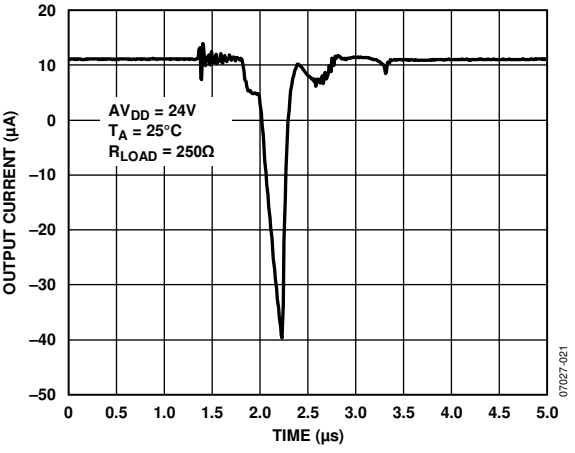


Figure 24. Output Current vs. Time on Output Enable

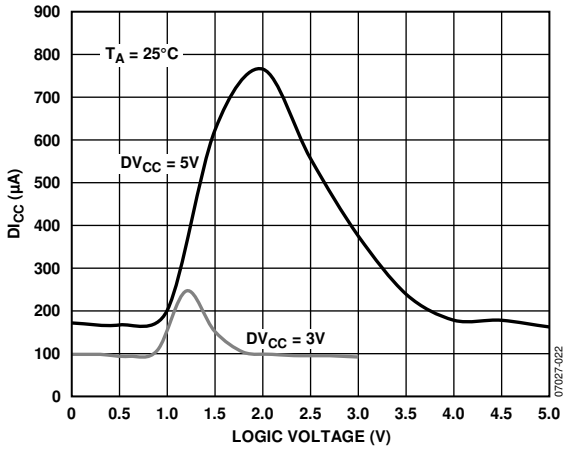


Figure 25. DI_{CC} vs. Logic Input Voltage

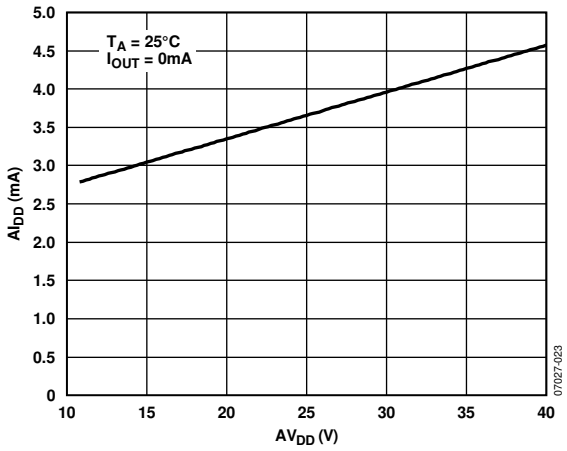


Figure 26. AI_{DD} vs. AV_{DD}

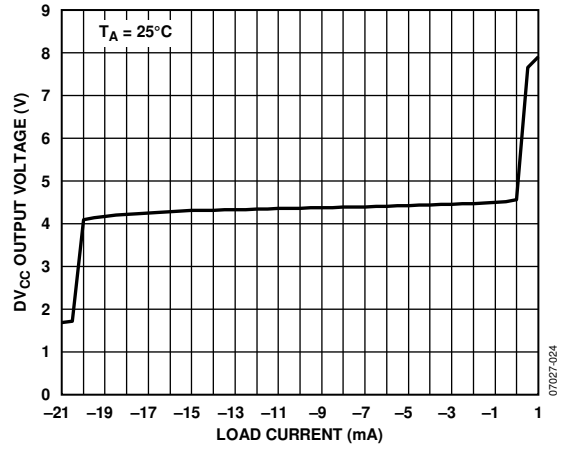


Figure 27. DV_{CC} Output Voltage vs. Load Current

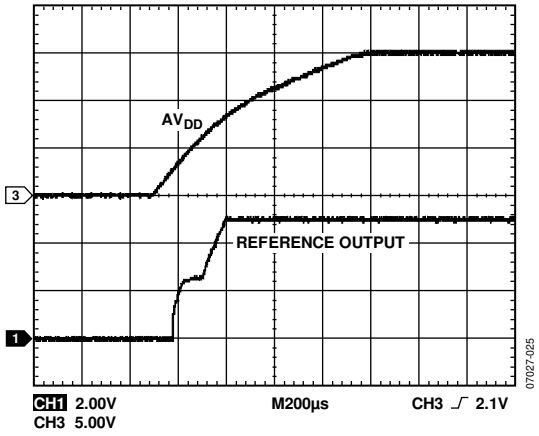


Figure 28. Reference Turn-on Transient

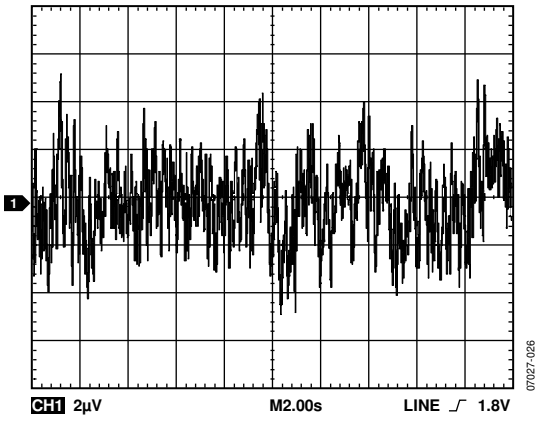


Figure 29. Reference Noise (0.1 Hz to 10 Hz Bandwidth)

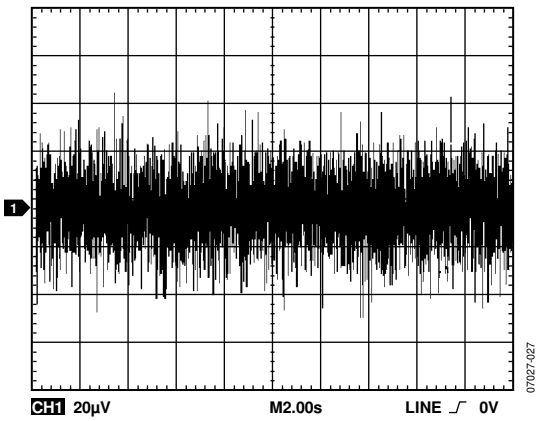


Figure 30. Reference Noise (100 kHz Bandwidth)

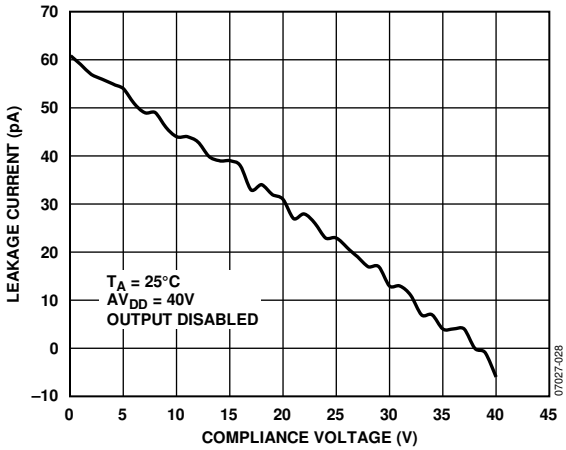


Figure 31. Output Leakage Current vs. Compliance Voltage

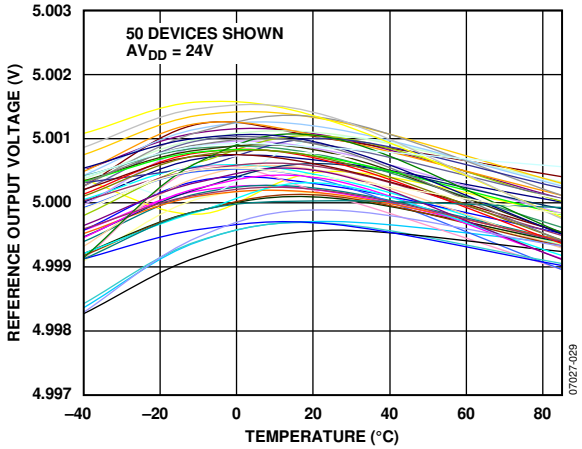


Figure 32. Reference Output Voltage vs. Temperature

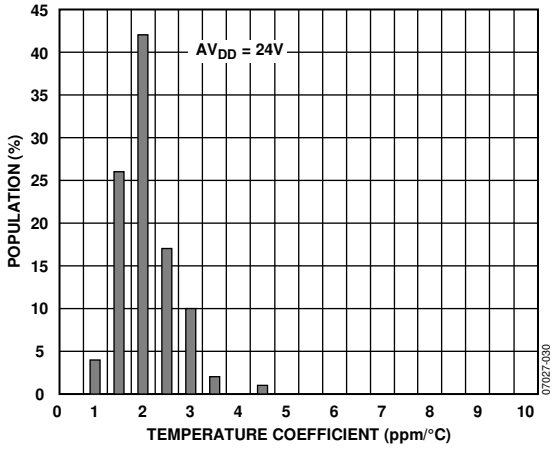


Figure 33. Reference Temperature Coefficient Histogram

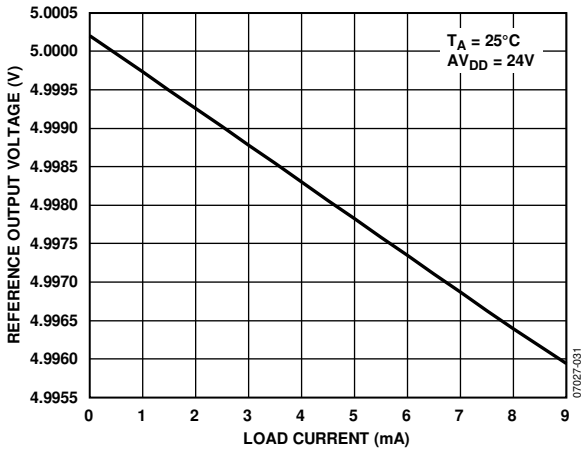


Figure 34. Reference Output Voltage vs. Load Current

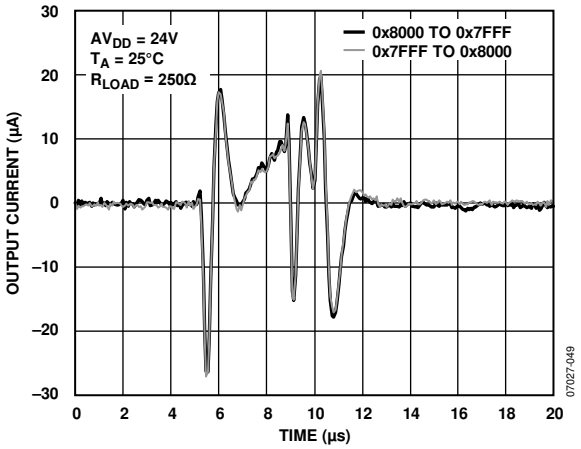


Figure 35. Digital-to-Analog Glitch

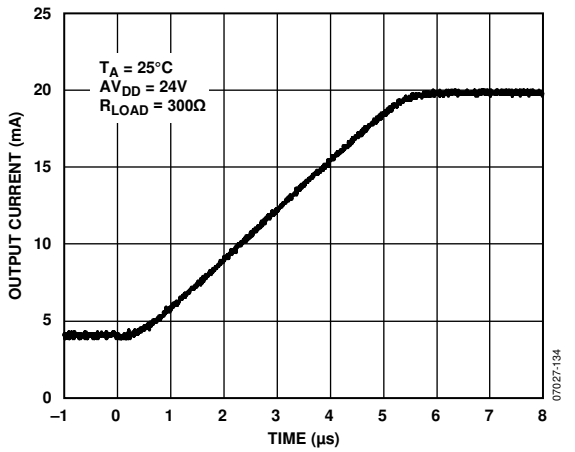


Figure 36. 4 mA to 20 mA Output Current Step

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation, in % FSR, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 7.

Differential Nonlinearity (DNL)
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 8.

Total Unadjusted Error (TUE)
Total unadjusted error (TUE) is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies and temperature. TUE is expressed in % FSR. A typical TUE vs. code plot can be seen in Figure 9.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5410/AD5420 are monotonic over their full operating temperature range.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code is loaded to the data register. Ideally, the output should be full-scale − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range (% FSR).

Full-Scale Error Temperature Coefficient (TC)
This is a measure of the change in full-scale error with changes in temperature. Full-scale error TC is expressed in ppm FSR/°C.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed in % FSR. A plot of gain error vs. temperature can be seen in Figure 15.

Gain Error Temperature Coefficient (TC)
This is a measure of the change in gain error with changes in temperature. Gain error TC is expressed in ppm FSR/°C.

Current Loop Compliance Voltage
This is the maximum voltage at the I_{OUT} pin for which the output current is equal to the programmed value.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

Voltage Reference Temperature Coefficient (TC)
Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The voltage reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range, expressed in ppm/°C as follows:

$$TC = \left[\frac{V_{REFmax} - V_{REFmin}}{V_{REFnom} \times TempRange} \right] \times 10^6$$

where:
V_{REFmax} is the maximum reference output measured over the total temperature range.
V_{REFmin} is the minimum reference output measured over the total temperature range.
V_{REFnom} is the nominal reference output voltage, 5 V.
TempRange is the specified temperature range, −40°C to +85°C.

Reference Load Regulation
Load regulation is the change in reference output voltage due to a specified change in load current. It is expressed in ppm/mA.

THEORY OF OPERATION

The AD5410/AD5420 are precision digital-to-current loop output converters designed to meet the requirements of industrial process control applications. They provide a high precision, fully integrated, low cost single-chip solution for generating current loop outputs. The current ranges available are 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA. The desired output configuration is user selectable via the control register.

ARCHITECTURE

The DAC core architecture of the AD5410/AD5420 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 37. The four MSBs of the 12-bit or 16-bit data-word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either ground or the reference buffer output. The remaining 8/12 bits of the data-word drive Switch S0 to Switch S7 or Switch S0 to Switch S11 of an 8-/12-bit voltage mode R-2R ladder network.

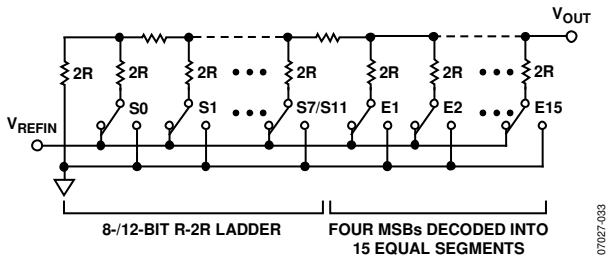


Figure 37. DAC Ladder Structure

The voltage output from the DAC core is converted to a current (see Figure 38) that is then mirrored to the supply rail so that the application simply sees a current source output with respect to ground.

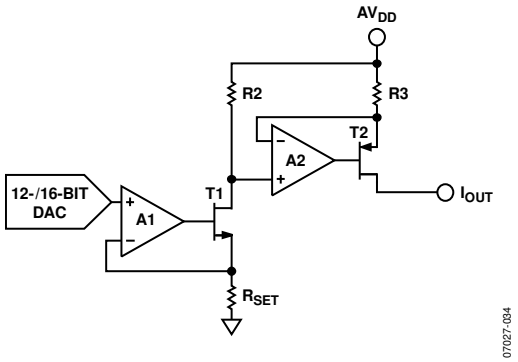


Figure 38. Voltage-to-Current Conversion Circuitry

SERIAL INTERFACE

The AD5410/AD5420 are controlled over a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz. They are compatible with SPI, QSPI, MICROWIRE, and DSP standards.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. Data is clocked in on the rising edge of SCLK. The input shift register consists of eight address bits and 16 data bits, as shown in Table 6. The 24-bit word is unconditionally latched on the rising edge of LATCH. Data continues to be clocked in irrespective of the state of LATCH. On the rising edge of LATCH, the data that is present in the input shift register is latched; that is, the last 24 bits to be clocked in before the rising edge of LATCH is the data that is latched. The timing diagram for this operation is shown in Figure 2.

Standalone Operation

The serial interface works with both a continuous and noncontinuous SCLK. A continuous SCLK source can be used only if LATCH is taken high after the correct number of data bits has been clocked in. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data. The first rising edge of SCLK that clocks in the MSB of the data-word marks the beginning of the write cycle. Exactly 24 rising clock edges must be applied to SCLK before LATCH is brought high. If LATCH is brought high before the 24th rising SCLK edge, the data written is invalid. If more than 24 rising SCLK edges are applied before LATCH is brought high, the input data is also invalid.

Table 6. Input Shift Register Format

MSB **LSB**

DB23 to DB16	DB15 to DB0
Address byte	Data-word

Table 7. Address Byte Functions

Address Byte	Function
00000000	No operation (NOP)
00000001	Data register
00000010	Readback register value as per read address (see Table 8)
01010101	Control register
01010110	Reset register

Daisy-Chain Operation

For systems that contain several devices, the SDO pin can be used to daisy-chain several devices together, as shown in Figure 39. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. Daisy-chain mode is enabled by setting the DCEN bit of the control register. The first rising edge of SCLK that clocks in the MSB of the data-word marks the beginning of the write cycle. SCLK is continuously applied to the input shift register. If more than 24 clock pulses are applied, the data ripples out of the input shift register and appears on the SDO line. This data, having been clocked out on the previous falling SCLK edge, is valid on the rising edge of SCLK. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses.

Therefore, the total number of clock cycles must equal 24 × N, where N is the total number of AD5410/AD5420 devices in the chain. When the serial transfer to all devices is complete, LATCH is taken high. This latches the input data in each device in the daisy chain. The serial clock can be a continuous or a gated clock.

A continuous SCLK source can be used only if LATCH is taken high after the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data. See Figure 4 for a timing diagram.

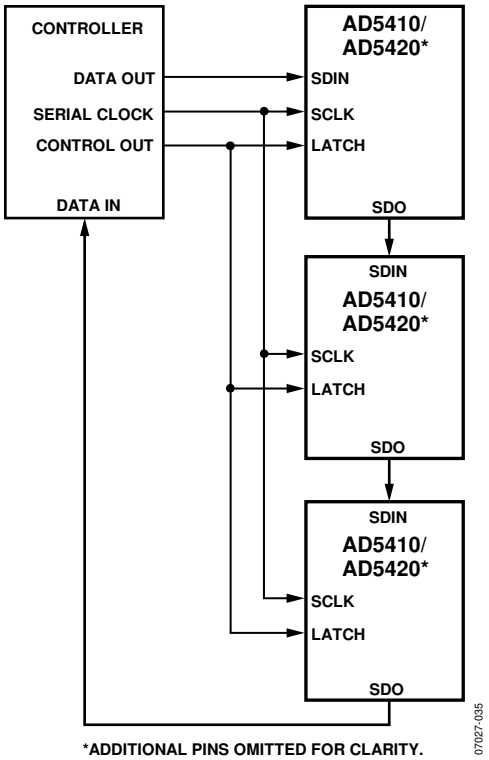


Figure 39. Daisy Chaining the AD5410/AD5420

Readback Operation

Readback mode is invoked by setting the address byte and read address as shown in Table 9 and Table 8 when writing to the input shift register. The next write to the AD5410/AD5420 should be a NOP command, which clocks out the data from the previously addressed register, as shown in Figure 3. By default, the SDO pin is disabled. After having addressed the AD5410/AD5420 for a read operation, a rising edge on LATCH enables the SDO pin in anticipation of data being clocked out. After the data has been clocked out on SDO, a rising edge on LATCH disables (tristate) the SDO pin once again. To read back the data register, for example, the following sequence should be implemented:

1. Write 0x020001 to the AD5410/AD5420 input shift register. This configures the part for read mode with the data register selected.
2. Follow this with a second write, a NOP condition, 0x000000. During this write, the data from the data register is clocked out on the SDO line.

Table 8. Read Address Decoding

Read Address	Function
00	Read status register
01	Read data register
10	Read control register

Table 9. Input Shift Register Contents for a Read Operation

MSB										LSB
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB2	DB1	DB0
0	0	0	0	0	0	1	0	X[1]	Read address	

[1] X = don't care.

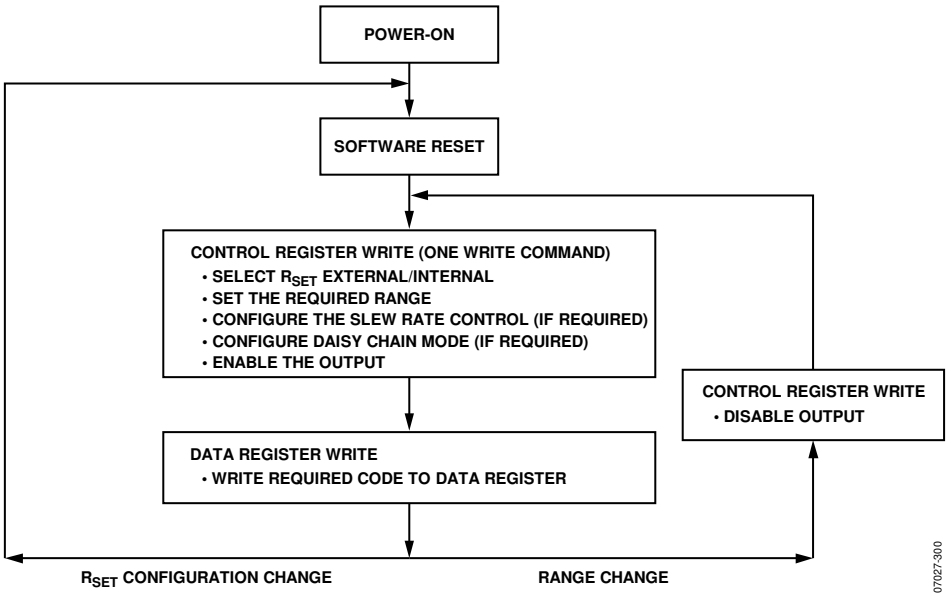


Figure 40. Programming Sequence to Write/Enable the Output Correctly

POWER-ON STATE

Upon power-on of the AD5410/AD5420, the power-on reset circuit ensures that all registers are loaded with zero code. As such, the output is disabled (tristate). Also upon power-on, internal calibration registers are read, and the data is applied to internal calibration circuitry. For a reliable read operation, there must be sufficient voltage on the AV_{DD} supply when the read event is triggered by the DV_{CC} power supply powering up. Powering up the DV_{CC} supply after the AV_{DD} supply has reached at least 5 V ensures this. If DV_{CC} and AV_{DD} are powered up simultaneously, then the supplies should be powered up at a rate greater than, typically, 5000 V/sec. If the internal DV_{CC} is enabled, the supplies should be powered up at a rate greater than, typically, 2000 V/sec. If this cannot be achieved, simply issue a reset command to the AD5410/AD5420 after power-on. This performs a power-on reset event, reading the calibration registers and ensuring specified operation of the AD5410/AD5420. To ensure correct calibration and to allow the internal reference to settle to its correct trim value, 40 µs should be allowed after a successful power on reset.

TRANSFER FUNCTION

For the 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA current output ranges, the output current is respectively expressed as

$$I_{OUT} = \left[\frac{20\text{ mA}}{2^N}\right] \times D$$

$$I_{OUT} = \left[\frac{24\text{ mA}}{2^N}\right] \times D$$

$$I_{OUT} = \left[\frac{16\text{ mA}}{2^N}\right] \times D + 4\text{ mA}$$

where:
D is the decimal equivalent of the code loaded to the DAC.
N is the bit resolution of the DAC.

DATA REGISTER

The data register is addressed by setting the address byte of the input shift register to 0x01. The data to be written to the data register is entered in Position DB15 to Position DB4 for the AD5410 and in Position DB15 to Position DB0 for the AD5420, as shown in Table 12 and Table 13, respectively.

CONTROL REGISTER

The control register is addressed by setting the address byte of the input shift register to 0x55. The data to be written to the control register is entered in Position DB15 to Position DB0, as shown in Table 14. The control register bit functions are described in Table 10.

Table 10. Control Register Bit Functions

Bit	Description
REXT	Setting this bit selects the external current setting resistor. See the AD5410/AD5420 Features section for further details. When using an external current setting resistor, it is recommended to only set REXT when also setting the OUTEN bit. Alternately, REXT can be set before the OUTEN bit is set, but the range (see Table 11) must be changed on the write in which the output is enabled. See Figure 40 for best practice.
OUTEN	Output enable. This bit must be set to enable the output.
SR Clock	Digital slew rate control. See the AD5410/AD5420 Features section.
SR Step	Digital slew rate control. See the AD5410/AD5420 Features section.
SREN	Digital slew rate control enable.
DCEN	Daisy-chain enable.
R2, R1, R0	Output range select. See Table 11.

Table 11. Output Range Options

R2	R1	R0	Output Range Selected
1	0	1	4 mA to 20 mA current range
1	1	0	0 mA to 20 mA current range
1	1	1	0 mA to 24 mA current range

Table 12. Programming the AD5410 Data Register

MSB															LSB
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
12-bit data-word												X[1]	X[1]	X[1]	X[1]

[1] X = don't care.

Table 13. Programming the AD5420 Data Register

MSB															LSB
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16-bit data-word															

Table 14. Programming the Control Register

MSB															LSB
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	REXT	OUTEN	SR clock				SR step			SREN	DCEN	R2	R1	R0

RESET REGISTER

The reset register is addressed by setting the address byte of the input shift register to 0x56. The reset register contains a single reset bit at Position DB0, as shown in Table 16. Writing a logic high to this bit performs a reset operation, restoring the part to its power-on state.

STATUS REGISTER

The status register is a read-only register. The status register bit functionality is shown in Table 15 and Table 17.

Table 15. Status Register Bit Functions

Bit	Description
I_{OUT} Fault	This bit is set if a fault is detected on the I_{OUT} pin.
Slew Active	This bit is set while the output value is slewing (slew rate control enabled).
Overtemp	This bit is set if the AD5410/AD5420 core temperature exceeds approximately 150°C.

Table 16. Programming the Reset Register

MSB															LSB
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Reserved															Reset

Table 17. Decoding the Status Register

MSB															LSB
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Reserved													I_{OUT} fault	Slew active	Overtemp

AD5410/AD5420 FEATURES

FAULT ALERT

The AD5410/AD5420 are equipped with a $\overline{\text{FAULT}}$ pin, which is an open-drain output allowing several AD5410/AD5420 devices to be connected together to one pull-up resistor for global fault detection. The $\overline{\text{FAULT}}$ pin is forced active by any one of the following fault scenarios:

- The voltage at I_{OUT} attempts to rise above the compliance range, due to an open-loop circuit or insufficient power supply voltage. The I_{OUT} current is controlled by a PMOS transistor and internal amplifier, as shown in Figure 38. The internal circuitry that develops the fault output avoids using a comparator with window limits because this requires an actual output error before the $\overline{\text{FAULT}}$ output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately 1 V of remaining drive capability (when the gate of the output PMOS transistor nearly reaches ground). Thus, the $\overline{\text{FAULT}}$ output activates slightly before the compliance limit is reached. Because the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open-loop gain and an output error does not occur before the $\overline{\text{FAULT}}$ output becomes active.
- If the core temperature of the AD5410/AD5420 exceeds approximately 150°C.

The I_{OUT} fault and overtemp bits of the status register are used in conjunction with the $\overline{\text{FAULT}}$ pin to inform the user which fault condition caused the $\overline{\text{FAULT}}$ pin to be asserted. See Table 17 and Table 15.

ASYNCHRONOUS CLEAR (CLEAR)

CLEAR is an active high clear that clears the current output to the bottom of its programmed range. It is necessary to maintain CLEAR high for a minimum amount of time (see Figure 2) to complete the operation. When the CLEAR signal is returned low, the output remains at the cleared value. The preclear value can be restored by pulsing the LATCH signal low without clocking any data. A new value cannot be programmed until the CLEAR pin is returned low.

INTERNAL REFERENCE

The AD5410/AD5420 contain an integrated +5 V voltage reference with initial accuracy of ±5 mV maximum and a temperature drift coefficient of 10 ppm/°C maximum. The reference voltage is buffered and externally available for use elsewhere within the system. See Figure 34 for a load regulation graph of the integrated reference.

EXTERNAL CURRENT SETTING RESISTOR

In Figure 38, R_{SET} is an internal sense resistor as part of the voltage-to-current conversion circuitry. The stability of the output current over temperature is dependent on the stability of the value of R_{SET}. An external precision 15 kΩ low drift resistor can be connected from the R_{SET} pin of the AD5410/AD5420 to ground; this improves the overall performance of the AD5410/AD5420. The external resistor is selected via the control register. See Table 14.

DIGITAL POWER SUPPLY

By default, the DV_{CC} pin accepts a power supply of 2.7 V to 5.5 V. Alternatively, via the DV_{CC} SELECT pin, an internal 4.5 V power supply can be output on the DV_{CC} pin for use as a digital power supply for other devices in the system or as a termination for pull-up resistors. This facility offers the advantage of not having to bring a digital supply across an isolation barrier. The internal power supply is enabled by leaving the DV_{CC} SELECT pin unconnected. To disable the internal supply, DV_{CC} SELECT should be tied to 0 V. DV_{CC} is capable of supplying up to 5 mA of current. See Figure 27 for a load regulation graph.

EXTERNAL BOOST FUNCTION

The addition of an external boost transistor, as shown in Figure 41, reduces the power dissipated in the AD5410/AD5420 by reducing the current flowing in the on-chip output transistor (dividing it by the current gain of the external circuit). A discrete NPN transistor with a breakdown voltage, BV_{CEO}, greater than 40 V can be used.

The external boost capability allows the AD5410/AD5420 to be used at the extremes of the supply voltage, load current, and temperature range. The boost transistor can also be used to reduce the amount of temperature-induced drift in the part. This minimizes the temperature-induced drift of the on-chip voltage reference, which improves drift and linearity.

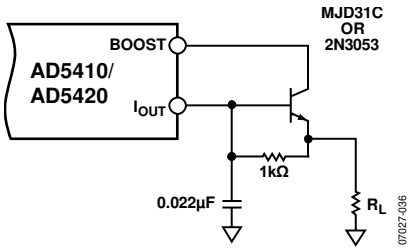


Figure 41. External Boost Configuration

HART COMMUNICATION

The AD5410/AD5420 contain a CAP2 pin, into which a HART signal can be coupled. The HART signal appears on the current output if the output is enabled. To achieve a 1 mA peak-to-peak current, the signal amplitude at the CAP2 pin must be 48 mV peak-to-peak. Assuming that the modem output amplitude is 500 mV peak-to-peak, its output must be attenuated by 500/48 = 10.42. If this voltage is used, the current output should meet the HART amplitude specifications. Figure 42 shows the recommended circuit for attenuating and coupling in the HART signal.

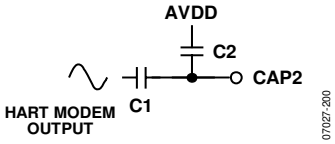


Figure 42. Coupling HART Signal

In determining the absolute values of the capacitors, ensure that the FSK output from the modem is passed undistorted. Thus, the bandwidth presented to the modem output signal must pass 1200 Hz and 2200 Hz frequencies. The recommended values are C1 = 2.2 nF and C2 = 22 nF. Digitally controlling the slew rate of the output is necessary to meet the analog rate of change requirements for HART.

DIGITAL SLEW RATE CONTROL

The slew rate control feature of the AD5410/AD5420 allows the user to control the rate at which the output current changes. With the slew rate control feature disabled, the output current changes at a rate of approximately 16 mA in 10 µs (see Figure 36). This varies with load conditions. To reduce the slew rate, enable the slew rate control feature. With the feature enabled via the SREN bit of the control register (see Table 14), the output, instead of slewing directly between two values, steps digitally at a rate defined by two parameters accessible via the control register, as shown in Table 14. The parameters are SR clock and SR step. SR clock defines the rate at which the digital slew is updated, SR step defines by how much the output value changes at each update. Both parameters together define the rate of change of the output current. Table 18 and Table 19 outline the range of values for both the SR clock and SR step parameters. Figure 43 shows the output current changing for ramp times of 10 ms, 50 ms, and 100 ms.

Table 18. Slew Rate Update Clock Values

SR Clock	Update Clock Frequency (Hz)
0000	257,730
0001	198,410
0010	152,440
0011	131,580
0100	115,740
0101	69,440
0110	37,590
0111	25,770
1000	20,160
1001	16,030
1010	10,290
1011	8280
1100	6900
1101	5530
1110	4240
1111	3300

Table 19. Slew Rate Step Size Options

SR Step	AD5410 Step Size (LSB)	AD5420 Step Size (LSB)
000	1/16	1
001	1/8	2
010	1/4	4
011	1/2	8
100	1	16
101	2	32
110	4	64
111	8	128

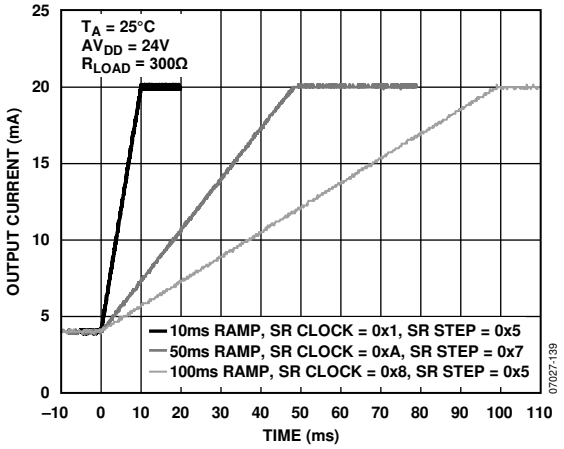


Figure 43. Output Current Slewing Under Control of the Digital Slew Rate Control Feature

The time it takes for the output current to slew over a given output range can be expressed as follows:

$$Slew\ Time = \frac{Output\ Change}{Step\ Size \times Update\ Clock\ Frequency \times LSB\ Size} \quad (1)$$

where:
Slew Time is expressed in seconds.
Output Change is expressed in amps.

When the slew rate control feature is enabled, all output changes change at the programmed slew rate. If the CLEAR pin is asserted, the output slews to the zero-scale value at the programmed slew rate. The output can be halted at its current value with a write to the control register. To avoid halting the output slew, the slew active bit can be read to check that the slew has completed before writing to any of the AD5410/AD5420 registers (see Table 17). The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range. Table 20 shows the range of programmable slew times for a full-scale change on any of the output ranges. The values in Table 20 were obtained using Equation 1. The digital slew rate control feature results in a staircase formation on the current output, as shown in Figure 47. Figure 47 also shows how the staircase can be removed by connecting capacitors to the CAP1 and CAP2 pins, as described in the I_{OUT} Filtering Capacitors section.

Table 20. Programmable Slew Time Values in Seconds for a Full-Scale Change on Any Output Range

	Step Size (LSBs)							
Update Clock Frequency (Hz)	**1**	**2**	**4**	**8**	**16**	**32**	**64**	**128**
257,730	0.25	0.13	0.06	0.03	0.016	0.008	0.004	0.0020
198,410	0.33	0.17	0.08	0.04	0.021	0.010	0.005	0.0026
152,440	0.43	0.21	0.11	0.05	0.027	0.013	0.007	0.0034
131,580	0.50	0.25	0.12	0.06	0.031	0.016	0.008	0.0039
115,740	0.57	0.28	0.14	0.07	0.035	0.018	0.009	0.0044
69,440	0.9	0.47	0.24	0.12	0.06	0.03	0.015	0.007
37,590	1.7	0.87	0.44	0.22	0.11	0.05	0.03	0.014
25,770	2.5	1.3	0.64	0.32	0.16	0.08	0.04	0.020
20,160	3.3	1.6	0.81	0.41	0.20	0.10	0.05	0.025
16,030	4.1	2.0	1.0	0.51	0.26	0.13	0.06	0.03
10,290	6.4	3.2	1.6	0.80	0.40	0.20	0.10	0.05
8280	7.9	4.0	2.0	1.0	0.49	0.25	0.12	0.06
6900	9.5	4.8	2.4	1.2	0.59	0.30	0.15	0.07
5530	12	5.9	3.0	1.5	0.74	0.37	0.19	0.09
4240	15	7.7	3.9	1.9	0.97	0.48	0.24	0.12
3300	20	9.9	5.0	2.5	1.24	0.62	0.31	0.16

I_{OUT} FILTERING CAPACITORS

Capacitors can be placed between CAP1 and AV_{DD}, and CAP2 and AV_{DD}, as shown in Figure 44.

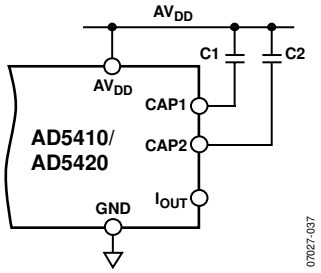


Figure 44. I_{OUT} Filtering Capacitors

The capacitors form a filter on the current output circuitry, as shown in Figure 45, reducing the bandwidth and the slew rate of the output current. Figure 46 shows the effect the capacitors have on the slew rate of the output current. To achieve significant reductions in the rate of change, very large capacitor values are required, which may not be suitable in some applications. In this case, the digital slew rate control feature should be used. The capacitors can be used in conjunction with the digital slew rate control feature as a means of smoothing out the steps caused by the digital code increments, as shown in Figure 47.

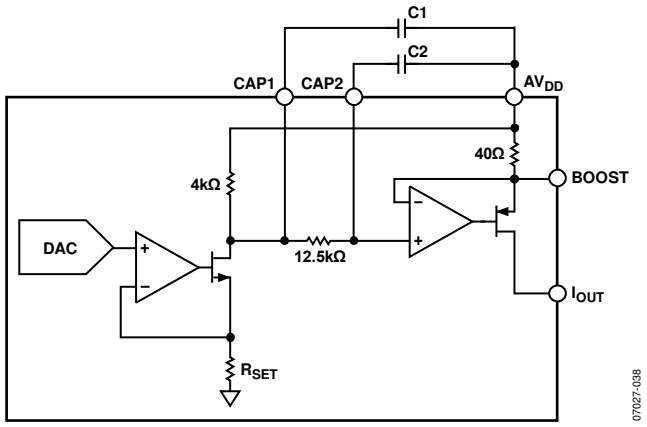


Figure 45. I_{OUT} Filter Circuitry

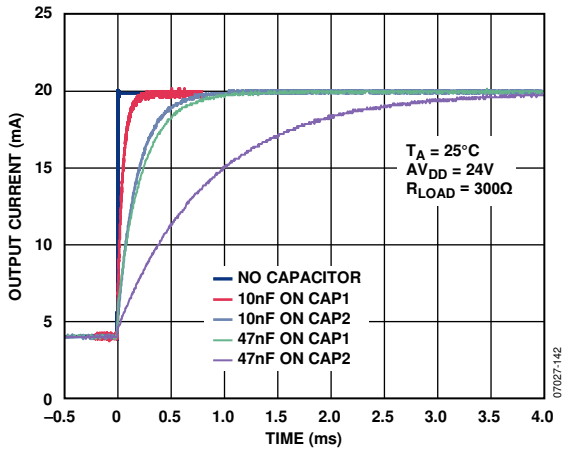


Figure 46. Slew Controlled 4 mA to 20 mA Output Current Step Using External Capacitors on the CAP1 and CAP2 Pins

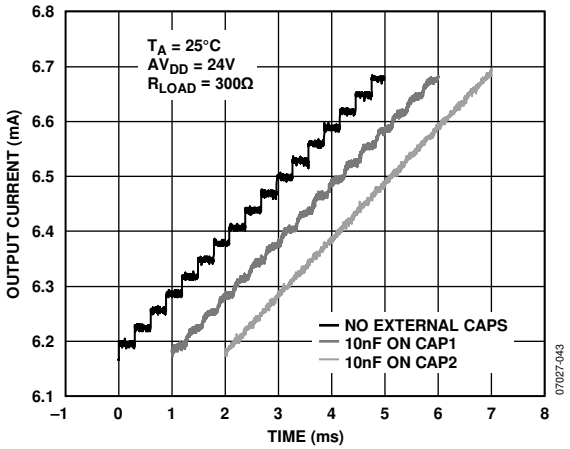


Figure 47. Smoothing Out the Steps Caused by the Digital Slew Rate Control Feature

FEEDBACK/MONITORING OF OUTPUT CURRENT

For feedback or monitoring of the output current value, a sense resistor can be placed in series with the I_{OUT} output pin and the voltage drop across it measured. As well as being an additional component, the resistor increases the compliance voltage required. An alternative method is to use a resistor that is already in place. R3 is such a resistor and is internal to the AD5410/AD5420, as shown in Figure 48. By measuring the voltage between the $R3_{SENSE}$ and BOOST pins, the value of the output current can be calculated as follows:

$$I_{OUT} = \frac{V_{R3}}{R3} - I_{BIAS} \quad (2)$$

where:

V_{R3} is the voltage drop across R3 measured between the $R3_{SENSE}$ and BOOST pins.

I_{BIAS} is a constant bias current flowing through R3 with a typical value of 444 µA.

R3 is the resistance value of resistor R3 with a typical value of 40 Ω.

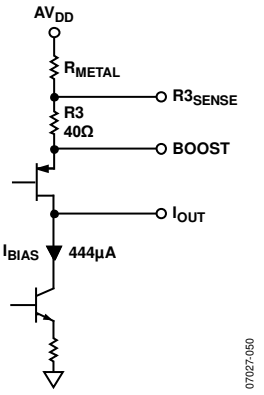


Figure 48. Structure of Current Output Circuit