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16-Bit, Serial Input, Loop-Powered, 4 mA to 20 mA DAC

Data Sheet **AD5421**

FEATURES

- 16-bit resolution and monotonicity
- Pin selectable NAMUR-compliant ranges
  - 4 mA to 20 mA
  - 3.8 mA to 21 mA
  - 3.2 mA to 24 mA
- NAMUR-compliant alarm currents
  - Downscale alarm current = 3.2 mA
  - Upscale alarm current = 22.8 mA/24 mA
- Total unadjusted error (TUE): 0.05% maximum
- INL error: 0.0035% FSR maximum
- Output TC: 3 ppm/°C typical
- Quiescent current: 300 µA maximum
- Flexible SPI-compatible serial digital interface with Schmitt triggered inputs
- On-chip fault alerts via FAULT pin or alarm current
- Automatic readback of fault register on each write cycle
- Slew rate control function
- Gain and offset adjust registers
- On-chip reference TC: 4 ppm/°C maximum
- Selectable regulated voltage output
- Loop voltage range: 5.5 V to 52 V
- Temperature range: −40°C to +105°C
- TSSOP and LFCSP packages

APPLICATIONS

- Industrial process control
- 4 mA to 20 mA loop-powered transmitters
- Smart transmitters
- HART network connectivity

GENERAL DESCRIPTION

The AD5421 is a complete, loop-powered, 4 mA to 20 mA digital-to-analog converter (DAC) designed to meet the needs of smart transmitter manufacturers in the industrial control industry. The DAC provides a high precision, fully integrated, low cost solution in compact TSSOP and LFCSP packages.

The AD5421 includes a regulated voltage output that is used to power itself and other devices in the transmitter. This regulator provides a regulated 1.8 V to 12 V output voltage. The AD5421 also contains 1.22 V and 2.5 V references, thus eliminating the need for a discrete regulator and voltage reference.

The AD5421 can be used with standard HART® FSK protocol communication circuitry without any degradation in specified performance. The high speed serial interface is capable of operating at 30 MHz and allows for simple connection to commonly used microprocessors and microcontrollers via a SPI-compatible, 3-wire interface.

The AD5421 is guaranteed monotonic to 16 bits. It provides 0.0015% integral nonlinearity, 0.0012% offset error, and 0.0006% gain error under typical conditions.

The AD5421 is available in a 28-lead TSSOP and a 32-lead LFCSP specified over the extended industrial temperature range of −40°C to +105°C.

COMPANION LOW POWER PRODUCTS

HART Modem: AD5700, AD5700-1
Microcontroller: ADuCM360

FUNCTIONAL BLOCK DIAGRAM

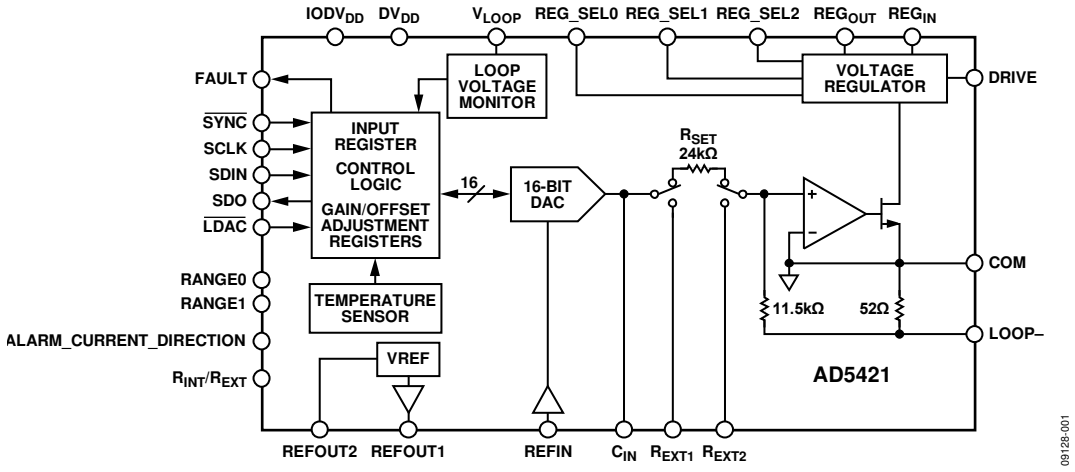

Figure 1.

Rev. H **Document Feedback**

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AD5421* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD5421 Evaluation Board

DOCUMENTATION

Application Notes

- AN-534: Adding HART® Capability to the AD421, Loop-Powered 4 mA–20 mA DAC Using the 20C15 HART Modem

User Guides

- UG-250: Evaluation Board for 16-Bit, Serial Input, Loop-Powered 4 mA to 20 mA DAC

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD5421 - Microcontroller No-OS Driver
- AD5421 IIO DAC Linux Driver
- AD5421 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design
- BeMicro FPGA Project for AD5421 with Nios driver

TOOLS AND SIMULATIONS

- AD5421 IBIS Model

REFERENCE DESIGNS

- CN0267
- CN0278
- CN0382

REFERENCE MATERIALS

Press

- Analog Devices' Analog Microcontroller with ARM Cortex M3 and Dual 24-Bit Sigma-delta A/D Converters Offers Highest Accuracy, Lowest Power
- Signal Chain Solution for 4-mA to 20-mA HART Enabled Field Instrument Applications

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

Technical Articles

- Design Trade-Offs for Loop-Powered Transmitters
- MS-2528: Power Consumption: A Primary Consideration in Smart Transmitter Design

DESIGN RESOURCES

- AD5421 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD5421 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

11/14—Rev. G to Rev. H

Changes to Offset Adjust Register Section and Gain Adjust Register Section 30

10/13—Rev. F to Rev. G

Added Figure 4; Renumbered Sequentially 10
Change to Table 7 11
Changes to Fault Alerts Section 21
Added Table 11; Renumbered Sequentially 24
Moved Figure 48 25
Changes to Applications Information Section 32
Changes to Figure 51 33

1/13—Rev. E to Rev. F

Moved Revision History Section 3
Change to Table 7 11
Changes to Table 8 13
Changes to On-Chip ADC Section 23
Changes to Table 19 and On-Chip ADC Transfer Function Equations Section 29

7/12—Rev. D to Rev. E

Changes to Figure 1 and Companion Products Section 1
Changes to Pin LOOP– Description 12
Changes to Applications Information Section and Figure 49 31
Added Figure 50 32

5/12—Rev. C to Rev. D

Changes to Features Section and Applications Section; Added Companion Products Section 1
Changes to Line Regulation Parameter, Table 1 5
Updated Outline Dimensions 33

12/11—Rev. B to Rev. C

Change to REFOUT1 Pin, Capacitive Load Parameter, Test Conditions, Table 1 4
Change to REGOUT Output, Capacitive Load Parameter, Test Conditions, Table 1 5
Changes to ESD Parameter, Table 6 10

12/11—Rev. A to Rev. B

Added 32-Lead LFCSP ..... Universal
Changes to the Specifications Section, Table 1 3
Changes to Table 7 10
Added Figure 5, Renumbered Sequentially 11
Changes to Table 8 11
Changes to Figure 33 17
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Changes to Figure 46 23
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Changes to the Register Readback Section 25
Updated Outline Dimensions 33
Changes to Ordering Guide 34

5/11—Rev. 0 to Rev. A

Changes to REGIN, REFOUT1, and REFOUT2 Pin Descriptions in Table 8 10
Change to Figure 45 22
Changes to Input Shift Register Section, Table 11, and Register Readback Section 24
Changes to Figure 48 30

2/11—Revision 0: Initial Version

SPECIFICATIONS

Loop voltage = 24 V; REFIN = 2.5 V external; R_L = 250 Ω; external NMOS connected; all loop current ranges; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY, INTERNAL R_{SET}					
Resolution	16			Bits	
Total Unadjusted Error (TUE)[2]	−0.126		+0.126	% FSR	C grade
	−0.041	±0.0064	+0.041	% FSR	C grade, T_A = 25°C
	−0.18		+0.18	% FSR	B grade
	−0.06	±0.011	+0.06	% FSR	B grade, T_A = 25°C
	−0.27		+0.27	% FSR	A grade
	−0.08	±0.011	+0.08		A grade, T_A = 25°C
TUE Long-Term Stability		210		ppm FSR	Drift after 1000 hours at T_A = 125°C
Relative Accuracy (INL)	−0.0035	±0.0015	+0.0035	% FSR	C grade
	−0.012	±0.006	+0.012	% FSR	B grade
	−0.024	±0.01	+0.024	% FSR	A grade
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.056		+0.056	% FSR	B grade and C grade
	−0.008	±0.0008	+0.008	% FSR	B grade and C grade, T_A = 25°C
	−0.11	±0.0008	+0.11	% FSR	A grade
Offset Error TC[3]		1		ppm FSR/°C	
Gain Error	−0.107		+0.107	% FSR	B grade and C grade
	−0.035	±0.0058	+0.035	% FSR	B grade and C grade, T_A = 25°C
	−0.2	±0.0058	+0.2	% FSR	A grade
Gain Error TC[3]		4		ppm FSR/°C	
Full-Scale Error	−0.126		+0.126	% FSR	B grade and C grade
	−0.041	±0.0065	+0.041	% FSR	B grade and C grade, T_A = 25°C
	−0.25	±0.0065	+0.25	% FSR	A grade
Full-Scale Error TC[3]		5		ppm FSR/°C	
Downscale Alarm Current	3.19		3.21	mA	
Upscale Alarm Current	22.77		22.83	mA	4 mA to 20 mA and 3.8 mA to 21 mA ranges
	23.97		24.03	mA	3.2 mA to 24 mA range
ACCURACY, EXTERNAL R_{SET} (24 kΩ)					Assumes ideal resistor, B grade and C grade only; not specified for A grade
Resolution	16			Bits	
Total Unadjusted Error (TUE)[2]	−0.048		+0.048	% FSR	C grade
	−0.027	±0.002	+0.027	% FSR	C grade, T_A = 25°C
	−0.08		+0.08	% FSR	B grade
	−0.04	±0.003	+0.04	% FSR	B grade, T_A = 25°C
TUE Long-Term Stability		40		ppm FSR	Drift after 1000 hours at T_A = 125°C
Relative Accuracy (INL)	−0.0035	±0.0015	+0.0035	% FSR	C grade
	−0.012	±0.006	+0.012	% FSR	B grade
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.021		+0.021	% FSR	
	−0.007	±0.0012	+0.007	% FSR	T_A = 25°C
Offset Error TC[3]		0.5		ppm FSR/°C	
Gain Error	−0.03		+0.03	% FSR	
	−0.023	±0.0006	+0.023	% FSR	T_A = 25°C

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Gain Error TC[3]		1		ppm FSR/°C	
Full-Scale Error	−0.047		+0.047	% FSR	
	−0.028	±0.0017	+0.028	% FSR	T_A = 25°C
Full-Scale Error TC[3]		1		ppm FSR/°C	
Downscale Alarm Current	3.08		3.21	mA	
Upscale Alarm Current	22.78		23	mA	4 mA to 20 mA and 3.8 mA to 21 mA ranges
	23.99		24.01	mA	3.2 mA to 24 mA range
OUTPUT CHARACTERISTICS[3]					
Loop Compliance Voltage[4]	LOOP− + 5.5			V	REG_{OUT} < 5.5 V, loop current = 24 mA
	LOOP− + 12.5			V	REG_{OUT} = 12 V, loop current = 24 mA
Loop Current Long-Term Stability		100		ppm FSR	Drift after 1000 hours at T_A = 125°C, loop current = 12 mA, internal R_{SET}
		15		ppm FSR	Drift after 1000 hours at T_A = 125°C, loop current = 12 mA, external R_{SET}
Loop Current Error vs. REG_{OUT} Load Current		1.2		µA/mA	Loop current = 12 mA, load current from REG_{OUT} = 5 mA
Resistive Load	0		2	kΩ	See Figure 21 for a load line graph
Inductive Load		50		mH	Stable operation
Power Supply Sensitivity			0.1	µA/V	Loop current = 12 mA
Output Impedance	12	400		MΩ	
Output TC		3		ppm FSR/°C	Loop current = 12 mA, internal R_{SET}
		1		ppm FSR/°C	Loop current = 12 mA, external R_{SET}
Output Noise					
0.1 Hz to 10 Hz		50		nA p-p	
500 Hz to 10 kHz		0.2		mV rms	HART bandwidth; measured across 500 Ω load
Noise Spectral Density		195		nA/√Hz	At 1 kHz
		256		nA/√Hz	At 10 kHz
REFERENCE INPUT (REFIN PIN)[3]					
Reference Input Voltage[5]		2.5		V	For specified performance
DC Input Impedance	75	800		MΩ	
REFERENCE OUTPUTS					
REFOUT1 Pin					
Output Voltage	2.498	2.5	2.503	V	T_A = 25°C
Temperature Coefficient		1.5	4	ppm/°C	C grade
		2	8	ppm/°C	B grade
		4	10	ppm/°C	A grade
Output Noise (0.1 Hz to 10 Hz)[3]		7.5		µV p-p	
Noise Spectral Density[3]		245		nV/√Hz	At 1 kHz
		70		nV/√Hz	At 10 kHz
Output Voltage Drift vs. Time[3]		200		ppm	Drift after 1000 hours at T_A = 125°C
Capacitive Load[3]		10		nF	Recommended operation
Load Current[3, 6]		4		mA	
Short-Circuit Current[3]		6.5		mA	Short circuit to COM
Power Supply Sensitivity[3]		2	12	µV/V	
Thermal Hysteresis[3]		285		ppm	First temperature cycle
		5		ppm	Second temperature cycle
Load Regulation[3]		0.1	0.2	mV/mA	Measured at 0 mA and 1 mA loads
Output Impedance		0.1		Ω	
REFOUT2 Pin					
Output Voltage	1.18	1.227	1.28	V	T_A = 25°C
Output Impedance		72		kΩ	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
REG_{OUT} OUTPUT					Voltage regulator output
Output Voltage	1.8		12	V	See Table 10
Output Voltage TC[3]		110		ppm/°C	
Output Voltage Accuracy	−4	±2	+4	%	
Externally Available Current[3, 6]	3.15			mA	Assuming 4 mA flowing in the loop and during HART communications
Short-Circuit Current		23		mA	
Line Regulation[3]		500		µV/V	Internal NMOS
		10		µV/V	External NMOS
Load Regulation[3]		8		mV/mA	
Inductive Load		50		mH	Stable operation
Capacitive Load	2	10		µF	Recommended operation
ADC ACCURACY					
Die Temperature		±5		°C	
V_{LOOP} Input		±1		%	
DV_{DD} OUTPUT					Can be overdriven up to 5.5 V
Output Voltage	3.17	3.3	3.48	V	
Externally Available Current[3, 6]	3.15			mA	Assuming 4 mA flowing in the loop and during HART communications
Short-Circuit Current		7.7		mA	
Load Regulation		45		mV/mA	Measured at 0 mA and 3 mA loads
DIGITAL INPUTS[3]					SCLK, $\overline{SYNC}$, SDIN, $\overline{LDAC}$
Input High Voltage, V_{IH}	$0.7 \times IODV_{DD}$			V	
Input Low Voltage, V_{IL}			$0.25 \times IODV_{DD}$	V	
Hysteresis		0.21		V	$IODV_{DD}$ = 1.8 V
		0.63		V	$IODV_{DD}$ = 3.3 V
		1.46		V	$IODV_{DD}$ = 5.5 V
Input Current	−0.015		+0.015	µA	Per pin
Pin Capacitance		5		pF	Per pin
DIGITAL OUTPUTS[3]					
SDO Pin					
Output Low Voltage, V_{OL}			0.4	V	
Output High Voltage, V_{OH}	$IODV_{DD} - 0.5$			V	
High Impedance Leakage Current	−0.01		+0.01	µA	
High Impedance Output Capacitance		5		pF	
FAULT Pin					
Output Low Voltage, V_{OL}			0.4	V	
Output High Voltage, V_{OH}	$IODV_{DD} - 0.5$			V	
FAULT THRESHOLDS					
I_{LOOP} Under		I_{LOOP} − 0.01% FSR		mA	
I_{LOOP} Over		I_{LOOP} + 0.01% FSR		mA	
Temp 140°C		133		°C	Fault removed when temperature ≤ 125°C
Temp 100°C		90		°C	Fault removed when temperature ≤ 85°C
V_{LOOP} 6V		0.3		V	Fault removed when $V_{LOOP} \geq 0.4$ V
V_{LOOP} 12V		0.6		V	Fault removed when $V_{LOOP} \geq 0.7$ V

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
REG_{IN}	5.5		52	V	With respect to LOOP−
$IODV_{DD}$	1.71		5.5	V	With respect to COM
Quiescent Current		260	300	μA	

[1] Temperature range: −40°C to +105°C; typical at +25°C.
[2] Total unadjusted error is the total measured error (offset error + gain error + linearity error + output drift over temperature) after factory calibration of the AD5421. System level total error can be reduced using the offset and gain registers.
[3] Guaranteed by design and characterization; not production tested.
[4] The voltage between LOOP− and REG_{IN} must be 5.5 V or greater.
[5] The AD5421 is factory calibrated with an external 2.5 V reference connected to REFIN.
[6] This is the current that the output is capable of sourcing. The load current originates from the loop and, therefore, contributes to the total current consumption figure.

Loop voltage = 24 V; REFIN = REFOUT1 (2.5 V internal reference); R_L = 250 Ω; external NMOS connected; all loop current ranges; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	C Grade				
Parameter[1, 2]	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
ACCURACY, INTERNAL R_{SET}					
Total Unadjusted Error (TUE)[3]	−0.157		+0.157	% FSR	
	−0.117	±0.0172	+0.117	% FSR	T_A = 25°C
Relative Accuracy (INL)	−0.004		+0.004	% FSR	
	−0.004	±0.0015	+0.004	% FSR	T_A = 25°C
Offset Error	−0.04		+0.04	% FSR	
	−0.025	±0.0025	+0.025	% FSR	T_A = 25°C
Offset Error TC		1		ppm FSR/°C	
Gain Error	−0.128		+0.128	% FSR	
	−0.093	±0.0137	+0.093	% FSR	T_A = 25°C
Gain Error TC		5		ppm FSR/°C	
Full-Scale Error	−0.157		+0.157	% FSR	
	−0.117	±0.0172	+0.117	% FSR	T_A = 25°C
Full-Scale Error TC		6		ppm FSR/°C	
ACCURACY, EXTERNAL R_{SET} (24 kΩ)					Assumes ideal resistor
Total Unadjusted Error (TUE)[3]	−0.133		+0.133	% FSR	
	−0.133	±0.0252	+0.133	% FSR	T_A = 25°C
Relative Accuracy (INL)	−0.004		+0.004	% FSR	
	−0.004	±0.0015	+0.004	% FSR	T_A = 25°C
Offset Error	−0.029		+0.029	% FSR	
	−0.029	±0.0038	+0.029	% FSR	T_A = 25°C
Offset Error TC		0.5		ppm FSR/°C	
Gain Error	−0.11		+0.11	% FSR	
	−0.106	±0.0197	+0.106	% FSR	T_A = 25°C
Gain Error TC		2		ppm FSR/°C	
Full-Scale Error	−0.133		+0.133	% FSR	
	−0.133	±0.0252	+0.133	% FSR	T_A = 25°C
Full-Scale Error TC		2		ppm FSR/°C	

[1] Temperature range: −40°C to +105°C; typical at +25°C.
[2] Specifications guaranteed by design and characterization; not production tested.
[3] Total unadjusted error is the total measured error (offset error + gain error + linearity error + output drift over temperature) after factory calibration of the AD5421. System level total error can be reduced using the offset and gain registers.

AC PERFORMANCE CHARACTERISTICS

Loop voltage = 24 V; REFIN = 2.5 V external; R_L = 250 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Loop Current Settling Time		50		µs	To 0.1% FSR, C_{IN} = open circuit
Loop Current Slew Rate		400		µA/µs	C_{IN} = open circuit
AC Loop Voltage Sensitivity		1.3		µA/V	1200 Hz to 2200 Hz, 5 V p-p, R_L = 3 kΩ

[1] Temperature range: −40°C to +105°C; typical at +25°C.

TIMING CHARACTERISTICS

Loop voltage = 24 V; REFIN = 2.5 V external; R_L = 250 Ω; all specifications T_{MIN} to T_{MAX}.

Table 4.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	17	ns min	SCLK high time
t_3	17	ns min	SCLK low time
t_4	17	ns min	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time
t_5	10	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_6	25	µs min	Minimum $\overline{\text{SYNC}}$ high time
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	25	µs min	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge
t_{10}	10	ns min	$\overline{\text{LDAC}}$ pulse width low
t_{11}	70	ns max	SCLK rising edge to SDO valid ($C_{L\ SDO}$ = 30 pF)
t_{12}	0	ns min	$\overline{\text{SYNC}}$ falling edge to SCLK rising edge setup time
t_{13}	70	ns max	$\overline{\text{SYNC}}$ rising edge to SDO tristate ($C_{L\ SDO}$ = 30 pF)

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.2 V.
[3] See Figure 2 and Figure 3.

Table 5. SPI Watchdog Timeout Periods

Parameter[1]						
T0	T1	T2	Min	Typ	Max	Unit
0	0	0	43	50	59	ms
0	0	1	87	100	117	ms
0	1	0	436	500	582	ms
0	1	1	873	1000	1163	ms
1	0	0	1746	2000	2326	ms
1	0	1	2619	3000	3489	ms
1	1	0	3493	4000	4652	ms
1	1	1	4366	5000	5814	ms

[1] Specifications guaranteed by design and characterization; not production tested.

Timing Diagrams

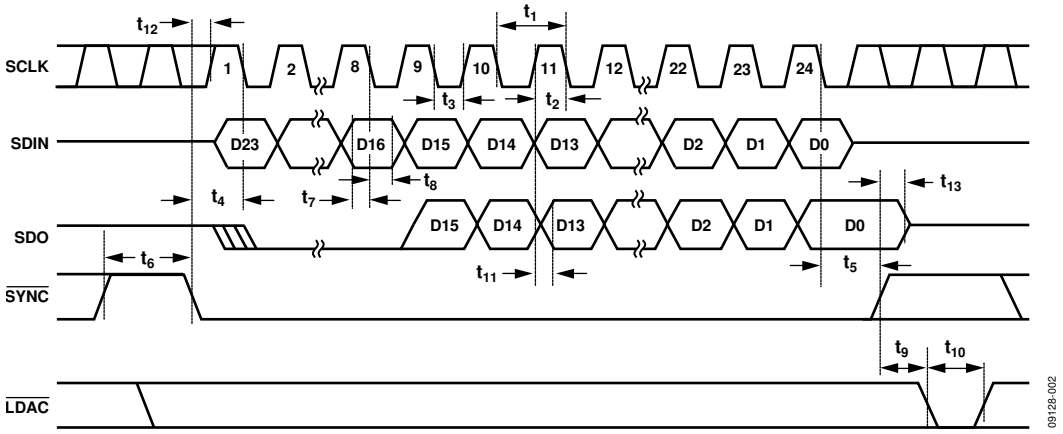

Figure 2. Serial Interface Timing Diagram

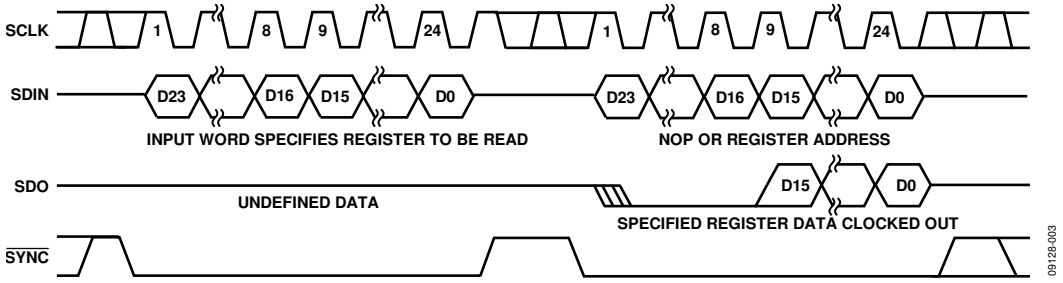

Figure 3. Readback Timing Diagram

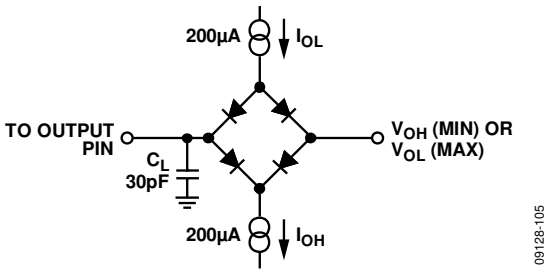

Figure 4. SDO Load Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 6.

Parameter	Rating
REG_{IN} to COM	−0.3 V to +60 V
REG_{OUT} to COM	−0.3 V to +14 V
Digital Inputs to COM, RANGE0, RANGE1, R_{INT}/R_{EXT}, ALARM_CURRENT_DIRECTION, REG_SEL0, REG_SEL1, REG_SEL2	−0.3 V to DV_{DD} + 0.3 V or +7 V (whichever is less)
Digital Inputs to COM SCLK, SDIN, $\overline{SYNC}$, $\overline{LDAC}$	−0.3 V to $IODV_{DD}$ + 0.3 V or +7 V (whichever is less)
Digital Outputs to COM, SDO, FAULT	−0.3 V to $IODV_{DD}$ + 0.3 V or +7 V (whichever is less)
REFIN to COM	−0.3 V to +7 V
REFOUT1, REFOUT2	−0.3 V to +4.7 V
V_{LOOP} to COM	−0.3 V to +60 V
LOOP− to COM	−5 V to +0.3 V
DV_{DD} to COM	−0.3 V to +7 V
$IODV_{DD}$ to COM	−0.3 V to +7 V
R_{EXT1}, C_{IN} to COM	−0.3 V to +4.3 V
R_{EXT2} to COM	−0.3 V to +0.3 V
DRIVE to COM	−0.3 V to +11 V
Operating Temperature Range (T_A)	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\,MAX}$)	125°C
Power Dissipation	$(T_{J\,MAX} - T_A)/\theta_{JA}$
Lead Temperature, Soldering (10 sec)	JEDEC Industry Standard J-STD-020
ESD	
Human Body Model	3 kV
Field Induced Charged Device Model	2 kV
Machine Model	200 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
28-Lead TSSOP_EP (RE-28-2)	32	9	°C/W
32-Lead LFCSP_WQ (CP-32-11)	40	7	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

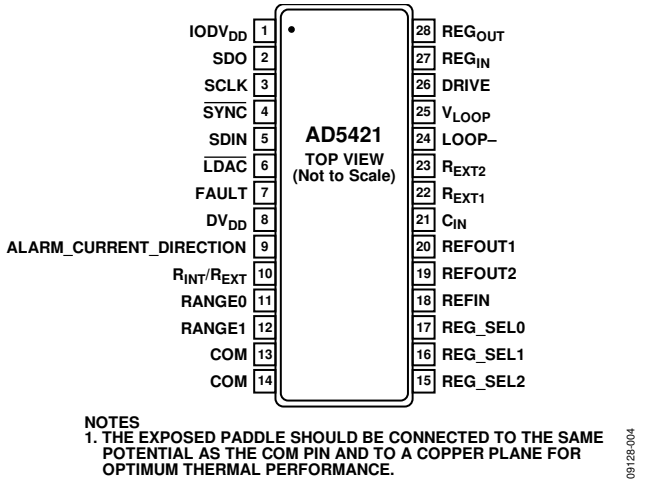

Figure 5. TSSOP Pin Configuration

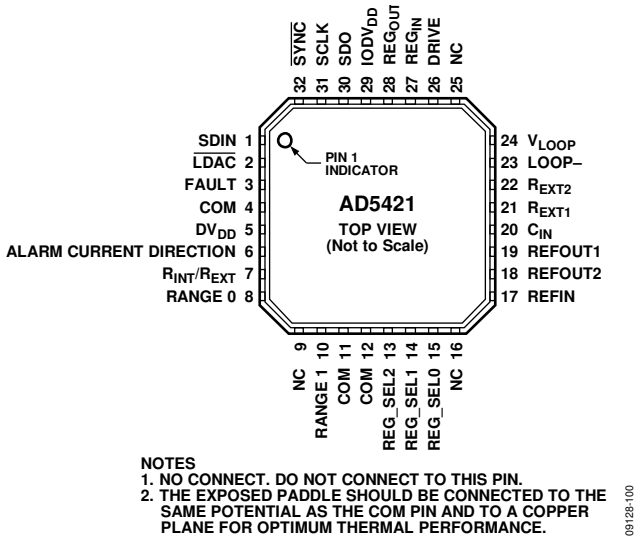

Figure 6. LFCSP Pin Configuration

Table 8. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	29	$IODV_{DD}$	Digital Interface Supply Pin. Digital thresholds are referenced to the voltage applied to this pin. A voltage from 1.71 V to 5.5 V can be applied to this pin.
2	30	SDO	Serial Data Output. Used to clock data from the input shift register. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
3	31	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This input operates at clock speeds up to 30 MHz.
4	32	$\overline{SYNC}$	Frame Synchronization Input, Active Low. This is the frame synchronization signal for the serial interface. When $\overline{SYNC}$ is low, data is transferred on the falling edge of SCLK. The input shift register data is latched on the rising edge of $\overline{SYNC}$.
5	1	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
6	2	$\overline{LDAC}$	Load DAC Input, Active Low. This pin is used to update the DAC register and, consequently, the output current. If $\overline{LDAC}$ is tied permanently low, the DAC register is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle, the input register is updated, but the output update is delayed until the falling edge of $\overline{LDAC}$. The $\overline{LDAC}$ pin should not be left unconnected.
7	3	FAULT	Fault Alert Output Pin, Active High. This pin is asserted high when a fault is detected. Detectable faults are loss of SPI interface control, communication error (PEC), loop current out of range, insufficient loop voltage, and overtemperature. For more information, see the Fault Alerts section.
8	5	DV_{DD}	3.3 V Digital Power Supply Output. This pin should be decoupled to COM with 100 nF and 4.7 µF capacitors.
9	6	ALARM_ CURRENT_ DIRECTION	Alarm Current Direction Select. This pin is used to select whether the alarm current is upscale (22.8 mA/24 mA) or downscale (3.2 mA). Connecting this pin to DV_{DD} selects an upscale alarm current (22.8 mA/24 mA); connecting this pin to COM selects a downscale alarm current (3.2 mA). For more information, see the Power-On Default section.
10	7	R_{INT}/R_{EXT}	Current Setting Resistor Select. When this pin is connected to DV_{DD}, the internal current setting resistor is selected. When this pin is connected to COM, the external current setting resistor is selected. An external resistor can be connected between the R_{EXT1} and R_{EXT2} pins.
11, 12	8, 10	RANGE0, RANGE1	Digital Input Pins. These two pins select the loop current range (see the Loop Current Range Selection section).

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
13, 14	4, 11, 12	COM	Ground Reference Pin for the AD5421. It is recommended that a 4.7 V Zener diode be placed between the LOOP− and COM pins. See the Applications Information section for more information.
15, 16, 17	13, 14, 15	REG_SEL2, REG_SEL1, REG_SEL0	These three pins together select the regulator output (REG_{OUT}) voltage (see the Voltage Regulator section).
18	17	REFIN	Reference Voltage Input. V_{REFIN} = 2.5 V for specified performance.
19	18	REFOUT2	Internal Reference Voltage Output (1.22 V). It is recommended to connect a 100 nF capacitor from this pin to COM.
20	19	REFOUT1	Internal Reference Voltage Output (2.5 V). It is recommended to connect a 100 nF capacitor from this pin to COM.
21	20	C_{IN}	External Capacitor Connection and HART FSK Input. An external capacitor connected from C_{IN} to COM implements an output slew rate control function (see the Loop Current Slew Rate Control section). HART FSK signaling can also be coupled through a capacitor to this pin (see the HART Communications section).
22, 23	21, 22	R_{EXT1}, R_{EXT2}	Connection for External Current Setting Resistor. A precision 24 kΩ resistor can be connected between these pins for improved performance.
24	23	LOOP−	Loop Current Return Pin. As shown in Figure 1, the COM and LOOP− pins can be used to sense the loop current across the internal 52 Ω resistor. Note that the voltage measured at LOOP− will be negative with respect to COM.
25	23	V_{LOOP}	Voltage Input Pin. Voltage input range is 0 V to 2.5 V. The voltage applied to this pin is digitized to eight bits, which are available in the fault register. This pin can be used for general-purpose voltage monitoring, but it is intended for monitoring of the loop supply voltage. Connecting the loop voltage to this pin via a 20:1 resistor divider allows the AD5421 to monitor and feedback the loop voltage. The AD5421 also generates an alert if the loop voltage is close to the minimum operating value (see the Loop Voltage Fault section).
26	26	DRIVE	Gate Connection for External Depletion Mode MOSFET. For more information, see the Connection to Loop Power Supply section.
27	27	REG_{IN}	Voltage Regulator Input. The loop voltage can be connected directly to this pin. Or, to reduce on-chip power dissipation, an external pass transistor can be connected at this pin to stand off the loop voltage. For more information, see the Connection to Loop Power Supply section.
28	28	REG_{OUT}	Voltage Regulator Output. Pin selectable values are from 1.8 V to 12 V via the REG_SEL0, REG_SEL1, and REG_SEL2 pins (see the Voltage Regulator section). If REGOUT is driving a microconverter supply (see Figure 50), this pin should be decoupled to COM with a >1 µF capacitor.
N/A[1]	9, 16, 25	NC	No Connect. Do not connect to this pin.
EPAD	EPAD	Exposed Pad	The exposed paddle should be connected to the same potential as the COM pin and to a copper plane for optimum thermal performance.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

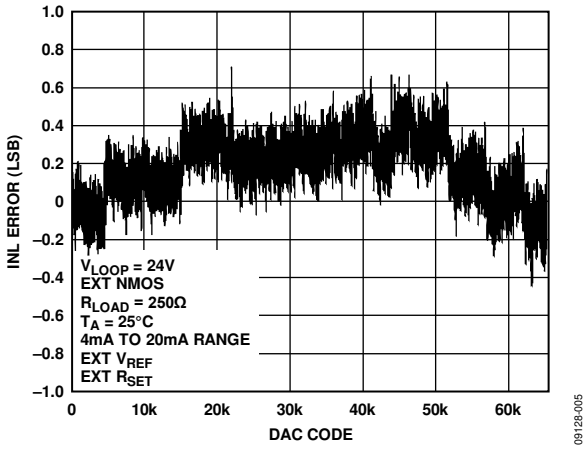

Figure 7. Integral Nonlinearity Error vs. Code

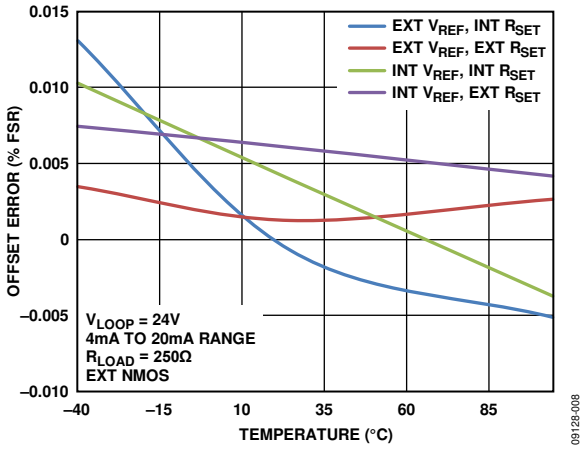

Figure 10. Offset Error vs. Temperature

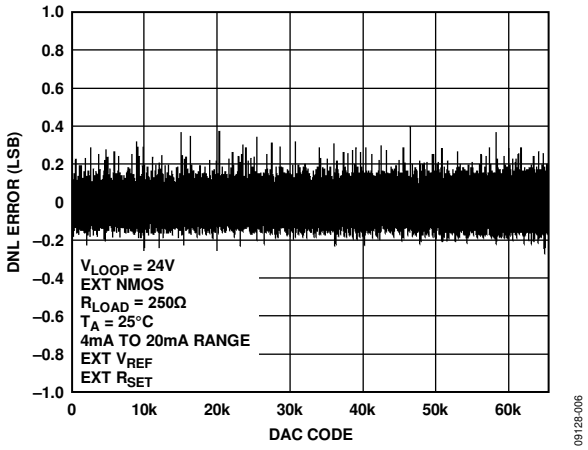

Figure 8. Differential Nonlinearity Error vs. Code

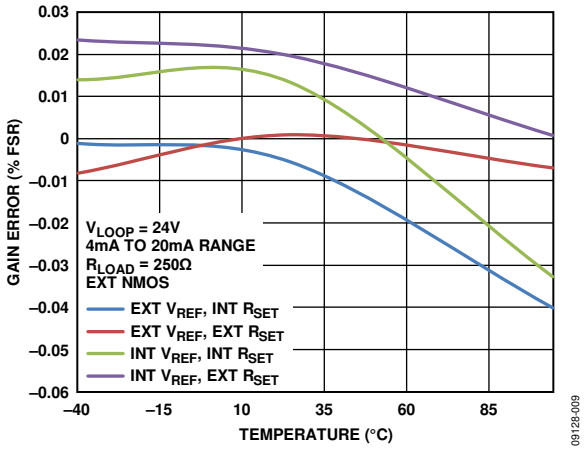

Figure 11. Gain Error vs. Temperature

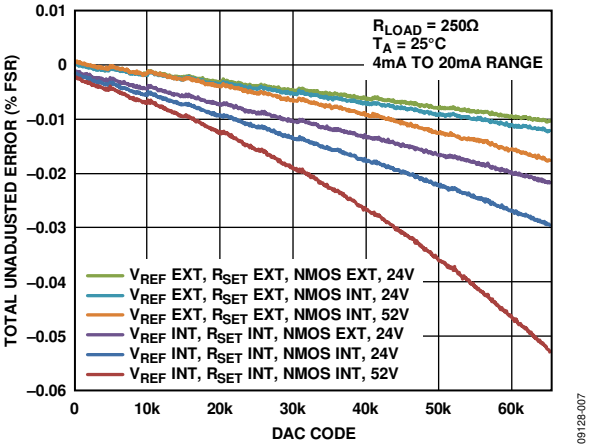

Figure 9. Total Unadjusted Error vs. Code

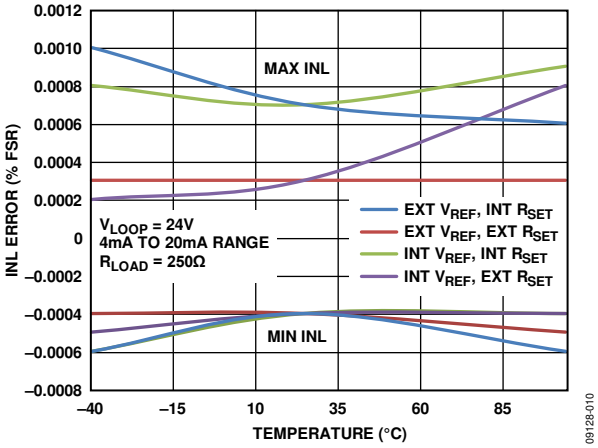

Figure 12. Integral Nonlinearity Error vs. Temperature

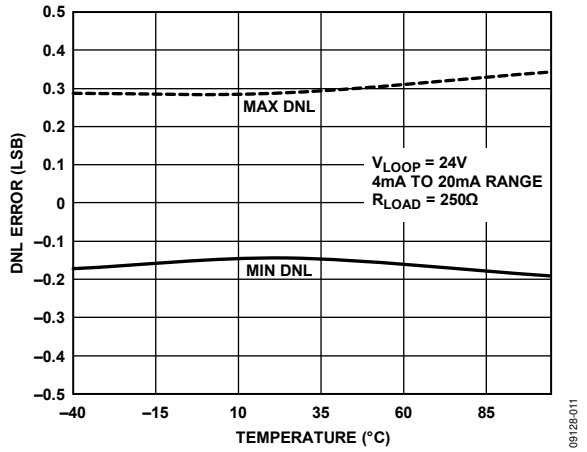

Figure 13. Differential Nonlinearity Error vs. Temperature

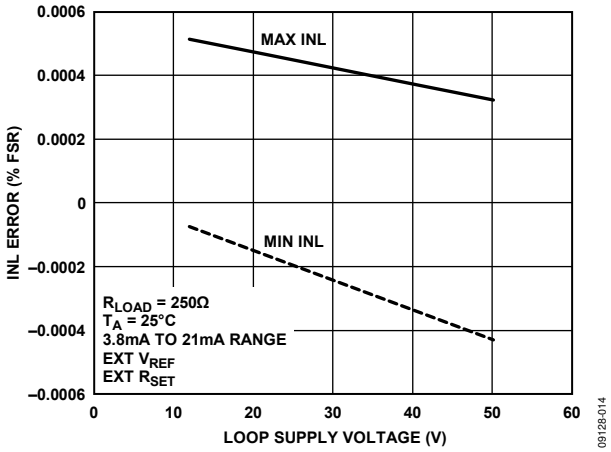

Figure 16. Integral Nonlinearity Error vs. Loop Supply Voltage

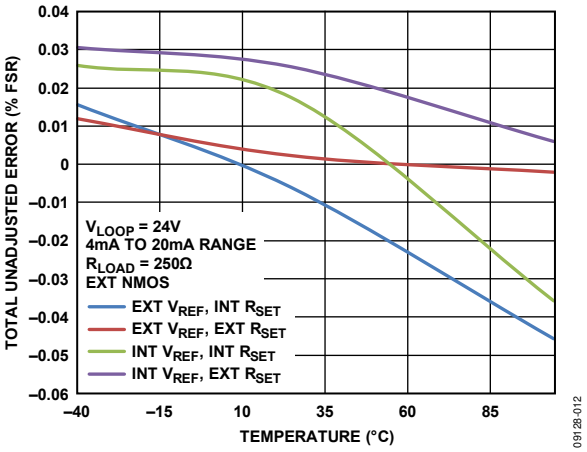

Figure 14. Total Unadjusted Error vs. Temperature

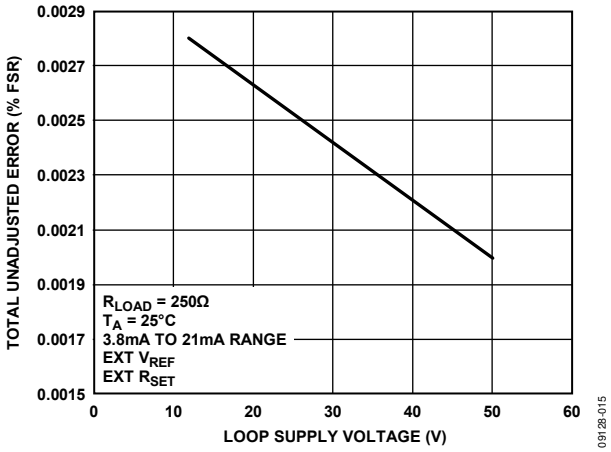

Figure 17. Total Unadjusted Error vs. Loop Supply Voltage

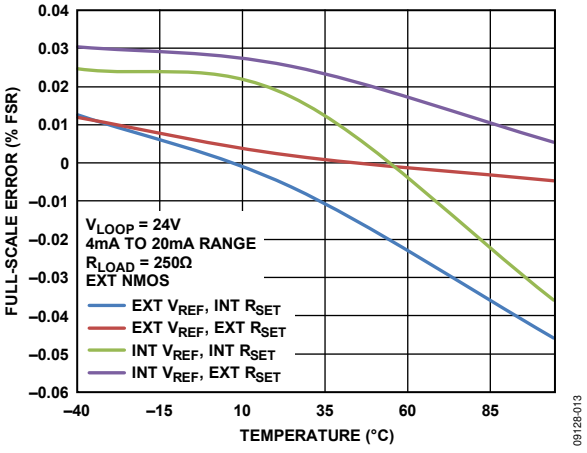

Figure 15. Full-Scale Error vs. Temperature

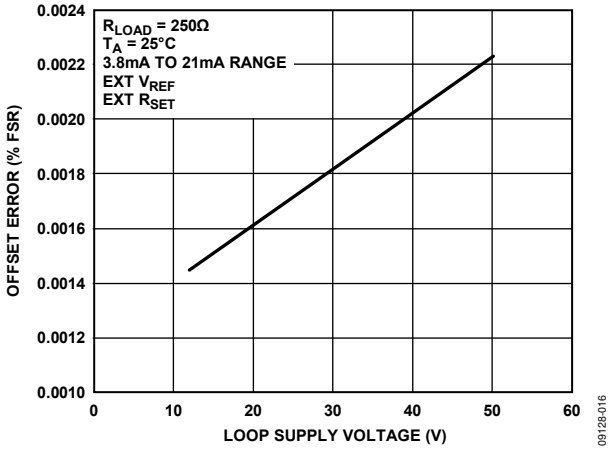

Figure 18. Offset Error vs. Loop Supply Voltage

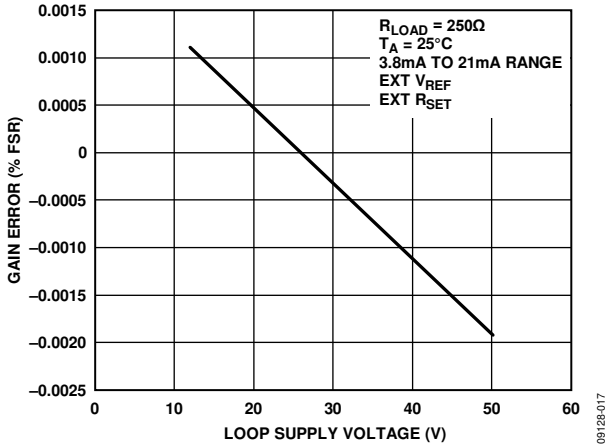

Figure 19. Gain Error vs. Loop Supply Voltage

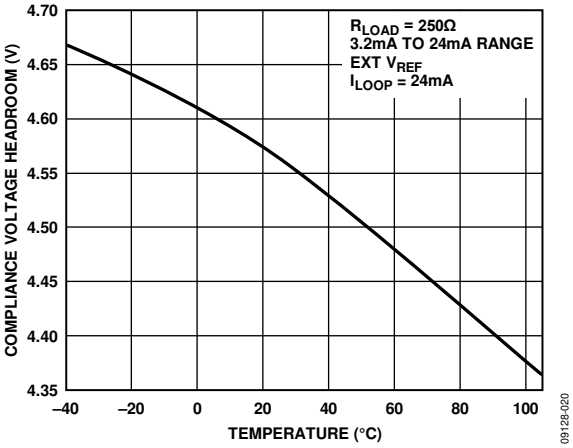

Figure 22. Compliance Voltage Headroom vs. Temperature

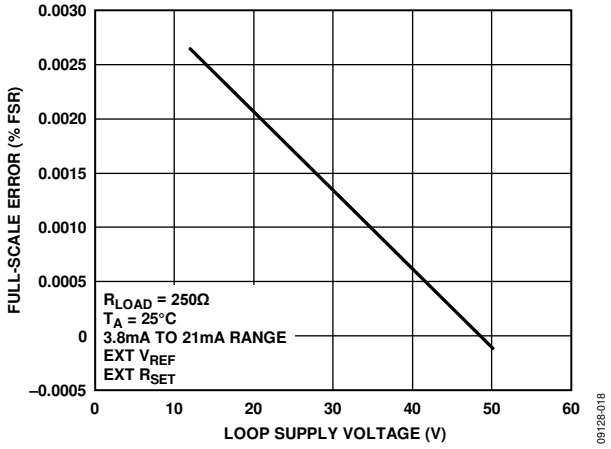

Figure 20. Full-Scale Error vs. Loop Supply Voltage

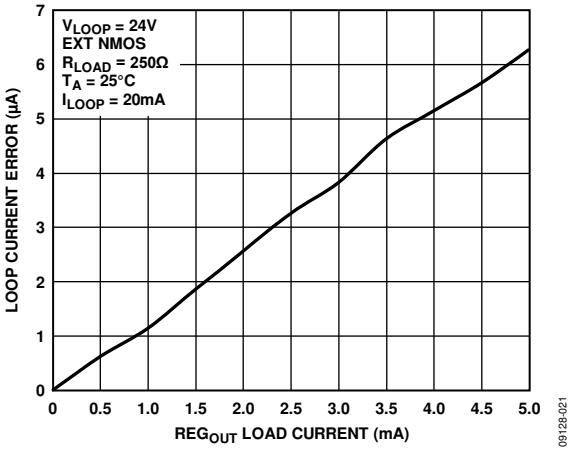

Figure 23. Loop Current Error vs. REG_{OUT} Load Current

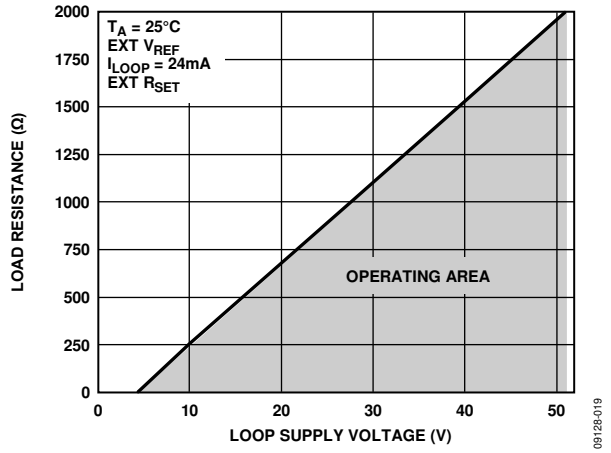

Figure 21. Load Resistance Load Line vs. Loop Supply Voltage (Voltage Between LOOP– and REG_{IN})

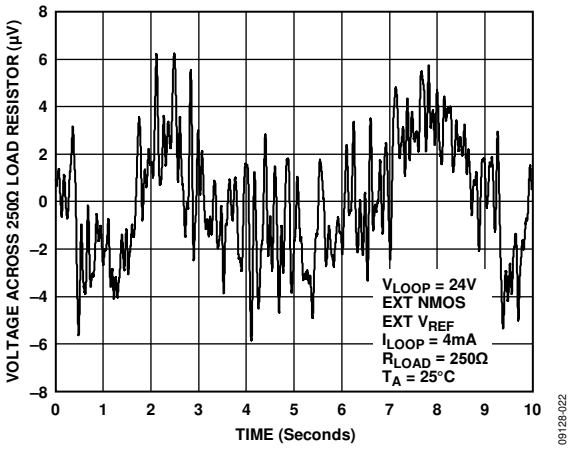

Figure 24. Loop Current Noise, 0.1 Hz to 10 Hz Bandwidth

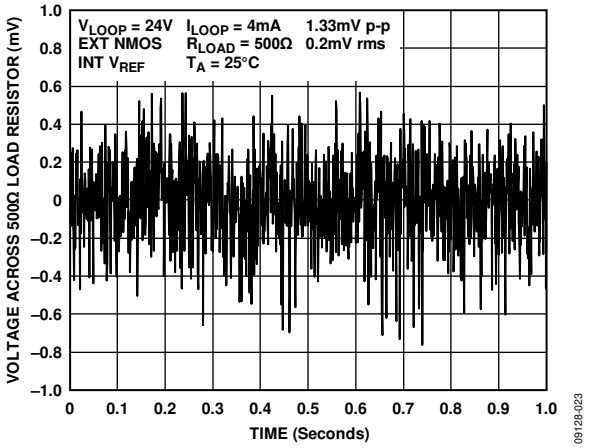

Figure 25. Loop Current Noise, 500 Hz to 10 kHz Bandwidth (HART Bandwidth)

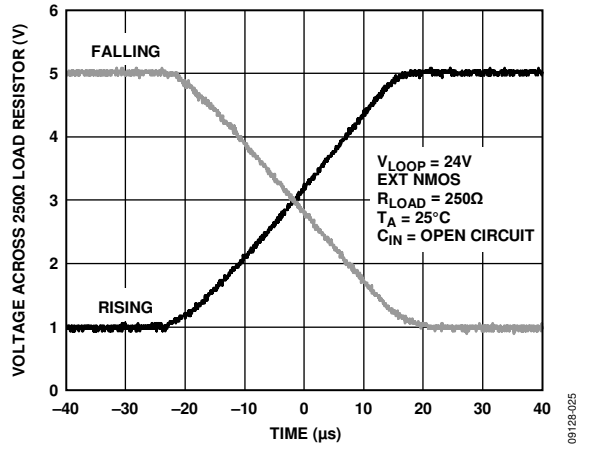

Figure 26. Full-Scale Loop Current Step

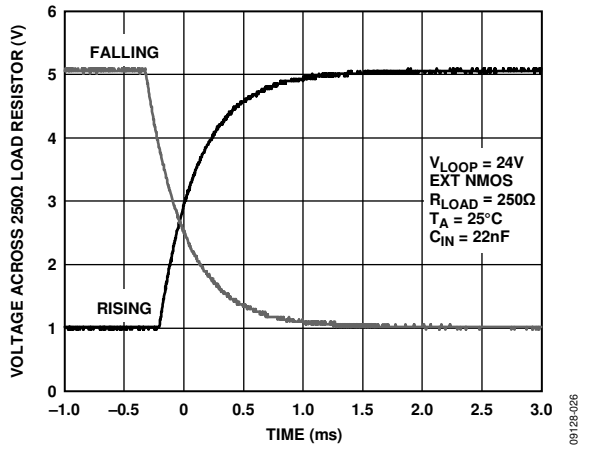

Figure 27. Full-Scale Loop Current Step, C_{IN} = 22 nF

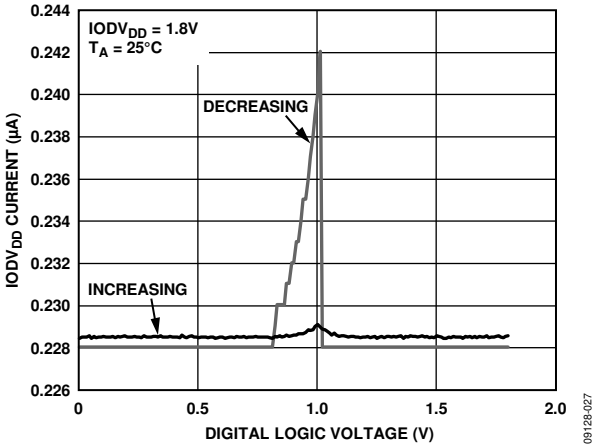

Figure 28. $IODV_{DD}$ Current vs. Digital Logic Voltage, Increasing and Decreasing, $IODV_{DD}$ = 1.8 V

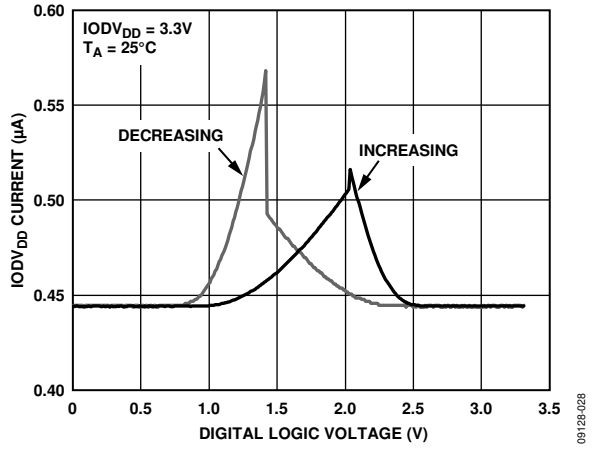

Figure 29. $IODV_{DD}$ Current vs. Digital Logic Voltage, Increasing and Decreasing, $IODV_{DD}$ = 3.3 V

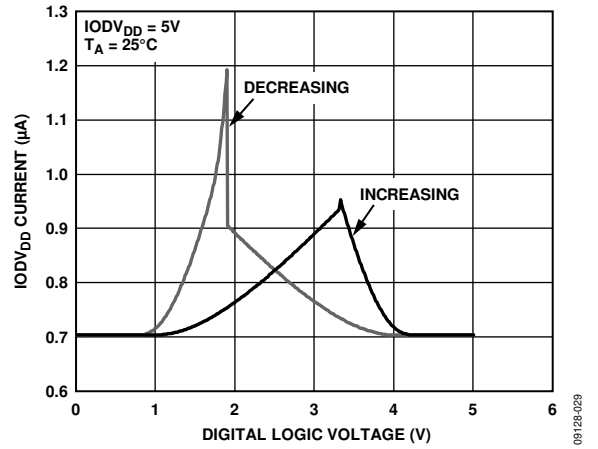

Figure 30. $IODV_{DD}$ Current vs. Digital Logic Voltage, Increasing and Decreasing, $IODV_{DD}$ = 5 V

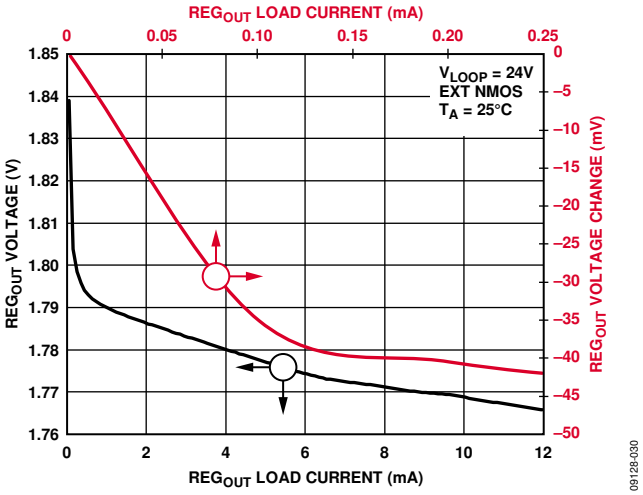

Figure 31. REG_{OUT} Voltage vs. Load Current

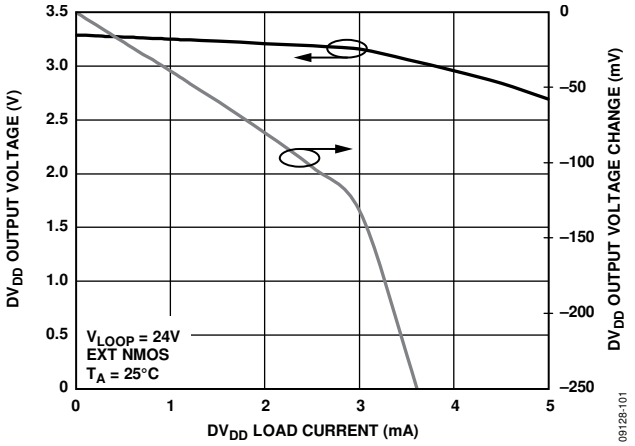

Figure 34. DV_{DD} Output Voltage vs. Load Current

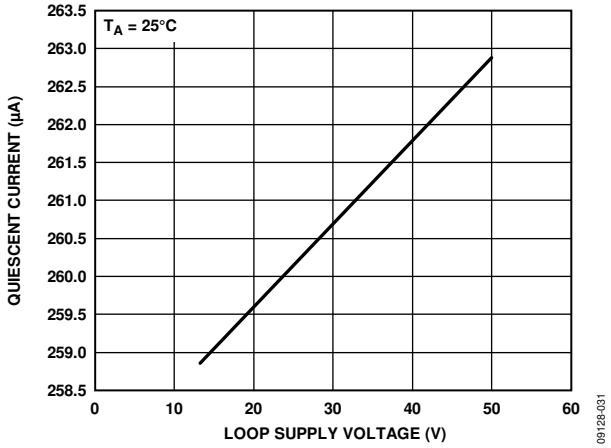

Figure 32. Quiescent Current vs. Loop Supply Voltage

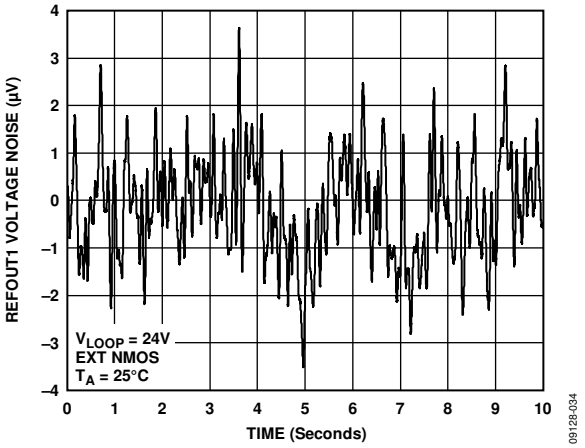

Figure 35. REFOUT1 Voltage Noise, 0.1 Hz to 10 Hz Bandwidth

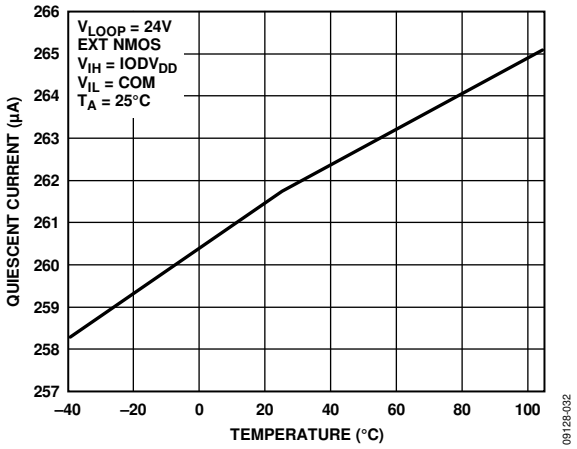

Figure 33. Quiescent Current vs. Temperature

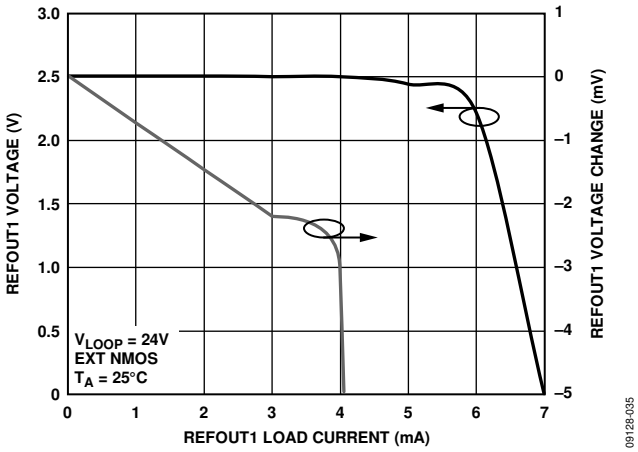

Figure 36. REFOUT1 Voltage vs. Load Current

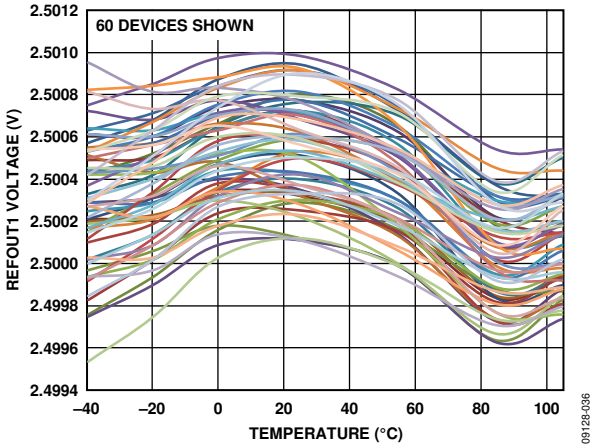

Figure 37. REFOUT1 Voltage vs. Temperature, 60 Devices Shown (C Grade Device)

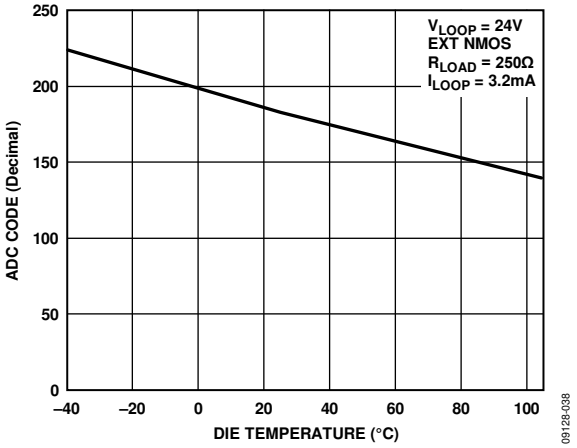

Figure 39. On-Chip ADC Code vs. Die Temperature

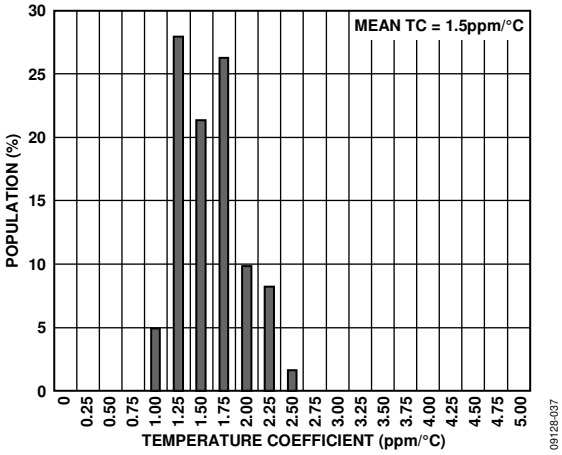

Figure 38. REFOUT1 Temperature Coefficient Histogram (C Grade Device)

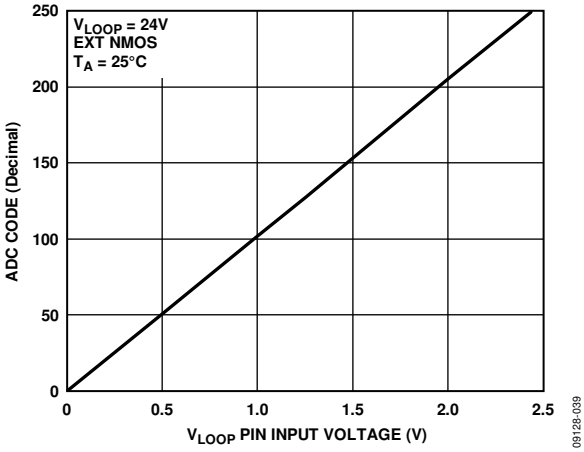

Figure 40. On-Chip ADC Code vs. V_{LOOP} Pin Input Voltage

TERMINOLOGY

Total Unadjusted Error
Total unadjusted error (TUE) is a measure of the total output error. TUE consists of INL error, offset error, gain error, and output drift over temperature, in the case of maximum TUE. TUE is expressed in % FSR.

Relative Accuracy or Integral Nonlinearity (INL) Error
Relative accuracy, or integral nonlinearity (INL) error, is a measure of the maximum deviation in the output current from a straight line passing through the endpoints of the transfer function. INL error is expressed in % FSR.

Differential Nonlinearity (DNL) Error
Differential nonlinearity (DNL) error is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Offset Error
Offset error is a measure of the output error when zero code is loaded to the DAC register and is expressed in % FSR.

Offset Error Temperature Coefficient (TC)
Offset error TC is a measure of the change in offset error with changes in temperature and is expressed in ppm FSR/°C.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer function from the ideal and is expressed in % FSR.

Gain Error Temperature Coefficient (TC)
Gain error TC is a measure of the change in gain error with changes in temperature and is expressed in ppm FSR/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code is loaded to the DAC register and is expressed in % FSR.

Full-Scale Error Temperature Coefficient (TC)
Full-scale error TC is a measure of the change in full-scale error with changes in temperature and is expressed in ppm FSR/°C.

Loop Compliance Voltage Headroom
Loop compliance voltage headroom is the minimum voltage between the LOOP− and REG_{IN} pins for which the output current is equal to the programmed value.

Output Temperature Coefficient (TC)
Output TC is a measure of the change in the output current at 12 mA with changes in temperature and is expressed in ppm FSR/°C.

Voltage Reference Thermal Hysteresis
Voltage reference thermal hysteresis is the difference in output voltage measured at +25°C compared to the output voltage measured at +25°C after cycling the temperature from +25°C to −40°C to +105°C and back to +25°C. The hysteresis is specified for the first and second temperature cycles and is expressed in mV.

Voltage Reference Temperature Coefficient (TC)
Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The voltage reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output voltage over a given temperature range. Voltage reference TC is expressed in ppm/°C as follows:

$$TC = \left(\frac{V_{REF\_MAX} - V_{REF\_MIN}}{V_{REF\_NOM} \times Temp\_Range} \right) \times 10^6$$

where:
V_{REF_MAX} is the maximum reference output voltage measured over the total temperature range.
V_{REF_MIN} is the minimum reference output voltage measured over the total temperature range.
V_{REF_NOM} is the nominal reference output voltage, 2.5 V.
Temp_Range is the specified temperature range (−40°C to +105°C).

THEORY OF OPERATION

The AD5421 is an integrated device designed for use in loop-powered, 4 mA to 20 mA smart transmitter applications. In a single chip, the AD5421 provides a 16-bit DAC and current amplifier for digital control of the loop current, a voltage regulator to power the entire transmitter, a voltage reference, fault alert functions, a flexible SPI-compatible serial interface, gain and offset adjust registers, as well as other features and functions. The features of the AD5421 are described in the following sections.

FAULT ALERTS

The AD5421 provides a number of fault alert features. All faults are signaled to the controller via the FAULT pin and the fault register. In the case of a loss of communication between the AD5421 and the microcontroller (SPI fault), the AD5421 programs the loop current to an alarm value. If the controller detects that the FAULT pin is set high, it should then read the fault register to determine the cause of the fault. Note that the watchdog timer does not reset and restart its condition with an alarm active. If the auto fault readback is disabled and an SPI fault occurs, such that the watchdog timer is timed out, the watchdog timer remains inactive until the status register is manually read back by the user. Following this readback, the watchdog timer resumes operation.

SPI Fault

The SPI fault is asserted if there is no valid communication to any register of the AD5421 for more than a user-defined period. The user can program the time period using the SPI watchdog timeout bits of the control register. The SPI fault bit of the fault register indicates the fault on the SPI bus. Because this fault is caused by a loss of communication between the controller and the AD5421, the loop current is also forced to the alarm value.

The direction of the alarm current (downscale or upscale) is selected via the ALARM_CURRENT_DIRECTION pin. Connecting this pin to DV_{DD} selects an upscale alarm current (22.8 mA/24 mA); connecting this pin to COM selects a downscale alarm current (3.2 mA).

Packet Error Checking

To verify that data has been received correctly in noisy environments, the AD5421 offers the option of error checking based on an 8-bit cyclic redundancy check (CRC). Packet error checking (PEC) is enabled by writing to the AD5421 with a 32-bit serial frame, where the least significant eight bits are the frame check sequence (FCS). The device controlling the AD5421 should generate the 8-bit FCS using the following polynomial:

$$C(x) = x^8 + x^2 + x + 1$$

The 8-bit FCS is appended to the end of the data-word, and 32 data bits are sent to the AD5421 before $\overline{SYNC}$ is taken high. If the check is valid, the data is accepted. If the check fails, the FAULT pin is asserted and the PEC bit of the fault register is set. After the fault register is read, the PEC bit is reset low and the FAULT pin returns low.

In the case of data readback, if the AD5421 is addressed with a 32-bit frame, it generates the 8-bit frame check sequence and appends it to the end of the 24-bit data stream to create a 32-bit data stream.

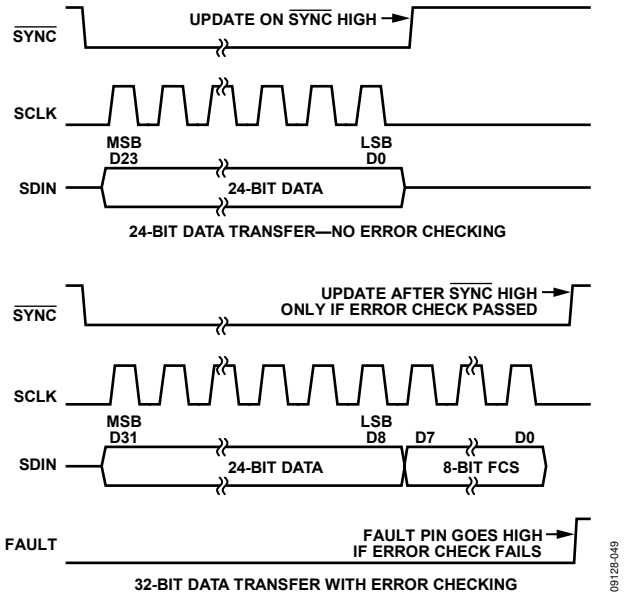

Figure 41. PEC Timing

Current Loop Fault

The current loop (I_{LOOP}) fault is asserted when the actual loop current is not within ±0.01% FSR of the programmed loop current. If the measured loop current is less than the programmed loop current, the I_{LOOP} Under bit of the fault register is set. If the measured loop current is greater than the programmed loop current, the I_{LOOP} Over bit of the fault register is set. The FAULT pin is set to logic high in either case.

An I_{LOOP} Over condition occurs when the value of the load current sourced from the AD5421 (via REG_{OUT}, REFOUT1, REFOUT2, or DV_{DD}) is greater than the loop current that is programmed to flow in the loop. An I_{LOOP} under condition occurs when there is insufficient compliance voltage to support the programmed loop current, caused by excessive load resistance or low loop supply voltage.

Overtemperature Fault

There are two overtemperature alert bits in the fault register: Temp 100°C and Temp 140°C. If the die temperature of the AD5421 exceeds either 100°C or 140°C, the appropriate bit is set. If the Temp 140°C bit is set in the fault register, the FAULT pin is set to logic high.

Loop Voltage Fault

There are two loop voltage alert bits in the fault register: V_{LOOP} 12V and V_{LOOP} 6V. If the voltage between the V_{LOOP} and COM pins falls below 0.6 V (corresponding to a 12 V loop supply value), the V_{LOOP} 12V bit is set; this bit is cleared when the voltage returns above 0.7 V. Similarly, if the voltage between the V_{LOOP} and COM pins falls below 0.3 V (corresponding to a 6 V loop supply value), the V_{LOOP} 6V bit is set; this bit is cleared when the voltage returns above 0.4 V. If the V_{LOOP} 6V bit is set in the fault register, the FAULT pin is set to logic high.

Figure 42 illustrates how a resistor divider enables the monitoring of the loop supply with the V_{LOOP} input. The recommended resistor divider consists of a 1 MΩ and a 19 MΩ resistor that provide a 20:1 ratio, allowing the 2.5 V input range of the V_{LOOP} pin to monitor loop supplies up to 50 V. With a 20:1 divider ratio, the preset V_{LOOP} 6V and V_{LOOP} 12V alert bits of the fault register generate loop supply faults according to their stated values. If another divider ratio is used, the fault bits generate faults at values that are not equal to 6 V and 12 V.

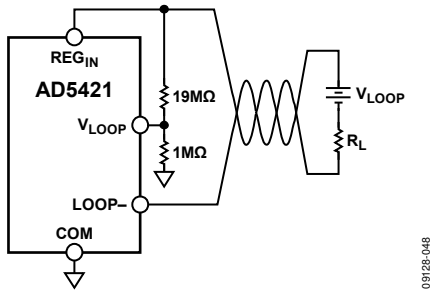

Figure 42. Resistor Divider Connection at V_{LOOP} Pin

EXTERNAL CURRENT SETTING RESISTOR

The 24 kΩ resistor R_{SET}, shown in Figure 1, converts the DAC output voltage to a current, which is then mirrored with a gain of 221 to the LOOP– pin. The stability of the loop current over temperature is dependent on the temperature coefficient of R_{SET}.

Table 1 and Table 2 outline the performance specifications of the AD5421 with both the internal R_{SET} resistor and an external, 24 kΩ R_{SET} resistor. Using the internal R_{SET} resistor, a total unadjusted error of better than 0.126% FSR can be expected. Using an external resistor gives improved performance of 0.048% FSR. This specification assumes an ideal resistor; the actual performance depends on the absolute value and temperature coefficient of the resistor used. For more information, see the Determining the Expected Total Error section.

LOOP CURRENT RANGE SELECTION

To select the loop current range, connect the RANGE0 and RANGE1 pins to the COM and DV_{DD} pins, as shown in Table 9.

Table 9. Selecting the Loop Current Range

RANGE1 Pin	RANGE0 Pin	Loop Current Range
COM	COM	4 mA to 20 mA
COM	DV_{DD}	3.8 mA to 21 mA
DV_{DD}	COM	3.2 mA to 24 mA
DV_{DD}	DV_{DD}	3.8 mA to 21 mA

CONNECTION TO LOOP POWER SUPPLY

The AD5421 is powered from the 4 mA to 20 mA current loop. Typically, the power supply is located far from the transmitter device and has a value of 24 V. The AD5421 can be connected directly to the loop power supply and can tolerate a voltage up to a maximum of 52 V (see Figure 43).

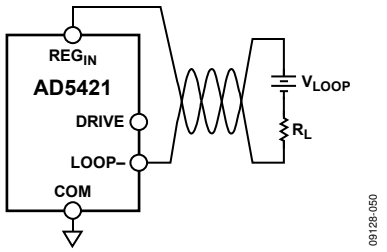

Figure 43. Direct Connection of the AD5421 to Loop Power Supply

Figure 43 shows how the AD5421 is connected directly to the loop power supply. An alternative power connection is shown in Figure 44, which shows a depletion mode N-channel MOSFET connected between the AD5421 and the loop power supply. The use of this device keeps the voltage drop across the AD5421 at approximately 12 V, limiting the worst-case on-chip power dissipation to 288 mW (12 V × 24 mA = 288 mW). If the AD5421 is connected directly to the loop supply as shown in Figure 43, the potential worst-case on-chip power dissipation for a 24 V loop power supply is 576 mW (24 V × 24 mA = 576 mW). The power dissipation changes in proportion to the loop power supply voltage.

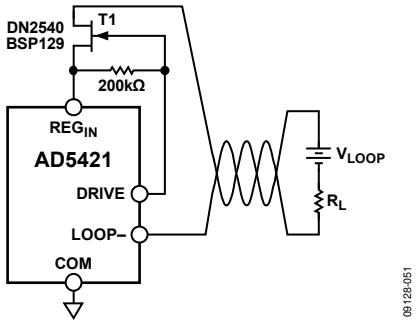

Figure 44. MOSFET Connecting the AD5421 to Loop Power Supply

ON-CHIP ADC

The AD5421 contains an on-chip ADC used to measure and feed back to the fault register either the temperature of the die or the voltage between the V_{LOOP} and COM pins. The select ADC input bit (Bit D8) of the control register selects the parameter to be converted. A conversion is initiated with command byte 00001000 (necessary only if auto fault readback is disabled). This command byte powers on the ADC and performs the conversion. A read of the fault register returns the conversion result. If auto readback of the fault register is required, the ADC must first be powered up by setting the on-chip ADC bit (Bit D7) of the control register.

Because the FAULT pin can go high for as long as 30 µs, care is required when performing a die temperature measurement after a readback of the V_{LOOP} voltage. When switching from a V_{LOOP} measurement to a die temperature measurement, the FAULT pin should not be read within 30 µs of switching, as a false trigger may occur (fault register contents are unaffected).

VOLTAGE REGULATOR

The on-chip voltage regulator provides a regulated voltage output to supply the AD5421 and the remainder of the transmitter circuitry. The output voltage range is from 1.8 V to 12 V and is selected by the states of three digital input pins (see Table 10). The regulator output is accessed at the REG_{OUT} pin.

Table 10. Setting the Voltage Regulator Output

REG_SEL2	REG_SEL1	REG_SEL0	Regulated Output Voltage (V)
COM	COM	COM	1.8
COM	COM	DV_{DD}	2.5
COM	DV_{DD}	COM	3.0
COM	DV_{DD}	DV_{DD}	3.3
DV_{DD}	COM	COM	5.0
DV_{DD}	COM	DV_{DD}	9.0
DV_{DD}	DV_{DD}	COM	12.0

LOOP CURRENT SLEW RATE CONTROL

The rate of change of the loop current can be controlled by connecting an external capacitor between the C_{IN} pin and COM. This reduces the rate of change of the loop current. The output resistance of the DAC (R_{DAC}) together with the C_{SLEW} capacitor generate a time constant that determines the response of the loop current (see Figure 45).

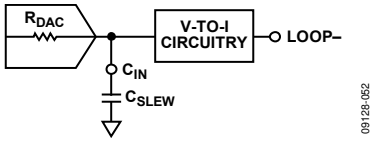

Figure 45. Slew Capacitor Circuit

The resistance of the DAC is typically 15.22 kΩ for the 4 mA to 20 mA and 3.8 mA to 21 mA loop current ranges. The DAC resistance changes to 16.11 kΩ when the 3.2 mA to 24 mA loop current range is selected.

The time constant of the circuit is expressed as

$$\tau = R_{DAC} \times C_{SLEW}$$

Taking five time constants as the required time to reach the final value, C_{SLEW} can be determined for a desired response time, *t*, as follows:

$$C_{SLEW} = \frac{t}{5 \times R_{DAC}}$$

where:
t is the desired time for the output current to reach its final value.
R_{DAC} is the resistance of the DAC core, either 15.22 kΩ or 16.11 kΩ, depending on the selected loop current range.

For a response time of 5 ms,

$$C_{SLEW} = \frac{5\text{ ms}}{5 \times 15{,}220} \approx 68\text{ nF}$$

For a response time of 10 ms,

$$C_{SLEW} = \frac{10\text{ ms}}{5 \times 15{,}220} \approx 133\text{ nF}$$

The responses for both of these configurations are shown in Figure 46.

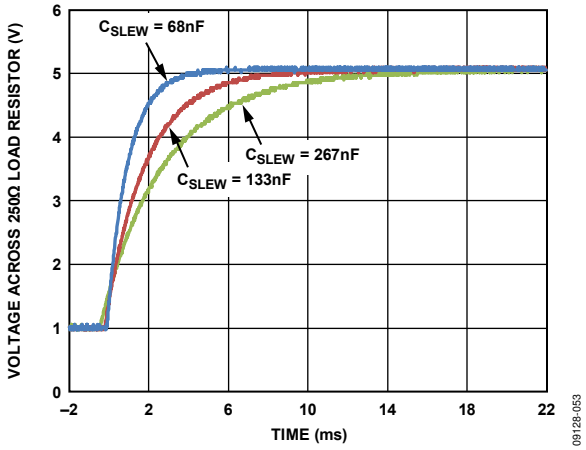

Figure 46. 4 mA to 20 mA Step with Slew Rate Control

The C_{IN} pin can also be used as a coupling input for HART FSK signaling. The HART signal must be ac-coupled to the C_{IN} input. The capacitor through which the HART signal is coupled must be considered in the preceding calculations, where the total capacitance is C_{SLEW} + C_{HART}. For more information, see the HART Communications section.

POWER-ON DEFAULT

The AD5421 powers on with all registers loaded with their default values and with the loop current in the alarm state set to 3.2 mA or 22.8 mA/24 mA (depending on the state of the ALARM_CURRENT_DIRECTION pin and the selected range). The AD5421 remains in this state until it is programmed with new values. The SPI watchdog timer is enabled by default with a timeout period of 1 sec. If there is no communication with the AD5421 within 1 sec of power-on, the FAULT pin is set.

Table 11.

Range	ALARM_CURRENT_DIRECTION	Power-On Loop Current (mA)
4 mA to 20 mA	0	3.2
4 mA to 20 mA	1	22.8
3.8 mA to 21 mA	0	3.2
3.8 mA to 21 mA	1	22.8
3.2 mA to 24 mA	0	3.2
3.2 mA to 24 mA	1	24

HART COMMUNICATIONS

The AD5421 can be interfaced to a Highway Addressable Remote Transducer (HART) modem to enable HART digital communications over the 2-wire loop connection. Figure 47 shows how the modem frequency shift keying (FSK) output is connected to the AD5421.

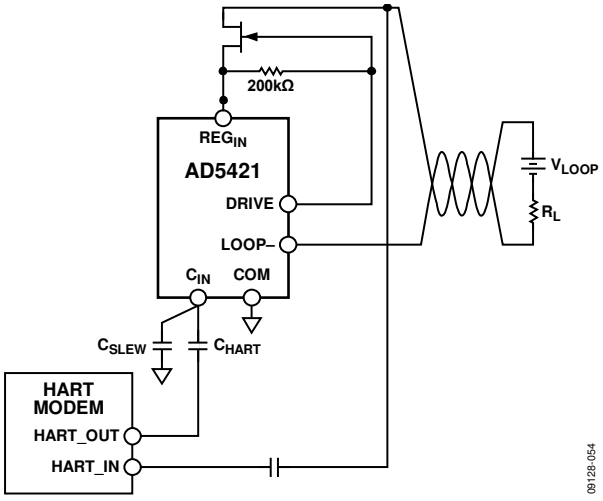

Figure 47. Connecting a HART Modem to the AD5421

To achieve a 1 mA p-p FSK current signal on the loop, the voltage at the C_{IN} pin must be 111 mV p-p. Assuming a 500 mV p-p output from the HART modem, this means that the signal must be attenuated by a factor of 4.5. The following equation can be used to calculate the values of the C_{HART} and C_{SLEW} capacitors.

$$4.5 = \frac{C_{HART} + C_{SLEW}}{C_{HART}}$$

From this equation, the ratio of C_{HART} to C_{SLEW} is 1 to 3.5. This ratio of the capacitor values sets the amplitude of the HART FSK signal on the loop. The absolute values of the capacitors set the response time of the loop current, as well as the bandwidth presented to the HART signal connected at the C_{IN} pin. The bandwidth must pass frequencies from 500 Hz to 10 kHz. The two capacitors and the internal impedance, R_{DAC}, form a high-pass filter. The 3 dB frequency of this high-pass filter should be less than 500 Hz and can be calculated as follows:

$$f_{3dB} = \frac{1}{2 \times \pi \times R_{DAC} \times (C_{HART} + C_{SLEW})}$$

To achieve a 500 Hz high-pass 3 dB frequency cutoff, the combined values of C_{HART} and C_{SLEW} should be 21 nF. To ensure the correct HART signal amplitude on the current loop, the final values for the capacitors are C_{HART} = 4.7 nF and C_{SLEW} = 16.3 nF.

Output Noise During Silence and Analog Rate of Change

The AD5421 has a direct influence on two important specifications relating to the HART communications protocol: output noise during silence and analog rate of change. Figure 25 shows the measurement of the AD5421 output noise in the HART extended bandwidth; the noise measurement is 0.2 mV rms, within the required 2.2 mV rms value.

To meet the analog rate of change specification, the rate of change of the 4 mA to 20 mA current must be slow enough so that it does not interfere with the HART digital signaling. This is determined by forcing a full-scale loop current change through a 500 Ω load resistor and applying the resulting voltage signal to the HART digital filter (HCF_TOOL-31). The peak amplitude of the signal at the filter output must be less than 150 mV. To achieve this, the rate of change of the loop current must be restricted to less than approximately 1.3 mA/ms.

The output of the AD5421 naturally slews at approximately 880 mA/ms, a rate that is far too great to comply with the HART specifications. To reduce the slew rate, a capacitor can be connected from the C_{IN} pin to COM, as described in the Loop Current Slew Rate Control section. To reduce the slew rate enough so that the HART specification is met, a capacitor value in the region of 4.7 µF is required, resulting in a full-scale transition time of 500 ms. Many applications regard this time as too slow, in which case the slew rate needs to be digitally controlled by writing a sequence of codes to the DAC register so that the output response follows the desired curve.