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8-/10-/12-/14-Bit High Bandwidth Multiplying DACs with Serial Interface

Data Sheet

AD5450/AD5451/AD5452/AD5453

FEATURES

- 12 MHz multiplying bandwidth
- Integral nonlinearity (INL) of ±0.25 LSB at 8-bit
- 8-lead TSOT and MSOP packages
- 2.5 V to 5.5 V supply operation
- Pin-compatible 8-/10-/12-/14-bit current output DACs
- ±10 V reference input
- 50 MHz serial interface
- 2.7 MSPS update rate
- Extended temperature range: –40°C to +125°C
- 4-quadrant multiplication
- Power-on reset with brownout detect
- <0.4 µA typical current consumption
- Guaranteed monotonic
- Qualified for automotive applications

APPLICATIONS

- Portable battery-powered applications
- Waveform generators
- Analog processing
- Instrumentation applications
- Programmable amplifiers and attenuators
- Digitally controlled calibration
- Programmable filters and oscillators
- Composite video
- Ultrasound
- Gain, offset, and voltage trimming
- Qualified for automotive applications

FUNCTIONAL BLOCK DIAGRAM

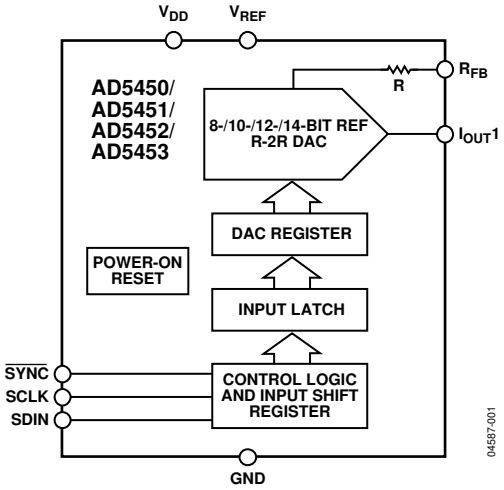

Figure 1.

GENERAL DESCRIPTION

The AD5450/AD5451/AD5452/AD5453[1] are CMOS 8-/10-/12-/14-bit current output digital-to-analog converters (DACs), respectively. These devices operate from a 2.5 V to 5.5 V power supply, making them suited to several applications including battery-powered applications.

As a result of manufacture on a CMOS submicron process, these DACs offer excellent 4-quadrant multiplication characteristics of up to 12 MHz.

These DACs use a double-buffered, 3-wire serial interface that is compatible with SPI, QSPI™, MICROWIRE™, and most digital signal processor (DSP) interface standards. Upon power-up, the internal shift register and latches are filled with 0s, and the DAC output is at zero scale.

[1] U.S. Patent Number 5,689,257.

The applied external reference input voltage (V_{REF}) determines the full-scale output current. These devices can handle ±10 V inputs on the reference, despite operating from a single-supply power supply of 2.5 V to 5.5 V. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external current to voltage precision amplifier.

The AD5450/AD5451/AD5452/AD5453 DACs are available in small 8-lead TSOT, and the AD5452/AD5453 are also available in MSOP packages. The AD5453 also comes in 8-lead LFCSP.

Rev. H
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12/15—Rev. G to Rev. H

Changed LFCSP_WD to LFCSP ... Throughout
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4/12—Rev. E to Rev. F

Changes to General Description Section ... 1
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Deleted Figure 65 and Figure 66 ... 26
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2/11—Rev. C to Rev. D

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3/06—Rev. A to Rev. B

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7/05—Rev. 0 to Rev. A

Added AD5453 ... Universal
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Change to Figure 21 ... 10
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1/05—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V. Temperature range for Y version: −40°C to +125°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. DC performance measured with OP177 and ac performance measured with AD8038, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
AD5450					
Resolution			8	Bits	
Relative Accuracy			±0.25	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic
Total Unadjusted Error			±0.5	LSB	
Gain Error			±0.25	LSB	
AD5451					
Resolution			10	Bits	
Relative Accuracy			±0.25	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic
Total Unadjusted Error			±0.5	LSB	
Gain Error			±0.25	LSB	
AD5452					
Resolution			12	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
Total Unadjusted Error			±1	LSB	
Gain Error			±0.5	LSB	
AD5453					
Resolution			14	Bits	
Relative Accuracy			±2	LSB	
Differential Nonlinearity			−1/+2	LSB	Guaranteed monotonic
Total Unadjusted Error			±4	LSB	
Gain Error			±2.5	LSB	
Gain Error Temperature Coefficient[1]		±2		ppm FSR/°C	
Output Leakage Current			±1	nA	Data = 0x0000, T_A = 25°C, I_{OUT}1
			±10	nA	Data = 0x0000, T_A = −40°C to +125°C, I_{OUT}1
REFERENCE INPUT[1]					
Reference Input Range		±10		V	
V_{REF} Input Resistance	7	9	11	kΩ	Input resistance, TC = −50 ppm/°C
R_{FB} Feedback Resistance	7	9	11	kΩ	Input resistance, TC = −50 ppm/°C
Input Capacitance					
Zero-Scale Code		18	22	pF	
Full-Scale Code		18	22	pF	
DIGITAL INPUTS/OUTPUTS[1]					
Input High Voltage, V_{IH}	2.0			V	V_{DD} = 3.6 V to 5 V
	1.7			V	V_{DD} = 2.5 V to 3.6 V
Input Low Voltage, V_{IL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
			0.7	V	V_{DD} = 2.5 V to 2.7 V
Output High Voltage, V_{OH}	V_{DD} − 1			V	V_{DD} = 4.5 V to 5 V, I_{SOURCE} = 200 µA
	V_{DD} − 0.5			V	V_{DD} = 2.5 V to 3.6 V, I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	V_{DD} = 4.5 V to 5 V, I_{SINK} = 200 µA
			0.4	V	V_{DD} = 2.5 V to 3.6 V, I_{SINK} = 200 µA
Input Leakage Current, I_{IL}			±1	nA	T_A = 25°C
			±10	nA	T_A = −40°C to +125°C
Input Capacitance			10	pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]					
Reference Multiplying BW		12		MHz	V_{REF} = ±3.5 V, DAC loaded with all 1s
Multiplying Feedthrough Error					V_{REF} = ±3.5 V, DAC loaded with all 0s
		72		dB	100 kHz
		64		dB	1 MHz
		44		dB	10 MHz
Output Voltage Settling Time					V_{REF} = 10 V, R_{LOAD} = 100 Ω; DAC latch alternately loaded with 0s and 1s
Measured to ±1 mV of FS		100	110	ns	
Measured to ±4 mV of FS		24	40	ns	
Measured to ±16 mV of FS		16	33	ns	
Digital Delay		20	40	ns	Interface delay time
10% to 90% Settling Time		10	30	ns	Rise and fall times, V_{REF} = 10 V, R_{LOAD} = 100 Ω
Digital-to-Analog Glitch Impulse		2		nV-s	1 LSB change around major carry, V_{REF} = 0 V
Output Capacitance					
$I_{OUT}1$		13		pF	DAC latches loaded with all 0s
		28		pF	DAC latches loaded with all 1s
$I_{OUT}2$		18		pF	DAC latches loaded with all 0s
		5		pF	DAC latches loaded with all 1s
Digital Feedthrough		0.5		nV-s	Feedthrough to DAC output with $\overline{CS}$ high and alternate loading of all 0s and all 1s
Analog THD		83		dB	V_{REF} = 3.5 V p-p, all 1s loaded, f = 1 kHz
Digital THD					Clock = 1 MHz, V_{REF} = 3.5 V
50 kHz f_{OUT}		71		dB	
20 kHz f_{OUT}		77		dB	
Output Noise Spectral Density		25		nV/√Hz	At 1 kHz
SFDR Performance (Wide Band)					Clock = 1 MHz, V_{REF} = 3.5 V
50 kHz f_{OUT}		78		dB	
20 kHz f_{OUT}		74		dB	
SFDR Performance (Narrow Band)					Clock = 1 MHz, V_{REF} = 3.5 V
50 kHz f_{OUT}		87		dB	
20 kHz f_{OUT}		85		dB	
Intermodulation Distortion		79		dB	f_1 = 20 kHz, f_2 = 25 kHz, clock = 1 MHz, V_{REF} = 3.5 V
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}		0.4	10	µA	T_A = −40°C to +125°C, logic inputs = 0 V or V_{DD}
			0.6	µA	T_A = 25°C, logic inputs = 0 V or V_{DD}
Power Supply Sensitivity[1]			0.001	%/%	ΔV_{DD} = ±5%

[1] Guaranteed by design and characterization, not subject to production test.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, temperature range for Y version: −40°C to +125°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	V_{DD} = 2.5 V to 5.5 V	Unit	Description
f_{SCLK}	50	MHz max	Maximum clock frequency
t_1	20	ns min	SCLK cycle time
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4	8	ns min	$\overline{\text{SYNC}}$ falling edge to SCLK active edge setup time
t_5	5	ns min	Data setup time
t_6	4.5	ns min	Data hold time
t_7	5	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK active edge
t_8	30	ns min	Minimum $\overline{\text{SYNC}}$ high time
Update Rate	2.7	MSPS	Consists of cycle time, $\overline{\text{SYNC}}$ high time, data setup, and output voltage settling time

[1] Guaranteed by design and characterization, not subject to production test.

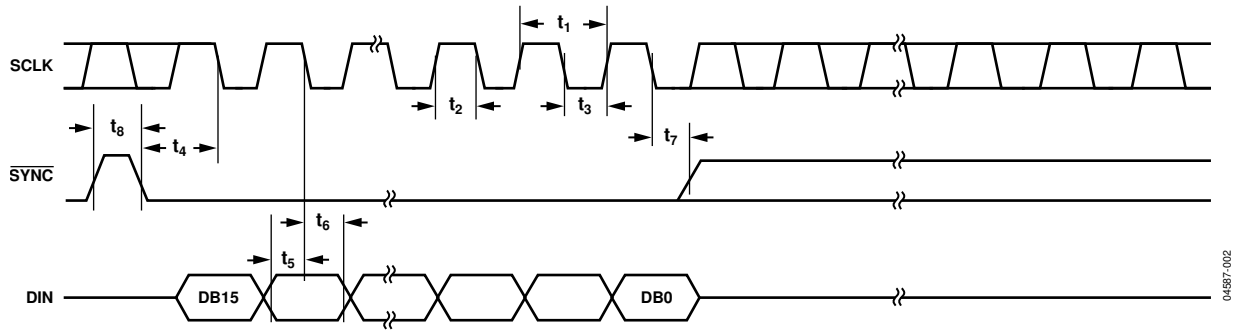

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Transient currents of up to 100 mA do not cause SCR latch-up.
T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{REF}, R_{FB} to GND	−12 V to +12 V
$I_{OUT}1$ to GND	−0.3 V to +7 V
Input Current to Any Pin Except Supplies	±10 mA
Logic Inputs and Output[1]	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range, Extended (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
8-Lead MSOP	206°C/W
8-Lead TSOT	211°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

[1] Overvoltages at SCLK, $\overline{SYNC}$, and SDIN are clamped by internal diodes.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

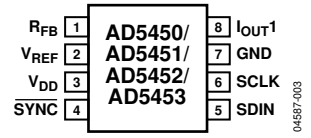

Figure 3. 8-Lead TSOT Pin Configuration

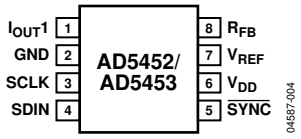

Figure 4. 8-Lead MSOP Pin Configuration

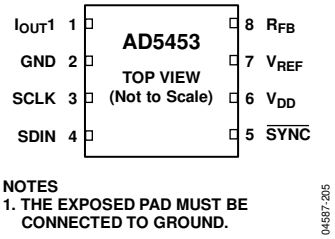

Figure 5. 8-Lead LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No[1]				
TSOT	**MSOP**	**LFCSP**	**Mnemonic**	**Description**
1	8	8	R_{FB}	DAC Feedback Resistor. Establish voltage output for the DAC by connecting to external amplifier output.
2	7	7	V_{REF}	DAC Reference Voltage Input.
3	6	6	V_{DD}	Positive Power Supply Input. These devices can operate from a supply of 2.5 V to 5.5 V.
4	5	5	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. Data is loaded to the shift register upon the active edge of the following clocks.
5	4	4	SDIN	Serial Data Input. Data is clocked into the 16-bit input register upon the active edge of the serial clock input. By default, in power-up mode data is clocked into the shift register upon the falling edge of SCLK. The control bits allow the user to change the active edge to a rising edge.
6	3	3	SCLK	Serial Clock Input. By default, data is clocked into the input shift register upon the falling edge of the serial clock input. Alternatively, by means of the serial control bits, the device can be configured such that data is clocked into the shift register upon the rising edge of SCLK.
7	2	2	GND	Ground Pin.
8	1	1	$I_{OUT}1$	DAC Current Output.
N/A	N/A	EPAD	EPAD	Exposed pad must be connected to ground.

[1] N/A = not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

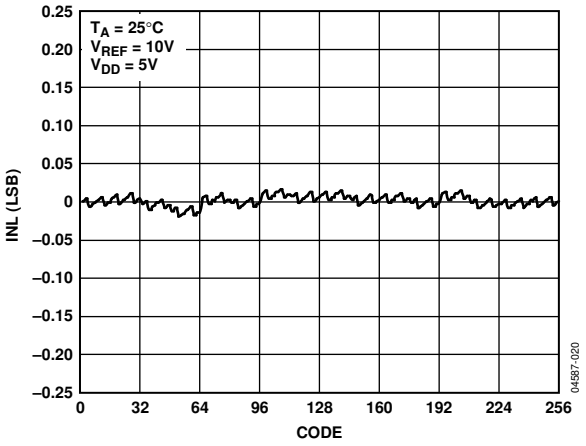

Figure 6. INL vs. Code (8-Bit DAC)

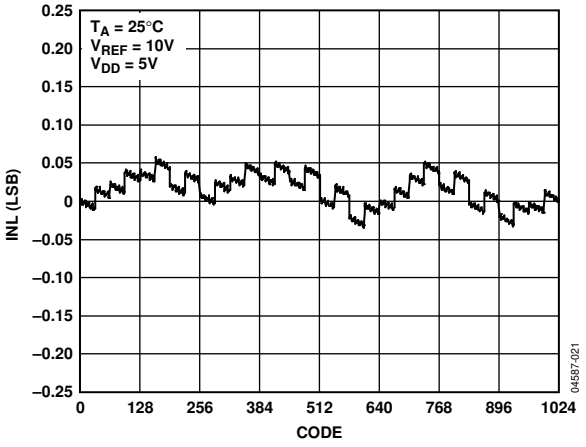

Figure 7. INL vs. Code (10-Bit DAC)

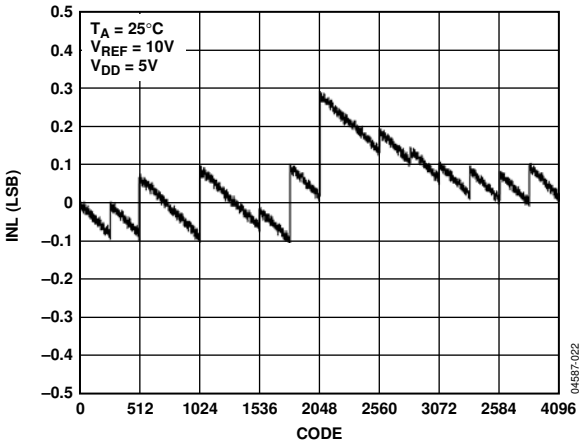

Figure 8. INL vs. Code (12-Bit DAC)

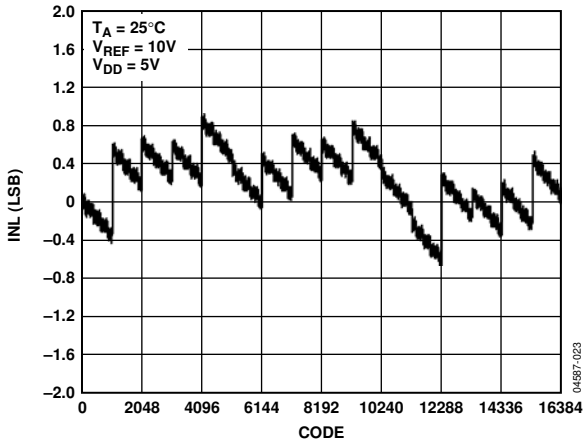

Figure 9. INL vs. Code (14-Bit DAC)

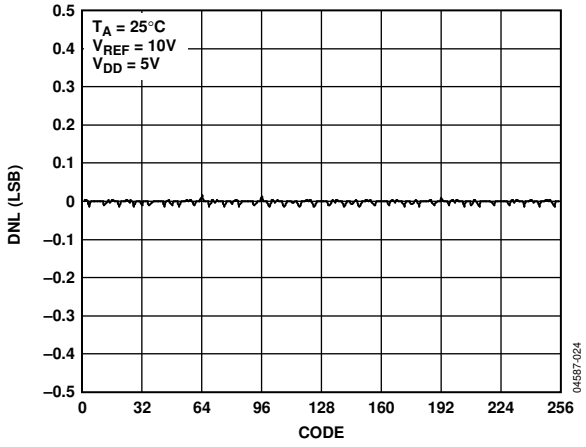

Figure 10. DNL vs. Code (8-Bit DAC)

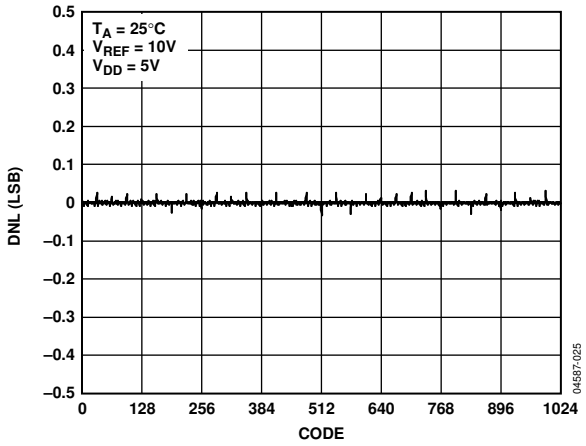

Figure 11. DNL vs. Code (10-Bit DAC)

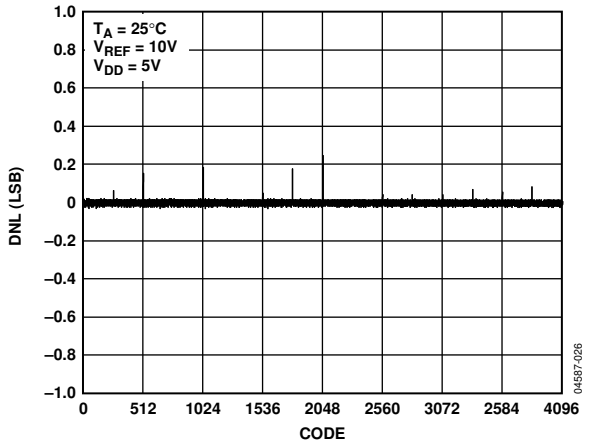

Figure 12. DNL vs. Code (12-Bit DAC)

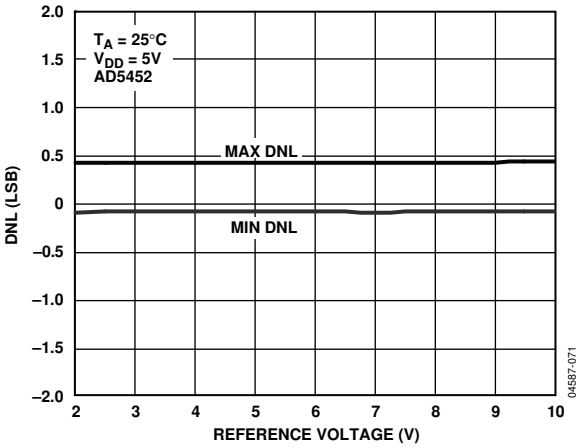

Figure 15. DNL vs. Reference Voltage

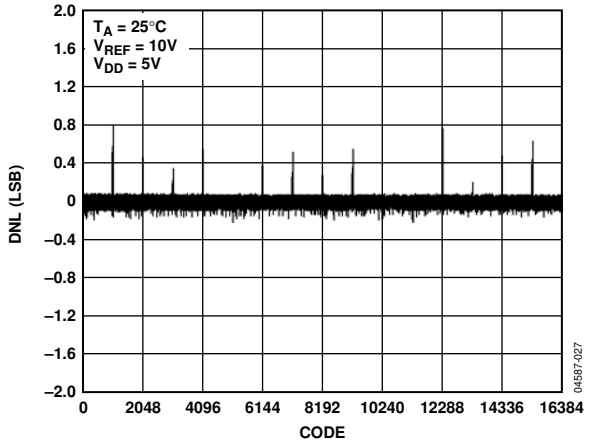

Figure 13. DNL vs. Code (14-Bit DAC)

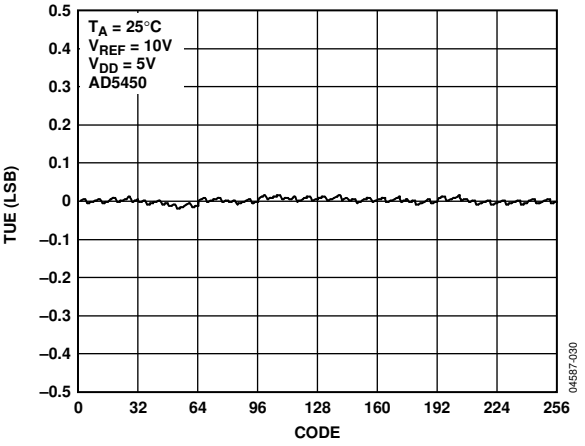

Figure 16. TUE vs. Code (8-Bit DAC)

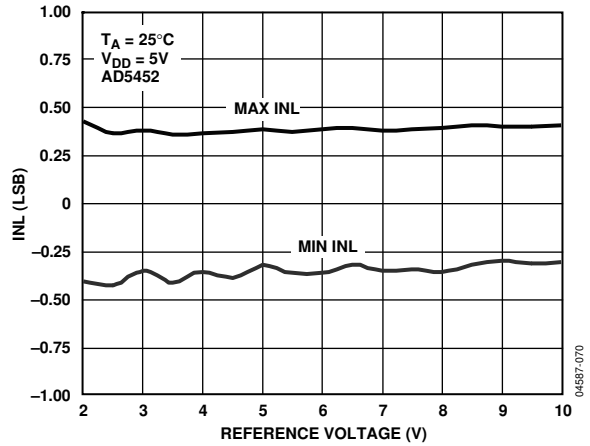

Figure 14. INL vs. Reference Voltage

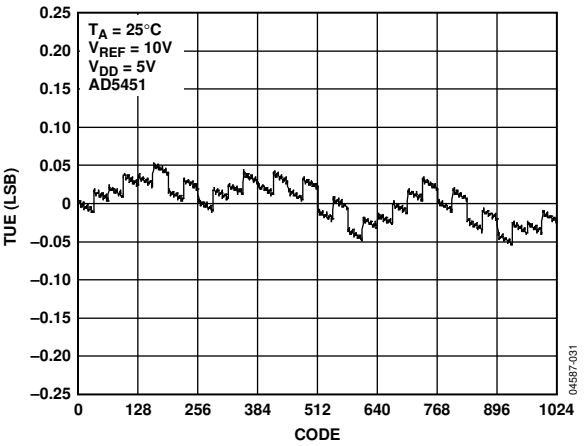

Figure 17. TUE vs. Code (10-Bit DAC)

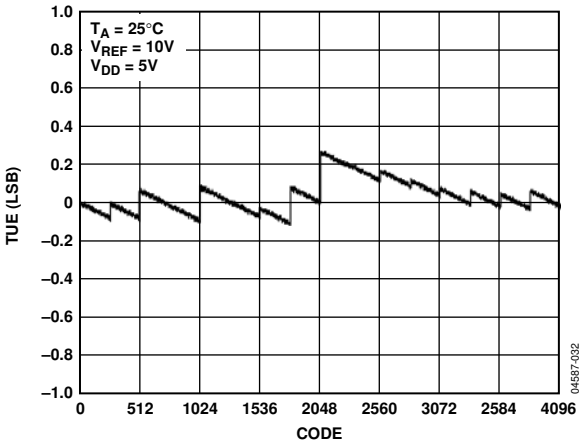

Figure 18. TUE vs. Code (12-Bit DAC)

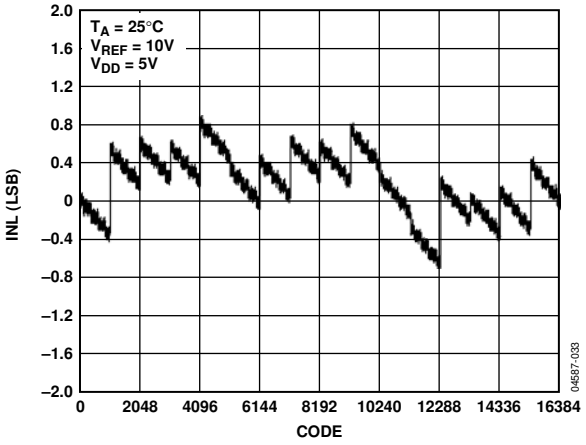

Figure 19. TUE vs. Code (14-Bit DAC)

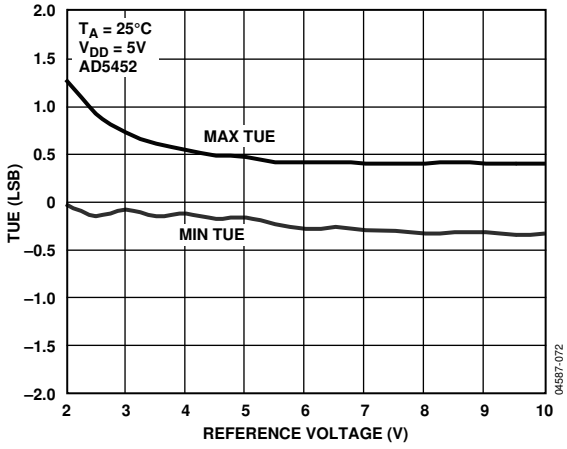

Figure 20. TUE vs. Reference Voltage

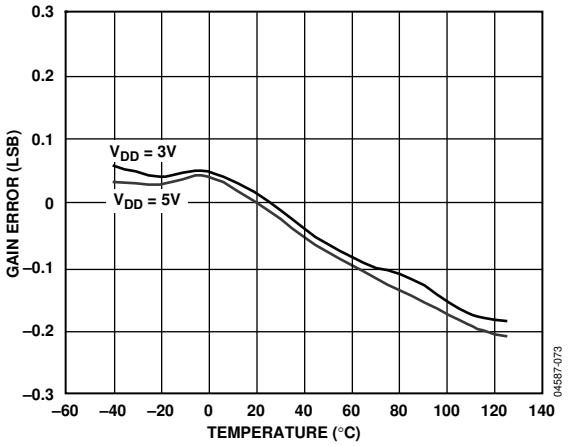

Figure 21. Gain Error (LSB) vs. Temperature

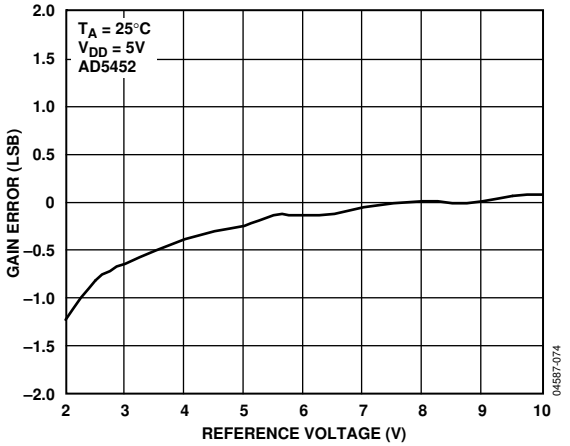

Figure 22. Gain Error (LSB) vs. Reference Voltage

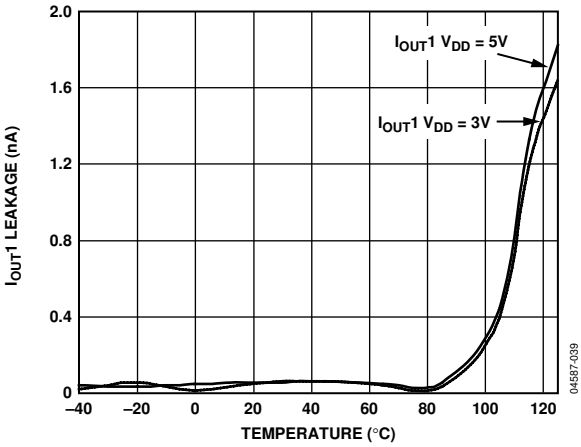

Figure 23. $I_{OUT}1$ Leakage Current vs. Temperature

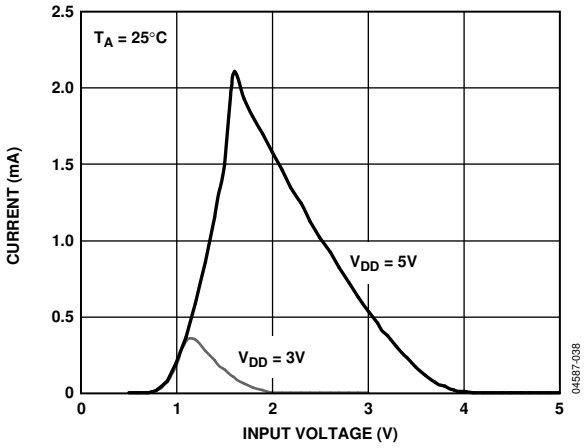

Figure 24. Supply Current vs. Logic Input Voltage

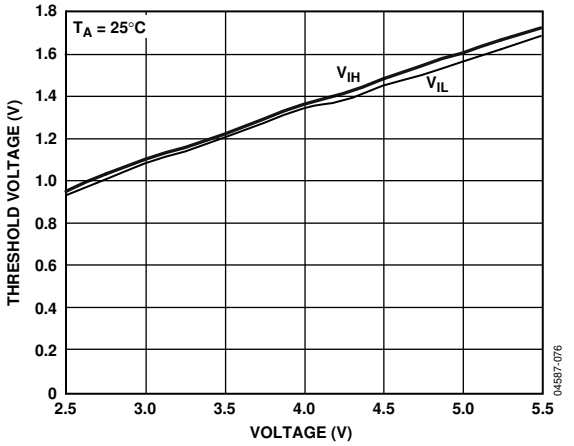

Figure 27. Threshold Voltage vs. Supply Voltage

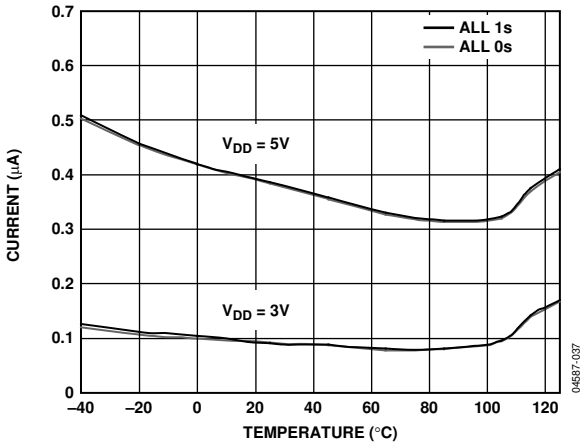

Figure 25. Supply Current vs. Temperature

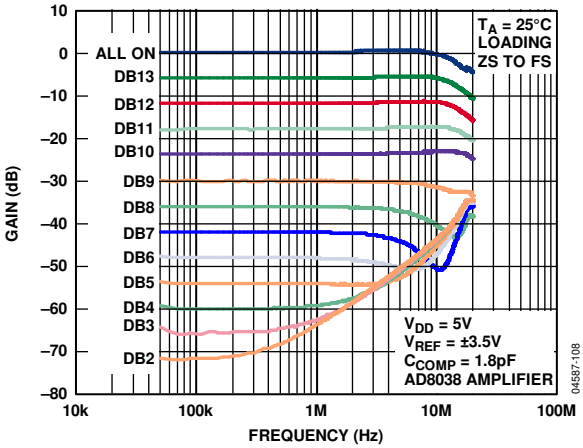

Figure 28. Reference Multiplying Bandwidth vs. Frequency and Code

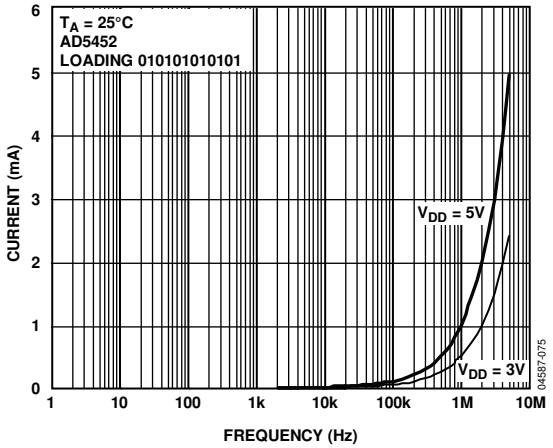

Figure 26. Supply Current vs. Update Rate

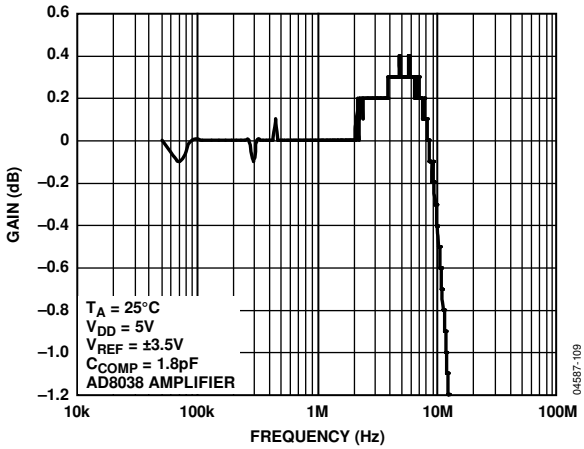

Figure 29. Reference Multiplying Bandwidth—All 1s Loaded

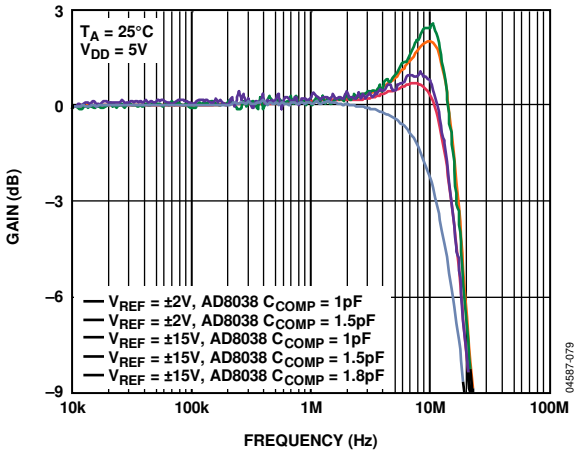

Figure 30. Reference Multiplying Bandwidth vs. Frequency and Compensation Capacitor

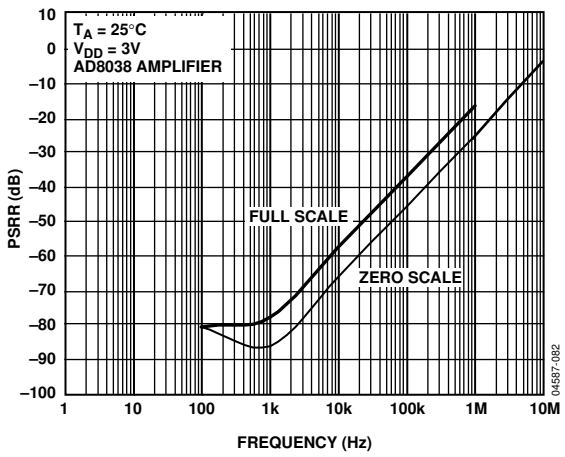

Figure 33. Power Supply Rejection Ratio vs. Frequency

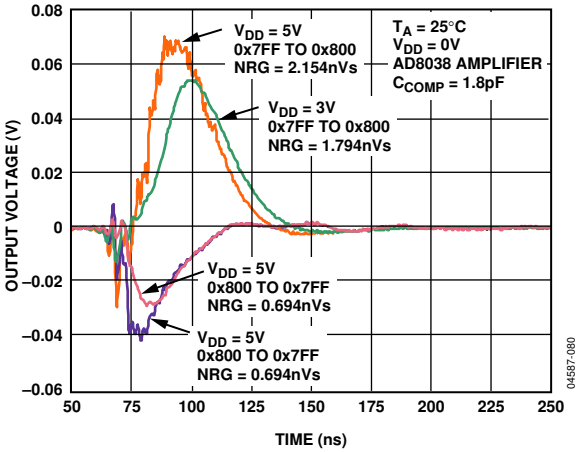

Figure 31. Midscale Transition, V_{REF} = 0 V

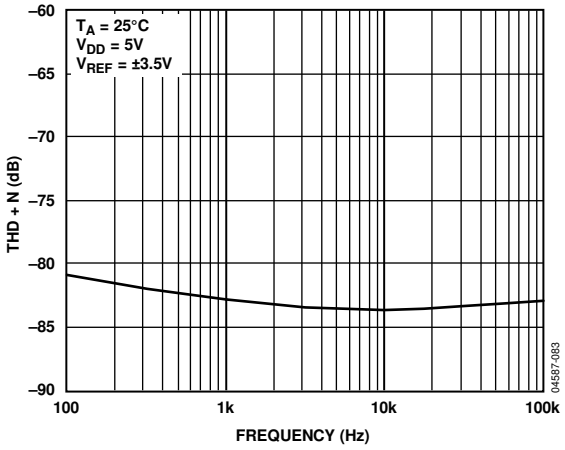

Figure 34. THD + Noise vs. Frequency

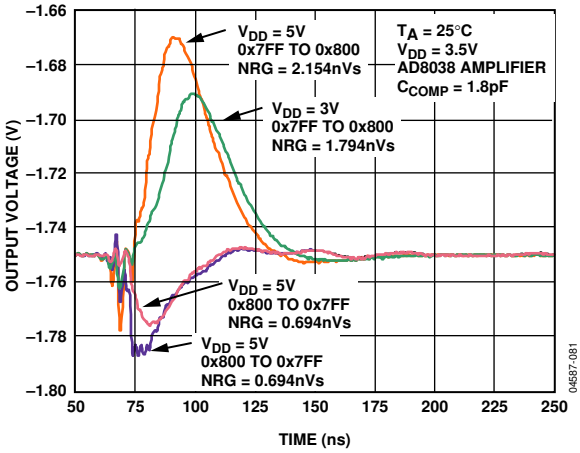

Figure 32. Midscale Transition, V_{REF} = 3.5 V

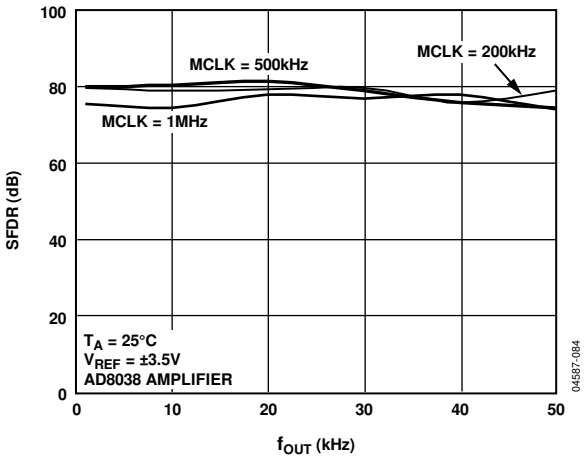

Figure 35. Wideband SFDR vs. f_{OUT} Frequency

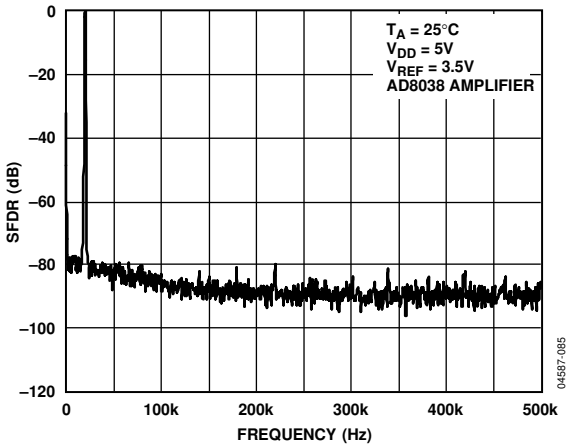

Figure 36. Wideband SFDR, f_{OUT} = 20 kHz, Clock = 1 MHz

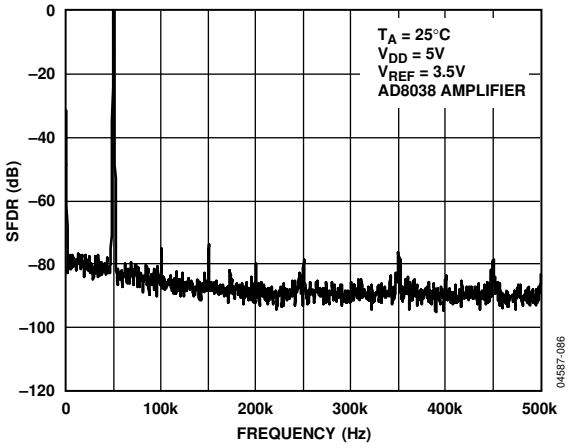

Figure 37. Wideband SFDR, f_{OUT} = 50 kHz, Clock = 1 MHz

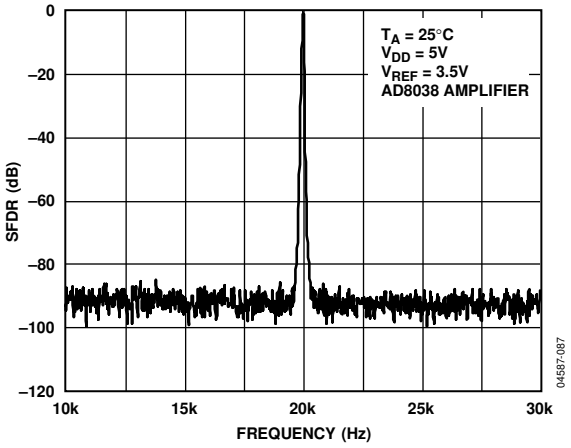

Figure 38. Narrow-Band SFDR, f_{OUT} = 20 kHz, Clock = 1 MHz

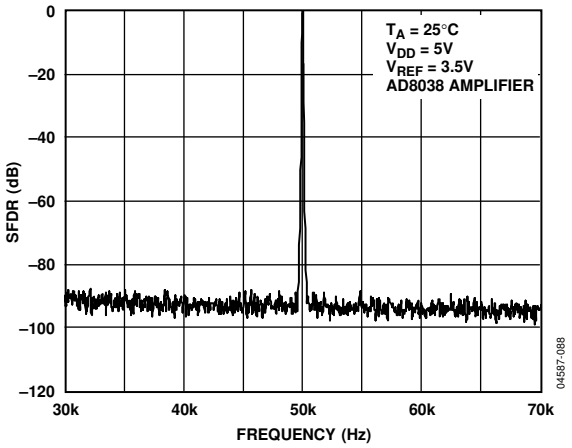

Figure 39. Narrow-Band SFDR , f_{OUT} = 50 kHz, Clock = 1 MHz

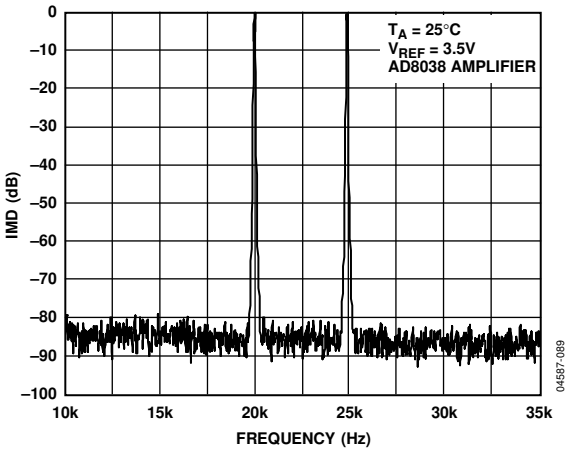

Figure 40. Narrow-Band IMD, f_{OUT} = 20 kHz, 25 kHz, Clock = 1 MHz

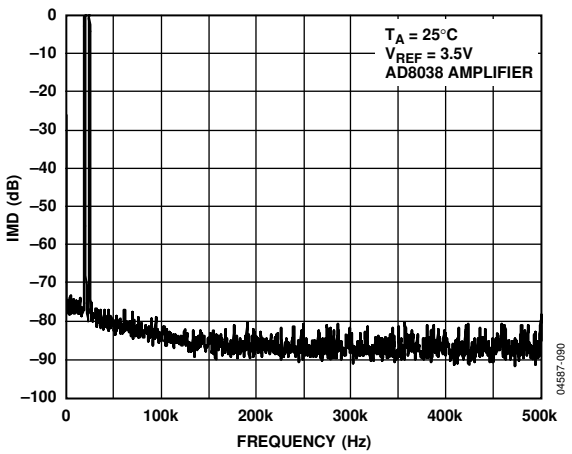

Figure 41. Wideband IMD, f_{OUT} = 20 kHz, 25 kHz, Clock = 1 MHz

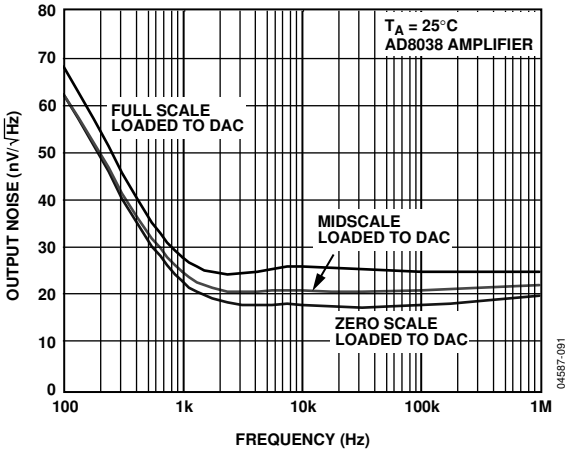

Figure 42. Output Noise Spectral Density

TERMINOLOGY

Relative Accuracy (Endpoint Nonlinearity)
A measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of the full-scale reading.

Differential Nonlinearity
The difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of −1 LSB maximum over the operating temperature range ensures monotonicity.

Gain Error (Full-Scale Error)
A measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is V_{REF} − 1 LSB. Gain error of the DACs is adjustable to zero with external resistance.

Output Leakage Current
The current that flows into the DAC ladder switches when it is turned off. For the $I_{OUT}1$ terminal, it can be measured by loading all 0s to the DAC and measuring the $I_{OUT}1$ current.

Output Capacitance
Capacitance from $I_{OUT}1$ to AGND.

Output Current Settling Time
The amount of time it takes for the output to settle to a specified level for a full-scale input change. For these devices, it is specified with a 100 Ω resistor to ground. The settling time specification includes the digital delay from the $\overline{SYNC}$ rising edge to the full-scale output change.

Digital-to-Analog Glitch Impulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-s or nV-s, depending on whether the glitch is measured as a current or voltage signal.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device's digital inputs may be capacitively coupled through the device and produce noise on the I_{OUT} pins. This noise is coupled from the outputs of the device onto follow on circuitry. This noise is digital feedthrough.

Multiplying Feedthrough Error
The error due to capacitive feedthrough from the DAC reference input to the DAC $I_{OUT}1$ terminal when all 0s are loaded to the DAC.

Total Harmonic Distortion (THD)
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower-order harmonics, such as second to fifth, are included.

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}$$

Digital Intermodulation Distortion (IMD)
Second-order intermodulation measurements are the relative magnitudes of the fa and fb tones generated digitally by the DAC and the second-order products at 2fa − fb and 2fb − fa.

Compliance Voltage Range
The maximum range of (output) terminal voltage for which the device provides the specified characteristics.

Spurious-Free Dynamic Range (SFDR)
The usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. SFDR is the measure of difference in amplitude between the fundamental and the largest harmonically or nonharmonically related spur from dc to full Nyquist bandwidth (half the DAC sampling rate or $f_S/2$). Narrow band SFDR is a measure of SFDR over an arbitrary window size, in this case 50% of the fundamental. Digital SFDR is a measure of the usable dynamic range of the DAC when the signal is a digitally generated sine wave.

GENERAL DESCRIPTION

DAC SECTION

The AD5450/AD5451/AD5452/AD5453 are 8-/10-/12-/14-bit current output DACs, respectively, consisting of a segmented (4-bit) inverting R-2R ladder configuration. A simplified diagram for the 12-bit AD5452 is shown in Figure 43.

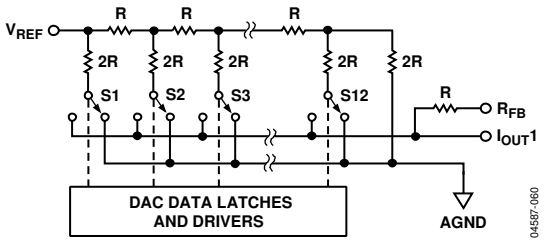

Figure 43. AD5452 Simplified Ladder

The feedback resistor, R_{FB}, has a value of R. The value of R is typically 9 kΩ (with a minimum value of 7 kΩ and a maximum value of 11 kΩ). If $I_{OUT}1$ is kept at the same potential as GND, a constant current flows in each ladder leg, regardless of digital input code. Therefore, the input resistance presented at V_{REF} is always constant and nominally of value R. The DAC output ($I_{OUT}1$) is code dependent, producing various resistances and capacitances. When choosing the external amplifier, take into account the variation in impedance generated by the DAC on the amplifier's inverting input node.

Access is provided to the V_{REF}, R_{FB}, and $I_{OUT}1$ terminals of the DAC, making the device extremely versatile and allowing it to be configured in several operating modes; for example, it can provide a unipolar output or can provide 4-quadrant multiplication in bipolar mode. Note that a matching switch is used in series with the internal R_{FB} feedback resistor. If users attempt to measure R_{FB}, power must be applied to V_{DD} to achieve continuity.

CIRCUIT OPERATION

Unipolar Mode

Using a single operational amplifier, these devices can easily be configured to provide a 2-quadrant multiplying operation or a unipolar output voltage swing, as shown in Figure 44. When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -\frac{D}{2^n} \times V_{REF}$$

where:
D is the fractional representation of the digital word loaded to the DAC.
D = 0 to 255 (8-bit AD5450).
= 0 to 1023 (10-bit AD5451).
= 0 to 4095 (12-bit AD5452).
= 0 to 16,383 (14-bit AD5453).
n is the number of bits.

Note that the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages.

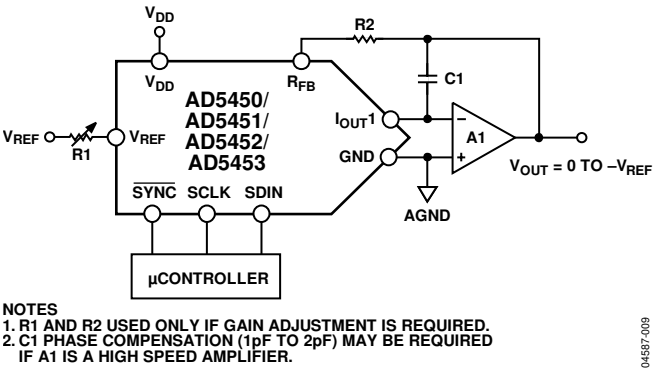

Figure 44. Unipolar Mode Operation

These DACs are designed to operate with either negative or positive reference voltages. The V_{DD} power pin is only used by the internal digital logic to drive the on and off states of the DAC switches.

These DACs are designed to accommodate ac reference input signals in the range of −10 V to +10 V.

With a fixed 10 V reference, the circuit shown in Figure 44 gives a unipolar 0 V to −10 V output voltage swing. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication.

Table 5 shows the relationship between the digital code and the expected output voltage for a unipolar operation using the 8-bit AD5450.

Table 5. Unipolar Code Table for the AD5450

Digital Input	Analog Output (V)
1111 1111	$-V_{REF}$ (255/256)
1000 0000	$-V_{REF}$ (128/256) = $-V_{REF}/2$
0000 0001	$-V_{REF}$ (1/256)
0000 0000	$-V_{REF}$ (0/256) = 0

Bipolar Mode

In some applications, it may be necessary to generate a full 4-quadrant multiplying operation or a bipolar output swing. This can be easily accomplished by using another external amplifier and some external resistors, as shown in Figure 45. In this circuit, the second amplifier, A2, provides a gain of 2. Biasing the external amplifier with an offset from the reference voltage results in full 4-quadrant multiplying operation. The transfer function of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from Code 0 ($V_{OUT} = -V_{REF}$) to midscale (V_{OUT} – 0 V) to full scale ($V_{OUT} = +V_{REF}$).

$$V_{OUT} = \left(V_{REF} \times \frac{D}{2^{n-1}} \right) - V_{REF}$$

where:
D is the fractional representation of the digital word loaded to the DAC.
D = 0 to 255 (8-bit AD5450).
= 0 to 1023 (10-bit AD5451).
= 0 to 4095 (12-bit AD5452).
n is the resolution of the DAC.

When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication. Table 6 shows the relationship between the digital code and the expected output voltage for a bipolar operation using the 8-bit AD5450.

Table 6. Bipolar Code Table for the AD5450

Digital Input	Analog Output (V)
1111 1111	$+V_{REF}$ (127/128)
1000 0000	0
0000 0001	$-V_{REF}$ (127/128)
0000 0000	$-V_{REF}$ (128/128)

Stability

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the operational amplifier must be connected as close as possible, and proper printed circuit board (PCB) layout techniques must be employed. Because every code change corresponds to a step function, gain peaking may occur if the operational amplifier has limited gain bandwidth product (GBP) and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open-loop response, which can cause ringing or instability in the closed-loop applications circuit.

An optional compensation capacitor, C1, can be added in parallel with R_{FB} for stability, as shown in Figure 44 and Figure 45. Too small a value of C1 can produce ringing at the output, and too large a value can adversely affect the settling time. C1 should be found empirically, but 1 pF to 2 pF is generally adequate for the compensation.

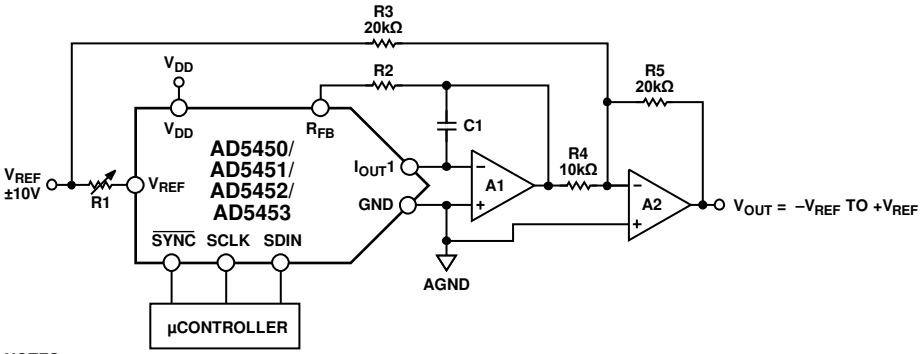

Figure 45. Bipolar Mode Operation (4-Quadrant Multiplication)

SINGLE-SUPPLY APPLICATIONS

Voltage Switching Mode

Figure 46 shows these DACs operating in the voltage switching mode. The reference voltage, V_{IN}, is applied to the $I_{OUT}1$ pin, and the output voltage is available at the V_{REF} terminal. In this configuration, a positive reference voltage results in a positive output voltage, making single-supply operation possible. The output from the DAC is voltage at a constant impedance (the DAC ladder resistance); therefore, an operational amplifier is necessary to buffer the output voltage. The reference input no longer sees constant input impedance, but one that varies with code; therefore, drive the voltage input from a low impedance source.

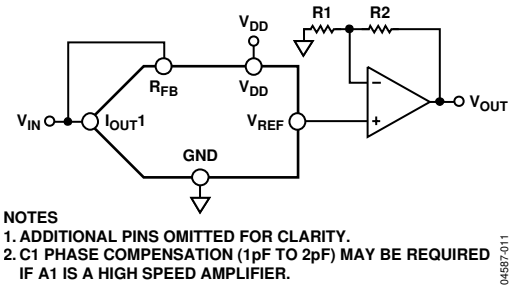

Figure 46. Single-Supply Voltage Switching Mode

It is important to note that with this configuration V_{IN} is limited to low voltages because the switches in the DAC ladder do not have the same source-drain drive voltage. As a result, the on resistance of the switches differs, which degrades the integral linearity of the DAC. Also, V_{IN} must not go negative by more than 0.3 V, or an internal diode turns on, causing the device to exceed the maximum ratings. In this type of application, the full range of multiplying capability of the DAC is lost.

ADDING GAIN

In applications in which the output voltage is required to be greater than V_{IN}, gain can be added with an additional external amplifier, or it can be achieved in a single stage. It is important to consider the effect of the temperature coefficients of the DAC thin film resistors. Simply placing a resistor in series with the RFB resistor causes mismatches in the temperature coefficients and results in larger gain temperature coefficient errors. Instead, increase the gain of the circuit by using the recommended configuration shown in Figure 47. R1, R2, and R3 must have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits where gains greater than 1 are required. Note that $R_{FB} \gg R2//R3$ and a gain error percentage of $100 \times (R2//R3)/R_{FB}$ must be taken into consideration.

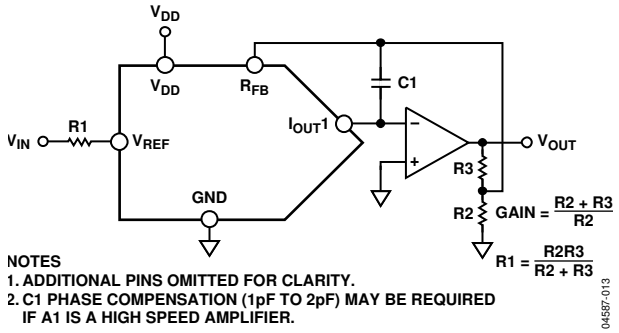

Figure 47. Increasing Gain of Current-Output DAC

DIVIDER OR PROGRAMMABLE GAIN ELEMENT

Current-steering DACs are very flexible and lend themselves to many different applications. If this type of DAC is connected as the feedback element of an operational amplifier and R_{FB} is used as the input resistor as shown in Figure 48, the output voltage is inversely proportional to the digital input fraction, D.

For $D = 1 - 2^{-n}$, the output voltage is

$$V_{OUT} = \frac{-V_{IN}}{D} = \frac{-V_{IN}}{(1-2^{-n})}$$

As D is reduced, the output voltage increases. For small values of the digital fraction, D, it is important to ensure that the amplifier does not saturate and that the required accuracy is met. For example, an 8-bit DAC driven with the binary code 0x10 (00010000), that is, 16 decimal, in the circuit of Figure 48 causes the output voltage to be 16 times V_{IN}.

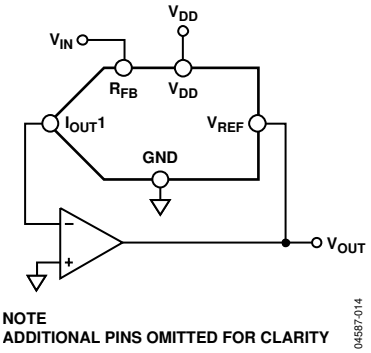

Figure 48. Current Steering DAC Used as a Divider or Programmable Gain Element

However, if the DAC has a linearity specification of ±0.5 LSB, D can have weight anywhere in the range of 15.5/256 to 16.5/256. Therefore, the possible output voltage is in the range of 15.5 V_{IN} to 16.5 V_{IN}—an error of 3%, even though the DAC itself has a maximum error of 0.2%.

DAC leakage current is also a potential error source in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the operational amplifier through the DAC. Because only a fraction, D, of the current in the V_{REF} terminal is routed to the $I_{OUT}1$ terminal, the output voltage changes as follows:

Output Error Voltage Dueto Leakage = (*Leakage* × *R*)/*D*

where *R* is the DAC resistance at the V_{REF} terminal.

For a DAC leakage current of 10 nA, R = 10 kΩ, and a gain (that is, 1/D) of 16, the error voltage is 1.6 mV.

REFERENCE SELECTION

When selecting a reference for use with this series of current output DACs, pay attention to the reference's output voltage temperature coefficient specification. This parameter not only affects the full-scale error, but also may affect the linearity (INL and DNL) performance.

The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system is required to hold its overall specification to within 1 LSB over the temperature range 0°C to 50°C, and the system's maximum temperature drift should be less than 78 ppm/°C.

A 12-bit system within 2 LSB accuracy requires a maximum drift of 10 ppm/°C. Choosing a precision reference with a low output temperature coefficient minimizes this error source. Table 7 lists some dc references available from Analog Devices, Inc., that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current steering mode is an amplifier with low input bias currents and low input offset voltage. The input offset voltage of an operational amplifier is multiplied by the variable gain of the circuit due to the code dependent output resistance of the DAC. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the offset voltage of the amplifier's input. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which if large enough, could cause the DAC to be nonmonotonic.

The input bias current of an operational amplifier generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor, R_{FB}. Most operational amplifiers have input bias currents low enough to prevent significant errors in 12-bit applications. However, for 14-bit applications, some consideration should be given to selecting an appropriate amplifier.

Common-mode rejection of the operational amplifier is important in voltage switching circuits because it produces a code-dependent error at the voltage output of the circuit. Most operational amplifiers have adequate common-mode rejection for use at 8-, 10-, and 12-bit resolutions.

Provided that the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage switching DAC circuit is determined largely by the output operational amplifier. To obtain minimum settling time in this configuration, it is important to minimize capacitance at the V_{REF} node (the voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

Most single-supply circuits include ground as part of the analog signal range, which in turn requires an amplifier that can handle rail-to-rail signals. There is a large range of single-supply amplifiers available from Analog Devices.

Table 7. Suitable Analog Devices Precision References

Part No.	Output Voltage (V)	Initial Tolerance (%)	Temp Drift (ppm/°C)	I_{SS} (mA)	Output Noise (µV p-p)	Package
ADR01	10	0.05	3	1	20	SOIC-8
ADR01	10	0.05	9	1	20	TSOT-23, SC70
ADR02	5	0.06	3	1	10	SOIC-8
ADR02	5	0.06	9	1	10	TSOT-23, SC70
ADR03	2.5	0.10	3	1	6	SOIC-8
ADR03	2.5	0.10	9	1	6	TSOT-23, SC70
ADR06	3	0.10	3	1	10	SOIC-8
ADR06	3	0.10	9	1	10	TSOT-23, SC70
ADR431	2.5	0.04	3	0.8	3.5	SOIC-8
ADR435	5	0.04	3	0.8	8	SOIC-8
ADR391	2.5	0.16	9	0.12	5	TSOT-23
ADR395	5	0.10	9	0.12	8	TSOT-23

Table 8. Suitable Analog Devices Precision Operational Amplifier

Part No.	Supply Voltage (V)	V_{OS} (Max) (µV)	I_B (Max) (nA)	0.1 Hz to 10 Hz Noise (µV p-p)	Supply Current (µA)	Package
OP97	±2 to ±20	25	0.1	0.5	600	SOIC-8
OP1177	±2.5 to ±15	60	2	0.4	500	MSOP, SOIC-8
AD8551	2.7 to 5	5	0.05	1	975	MSOP, SOIC-8
AD8603	1.8 to 6	50	0.001	2.3	50	TSOT
AD8628	2.7 to 6	5	0.1	0.5	850	TSOT, SOIC-8

Table 9. Suitable Analog Devices High Speed Operational Amplifier

Part No.	Supply Voltage (V)	BW at ACL (MHz)	Slew Rate (V/µs)	VOS (Max) (µV)	I_B (Max) (nA)	Package
AD8065	5 to 24	145	180	1500	0.006	SOIC-8, SOT-23, MSOP
AD8021	±2.5 to ±12	490	120	1000	10500	SOIC-8, MSOP
AD8038	3 to 12	350	425	3000	750	SOIC-8, SC70-5
AD9631	±3 to ±6	320	1300	10000	7000	SOIC-8

SERIAL INTERFACE

The AD5450/AD5451/AD5452/AD5453 have an easy to use 3-wire interface that is compatible with SPI, QSPI, MICROWIRE, and most DSP interface standards. Data is written to the device in 16-bit words. This 16-bit word consists of two control bits and 8, 10, 12, or 14 data bits, as shown in Figure 49, Figure 50, Figure 51, and Figure 52. The AD5453 uses all 14 bits of DAC data, the AD5452 uses 12 bits and ignores the two LSBs, the AD5451 uses 10 bits and ignores the four LSBs, and the AD5450 uses 8 bits and ignores the six LSBs.

DAC Control Bits C1, C0

Control Bits C1 and C0 allow the user to load and update the new DAC code and to change the active clock edge. By default, the shift register clocks data upon the falling edge; this can be changed via the control bits. If changed, the DAC core is inoperative until the next data frame, and a power recycle is required to return it to active on the falling edge. A power cycle resets the core to default condition. On-chip power-on reset circuitry ensures that the device powers on with zero scale loaded to the DAC register and I_{OUT} line.

Table 10. DAC Control Bits

C1	C0	Function Implemented
0	0	Load and update (power-on default)
0	1	Reserved
1	0	Reserved
1	1	Clock data to shift register upon rising edge

$\overline{SYNC}$ Function

$\overline{SYNC}$ is an edge triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred to the device while $\overline{SYNC}$ is low. To start the serial data transfer, $\overline{SYNC}$ should be taken low, observing the minimum $\overline{SYNC}$ falling to SCLK falling edge setup time, t_4. To minimize the power consumption of the device, the interface powers up fully only when the device is being written to, that is, upon the falling edge of $\overline{SYNC}$. The SCLK and SDIN input buffers are powered down upon the rising edge of $\overline{SYNC}$.

After the falling edge of the 16th SCLK pulse, bring $\overline{SYNC}$ high to transfer data from the input shift register to the DAC register.

The serial interface to the AD5450 uses a 16-bit shift register. Take care to avoid incomplete data sequences as these will be latched to update the DAC output.

For example,

- Loading 0x3FFF (a complete data sequence) will update the output to 10 V (full scale).
- User intends to write 0x3200 but after 12 active edges $\overline{SYNC}$ goes high (incomplete write sequence). This will update the following code: 0xF200.
- The user expects an output of 5.6 V. However, if $\overline{SYNC}$ goes high after 12 valid clock edges then an incomplete data sequence of 12 bits is loaded. To complete the shift register the 4 LSBs from the previous sequence are taken and used as the 4 MSBs missing. The addition of these 4 bits will put the device in rising edge mode and the output will show no change. Figure 53, Figure 54, and Table 11 show the data frames for this example.

Also note that if more then 16-bits are loaded to the device before $\overline{SYNC}$ goes high the last 16-bits will be latched.

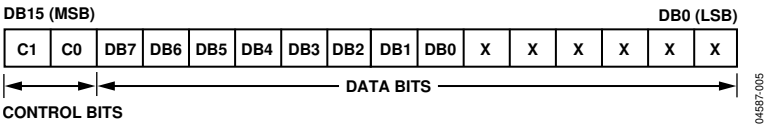

Figure 49. AD5450 8-Bit Input Shift Register Contents

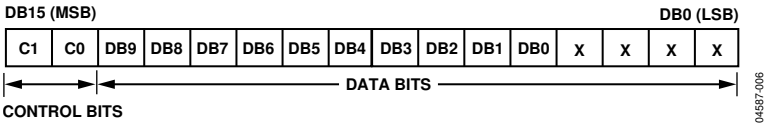

Figure 50. AD5451 10-Bit Input Shift Register Contents

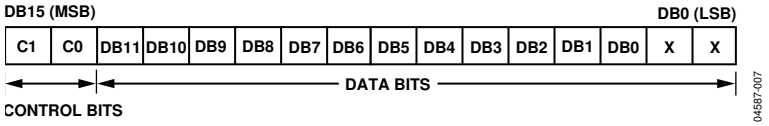

Figure 51. AD5452 12-Bit Input Shift Register Contents

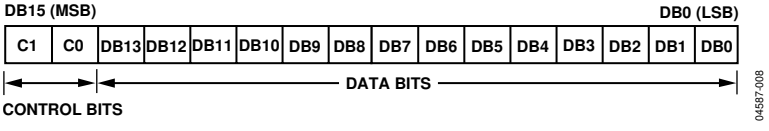

Figure 52. AD5453 14-Bit Input Shift Register Contents

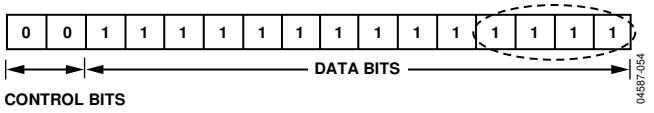

Figure 53. AD5453 First Write, Complete Data Sequence (0x3FFF)

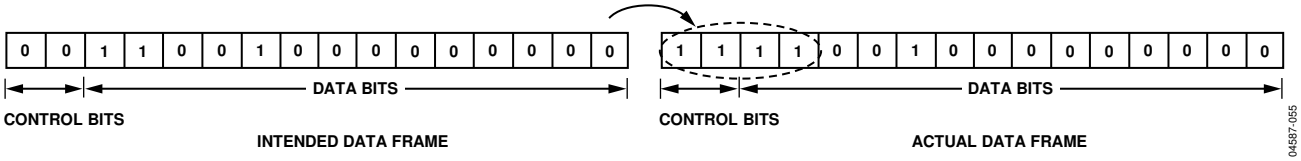

Figure 54. AD5453 Second Write, Incomplete Data Sequence (0x3200) and Subsequent Additional Bits (0xF200)

Table 11.

Writing Sequence	Data Write in Shift Register	Action Expected	Data Transfer to the Device	Action Carried Out
1	0x3FFF	Load and update 0x3FFF	0x3FFF	Load and update 0x3FFF
2	0x3200	Load and update 0x3200	0xF200	Clock data to shift register upon rising edge (0xF200)

MICROPROCESSOR INTERFACING

Microprocessor interfacing to a AD5450/AD5451/AD5452/AD5453 DAC is through a serial bus that uses standard protocol and is compatible with microcontrollers and DSP processors. The communication channel is a 3-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5450/AD5451/AD5452/AD5453 require a 16-bit word, with the default being data valid upon the falling edge of SCLK, but this is changeable using the control bits in the data-word.

ADSP-21xx Processors to AD5450/AD5451/AD5452/AD5453 Interface

The ADSP-21xx device family of DSPs is easily interfaced to a AD5450/AD5451/AD5452/AD5453 DAC without the need for extra glue logic. Figure 55 is an example of an SPI interface between the DAC and the ADSP-2191M. SCK of the DSP drives the serial data line, SDIN. $\overline{\text{SYNC}}$ is driven from one of the port lines, in this case $\overline{\text{SPIxSEL}}$.

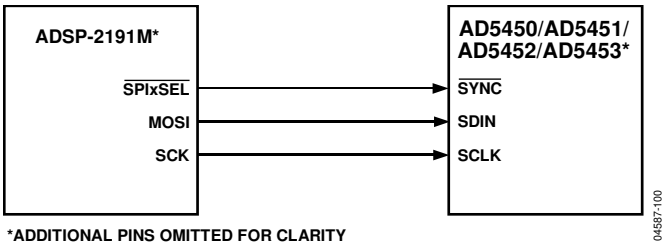

Figure 55. ADSP-2191M SPI to AD5450/AD5451/AD5452/AD5453 Interface

A serial interface between the DAC and DSP SPORT is shown in Figure 56. In this example, SPORT0 is used to transfer data to the DAC shift register. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. In a write sequence, data is clocked out upon each rising edge of the DSP's serial clock and clocked into the DAC input shift register upon the falling edge of its SCLK. The update of the DAC output takes place upon the rising edge of the $\overline{\text{SYNC}}$ signal.

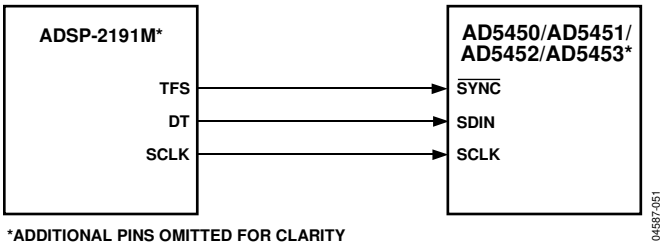

Figure 56. ADSP-2191M to AD5450/AD5451/AD5452/AD5453 Interface

Communication between two devices at a given clock speed is possible when the following specifications are compatible: frame $\overline{\text{SYNC}}$ delay and frame $\overline{\text{SYNC}}$ setup and hold, data delay and data setup and hold, and SCLK width. The DAC interface expects a t_4 ($\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time) of 13 ns minimum. See the ADSP-21xx device family for information on clock and frame $\overline{\text{SYNC}}$ frequencies for the SPORT register. Table 12 shows the setup for the SPORT control register.

Table 12. SPORT Control Register Setup

Name	Setting	Description
TFSW	1	Alternate framing
INVTFS	1	Active low frame signal
DTYPE	00	Right justify data
ISCLK	1	Internal serial clock
TFSR	1	Frame every word
ITFS	1	Internal framing signal
SLEN	1111	16-bit data-word

ADSP-BF504 to ADSP-BF592 Device Family to AD5450/AD5451/AD5452/AD5453 Interface

The ADSP-BF504 to ADSP-BF592 device family of processors has an SPI-compatible port that enables the processor to communicate with SPI-compatible devices. A serial interface between the BlackFin® processor and the AD5450/AD5451/AD5452/AD5453 DAC is shown in Figure 57. In this configuration, data is transferred through the MOSI (master output, slave input) pin. $\overline{\text{SYNC}}$ is driven by the $\overline{\text{SPIxSEL}}$ pin, which is a reconfigured programmable flag pin.

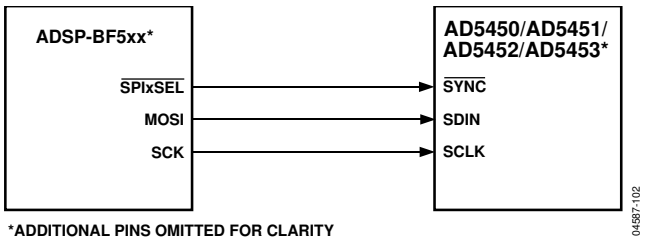

Figure 57. ADSP-BF504 to ADSP-BF592 Device Family to AD5450/AD5451/AD5452/AD5453 Interface (ADSP-BFxx Denotes the ADSP-BF504 to ADSP-BF592)

The ADSP-BF504 to ADSP-BF592 processors incorporate channel synchronous serial ports (SPORT). A serial interface between the DAC and the DSP SPORT is shown in Figure 58. When the SPORT is enabled, initiate transmission by writing a word to the Tx register. The data is clocked out upon each rising edge of the DSP's serial clock and clocked into the DAC's input shift register upon the falling edge its SCLK. The DAC output is updated by using the transmit frame synchronization (TFS) line to provide a $\overline{\text{SYNC}}$ signal.

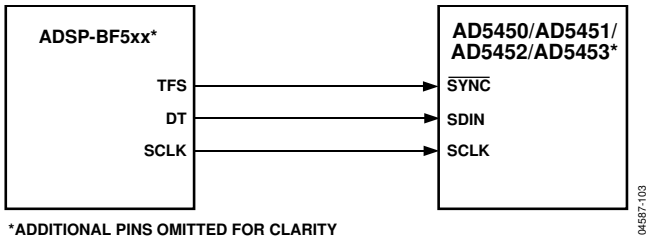

Figure 58. ADSP-BF504 to ADSP-BF592 Device Family SPORT to AD5450/AD5451/AD5452/AD5453 Interface (ADSP-BFxx Denotes the ADSP-BF504 to ADSP-BF592)

80C51/80L51 to AD5450/AD5451/AD5452/AD5453 Interface

A serial interface between the DAC and the 80C51/80L51 is shown in Figure 59. TxD of the 80C51/80L51 drives SCLK of the DAC serial interface, and RxD drives the serial data line, SDIN. P1.1 is a bit-programmable pin on the serial port and is used to drive $\overline{\text{SYNC}}$. As data is transmitted to the switch, P1.1 is taken low. The 80C51/80L51 transmit data only in 8-bit bytes; therefore, only eight falling clock edges occur in the transmit cycle.

To load data correctly to the DAC, P1.1 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. Data on RxD is clocked out of the microcontroller upon the rising edge of TxD and is valid upon the falling edge. As a result, no glue logic is required between the DAC and microcontroller interface. P1.1 is taken high following the completion of this cycle. The 80C51/80L51 provide the LSB of its SBUF register as the first bit in the data stream. The DAC input register acquires its data with the MSB as the first bit received. The transmit routine should take this into account.

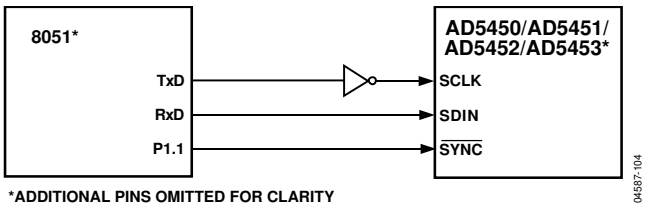

Figure 59. 80C51/80L51 to AD5450/AD5451/AD5452/AD5453 Interface

MC68HC11 to AD5450/AD5451/AD5452/AD5453 Interface

Figure 60 is an example of a serial interface between the DAC and the MC68HC11 microcontroller (Motorola). The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR) = 1, clock polarity bit (CPOL) = 0, and clock phase bit (CPHA) = 1. The SPI is configured by writing to the SPI control register (SPCR). SCK of the 68HC11 drives the SCLK of the DAC interface; the MOSI output drives the serial data line (SDIN) of the DAC.

The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). When data is being transmitted to the AD5450/AD5451/AD5452/AD5453, the $\overline{\text{SYNC}}$ line is taken low (PC7). Data appearing on the MOSI output is valid upon the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the DAC, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.

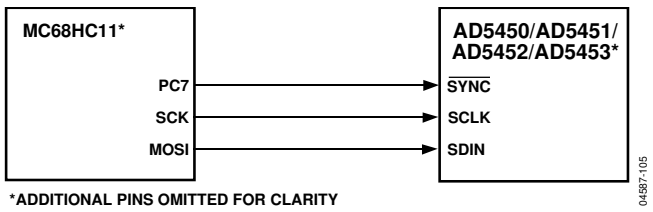

Figure 60. MC68HC11 to AD5450/AD5451/AD5452/AD5453 Interface

If the user wants to verify the data previously written to the input shift register, the SDO line can be connected to MISO of the MC68HC11. In this configuration with $\overline{\text{SYNC}}$ low, the shift register clocks data out upon the rising edges of SCLK.

MICROWIRE to AD5450/AD5451/AD5452/AD5453 Interface

Figure 61 shows an interface between the DAC and any MICROWIRE-compatible device. Serial data is shifted out upon the falling edge of the serial clock, SK, and is clocked into the DAC input shift register upon the rising edge of SK, which corresponds to the falling edge of the DAC's SCLK.

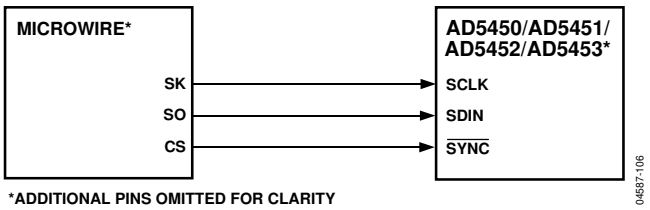

Figure 61. MICROWIRE to AD5450/AD5451/AD5452/AD5453 Interface

PIC16C6x/PIC16C7x to AD5450/AD5451/AD5452/AD5453 Interface

The PIC16C6x/PIC16C7x (Microchip) synchronous serial port (SSP) is configured as an SPI master with the clock polarity bit (CKP) = 0. This is done by writing to the synchronous serial port control register (SSPCON).

In this example, input/output Port RA1 is used to provide a $\overline{\text{SYNC}}$ signal and enable the serial port of the DAC. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, two consecutive write operations are required. Figure 62 shows the connection diagram.

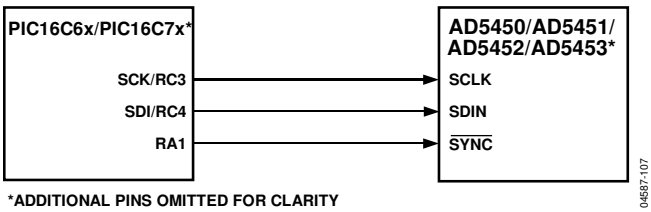

Figure 62. PIC16C6x/PIC16C7x to AD5450/AD5451/AD5452/AD5453 Interface

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which a AD5450/AD5451/AD5452/AD5453 DAC is mounted should be designed so the analog and digital sections are separated and confined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND to DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

These DACs should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Components, such as clocks, that produce fast switching signals should be shielded with a digital ground to avoid radiating noise to other devices of the board and should never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is the best solution, but its use is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane and signal traces are placed on the solder side.

It is good practice to employ compact, minimum lead length PCB layout design. Leads to the input should be as short as possible to minimize IR drops and stray inductance.

The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error. To optimize high frequency performance, the I-to-V amplifier should be located as close to the device as possible.

Table 13. Overview of the AD5405 to AD5453 Device Family and the AD5543 to AD5557 Device Family

Part No.	Resolution	No. DACs	INL (LSB)	Interface	Package[1]	Features
AD5424	8	1	±0.25	Parallel	RU-16, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5426	8	1	±0.25	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5428	8	2	±0.25	Parallel	RU-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5429	8	2	±0.25	Serial	RU-10	10 MHz BW, 50 MHz serial
AD5450	8	1	±0.25	Serial	UJ-8	12 MHZ BW, 50 MHz serial interface
AD5432	10	1	±0.5	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5433	10	1	±0.5	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5439	10	2	±0.5	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5440	10	2	±0.5	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5451	10	1	±0.25	Serial	UJ-8	12 MHz BW, 50 MHz serial interface
AD5443	12	1	±1	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5444	12	1	±0.5	Serial	RM-10	12 MHz BW, 50 MHz serial
AD5415	12	2	±1	Serial	RU-24	10 MHz BW, 50 MHz serial
AD5405	12	2	±1	Parallel	CP-40	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5445	12	2	±1	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5447	12	2	±1	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5449	12	2	±1	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5452	12	1	±0.5	Serial	UJ-8, RM-8	12 MHz BW, 50 MHz serial interface
AD5446	14	1	±1	Serial	RM-10	12 MHz BW, 50 MHz serial
AD5453	14	1	±2	Serial	UJ-8, RM-8	12 MHz BW, 50 MHz serial
AD5553	14	1	±1	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5556	14	1	±1	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5555	14	2	±1	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5557	14	2	±1	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5543	16	1	±2	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5546	16	1	±2	Parallel	RU-28	4 MHz BW, 20 n $\overline{WR}$ pulse width
AD5545	16	2	±2	Serial	RU-16	4 MHz BW, 50 MHz serial clock
AD5547	16	2	±2	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ pulse width

[1] RU = TSSOP, CP = LFCSP, RM = MSOP, UJ = TSOT.