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Quad Parametric Measurement Unit with Integrated 16-Bit Level Setting DACs

Data Sheet

AD5522

FEATURES

- Quad parametric measurement unit (PMU)
  - FV, FI, FN (high-Z), MV, MI functions
- 4 programmable current ranges (internal R_{SENSE})
  - ±5 µA, ±20 µA, ±200 µA, and ±2 mA
- 1 programmable current range up to ±80 mA (external R_{SENSE})
- 22.5 V FV range with asymmetrical operation
- Integrated 16-bit DACs provide programmable levels
- Gain and offset correction on chip
- Low capacitance outputs suited to relayless systems
- On-chip comparators per channel
- FI voltage clamps and FV current clamps
- Guard drive amplifier
- System PMU connections
- Programmable temperature shutdown
- SPI- and LVDS-compatible interfaces
- Compact 80-lead TQFP with exposed pad (top or bottom)

APPLICATIONS

- Automated test equipment (ATE)
  - Per-pin parametric measurement unit
  - Continuity and leakage testing
  - Device power supply
- Instrumentation
  - Source measure unit (SMU)
  - Precision measurement

FUNCTIONAL BLOCK DIAGRAM

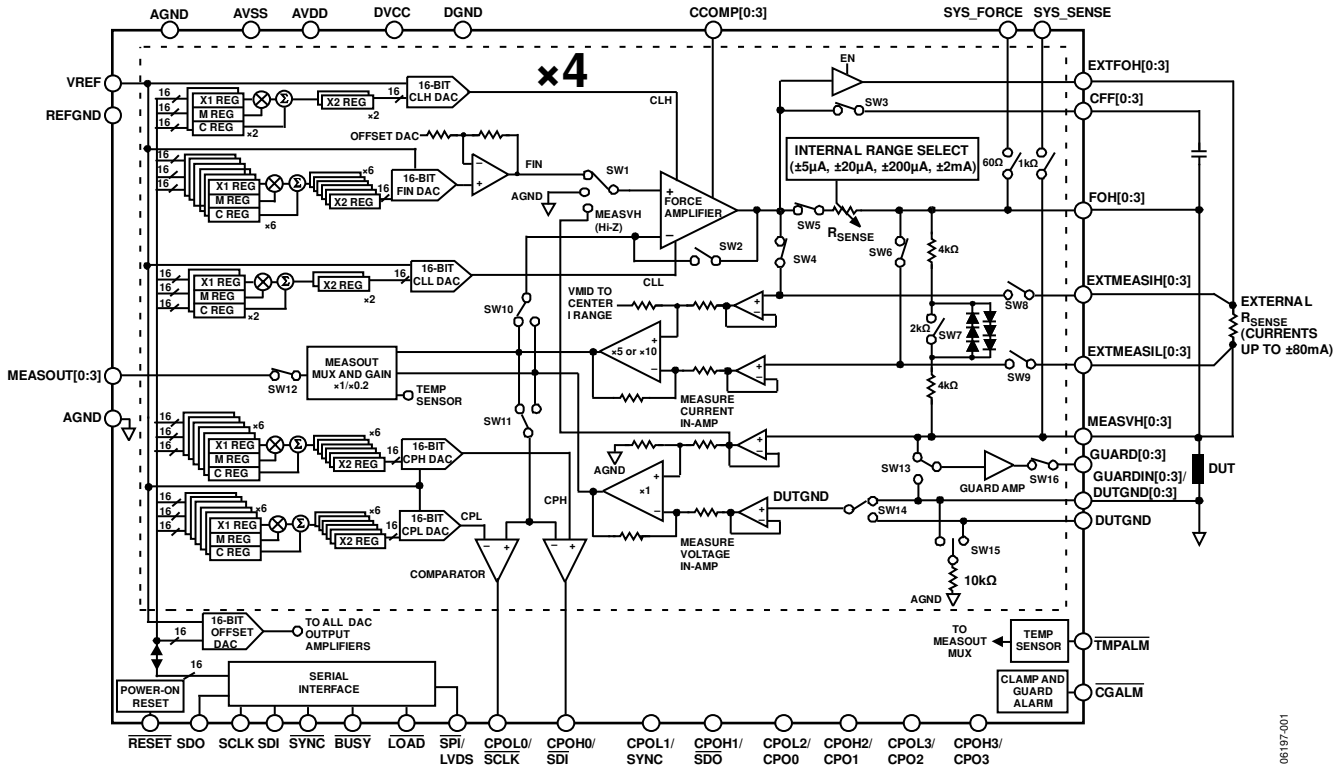

Figure 1.

Rev. E

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COMPARABLE PARTS

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EVALUATION KITS

- AD5522 Evaluation Board

DOCUMENTATION

Data Sheet

- AD5522: Quad Parametric Measurement Unit with Integrated 16-Bit Level Setting DACs Datasheet

User Guides

- User Guide for the AD5522 Evaluation board

REFERENCE DESIGNS

- CN0104

DESIGN RESOURCES

- AD5522 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD5522 EngineerZone Discussions.

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7/08—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD5522 is a high performance, highly integrated parametric measurement unit consisting of four independent channels. Each per-pin parametric measurement unit (PPMU) channel includes five 16-bit, voltage output DACs that set the programmable input levels for the force voltage inputs, clamp inputs, and comparator inputs (high and low). Five programmable force and measure current ranges are available, ranging from ±5 μA to ±80 mA. Four of these ranges use on-chip sense resistors; one high current range up to ±80 mA is available per channel using off-chip sense resistors. Currents in excess of ±80 mA require an external amplifier. Low capacitance DUT connections (FOHx and EXTFOHx) ensure that the device is suited to relayless test systems.

The PMU functions are controlled via a simple 3-wire serial interface compatible with SPI, QSPI™, MICROWIRE™, and DSP interface standards. Interface clocks of 50 MHz allow fast updating of modes. The low voltage differential signaling (LVDS) interface protocol at 83 MHz is also supported. Comparator outputs are provided per channel for device go-no-go testing and characterization. Control registers allow the user to easily change force or measure conditions, DAC levels, and selected current ranges. The SDO (serial data output) pin allows the user to read back information for diagnostic purposes.

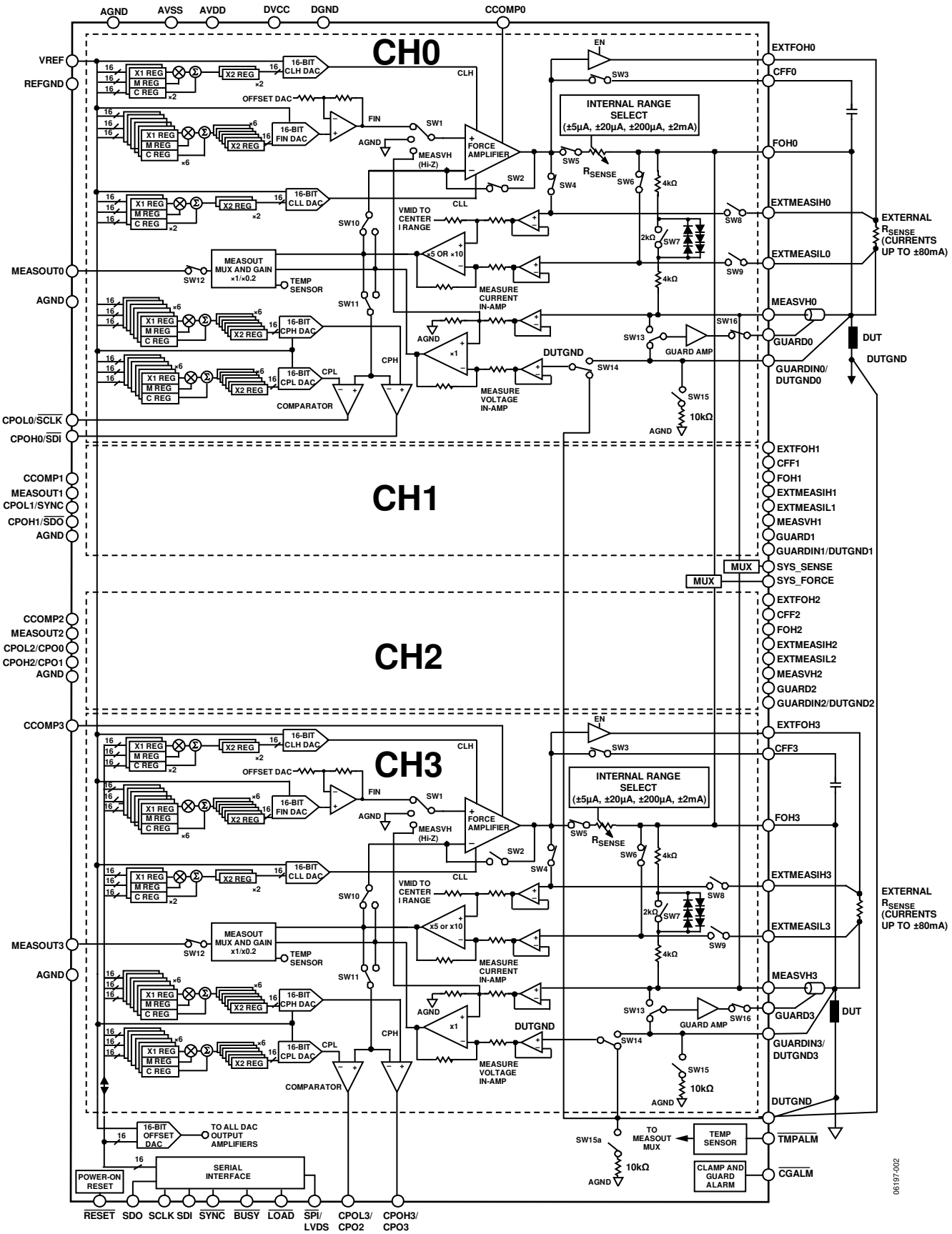


Figure 2. Detailed Block Diagram

SPECIFICATIONS

AVDD ≥ 10 V; AVSS ≤ −5 V; |AVDD − AVSS| ≥ 20 V and ≤ 33 V; DVCC = 2.3 V to 5.25 V; VREF = 5 V; REFGND = DUTGND = AGND = 0 V; gain (M), offset (C), and DAC offset registers at default values; T_J = 25°C to 90°C, unless otherwise noted. (FV = force voltage, FI = force current, MV = measure voltage, MI = measure current, FS = full scale, FSR = full-scale range, FSVR = full-scale voltage range, FSCR = full-scale current range.)

Table 1.

Parameter	Min	Typ [1]	Max	Unit	Test Conditions/Comments
FORCE VOLTAGE					
FOHx Output Voltage Range[2]	AVSS + 4		AVDD − 4	V	All current ranges from FOHx at full-scale current; includes ±1 V dropped across sense resistor
EXTFOHx Output Voltage Range[2]	AVSS + 3		AVDD − 3	V	External high current range at full-scale current; does not include ±1 V dropped across sense resistor
Output Voltage Span		22.5		V	
Offset Error	−50		+50	mV	Measured at midscale code; prior to calibration
Offset Error Tempco[2]		−10		µV/°C	Standard deviation = 20 µV/°C
Gain Error	−0.5		+0.5	% FSR	Prior to calibration
Gain Error Tempco[2]		0.5		ppm/°C	Standard deviation = 0.5 ppm/°C
Linearity Error	−0.01		+0.01	% FSR	FSR = full-scale range (±10 V), gain and offset errors calibrated out
Short-Circuit Current Limit[2]	−150		+150	mA	±80 mA range
	−10		+10	mA	All other ranges
Noise Spectral Density (NSD)[2]		320		nV/√Hz	1 kHz, at FOHx in FV mode
MEASURE CURRENT					Measure current = (I_{DUT} × R_{SENSE} × gain); amplifier gain = 5 or 10, unless otherwise noted
Differential Input Voltage Range[2]	−1.125		+1.125	V	Voltage across R_{SENSE}; gain = 5 or 10
Output Voltage Span		22.5		V	Measure current block with VREF = 5 V, MEASOUT scaling happens after
Offset Error	−0.5		+0.5	% FSCR	V(R_{SENSE}) = ±1 V, measured with zero current flowing
Offset Error Tempco[2]		1		µV/°C	Referred to MI input; standard deviation = 4 µV/°C
Gain Error	−1		+1	% FSCR	Using internal current ranges
	−0.5		+0.5	% FSCR	Measure current amplifier alone
Gain Error Tempco[2]		−2		ppm/°C	Standard deviation = 2 ppm/°C Measure current amplifier alone; internal sense resistor 25 ppm/°C
Linearity Error (MEASOUTx Gain = 1)	−0.015		+0.015	% FSR	MI gain = 10
	−0.01		+0.01	% FSR	MI gain = 5
Linearity Error (MEASOUTx Gain = 0.2)	−0.06		+0.06	% FSR	MI gain = 10, AVDD = 28 V, AVSS = −5 V, offset DAC = 0x0
	−0.11		+0.11	% FSR	MI gain = 10, AVDD = 10 V, AVSS = −23 V, offset DAC = 0x0EDB7
	−0.015		+0.015	% FSR	MI gain = 10, AVDD = 15.25 V, AVSS = −15.25 V, offset DAC = 0xA492
	−0.06		+0.06	% FSR	MI gain = 5, AVDD = 28 V, AVSS = −5 V, offset DAC = 0x0
	−0.01		+0.01	% FSR	MI gain = 5, AVDD = 10 V, AVSS = −23 V, offset DAC = 0xEDB7
	−0.01		+0.01	% FSR	MI gain = 5, AVDD = 15.25 V, AVSS = −15.25 V, offset DAC = 0xA492
Common-Mode Voltage Range[2]	AVSS + 4		AVDD − 4	V	
Common-Mode Error (Gain = 5)	−0.01		+0.01	% FSCR/V	% of full-scale change at force output per V change in DUT voltage
Common-Mode Error (Gain = 10)	−0.005		+0.005	% FSCR/V	% of full-scale change at force output per V change in DUT voltage
Sense Resistors					Sense resistors are trimmed to within 1%
		200		kΩ	±5 µA range
		50		kΩ	±20 µA range
		5		kΩ	±200 µA range
		0.5		kΩ	±2 mA range

Parameter	Min	Typ [1]	Max	Unit	Test Conditions/Comments
Measure Current Ranges[2]					Specified current ranges are achieved with VREF = 5 V and MI gain = 10, or with VREF = 2.5 V and MI gain = 5
		±5		µA	Set using internal sense resistor
		±20		µA	Set using internal sense resistor
		±200		µA	Set using internal sense resistor
		±2		mA	Set using internal sense resistor
			±80	mA	Set using external sense resistor; internal amplifier can drive up to ±80 mA
Noise Spectral Density (NSD)[2]		400		nV/√Hz	1 kHz, MI amplifier only, inputs grounded
FORCE CURRENT					
Voltage Compliance, FOHx[2]	AVSS + 4		AVDD − 4	V	
Voltage Compliance, EXTFOHx[2]	AVSS + 3		AVDD − 3	V	
Offset Error	−0.5		+0.5	% FSCR	Measured at midscale code, 0 V, prior to calibration
Offset Error Tempco[2]		5		ppm FS/°C	Standard deviation = 5 ppm/°C
Gain Error	−1.5		+1.5	% FSCR	Prior to calibration
Gain Error Tempco[2]		−6		ppm/°C	Standard deviation = 5 ppm/°C
Linearity Error	−0.02		+0.02	% FSCR	
Common-Mode Error (Gain = 5)	−0.01		+0.01	% FSCR/V	% of full-scale change per V change in DUT voltage
Common-Mode Error (Gain = 10)	−0.006		+0.006	% FSCR/V	% of full-scale change per V change in DUT voltage
Force Current Ranges					Specified current ranges achieved with VREF = 5 V and MI gain = 10, or with VREF = 2.5 V and MI gain = 5 V
		±5		µA	Set using internal sense resistor, 200 kΩ
		±20		µA	Set using internal sense resistor, 50 kΩ
		±200		µA	Set using internal sense resistor, 5 kΩ
		±2		mA	Set using internal sense resistor, 500 Ω
			±80	mA	Set using external sense resistor; internal amplifier can drive up to ±80 mA
MEASURE VOLTAGE					
Measure Voltage Range[2]	AVSS + 4		AVDD − 4	V	
Offset Error	−10		+10	mV	Gain = 1, measured at 0 V
	−25		+25	mV	Gain = 0.2, measured at 0 V
Offset Error Tempco[2]		−1		µV/°C	Standard deviation = 6 µV/°C
Gain Error	−0.25		+0.25	% FSR	MEASOUTx gain = 1
	−0.5		+0.5	% FSR	MEASOUTx gain = 0.2
Gain Error Tempco[2]		1		ppm/°C	Standard deviation = 4 ppm/°C
Linearity Error (MEASOUTx Gain = 1)	−0.01		+0.01	% FSR	
Linearity Error (MEASOUTx Gain = 0.2)	−0.01		+0.01	% FSR	AVDD = 15.25 V, AVSS = −15.25 V, offset DAC = 0xA492
	−0.06		+0.06	% FSR	AVDD = 28 V, AVSS = −5 V, offset DAC = 0x0
	−0.1		+0.1	% FSR	AVDD = −10 V, AVSS = −23 V, offset DAC = 0x3640
Noise Spectral Density (NSD)[2]		100		nV/√Hz	1 kHz; measure voltage amplifier only, inputs grounded
OFFSET DAC					
Span Error		±30		mV	
COMPARATOR					
Comparator Span		22.5		V	
Offset Error	−2	+1	+2	mV	Measured directly at comparator; does not include measure block errors
Offset Error Tempco[2]		1		µV/°C	Standard deviation = 2 µV/°C
Propagation Delay[2]		0.25		µs	
VOLTAGE CLAMPS					
Clamp Span		22.5		V	
Positive Clamp Accuracy			155	mV	
Negative Clamp Accuracy	−155			mV	
CLL to CLH[2]	500			mV	CLL < CLH and minimum voltage apart
Recovery Time[2]		0.5	1.5	µs	
Activation Time[2]		1.5	3	µs	

Parameter	Min	Typ [1]	Max	Unit	Test Conditions/Comments
CURRENT CLAMPS					
Clamp Accuracy	Programmed clamp value		Programmed clamp value ± 10	% FSC	MI gain = 10, clamp current scales with selected range
	Programmed clamp value		Programmed clamp value ± 20	% FSC	MI gain = 5, clamp current scales with selected range
CLL to CLH[2]	5			% of I_{RANGE}	CLL < CLH and minimum setting apart, MI gain = 10
	10			% of I_{RANGE}	CLL < CLH and minimum setting apart, MI gain = 5
Recovery Time[2]		0.5	1.5	µs	
Activation Time[2]		1.5	3	µs	
FOHx, EXTFOHx, EXTMEASILx, EXTMEASIHx, CFFx PINS					
Pin Capacitance[2]		10		pF	
Leakage Current	−3		+3	nA	Individual pin on or off switch leakage, measured with ±11 V stress applied to pin, channel enabled, but tristate
Leakage Current Tempco[2]		±0.01		nA/°C	
MEASVHx PIN					
Pin Capacitance[2]		3		pF	
Leakage Current	−3		+3	nA	Measured with ±11 V stress applied to pin, channel enabled, but tristate
Leakage Current Tempco[2]		±0.01		nA/°C	
SYS_SENSE PIN					SYS_SENSE connected, force amplifier inhibited
Pin Capacitance[2]		3		pF	
Switch Impedance		1	1.3	kΩ	
Leakage Current	−3		+3	nA	Measured with ±11 V stress applied to pin, switch off
Leakage Current Tempco[2]		±0.01		nA/°C	
SYS_FORCE PIN					SYS_FORCE connected, force amplifier inhibited
Pin Capacitance[2]		6		pF	
Switch Impedance		60	80	Ω	
Leakage Current	−3		+3	nA	Measured with ±11 V stress applied to pin, switch off
Leakage Current Tempco[2]		±0.01		nA/°C	
COMBINED LEAKAGE AT DUT					Includes FOHx, MEASVHx, SYS_SENSE, SYS_FORCE, EXTMEASILx, EXTMEASIHx, EXTFOHx, and CFFx; calculation of all the individual leakage contributors
Leakage Current	−15		+15	nA	T_J = 25°C to 70°C
	−25		+25	nA	T_J = 25°C to 90°C
Leakage Current Tempco[2]		±0.1		nA/°C	
DUTGNDx PIN					
Voltage Range	−500		+500	mV	
Leakage Current	−30		+30	nA	
MEASOUTx PIN					With respect to AGND
Output Voltage Span		22.5		V	Software programmable output range
Output Impedance		60	80	Ω	
Output Leakage Current	−3		+3	nA	With SW12 off
Output Capacitance[2]			15	pF	
Maximum Load Capacitance[2]			0.5	µF	
Output Current Drive[2]		2		mA	
Short-Circuit Current	−10		+10	mA	
Slew Rate[2]		2		V/µs	
Enable Time[2]		150	320	ns	Closing SW12, measured from $\overline{BUSY}$ rising edge
Disable Time[2]		400	1100	ns	Opening SW12, measured from $\overline{BUSY}$ rising edge
MI to MV Switching Time[2]		200		ns	Measured from $\overline{BUSY}$ rising edge; does not include slewing or settling

Parameter	Min	Typ [1]	Max	Unit	Test Conditions/Comments
GUARDx PIN					
Output Voltage Span		22.5		V	
Output Offset	−10		+10	mV	
Short-Circuit Current	−15		+15	mA	
Maximum Load Capacitance[2]			100	nF	
Output Impedance		85		Ω	
Tristate Leakage Current[2]	−30		+30	nA	When guard amplifier is disabled
Slew Rate[2]		5		V/µs	C_{LOAD} = 10 pF
Alarm Activation Time[2]		200		µs	Alarm delayed to eliminate false alarms
FORCE AMPLIFIER[2]					
Slew Rate		0.4		V/µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
Gain Bandwidth		1.3		MHz	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
Max Stable Load Capacitance			10,000	pF	CCOMPx = 100 pF, larger C_{LOAD} requires larger CCOMP capacitor
			100	nF	CCOMPx = 1 nF, larger C_{LOAD} requires larger CCOMP capacitor
FV SETTLING TIME TO 0.05% OF FS[2]					Midscale to full-scale change; measured from $\overline{SYNC}$ rising edge, clamps on
±80 mA Range		22	40	µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±2 mA Range		24	40	µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±200 µA Range		40	80	µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±20 µA Range		300		µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±5 µA Range		1400		µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
MI SETTLING TIME TO 0.05% OF FS[2]					Midscale to full-scale change; driven from force amplifier in FV mode, so includes FV settling time; measured from $\overline{SYNC}$ rising edge, clamps on
±80 mA Range		22	40	µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±2 mA Range		24	40	µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±200 µA Range		60	100	µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±20 µA Range		462		µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±5 µA Range		1902		µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
FI SETTLING TIME TO 0.05% OF FS[2]					Midscale to full-scale change; measured from $\overline{SYNC}$ rising edge, clamps on
±80 mA Range		24	55	µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±2 mA Range		24	60	µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±200 µA Range		50	120	µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±20 µA Range		450		µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±5 µA Range		2700		µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
MV SETTLING TIME TO 0.05% OF FS[2]					Midscale to full-scale change; driven from force amplifier in FV mode, so includes FV settling time; measured from $\overline{SYNC}$ rising edge, clamps on
±80 mA Range		24	55	µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±2 mA Range		24	60	µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±200 µA Range		50	120	µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±20 µA Range		450		µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±5 µA Range		2700		µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
DAC SPECIFICATIONS					
Resolution			16	Bits	
Output Voltage Span[2]		22.5		V	VREF = 5 V, within a range of −16.25 V to +22.5 V
Differential Nonlinearity[2]	−1		+1	LSB	Guaranteed monotonic by design over temperature
COMPARATOR DAC DYNAMIC SPECIFICATIONS[2]					
Output Voltage Settling Time		1		µs	500 mV change to ±½ LSB
Slew Rate		5.5		V/µs	
Digital-to-Analog Glitch Energy		20		nV-sec	
Glitch Impulse Peak Amplitude		10		mV	
REFERENCE INPUT					
VREF DC Input Impedance	1	100		MΩ	
VREF Input Current	−10	+0.03	+10	µA	
VREF Range[2]	2		5	V	

Parameter	Min	Typ [1]	Max	Unit	Test Conditions/Comments
DIE TEMPERATURE SENSOR					
Accuracy[2]		±7		°C	
Output Voltage at 25°C		1.5		V	
Output Scale Factor[2]		4.6		mV/°C	
Output Voltage Range[2]	0		3	V	
INTERACTION AND CROSSTALK[2]					
DC Crosstalk (FOHx)		0.05	0.65	mV	DC change resulting from a dc change in any DAC in the device, FV and FI modes, ±2 mA range, C_{LOAD} = 200 pF, R_{LOAD} = 5.6 kΩ
DC Crosstalk (MEASOUTx)		0.05	0.65	mV	DC change resulting from a dc change in any DAC in the device, MV and MI modes, ±2 mA range, C_{LOAD} = 200 pF, R_{LOAD} = 5.6 kΩ
DC Crosstalk Within a Channel		0.05		mV	All channels in FVMI mode, one channel at midscale; measure the current for one channel in the lowest current range for a change in comparator or clamp DAC levels for that PMU
SPI INTERFACE LOGIC INPUTS					
Input High Voltage, V_{IH}	1.7/2.0			V	(2.3 V to 2.7 V)/(2.7 V to 5.25 V), JEDEC-compliant input levels
Input Low Voltage, V_{IL}			0.7/0.8	V	(2.3 V to 2.7 V)/(2.7 V to 5.25 V), JEDEC-compliant input levels
Input Current, I_{INH}, I_{INL}	−1		+1	µA	
Input Capacitance, C_{IN}[2]			10	pF	
CMOS LOGIC OUTPUTS					SDO, CPOx
Output High Voltage, V_{OH}	DVCC − 0.4			V	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
Tristate Leakage Current	−2		+2	µA	SDO, CPOH1/$\overline{SDO}$
	−1		+1	µA	All other output pins
Output Capacitance[2]			10	pF	
OPEN-DRAIN LOGIC OUTPUTS					$\overline{BUSY}$, $\overline{TMPALM}$, $\overline{CGALM}$
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA, C_{LOAD} = 50 pF, R_{PULLUP} = 1 kΩ
Output Capacitance[2]			10	pF	
LVDS INTERFACE LOGIC INPUTS REDUCED RANGE LINK[2]					
Input Voltage Range	875		1575	mV	
Input Differential Threshold	−100		+100	mV	
External Termination Resistance	80	100	120	Ω	
Differential Input Voltage	100			mV	
LVDS INTERFACE LOGIC OUTPUTS REDUCED RANGE LINK					
Output Offset Voltage		1200		mV	
Output Differential Voltage		400		mV	
POWER SUPPLIES					
AVDD	10		28	V	|AVDD − AVSS| ≤ 33 V
AVSS	−23		−5	V	
DVCC	2.3		5.25	V	
AI_{DD}			26	mA	Internal ranges (±5 µA to ±2 mA), excluding load conditions; comparators and guard disabled
AI_{SS}	−26			mA	Internal ranges (±5 µA to ±2 mA), excluding load conditions; comparators and guard disabled
AI_{DD}			28	mA	Internal ranges (±5 µA to ±2 mA), excluding load conditions; comparators and guard enabled
AI_{SS}	−28			mA	Internal ranges (±5 µA to ±2 mA), excluding load conditions; comparators and guard enabled
AI_{DD}			36	mA	External range, excluding load conditions
AI_{SS}	−36			mA	External range, excluding load conditions
DI_{CC}			1.5	mA	
Maximum Power Dissipation[2]			7	W	Maximum power that should be dissipated in this package under worst-case load conditions; careful consideration should be given to supply selection and thermal design

Parameter	Min	Typ [1]	Max	Unit	Test Conditions/Comments
Power Supply Sensitivity[2]					From dc to 1 kHz
ΔForced Voltage/ΔAVDD		−80		dB	
ΔForced Voltage/ΔAVSS		−80		dB	
ΔMeasured Current/ΔAVDD		−85		dB	
ΔMeasured Current/ΔAVSS		−75		dB	
ΔForced Current/ΔAVDD		−75		dB	
ΔForced Current/ΔAVSS		−75		dB	
ΔMeasured Voltage/ΔAVDD		−85		dB	
ΔMeasured Voltage/ΔAVSS		−80		dB	
ΔForced Voltage/ΔDVCC		−90		dB	
ΔMeasured Current/ΔDVCC		−90		dB	
ΔForced Current/ΔDVCC		−90		dB	
ΔMeasured Voltage/ΔDVCC		−90		dB	

[1] Typical specifications are at 25°C and nominal supply, ±15.25 V, unless otherwise noted.
[2] Guaranteed by design and characterization; not production tested. Tempco values are mean and standard deviation, unless otherwise noted.

TIMING CHARACTERISTICS

AVDD ≥ 10 V, AVSS ≤ −5 V, |AVDD − AVSS| ≥ 20 V and ≤ 33 V, DVCC = 2.3 V to 5.25 V, VREF = 5 V, T_J = 25°C to 90°C, unless otherwise noted.

Table 2. SPI Interface

	DVCC, Limit at T_{MIN}, T_{MAX}				
Parameter [1, 2, 3]	**2.3 V to 2.7 V**	**2.7 V to 3.6 V**	**4.5 V to 5.25 V**	**Unit**	**Description**
t_{WRITE}[4]	1030	735	735	ns min	Single channel update cycle time (X1 register write)
	950	655	655	ns min	Single channel update cycle time (any other register write)
t_1	30	20	20	ns min	SCLK cycle time
t_2	8	8	8	ns min	SCLK high time
t_3	8	8	8	ns min	SCLK low time
t_4	10	10	10	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5[4]	150	150	150	ns min	Minimum $\overline{SYNC}$ high time in write mode after X1 register write (one channel)
	70	70	70	ns min	Minimum $\overline{SYNC}$ high time in write mode after any other register write
t_6	10	5	5	ns min	29th SCLK falling edge to $\overline{SYNC}$ rising edge
t_7	5	5	5	ns min	Data setup time
t_8	9	7	4.5	ns min	Data hold time
t_9	120	75	55	ns max	$\overline{SYNC}$ rising edge to $\overline{BUSY}$ falling edge
t_{10}					$\overline{BUSY}$ pulse width low for X1 and some PMU register writes; see Table 17 and Table 18
1 DAC X1	1.65	1.65	1.65	µs max	
2 DAC X1	2.3	2.3	2.3	µs max	
3 DAC X1	2.95	2.95	2.95	µs max	
4 DAC X1	3.6	3.6	3.6	µs max	
Other Registers	270	270	270	ns max	System control register/PMU registers
t_{11}	20	20	20	ns min	29th SCLK falling edge to $\overline{LOAD}$ falling edge
t_{12}	20	20	20	ns min	$\overline{LOAD}$ pulse width low
t_{13}	150	150	150	ns min	$\overline{BUSY}$ rising edge to FOHx output response time
t_{14}	0	0	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LOAD}$ falling edge
t_{15}	100	100	100	ns max	$\overline{LOAD}$ falling edge to FOHx output response time

Parameter [1, 2, 3]	DVCC, Limit at T_{MIN}, T_{MAX}			Unit	Description
	2.3 V to 2.7 V	2.7 V to 3.6 V	4.5 V to 5.25 V		
t_{16}	1.8	1.2	0.9	µs min	$\overline{\text{RESET}}$ pulse width low
t_{17}	670	700	750	µs max	$\overline{\text{RESET}}$ time indicated by $\overline{\text{BUSY}}$ low
t_{18}	400	400	400	ns min	Minimum $\overline{\text{SYNC}}$ high time in readback mode
t_{19} [5, 6]	60	45	25	ns max	SCLK rising edge to SDO valid; DVCC = 5 V to 5.25 V

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F = 2$ ns (10% to 90% of DVCC) and timed from a voltage level of 1.2 V.
[3] See Figure 5 and Figure 6.
[4] Writes to more than one X1 register engages the calibration engine for longer times, shown by the $\overline{\text{BUSY}}$ low time, t_{10}. Subsequent writes to one or more X1 registers should either be timed or should wait until $\overline{\text{BUSY}}$ returns high (see Figure 56). This is required to ensure that data is not lost or overwritten.
[5] t_{19} is measured with the load circuit shown in Figure 4.
[6] SDO output slows with lower DVCC supply and may require use of a slower SCLK.

Table 3. LVDS Interface

Parameter [1, 2, 3]	DVCC, Limit at T_{MIN}, T_{MAX}		Unit	Description
	2.7 V to 3.6 V	4.5 V to 5.25 V		
t_1	20	12	ns min	SCLK cycle time
t_2	8	5	ns min	SCLK pulse width high and low time
t_3	3	3	ns min	$\overline{\text{SYNC}}$ to SCLK setup time
t_4	3	3	ns min	Data setup time
t_5	5	3	ns min	Data hold time
t_6	3	3	ns min	SCLK to $\overline{\text{SYNC}}$ hold time
t_7 [4]	45	25	ns min	SCLK rising edge to SDO valid
t_8	150	150	ns min	Minimum $\overline{\text{SYNC}}$ high time in write mode after X1 register write
	70	70	ns min	Minimum $\overline{\text{SYNC}}$ high time in write mode after any other register write
	400	400	ns min	Minimum $\overline{\text{SYNC}}$ high time in readback mode

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F = 2$ ns (10% to 90% of DVCC) and timed from a voltage level of 1.2 V.
[3] See Figure 7.
[4] SDO output slows with lower DVCC supply and may require use of slower SCLK.

Circuit and Timing Diagrams

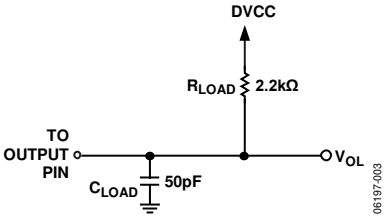


Figure 3. Load Circuit for $\overline{CGALM}$, $\overline{TMPALM}$

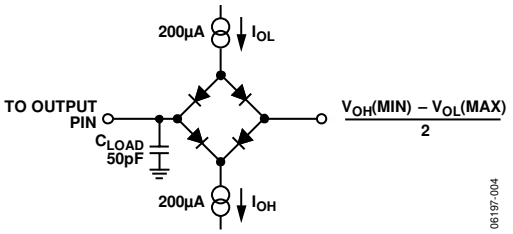


Figure 4. Load Circuit for SDO, $\overline{BUSY}$ Timing Diagram

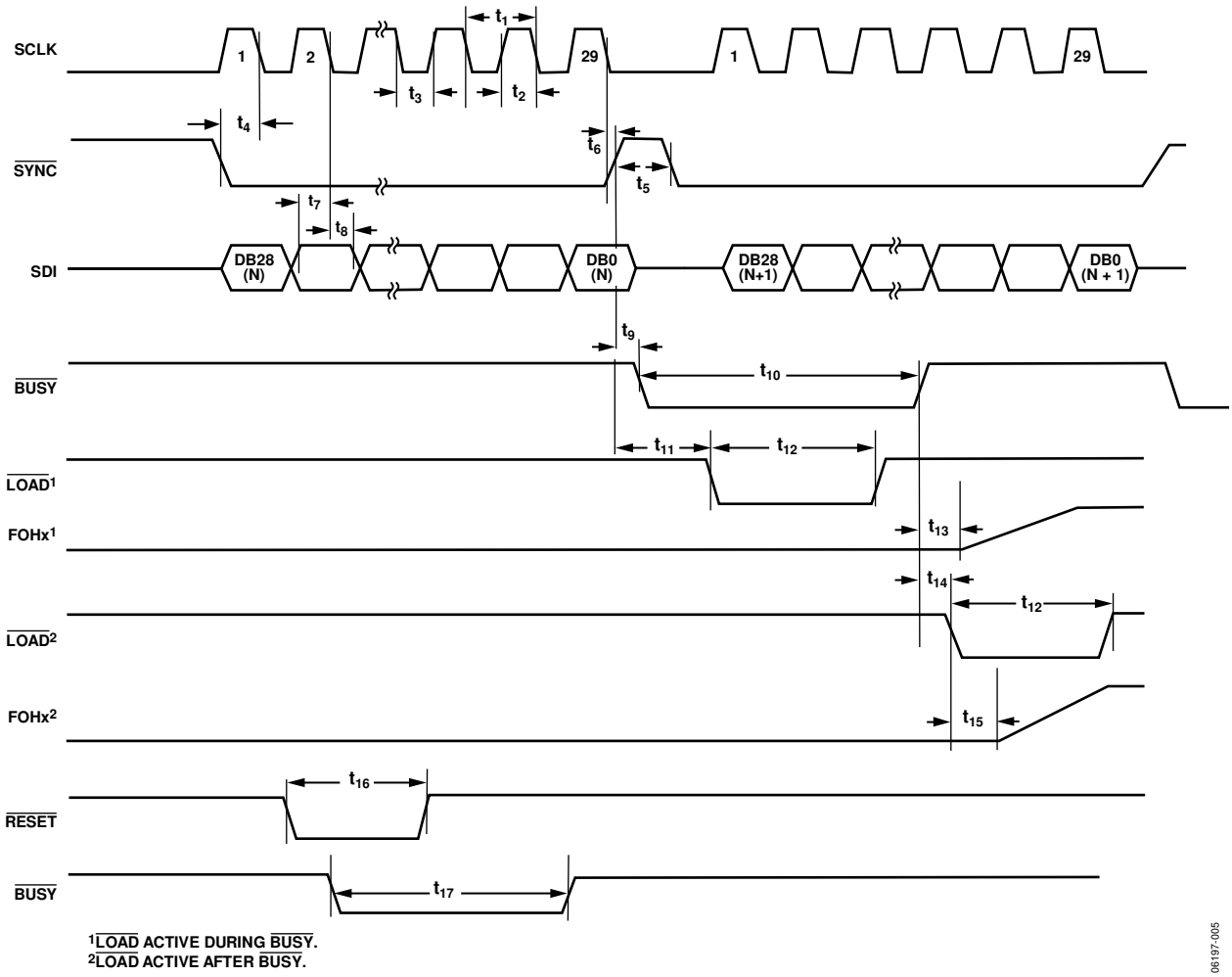


Figure 5. SPI Write Timing (Write Word Contains 29 Bits)

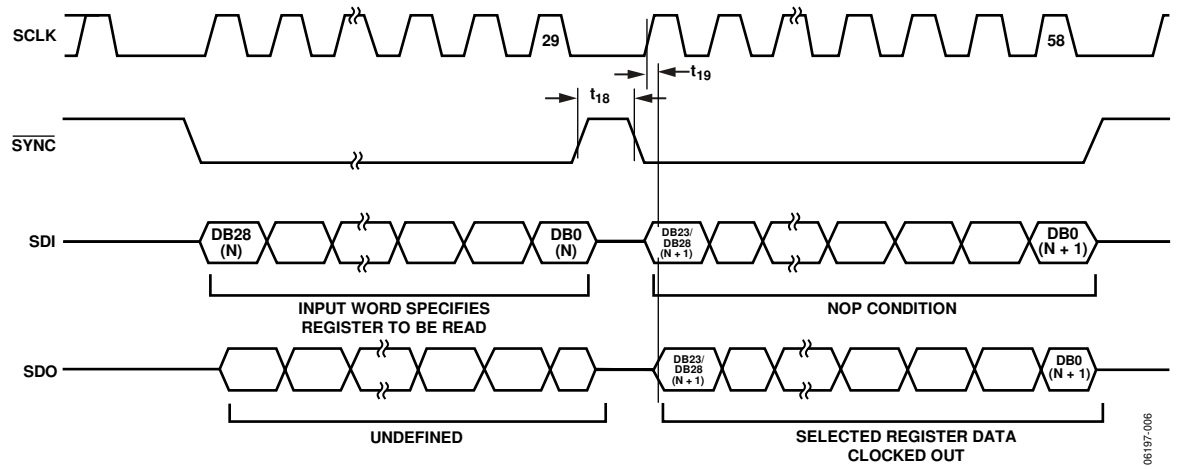


Figure 6. SPI Read Timing (Readback Word Contains 24 Bits and Can Be Clocked Out with a Minimum of 24 Clock Edges)

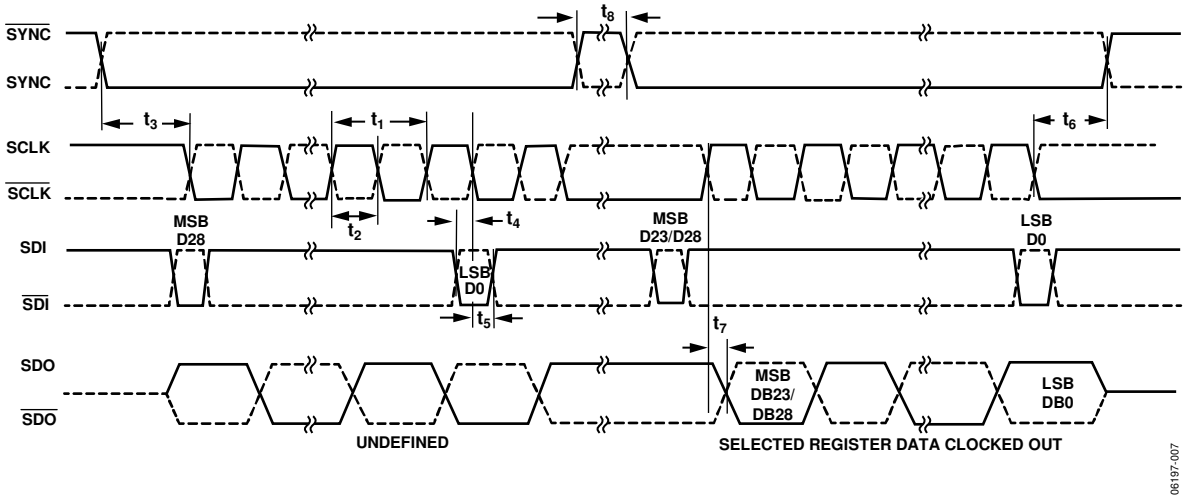


Figure 7. LVDS Read and Write Timing (Readback Word Contains 24 Bits and Can Be Clocked Out with a Minimum of 24 Clock Edges)

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage, AVDD to AVSS	34 V
AVDD to AGND	−0.3 V to +34 V
AVSS to AGND	+0.3 V to −34 V
VREF to AGND	−0.3 V to +7 V
DUTGND to AGND	AVDD + 0.3 V to AVSS − 0.3 V
REFGND to AGND	AVDD + 0.3 V to AVSS − 0.3 V
DVCC to DGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
Digital Inputs to DGND	−0.3 V to DVCC + 0.3 V
Analog Inputs to AGND	AVSS − 0.3 V to AVDD + 0.3 V
Storage Temperature Range	−65°C to +125°C
Operating Junction Temperature Range (J Version)	25°C to 90°C
Reflow Soldering	JEDEC Standard (J-STD-020)
Junction Temperature	150°C max

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal resistance values are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance[1] (JEDEC 4-Layer (1S2P) Board)

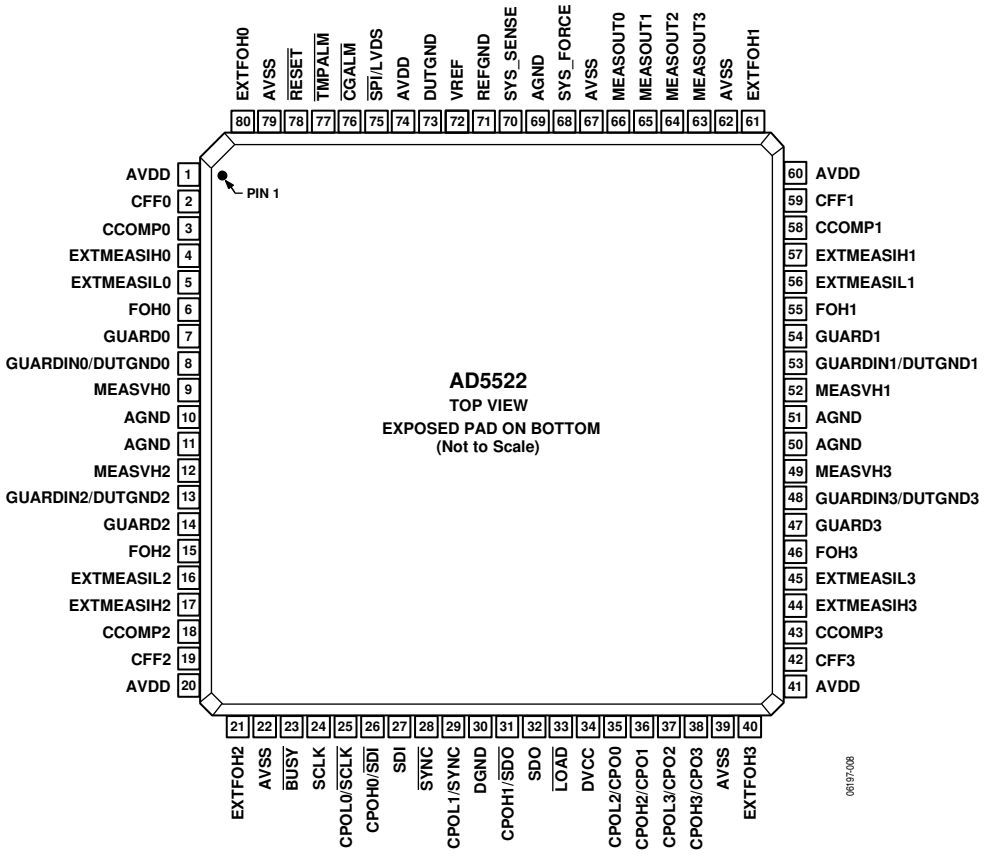
Package Type	Airflow (LFPM)	θ_{JA}	θ_{JC}	Unit
TQFP Exposed Pad on Bottom			4.8	°C/W
No Heat Sink[2]	0	22.3		°C/W
	200	17.2		°C/W
	500	15.1		°C/W
With Cooling Plate at 45°C[3]	N/A[4]	5.4	4.8	°C/W
TQFP Exposed Pad on Top			2	°C/W
No Heat Sink[2]	0	42.4		°C/W
	200	37.2		°C/W
	500	35.7		°C/W
With Cooling Plate at 45°C[3]	N/A[4]	3.0	2	°C/W

[1] The information in this section is based on simulated thermal information.
[2] These values apply to the package with no heat sink attached. The actual thermal performance of the package depends on the attached heat sink and environmental conditions.
[3] Natural convection at 55°C ambient. Assumes perfect thermal contact between the cooling plate and the exposed paddle.
[4] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS INTERNALLY ELECTRICALLY CONNECTED TO AVSS. FOR ENHANCED THERMAL, ELECTRICAL, AND BOARD LEVEL PERFORMANCE, THE EXPOSED PADDLE ON THE BOTTOM OF THE PACKAGE SHOULD BE SOLDERED TO A CORRESPONDING THERMAL LAND PADDLE ON THE PCB.

Figure 8. Pin Configuration, Exposed Pad on Bottom

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
	Exposed pad	The exposed pad is internally electrically connected to AVSS. For enhanced thermal, electrical, and board level performance, the exposed paddle on the bottom of the package should be soldered to a corresponding thermal land paddle on the PCB.
1, 20, 41, 60, 74	AVDD	Positive Analog Supply Voltage.
2	CFF0	External Capacitor for Channel 0. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
3	CCOMP0	Compensation Capacitor Input for Channel 0. See the Compensation Capacitors section.
4	EXTMEASIH0	Sense Input (High Sense) for High Current Range (Channel 0).
5	EXTMEASIL0	Sense Input (Low Sense) for High Current Range (Channel 0).
6	FOH0	Force Output for Internal Current Ranges (Channel 0).
7	GUARD0	Guard Output Drive for Channel 0.
8	GUARDIN0/ DUTGND0	Guard Amplifier Input for Channel 0/DUTGND Input for Channel 0. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN0. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH0. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
9	MEASVH0	DUT Voltage Sense Input (High Sense) for Channel 0.
10, 11, 50, 51, 69	AGND	Analog Ground. These pins are the reference points for the analog supplies and the measure circuitry.
12	MEASVH2	DUT Voltage Sense Input (High Sense) for Channel 2.

Pin No.	Mnemonic	Description
13	GUARDIN2/ DUTGND2	Guard Amplifier Input for Channel 2/DUTGND Input for Channel 2. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN2. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH2. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
14	GUARD2	Guard Output Drive for Channel 2.
15	FOH2	Force Output for Internal Current Ranges (Channel 2).
16	EXTMEASIL2	Sense Input (Low Sense) for High Current Range (Channel 2).
17	EXTMEASIH2	Sense Input (High Sense) for High Current Range (Channel 2).
18	CCOMP2	Compensation Capacitor Input for Channel 2. See the Compensation Capacitors section.
19	CFF2	External Capacitor for Channel 2. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
21	EXTFOH2	Force Output for High Current Range (Channel 2). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
22, 39, 62, 67, 79	AVSS	Negative Analog Supply Voltage.
23	$\overline{\text{BUSY}}$	Digital Input/Open-Drain Output. This pin indicates the status of the interface. See the $\overline{\text{BUSY}}$ and $\overline{\text{LOAD}}$ Functions section for more information.
24	SCLK	Serial Clock Input, Active Falling Edge. Data is clocked into the shift register on the falling edge of SCLK. This pin operates at clock speeds up to 50 MHz.
25	CPOL0/$\overline{\text{SCLK}}$	Comparator Output Low (Channel 0) for SPI Interface/Differential Serial Clock Input (Complement) for LVDS Interface.
26	CPOH0/$\overline{\text{SDI}}$	Comparator Output High (Channel 0) for SPI Interface/Differential Serial Data Input (Complement) for LVDS Interface.
27	SDI	Serial Data Input for SPI or LVDS Interface.
28	$\overline{\text{SYNC}}$	Active Low Frame Synchronization Input for SPI or LVDS Interface.
29	CPOL1/SYNC	Comparator Output Low (Channel 1) for SPI Interface/Differential SYNC Input for LVDS Interface.
30	DGND	Digital Ground Reference Point.
31	CPOH1/$\overline{\text{SDO}}$	Comparator Output High (Channel 1) for SPI Interface/Differential Serial Data Output (Complement) for LVDS Interface.
32	SDO	Serial Data Output for SPI or LVDS Interface. This pin can be used for data readback and diagnostic purposes.
33	$\overline{\text{LOAD}}$	Logic Input (Active Low). This pin synchronizes updates within one device or across a group of devices. If synchronization is not required, $\overline{\text{LOAD}}$ can be tied low; in this case, DAC channels and PMU modes are updated immediately after $\overline{\text{BUSY}}$ goes high. See the $\overline{\text{BUSY}}$ and $\overline{\text{LOAD}}$ Functions section for more information.
34	DVCC	Digital Supply Voltage.
35	CPOL2/CPO0	Comparator Output Low (Channel 2) for SPI Interface/Comparator Output Window (Channel 0) for LVDS Interface.
36	CPOH2/CPO1	Comparator Output High (Channel 2) for SPI Interface/Comparator Output Window (Channel 1) for LVDS Interface.
37	CPOL3/CPO2	Comparator Output Low (Channel 3) for SPI Interface/Comparator Output Window (Channel 2) for LVDS Interface.
38	CPOH3/CPO3	Comparator Output High (Channel 3) for SPI Interface/Comparator Output Window (Channel 3) for LVDS Interface.
40	EXTFOH3	Force Output for High Current Range (Channel 3). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
42	CFF3	External Capacitor for Channel 3. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
43	CCOMP3	Compensation Capacitor Input for Channel 3. See the Compensation Capacitors section.
44	EXTMEASIH3	Sense Input (High Sense) for High Current Range (Channel 3).
45	EXTMEASIL3	Sense Input (Low Sense) for High Current Range (Channel 3).
46	FOH3	Force Output for Internal Current Ranges (Channel 3).
47	GUARD3	Guard Output Drive for Channel 3.
48	GUARDIN3/ DUTGND3	Guard Amplifier Input for Channel 3/DUTGND Input for Channel 3. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN3. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH3. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.

Pin No.	Mnemonic	Description
49	MEASVH3	DUT Voltage Sense Input (High Sense) for Channel 3.
52	MEASVH1	DUT Voltage Sense Input (High Sense) for Channel 1.
53	GUARDIN1/ DUTGND1	Guard Amplifier Input for Channel 1/DUTGND Input for Channel 1. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN1. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH1. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
54	GUARD1	Guard Output Drive for Channel 1.
55	FOH1	Force Output for Internal Current Ranges (Channel 1).
56	EXTMEASIL1	Sense Input (Low Sense) for High Current Range (Channel 1).
57	EXTMEASIH1	Sense Input (High Sense) for High Current Range (Channel 1).
58	CCOMP1	Compensation Capacitor Input for Channel 1. See the Compensation Capacitors section.
59	CFF1	External Capacitor for Channel 1. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
61	EXTFOH1	Force Output for High Current Range (Channel 1). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
63	MEASOUT3	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 3. This pin is referenced to AGND.
64	MEASOUT2	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 2. This pin is referenced to AGND.
65	MEASOUT1	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 1. This pin is referenced to AGND.
66	MEASOUT0	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 0. This pin is referenced to AGND.
68	SYS_FORCE	External Force Signal Input. This pin enables the connection of the system PMU.
70	SYS_SENSE	External Sense Signal Output. This pin enables the connection of the system PMU.
71	REFGND	Accurate Analog Reference Input Ground.
72	VREF	Reference Input for DAC Channels (5 V for specified performance).
73	DUTGND	DUT Voltage Sense Input (Low Sense). By default, this input is shared among all four PMU channels. If a DUTGND input is required for each channel, the user can configure the GUARDINx/DUTGNDx pins as DUTGND inputs for each PMU channel.
75	$\overline{\text{SPI}}$/LVDS	Interface Select Pin. Logic low selects SPI-compatible interface mode; logic high selects LVDS interface mode. This pin has a pull-down current source (~350 µA). In LVDS interface mode, the CPOHx and CPOLx pins default to differential interface pins.
76	$\overline{\text{CGALM}}$	Open-Drain Output for Guard and Clamp Alarms. This open-drain pin provides shared alarm information about the guard amplifier and clamp circuitry. By default, this output pin is disabled. The system control register allows the user to enable this function and to set the open-drain output as a latched output. The user can also choose to enable alarms for the guard amplifier, the clamp circuitry, or both. When this pin flags an alarm, the origins of the alarm can be determined by reading back the alarm status register. Two flags per channel in this word (one latched, one unlatched) indicate which function caused the alarm and whether the alarm is still present.
77	$\overline{\text{TMPALM}}$	Open-Drain Output for Temperature Alarm. This latched, active low, open-drain output flags a temperature alarm to indicate that the junction temperature has exceeded the default temperature setting (130°C) or the user programmed temperature setting. Two flags in the alarm status register (one latched, one unlatched) indicate whether the temperature has dropped below 130°C or remains above 130°C. User action is required to clear this latched alarm flag by writing to the clear bit (Bit 6) in any of the PMU registers.
78	$\overline{\text{RESET}}$	Digital Reset Input. This active low, level sensitive input resets all internal nodes on the device to their power-on reset values.
80	EXTFOH0	Force Output for High Current Range (Channel 0). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.

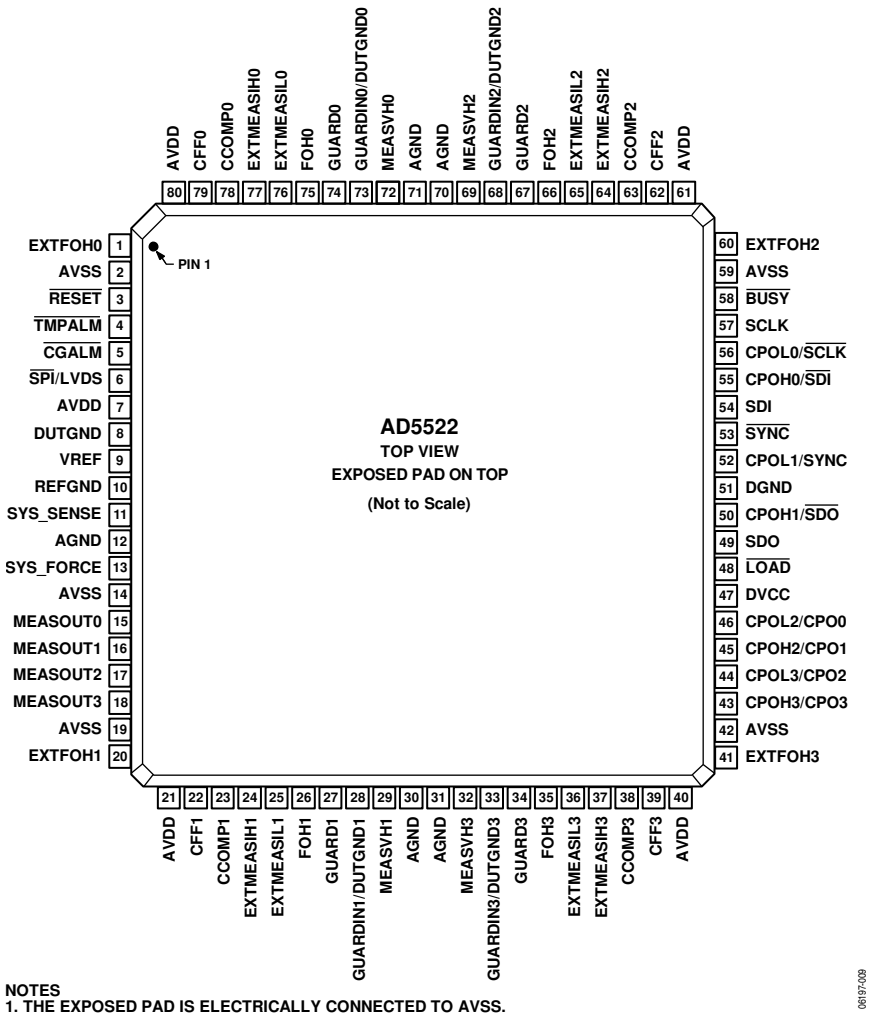


Figure 9. Pin Configuration, Exposed Pad on Top

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
	Exposed pad	The exposed pad is electrically connected to AVSS.
1	EXTFOH0	Force Output for High Current Range (Channel 0). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
2, 14, 19, 42, 59	AVSS	Negative Analog Supply Voltage.
3	$\overline{\text{RESET}}$	Digital Reset Input. This active low, level sensitive input resets all internal nodes on the device to their power-on reset values.
4	$\overline{\text{TMPALM}}$	Open-Drain Output for Temperature Alarm. This latched, active low, open-drain output flags a temperature alarm to indicate that the junction temperature has exceeded the default temperature setting (130°C) or the user programmed temperature setting. Two flags in the alarm status register (one latched, one unlatched) indicate whether the temperature has dropped below 130°C or remains above 130°C. User action is required to clear this latched alarm flag by writing to the clear bit (Bit 6) in any of the PMU registers.
5	$\overline{\text{CGALM}}$	Open-Drain Output for Guard and Clamp Alarms. This open-drain pin provides shared alarm information about the guard amplifier and clamp circuitry. By default, this output pin is disabled. The system control register allows the user to enable this function and to set the open-drain output as a latched output. The user can also choose to enable alarms for the guard amplifier, the clamp circuitry, or both. When this pin flags an alarm, the origins of the alarm can be determined by reading back the alarm status register. Two flags per channel in this word (one latched, one unlatched) indicate which function caused the alarm and whether the alarm is still present.

Pin No.	Mnemonic	Description
6	$\overline{\text{SPI}}$/LVDS	Interface Select Pin. Logic low selects SPI-compatible interface mode; logic high selects LVDS interface mode. This pin has a pull-down current source (~350 µA). In LVDS interface mode, the CPOHx and CPOLx pins default to differential interface pins.
7, 21, 40, 61, 80	AVDD	Positive Analog Supply Voltage.
8	DUTGND	DUT Voltage Sense Input (Low Sense). By default, this input is shared among all four PMU channels. If a DUTGND input is required for each channel, the user can configure the GUARDINx/DUTGNDx pins as DUTGND inputs for each PMU channel.
9	VREF	Reference Input for DAC Channels. 5 V for specified performance.
10	REFGND	Accurate Analog Reference Input Ground.
11	SYS_SENSE	External Sense Signal Output. This pin enables the connection of the system PMU.
12, 30, 31, 70, 71	AGND	Analog Ground. These pins are the reference points for the analog supplies and the measure circuitry.
13	SYS_FORCE	External Force Signal Input. This pin enables the connection of the system PMU.
15	MEASOUT0	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 0. This pin is referenced to AGND.
16	MEASOUT1	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 1. This pin is referenced to AGND.
17	MEASOUT2	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 2. This pin is referenced to AGND.
18	MEASOUT3	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 3. This pin is referenced to AGND.
20	EXTFOH1	Force Output for High Current Range (Channel 1). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
22	CFF1	External Capacitor for Channel 1. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
23	CCOMP1	Compensation Capacitor Input for Channel 1. See the Compensation Capacitors section.
24	EXTMEASIH1	Sense Input (High Sense) for High Current Range (Channel 1).
25	EXTMEASIL1	Sense Input (Low Sense) for High Current Range (Channel 1).
26	FOH1	Force Output for Internal Current Ranges (Channel 1).
27	GUARD1	Guard Output Drive for Channel 1.
28	GUARDIN1/ DUTGND1	Guard Amplifier Input for Channel 1/DUTGND Input for Channel 1. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN1. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH1. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
29	MEASVH1	DUT Voltage Sense Input (High Sense) for Channel 1.
32	MEASVH3	DUT Voltage Sense Input (High Sense) for Channel 3.
33	GUARDIN3/ DUTGND3	Guard Amplifier Input for Channel 3/DUTGND Input for Channel 3. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN3. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH3. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
34	GUARD3	Guard Output Drive for Channel 3.
35	FOH3	Force Output for Internal Current Ranges (Channel 3).
36	EXTMEASIL3	Sense Input (Low Sense) for High Current Range (Channel 3).
37	EXTMEASIH3	Sense Input (High Sense) for High Current Range (Channel 3).
38	CCOMP3	Compensation Capacitor Input for Channel 3. See the Compensation Capacitors section.
39	CFF3	External Capacitor for Channel 3. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
41	EXTFOH3	Force Output for High Current Range (Channel 3). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
43	CPOH3/CPO3	Comparator Output High (Channel 3) for SPI Interface/Comparator Output Window (Channel 3) for LVDS Interface.
44	CPOL3/CPO2	Comparator Output Low (Channel 3) for SPI Interface/Comparator Output Window (Channel 2) for LVDS Interface.
45	CPOH2/CPO1	Comparator Output High (Channel 2) for SPI Interface/Comparator Output Window (Channel 1) for LVDS Interface.

Pin No.	Mnemonic	Description
46	CPOL2/CPO0	Comparator Output Low (Channel 2) for SPI Interface/Comparator Output Window (Channel 0) for LVDS Interface.
47	DVCC	Digital Supply Voltage.
48	$\overline{\text{LOAD}}$	Logic Input (Active Low). This pin synchronizes updates within one device or across a group of devices. If synchronization is not required, $\overline{\text{LOAD}}$ can be tied low; in this case, DAC channels and PMU modes are updated immediately after $\overline{\text{BUSY}}$ goes high. See the $\overline{\text{BUSY}}$ and $\overline{\text{LOAD}}$ Functions section for more information.
49	SDO	Serial Data Output for SPI or LVDS Interface. This pin can be used for data readback and diagnostic purposes.
50	CPOH1/$\overline{\text{SDO}}$	Comparator Output High (Channel 1) for SPI Interface/Differential Serial Data Output (Complement) for LVDS Interface.
51	DGND	Digital Ground Reference Point.
52	CPOL1/SYNC	Comparator Output Low (Channel 1) for SPI Interface/Differential SYNC Input for LVDS Interface.
53	$\overline{\text{SYNC}}$	Active Low Frame Synchronization Input for SPI or LVDS Interface.
54	SDI	Serial Data Input for SPI or LVDS Interface.
55	CPOH0/$\overline{\text{SDI}}$	Comparator Output High (Channel 0) for SPI Interface/Differential Serial Data Input (Complement) for LVDS Interface.
56	CPOL0/$\overline{\text{SCLK}}$	Comparator Output Low (Channel 0) for SPI Interface/Differential Serial Clock Input (Complement) for LVDS Interface.
57	SCLK	Serial Clock Input, Active Falling Edge. Data is clocked into the shift register on the falling edge of SCLK. This pin operates at clock speeds up to 50 MHz.
58	$\overline{\text{BUSY}}$	Digital Input/Open-Drain Output. This pin indicates the status of the interface. See the $\overline{\text{BUSY}}$ and $\overline{\text{LOAD}}$ Functions section for more information.
60	EXTFOH2	Force Output for High Current Range (Channel 2). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
62	CFF2	External Capacitor for Channel 2. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
63	CCOMP2	Compensation Capacitor Input for Channel 2. See the Compensation Capacitors section.
64	EXTMEASIH2	Sense Input (High Sense) for High Current Range (Channel 2).
65	EXTMEASIL2	Sense Input (Low Sense) for High Current Range (Channel 2).
66	FOH2	Force Output for Internal Current Ranges (Channel 2).
67	GUARD2	Guard Output Drive for Channel 2.
68	GUARDIN2/ DUTGND2	Guard Amplifier Input for Channel 2/DUTGND Input for Channel 2. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN2. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH2. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
69	MEASVH2	DUT Voltage Sense Input (High Sense) for Channel 2.
72	MEASVH0	DUT Voltage Sense Input (High Sense) for Channel 0.
73	GUARDIN0/ DUTGND0	Guard Amplifier Input for Channel 0/DUTGND Input for Channel 0. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN0. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH0. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
74	GUARD0	Guard Output Drive for Channel 0.
75	FOH0	Force Output for Internal Current Ranges (Channel 0).
76	EXTMEASIL0	Sense Input (Low Sense) for High Current Range (Channel 0).
77	EXTMEASIH0	Sense Input (High Sense) for High Current Range (Channel 0).
78	CCOMP0	Compensation Capacitor Input for Channel 0. See the Compensation Capacitors section.
79	CFF0	External Capacitor for Channel 0. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.

TYPICAL PERFORMANCE CHARACTERISTICS

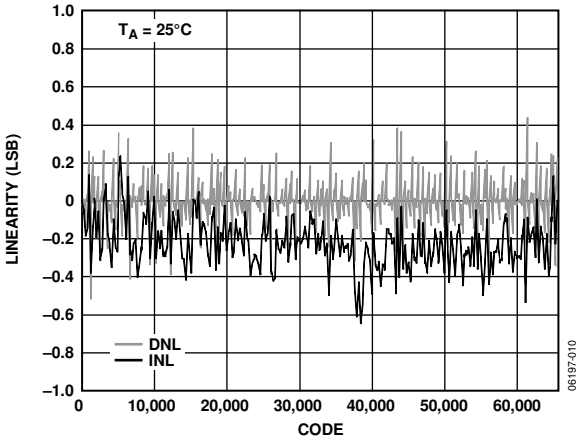


Figure 10. Force Voltage Linearity vs. Code, All Ranges, 1 LSB = 0.0015% FSR (20 V FSR)

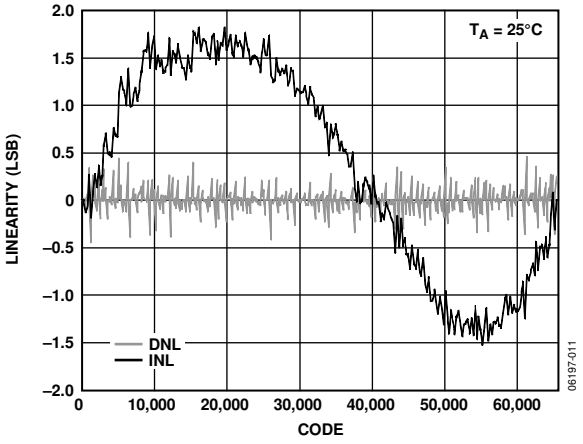


Figure 11. Force Current Linearity vs. Code, All Ranges, 1 LSB = 0.0015% FSR (20 V FSR)

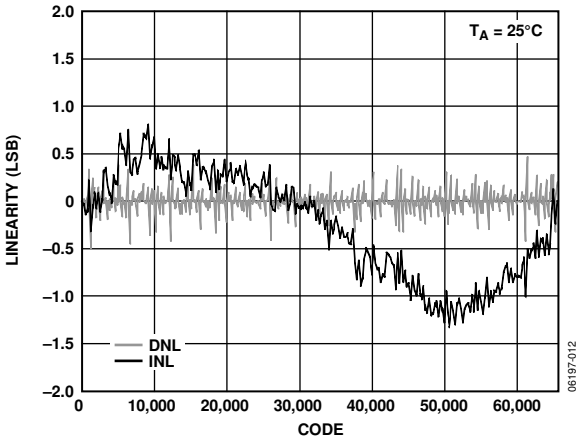


Figure 12. Measure Voltage Linearity vs. Code, All Ranges, 1 LSB = 0.0015% FSR (20 V FSR), MEASOUTx Gain = 1

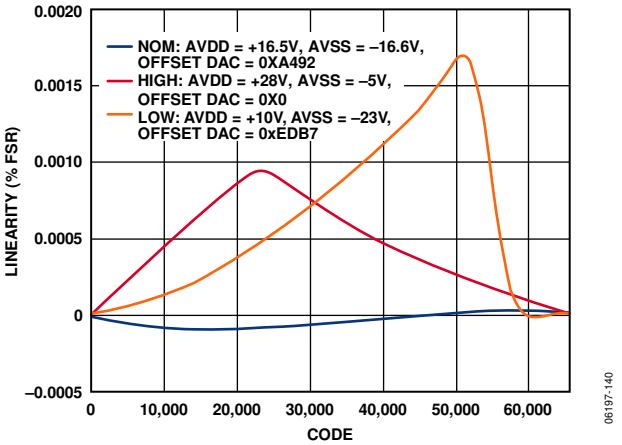


Figure 13. Measure Voltage Linearity vs. Code, All Ranges, MEASOUTx Gain = 0.2

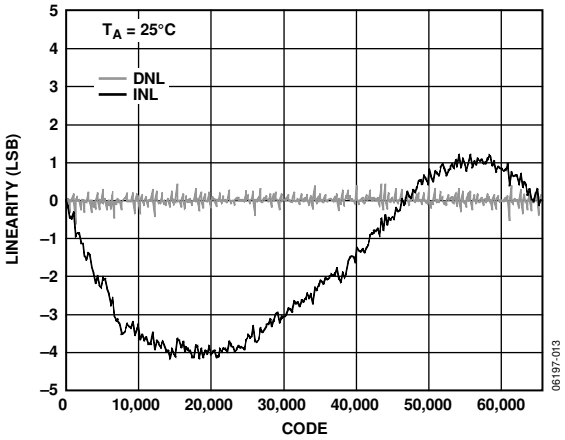


Figure 14. Measure Current Linearity vs. Code, All Ranges, 1 LSB = 0.0015% FSR (20 V FSR), MI Gain = 10, MEASOUTx Gain = 1

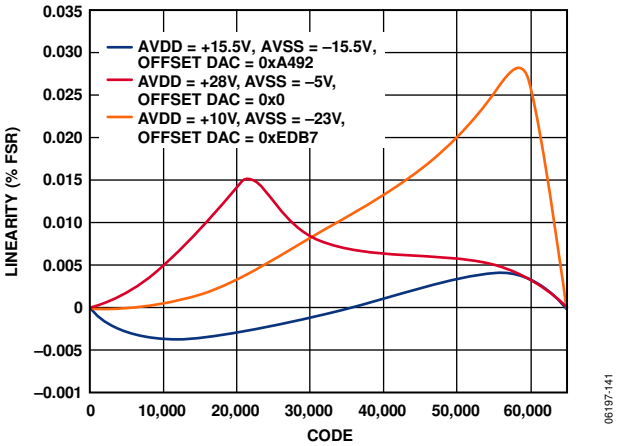


Figure 15. Measure Current Linearity vs. Code, All Ranges, MEASOUTx Gain = 0.2, MI Gain = 10

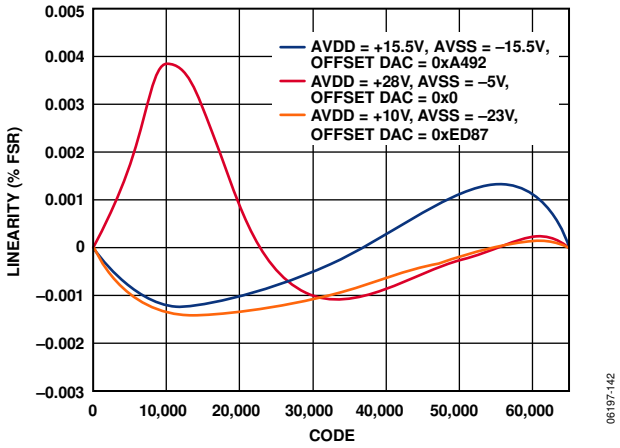


Figure 16. Measure Current Linearity vs. Code, All Ranges, MEASOUTx Gain = 0.2, MI Gain = 5

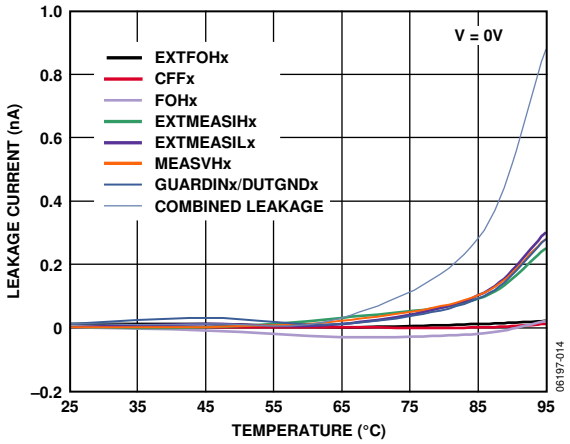


Figure 17. Leakage Current vs. Temperature (Stress Voltage = 0 V)

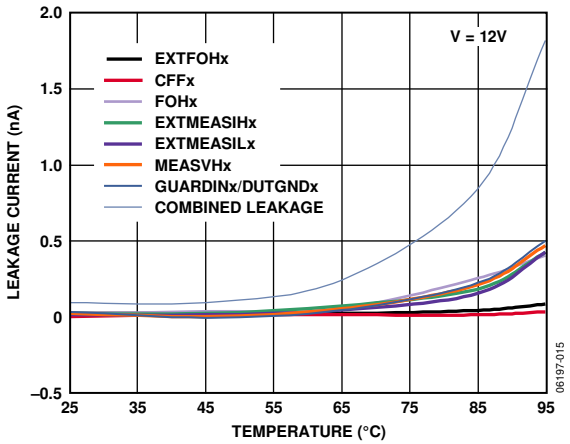


Figure 18. Leakage Current vs. Temperature (Stress Voltage = 12 V)

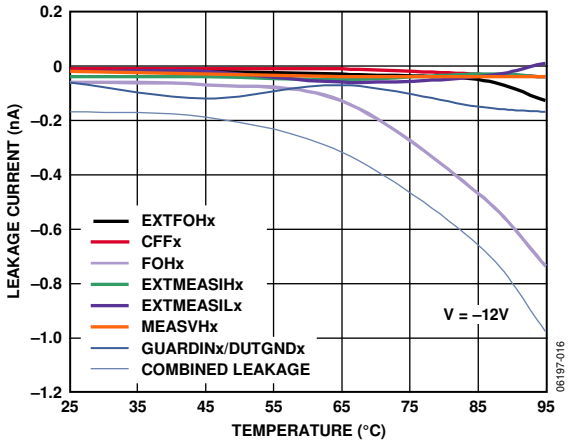


Figure 19. Leakage Current vs. Temperature (Stress Voltage = –12 V)

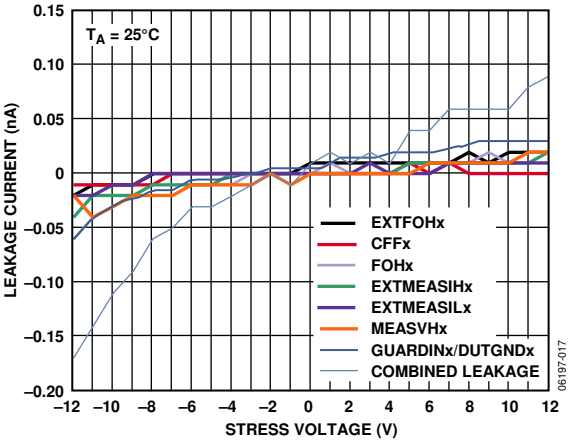


Figure 20. Leakage Current vs. Stress Voltage

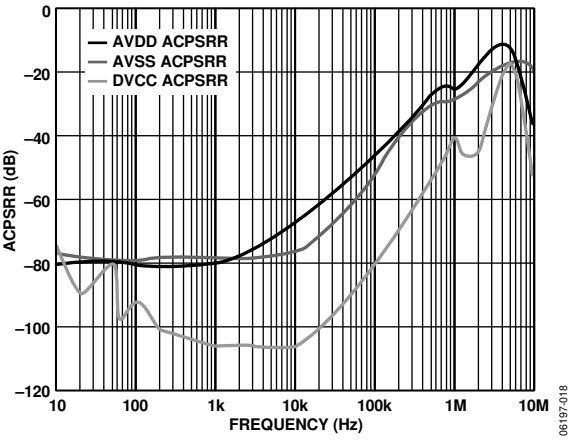


Figure 21. ACPSRR at FOHx in Force Voltage Mode vs. Frequency

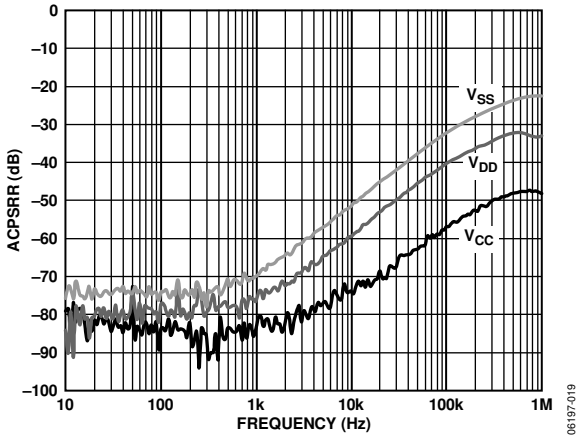


Figure 22. ACPSRR at FOHx in Force Current Mode vs. Frequency (MI Gain = 10)

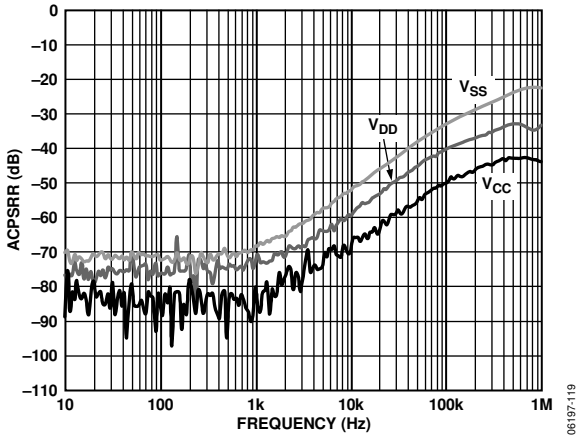


Figure 23. ACPSRR at FOHx in Force Current Mode vs. Frequency (MI Gain = 5)

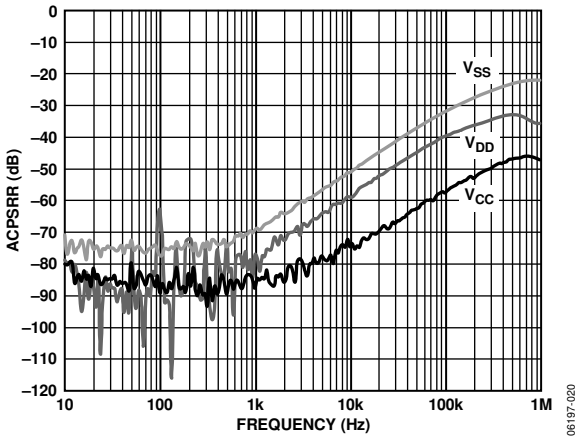


Figure 24. ACPSRR at MEASOUTx in Measure Voltage Mode vs. Frequency (MEASOUT Gain = 1)

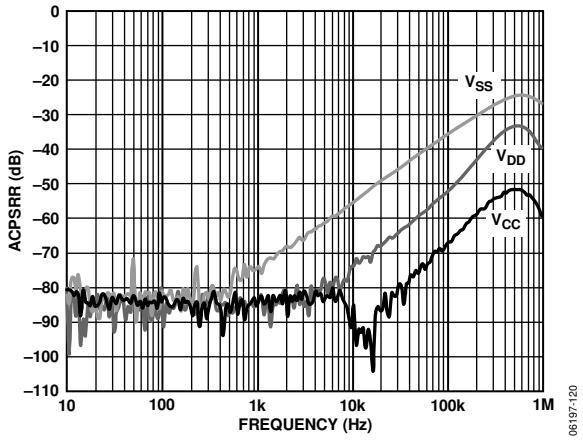


Figure 25. ACPSRR at MEASOUTx in Measure Voltage Mode vs. Frequency (MEASOUT Gain = 0.2)

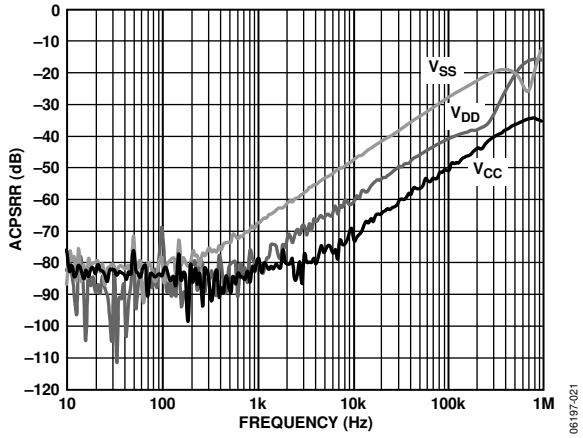


Figure 26. ACPSRR at MEASOUTx in Measure Current Mode vs. Frequency (MI Gain = 10, MEASOUT Gain = 1)

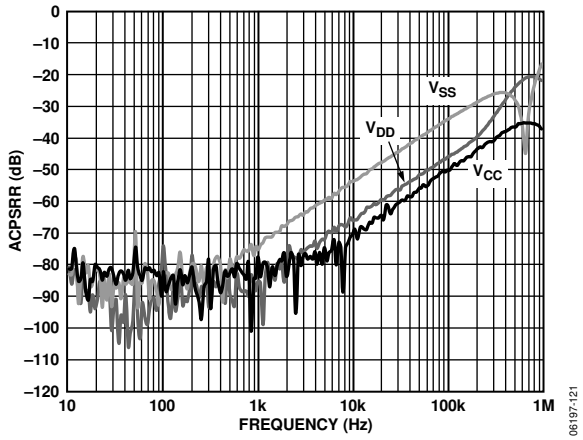


Figure 27. ACPSRR at MEASOUTx in Measure Current Mode vs. Frequency (MI Gain = 5, MEASOUT Gain = 1)