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Dual, Current-Output, Serial-Input, 16-/14-Bit DACs

Data Sheet

AD5545/AD5555

FEATURES

- 16-bit resolution AD5545
- 14-bit resolution AD5555
- ±1 LSB DNL monotonic
- ±1 LSB INL
- 2 mA full-scale current ±20%, with V_{REF} = 10 V
- 0.5 µs settling time
- 2Q multiplying reference-input 6.9 MHz BW
- Zero or midscale power-up preset
- Zero or midscale dynamic reset
- 3-wire interface
- Compact 16-lead TSSOP package

APPLICATIONS

- Automatic test equipment
- Instrumentation
- Digitally controlled calibration
- Industrial control PLCs
- Programmable attenuator

FUNCTIONAL BLOCK DIAGRAM

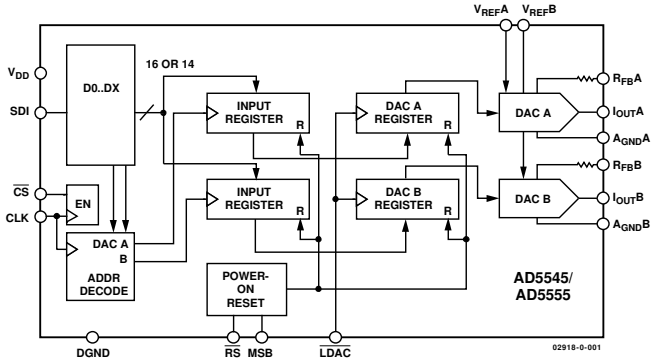

Figure 1.

PRODUCT OVERVIEW

The AD5545/AD5555 are 16-bit/14-bit, current-output, digital-to-analog converters designed to operate from a 4.5 V to 5.5 V supply range.

An external reference is needed to establish the full-scale output-current. An internal feedback resistor (R_{FB}) enhances the resistance and temperature tracking when combined with an external op amp to complete the I-to-V conversion.

A serial data interface offers high speed, 3-wire microcontroller compatible inputs using serial data in (SDI), clock (CLK), and chip select ($\overline{CS}$). Additional $\overline{LDAC}$ function allows simultaneous update operation. The internal reset logic allows power-on preset and dynamic reset at either zero or midscale, depending on the state of the MSB pin.

The AD5545/AD5555 are packaged in the compact TSSOP-16 package and can be operated from −40°C to +85°C.

Rev. I

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = 5 V ± 10%, I_{OUT} = virtual GND, GND = 0 V, V_{REF} = 10 V, T_A = full operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE[1]						
Resolution	N	AD5545, 1 LSB = $V_{REF}/2^{16}$ = 153 µV when V_{REF} = 10 V			16	Bits
		AD5555, 1 LSB = $V_{REF}/2^{14}$ = 610 µV when V_{REF} = 10 V			14	Bits
Relative Accuracy	INL	AD5545B			±2	LSB
		AD5555C			±1	LSB
		AD5545C			±1	LSB
Differential Nonlinearity	DNL	Monotonic			±1	LSB
Output Leakage Current	I_{OUT}	Data = 0x0000, T_A = 25°C			10	nA
		Data = 0x0000, T_A = T_A Max			20	nA
Full-Scale Gain Error	G_{FSE}	Data = full scale		±1	±4	mV
Full-Scale Temperature Coefficient[2]	TCV_{FS}			1		ppm/°C
REFERENCE INPUT						
V_{REF} Range	V_{REF}		−12		+12	V
Input Resistance	R_{REF}			5		kΩ[3]
Input Capacitance[2]	C_{REF}			5		pF
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = full scale		2		mA
Output Capacitance[2]	C_{OUT}	Code dependent		200		pF
LOGIC INPUTS AND OUTPUT						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance[2]	C_{IL}				10	pF
INTERFACE TIMING[2, 4]						
Clock Input Frequency	f_{CLK}				50	MHz
Clock Width High	t_{CH}		10			ns
Clock Width Low	t_{CL}		10			ns
$\overline{CS}$ to Clock Setup	t_{CSS}		0			ns
Clock to $\overline{CS}$ Hold	t_{CSH}		10			ns
Data Setup	t_{DS}		5			ns
Data Hold	t_{DH}		10			ns
$\overline{LDAC}$ Setup	t_{LDS}		5			ns
Hold	t_{LDH}		10			ns
$\overline{LDAC}$ Width	t_{LDAC}		10			ns
SUPPLY CHARACTERISTICS						
Power Supply Range	V_{DD} range		4.5		5.5	V
Positive Supply Current	I_{DD}	Logic inputs = 0 V			10	µA
Power Dissipation	P_{DISS}	Logic inputs = 0 V			0.055	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%			0.006	%/%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AC CHARACTERISTICS						
Output Voltage Setting Time	t_S	To ±0.1% full scale, data = zero scale to full scale to zero scale		0.5		µs
Reference Multiplying BW	BW	V_{REF} = 100 mV rms, data = full scale, C1 = 5.6 pF		6.9		MHz
DAC Glitch Impulse	Q	V_{REF} = 0 V, data = midscale minus 1 to midscale		–2		nV-s
Feedthrough Error	V_{OUT}/V_{REF}	Data = zero scale, V_{REF} = 100 mV rms, f = 1 kHz, same channel		–81		dB
Digital Feedthrough	Q	$\overline{CS}$ = logic high and f_{CLK} = 1 MHz		7		nV-s
Total Harmonic Distortion	THD	V_{REF} = 5 V p-p, data = full scale, f = 1 kHz to 10 kHz		–104		dB
Analog Crosstalk	C_{TA}	V_{REFB} = 0 V, measure V_{OUTB} with V_{REFA} = 5 V p-p sine wave, data = full scale, f = 1 kHz to 10 kHz		–95		dB
Output Spot Noise Voltage	e_N	f = 1 kHz, BW = 1 Hz		12		nV/√Hz

[1] All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OP1177 I-to-V converter amplifier. The AD5545 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C.
[2] These parameters are guaranteed by design and not subject to production testing.
[3] All ac characteristic tests are performed in a closed-loop system using an AD8038 I-to-V converter amplifier and the AD8065 for the THD specification.
[4] All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

TIMING DIAGRAMS

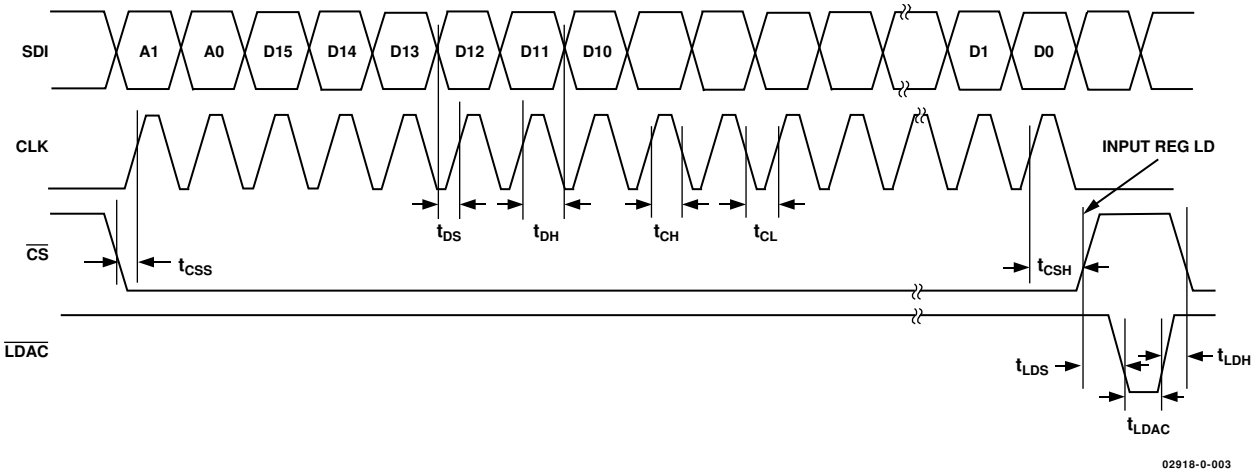

Figure 2. AD5545 18-Bit Data Word Timing Diagram

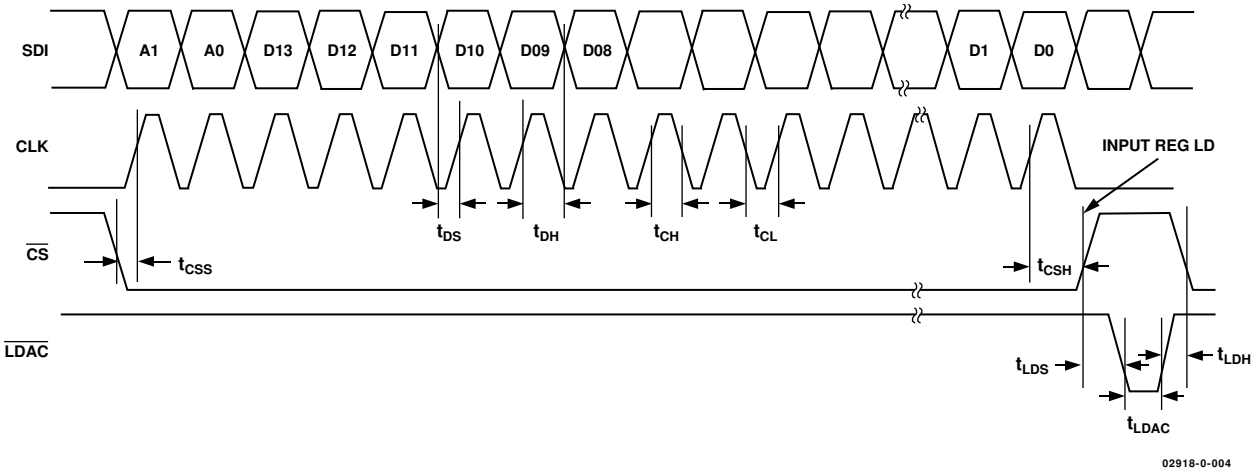

Figure 3. AD5555 16-Bit Data Word Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD} to GND	–0.3 V to +8 V
V_{REF} to GND	–18 V to +18 V
Logic Inputs to GND	–0.3 V to +8 V
V(I_{OUT}) to GND	–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin except Supplies	±50 mA
Package Power Dissipation	(T_J max – T_A)/θ_{JA}
Thermal Resistance θ_{JA}	
16-Lead TSSOP	150°C/W
Maximum Junction Temperature (T_J max)	150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature	
RU-16 (Vapor Phase, 60 sec)	215°C
RU-16 (Infrared, 15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

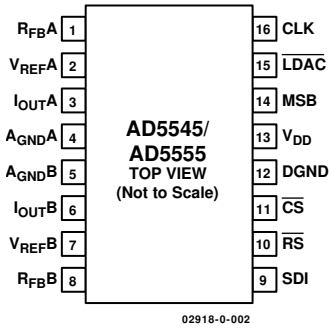

Figure 4. 16-Lead TSSOP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$R_{FB}A$	Establish voltage output for DAC A by connecting this pin to an external amplifier output.
2	$V_{REF}A$	DAC A Reference Voltage Input Terminal. Establishes DAC A full-scale output voltage. This pin can be tied to the V_{DD} pin.
3	$I_{OUT}A$	DAC A Current Output.
4	$A_{GND}A$	DAC A Analog Ground.
5	$A_{GND}B$	DAC B Analog Ground.
6	$I_{OUT}B$	DAC B Current Output.
7	$V_{REF}B$	DAC B Reference Voltage Input Terminal. Establishes DAC B full-scale output voltage. This pin can be tied to the V_{DD} pin.
8	$R_{FB}B$	Establish voltage output for DAC B by the $R_{FB}B$ pin connecting to an external amplifier output.
9	SDI	Serial Data Input. Input data loads directly into the shift register.
10	$\overline{RS}$	Reset Pin, Active Low Input. Input registers and DAC registers are set to all 0s or midscale. Register Data = 0x0000 when MSB = 0. Register Data = 0x8000 for AD5545 and 0x2000 for AD5555 when MSB = 1.
11	$\overline{CS}$	Chip Select, Active Low Input. Disables shift register loading when high. Transfers serial register data to the input register when $\overline{CS}$/$\overline{LDAC}$ returns high. This does not affect $\overline{LDAC}$ operation.
12	DGND	Digital Ground Pin.
13	V_{DD}	Positive Power Supply Input. Specified range of operation 5 V ± 10%.
14	MSB	MSB bit sets output to either 0 or midscale during a RESET pulse ($\overline{RS}$) or at system power-on. Output equals zero scale when MSB = 0 and midscale when MSB = 1. MSB pin can also be tied permanently to ground or V_{DD}.
15	$\overline{LDAC}$	Load DAC Register Strobe, Level Sensitive Active Low. Transfers all input register data to DAC registers. Asynchronous active low input. See Table 7 and Table 8 for operation.
16	CLK	Clock Input. Positive edge clocks data into shift register.

TYPICAL PERFORMANCE CHARACTERISTICS

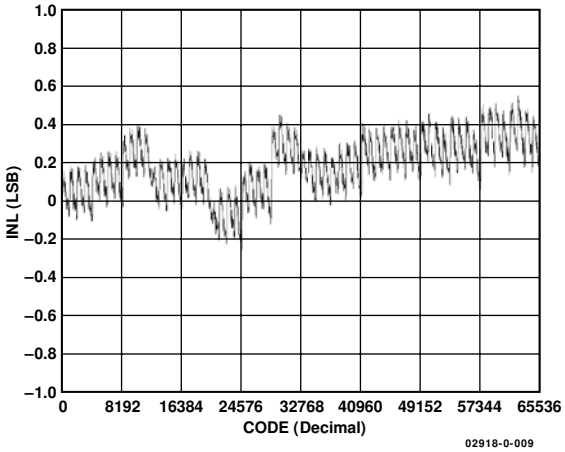

Figure 5. AD5545 Integral Nonlinearity Error

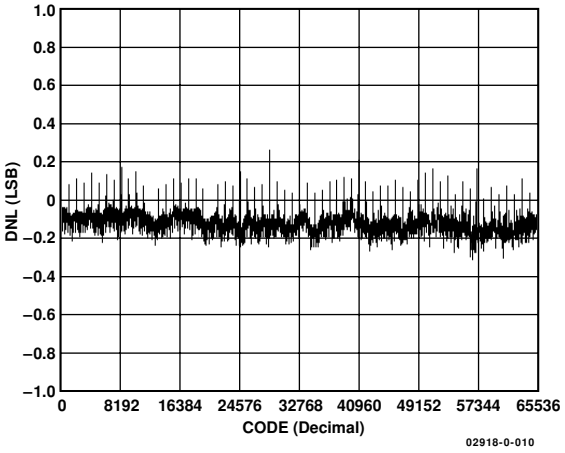

Figure 6. AD5545 Differential Nonlinearity Error

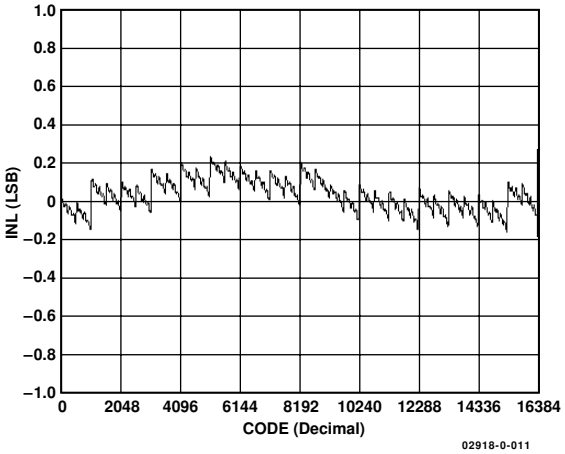

Figure 7. AD5555 Integral Nonlinearity Error

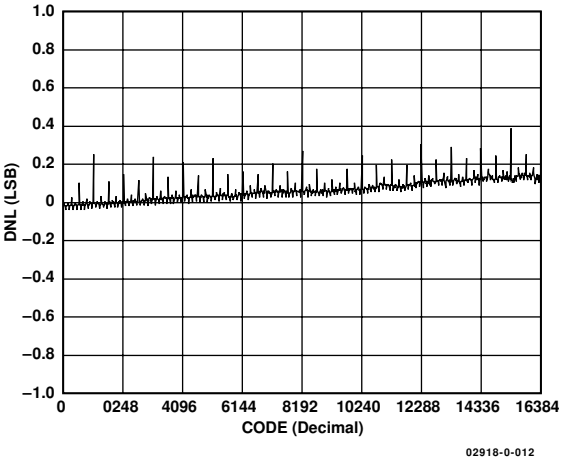

Figure 8. AD5555 Differential Nonlinearity Error

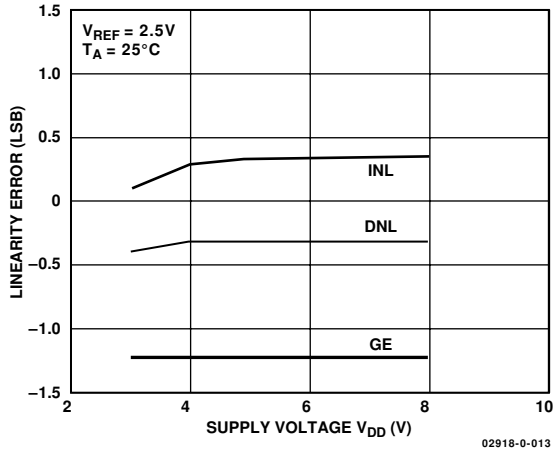

Figure 9. Linearity Errors vs. V_{DD}

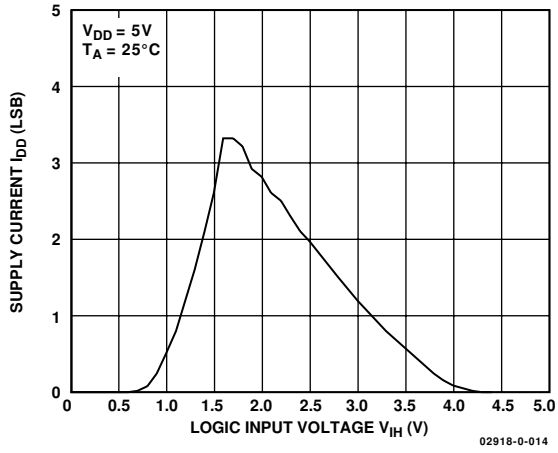

Figure 10. Supply Current vs. Logic Input Voltage

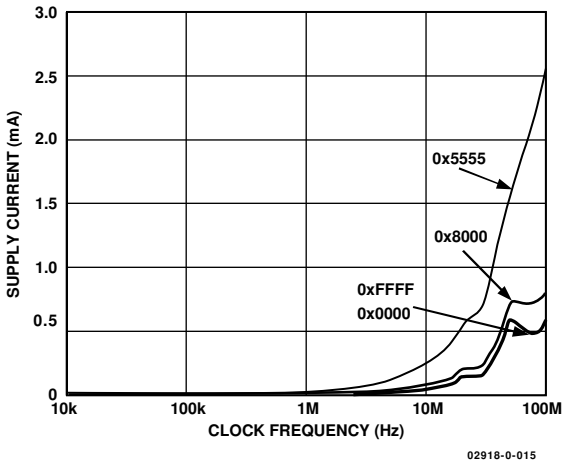

Figure 11. Supply Current vs. Clock Frequency

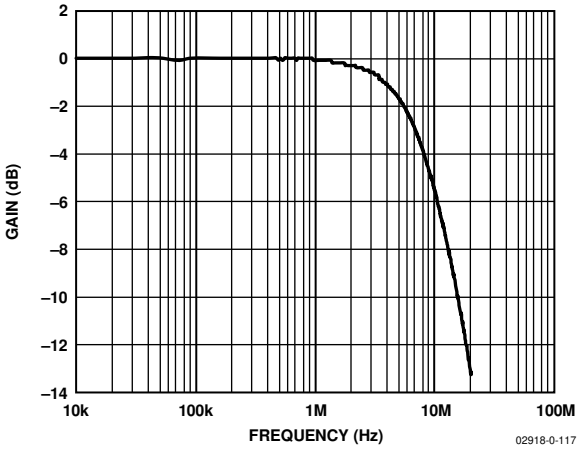

Figure 14. Reference Multiplying Bandwidth

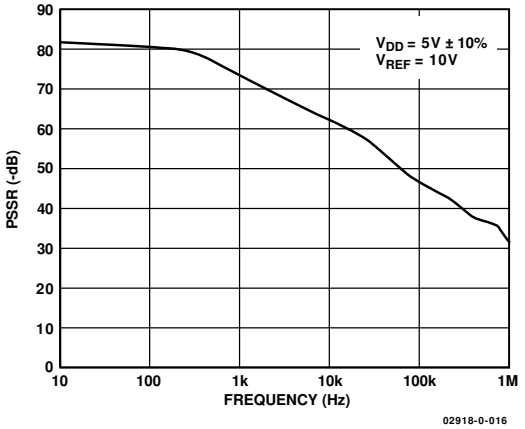

Figure 12. Power Supply Rejection Ration vs. Frequency

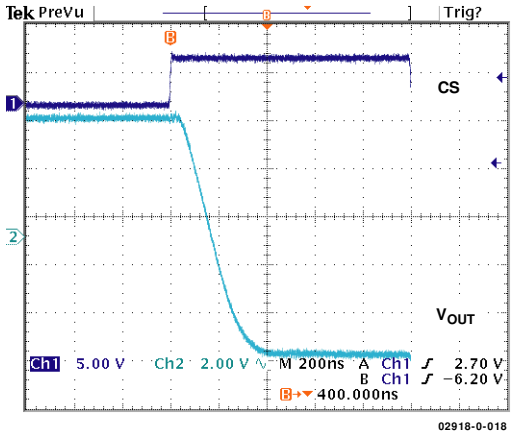

Figure 15. Settling Time

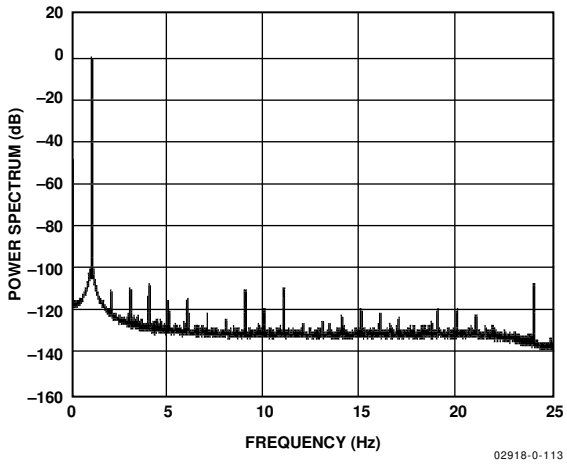

Figure 13. AD5545/AD5555 Analog THD

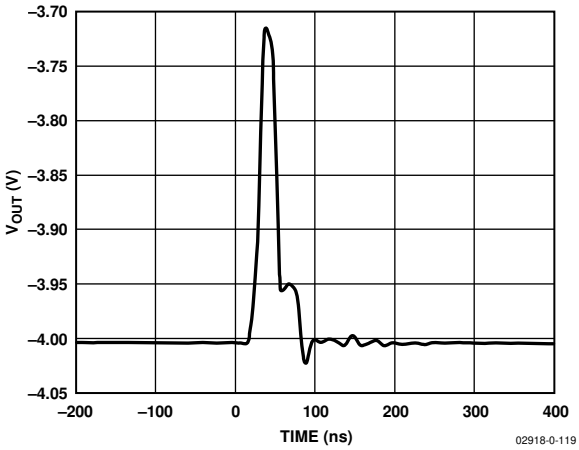

Figure 16. Midscale Transition and Digital Feedthrough

THEORY OF OPERATION

The AD5545/AD5555 contain a 16-/14-bit, current-output, digital-to-analog converter, a serial-input register, and a DAC register. Both parts require a minimum of a 3-wire serial data interface with an additional $\overline{\text{LDAC}}$ for dual channel simultaneous update.

DIGITAL-TO-ANALOG CONVERTER

The DAC architecture uses a current-steering R-2R ladder design. Figure 17 shows the typical equivalent DAC. The DAC contains a matching feedback resistor for use with an external I-to-V converter amplifier. The R_{FB} pin is connected to the output of the external amplifier. The I_{OUT} terminal is connected to the inverting input of the external amplifier. These DACs are designed to operate with either negative or positive reference voltages. The V_{DD} power pin is used only by the logic to drive the DAC switches on and off. Note that a matching switch is used in series with the internal 5 kΩ feedback resistor. If users attempt to measure the R_{FB} value, power must be applied to V_{DD} to achieve continuity. The V_{REF} input voltage and the digital data (D) loaded into the corresponding DAC register, according to Equation 1 and Equation 2, determine the DAC output voltage.

$$V_{OUT} = -V_{REF} \times D / 65{,}536 \quad (1)$$

$$V_{OUT} = -V_{REF} \times D / 16{,}384 \quad (2)$$

Note that the output full-scale polarity is the opposite of the V_{REF} polarity for dc reference voltages.

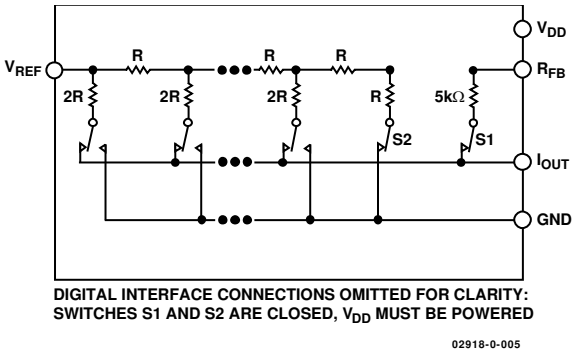

Figure 17. Equivalent R-2R DAC Circuit

These DACs are also designed to accommodate ac reference input signals. The AD5545/AD5555 accommodate input reference voltages in the range of –12 V to +12 V. The reference voltage inputs exhibit a constant nominal input-resistance value of 5 kΩ, ±30%. The DAC output (I_{OUT}) is code dependent, producing various output resistances and capacitances. When choosing an external amplifier, the user should take into account the variation in impedance generated by the AD5545/AD5555 on the amplifiers inverting input node. The feedback resistance in parallel with the DAC ladder resistance dominates output voltage noise.

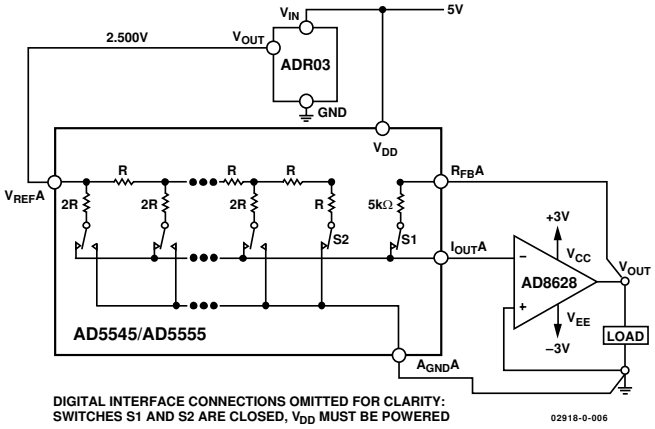

Figure 18. Recommended System Connections

SERIAL DATA INTERFACE

The AD5545/AD5555 use a minimum 3-wire ($\overline{CS}$, SDI, CLK) serial data interface for single channel update operation. With Table 7 as an example (AD5545), users can tie $\overline{LDAC}$ low and $\overline{RS}$ high, and then pull $\overline{CS}$ low for an 18-bit duration. New serial data is then clocked into the serial-input register in an 18-bit data-word format with the MSB bit loaded first. Table 8 defines the truth table for the AD5555. Data is placed on the SDI pin and clocked into the register on the positive clock edge of CLK. For the AD5545, only the last 18-bits clocked into the serial register are interrogated when the $\overline{CS}$ pin is strobed high, transferring the serial register data to the DAC register and updating the output. If the applied microcontroller outputs serial data in different lengths than the AD5545, such as 8-bit bytes, three right justified data bytes can be written to the AD5545. The AD5545 ignores the six MSB and recognizes the 18 LSB as valid data. After loading the serial register, the rising edge of $\overline{CS}$ transfers the serial register data to the DAC register and updates the output; during the $\overline{CS}$ strobe, the CLK should not be toggled.

If users want to program each channel separately but update them simultaneously, program $\overline{LDAC}$ and $\overline{RS}$ high initially, then pull $\overline{CS}$ low for an 18-bit duration and program DAC A with the proper address and data bits. $\overline{CS}$ is then pulled high to latch data to the DAC A register. At this time, the output is not updated. To load DAC B data, pull $\overline{CS}$ low for an 18-bit duration and program DAC B with the proper address and data, then pull $\overline{CS}$ high to latch data to the DAC B register. Finally, pull $\overline{LDAC}$ low and then high to update both the DAC A and DAC B outputs simultaneously.

Table 6 shows that each DAC A and DAC B can be individually loaded with a new data value. In addition, a common new data value can be loaded into both DACs simultaneously by setting Bit A1 = A0 = high. This command enables the parallel combination of both DACs, with $I_{OUT}A$ and $I_{OUT}B$ tied together, to act as one DAC with significant improved noise performance.

ESD Protection Circuits

All logic input pins contain back-biased ESD protection Zeners connected to digital ground (DGND) and V_{DD} as shown in Figure 19.

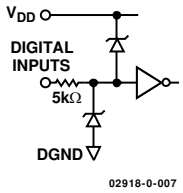

Figure 19. Equivalent ESD Protection Circuits

Table 4. AD5545 Serial Input Register Data Format, Data Is Loaded in the MSB-First Format[1]

	MSB																	LSB
Bit Position	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

[1] Note that only the last 18 bits of data clocked into the serial register (address + data) are inspected when the $\overline{CS}$ line's positive edge returns to logic high. At this point, an internally generated load strobe transfers the serial register data contents (Bit D15 to Bit D0) to the decoded DAC input register address determined by Bit A1 and Bit A0. Any extra bits clocked into the AD5545 shift register are ignored; only the last 18 bits clocked in are used. If double-buffered data is not needed, the $\overline{LDAC}$ pin can be tied logic low to disable the DAC registers.

Table 5. AD5555 Serial Input Register Data Format, Data Is Loaded in the MSB-First Format[1]

	MSB														LSB
Bit Position	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

[1] Note that only the last 16 bits of data clocked into the serial register (address + data) are inspected when the $\overline{CS}$ line's positive edge returns to logic high. At this point, an internally generated load strobe transfers the serial register data contents (Bit D13 to Bit D0) to the decoded DAC input register address determined by Bit A1 and Bit A0. Any extra bits clocked into the AD5555 shift register are ignored; only the last 16 bits clocked in are used. If double-buffered data is not needed, the $\overline{LDAC}$ pin can be tied logic low to disable the DAC registers.

Table 6. Address Decode

A1	A0	DAC Decoded
0	0	None
0	1	DAC A
1	0	DAC B
1	1	DAC A and DAC B

Table 7. AD5545 Control Logic Truth Table[1, 2]

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB	Serial Shift Register Function	Input Register Function	DAC Register
H	X	H	H	X	No effect	Latched	Latched
L	L	H	H	X	No effect	Latched	Latched
L	↑+	H	H	X	Shift register data advanced one bit	Latched	Latched
L	H	H	H	X	No effect	Latched	Latched
↑+	L	H	H	X	No effect	Selected DAC updated with current SR current	Latched
H	X	L	H	X	No effect	Latched	Transparent
H	X	H	H	X	No effect	Latched	Latched
H	X	↑+	H	X	No effect	Latched	Latched
H	X	H	L	0	No effect	Latched data = 0x0000	Latched data = 0x0000
H	X	H	L	H	No effect	Latched data = 0x8000	Latched data = 0x8000

[1] SR = shift register, ↑+ = positive logic transition, and X = don't care.
[2] At power-on, both the input register and the DAC register are loaded with all 0s.

Table 8. AD5555 Control Logic Truth Table[1, 2]

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB	Serial Shift Register Function	Input Register Function	DAC Register
H	X	H	H	X	No effect	Latched	Latched
L	L	H	H	X	No effect	Latched	Latched
L	↑+	H	H	X	Shift register data advanced one bit	Latched	Latched
L	H	H	H	X	No effect	Latched	Latched
↑+	L	H	H	X	No effect	Selected DAC updated with current SR current	Latched
H	X	L	H	X	No effect	Latched	Transparent
H	X	H	H	X	No effect	Latched	Latched
H	X	↑+	H	X	No effect	Latched	Latched
H	X	H	L	0	No effect	Latched data = 0x0000	Latched data = 0x0000
H	X	H	L	H	No effect	Latched data = 0x2000	Latched data = 0x2000

[1] SR = shift register, ↑+ = positive logic transition, and X = don't care.
[2] At power-on, both the input register and the DAC register are loaded with all 0s.

POWER-UP SEQUENCE

It is recommended to power-up V_{DD} and ground prior to any reference voltages. The ideal power-up sequence is $A_{GND}x$, DGND, V_{DD}, $V_{REF}x$, and digital inputs. A noncompliance power-up sequence can elevate reference current, but the device will resume normal operation once V_{DD} is powered.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length layout design. The input leads should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF disc or chip ceramic capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at V_{DD} to minimize any transient disturbance and to filter any low frequency ripple (see Figure 20). Users should not apply switching regulators for V_{DD} due to the power supply rejection ratio degradation over frequency.

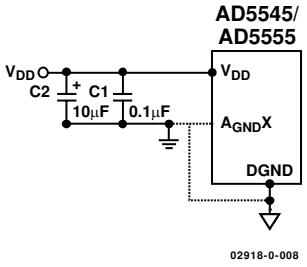

Figure 20. Power Supply Bypassing and Grounding Connection

GROUNDING

The DGND and $A_{GND}x$ pins of the AD5545/AD5555 refer to the digital and analog ground references. To minimize the digital ground bounce, the DGND terminal should be joined remotely at a single point to the analog ground plane (see Figure 20).

APPLICATIONS INFORMATION

STABILITY

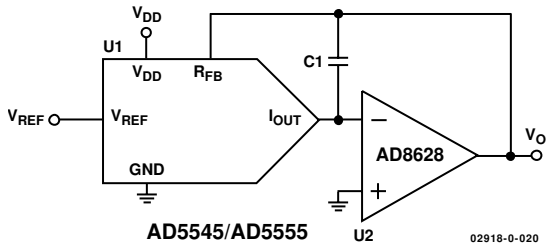

Figure 21. Operational Compensation Capacitor for Gain Peaking Prevention

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the op amp must be connected as close as possible, and proper PCB layout techniques must be employed. Because every code change corresponds to a step function, gain peaking may occur if the op amp has limited GBP, and if there is excessive parasitic capacitance at the inverting node.

An optional compensation capacitor, C1, can be added for stability as shown in Figure 21. C1 should be found empirically, but 6 pF is generally more than adequate for the compensation.

BIPOLAR OUTPUT

The AD5545/AD5555 is inherently a 2-quadrant multiplying DAC. It can easily be set up for unipolar output operation. The full-scale output polarity is the inverse of the reference input voltage.

In some applications, it may be necessary to generate the full 4-quadrant multiplying capability or a bipolar output swing. This is easily accomplished by using an additional external amplifier, U4, configured as a summing amplifier (see Figure 22). In this circuit, the second amplifier, U4, provides a gain of 2, which increases the output span magnitude to 5 V. Biasing the external amplifier with a 2.5 V offset from the reference voltage results in a full 4-quadrant multiplying circuit. The transfer equation of this circuit shows that both negative and positive output voltages are created because the input data (D) is incremented from code zero (V_{OUT} = −2.5 V) to midscale (V_{OUT} = 0 V) to full scale (V_{OUT} = +2.5 V).

$$V_{OUT} = (D/32{,}768 - 1) \times V_{REF} \text{ (AD5545)} \quad (3)$$

$$V_{OUT} = (D/8192 - 1) \times V_{REF} \text{ (AD5555)} \quad (4)$$

For the AD5545, the external resistance tolerance becomes the dominant error that users should be aware of.

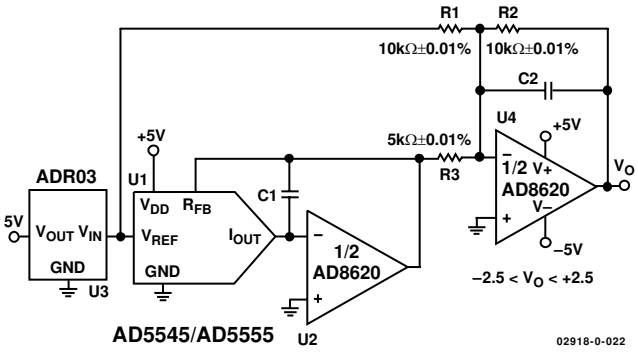

Figure 22. Four-Quadrant Multiplying Application Circuit

PROGRAMMABLE CURRENT SOURCE

Figure 23 shows a versatile V-to-I conversion circuit using improved Howland Current Pump. In addition to the precision current conversion it provides, this circuit enables a bidirectional current flow and high voltage compliance. This circuit can be used in a 4 mA to 20 mA current transmitter with up to a 500 Ω of load. In Figure 23, it shows that if the resistor network is matched, the load current is

$$I_L = \frac{\frac{(R2+R3)}{R1}}{R3} \times V_{REF} \times D \quad (5)$$

R3, in theory, can be made small to achieve the current needed within the U3 output current driving capability. This circuit is versatile such that the AD8510 can deliver ±20 mA in both directions, and the voltage compliance approaches 15 V, which is mainly limited by the supply voltages of U3. However, users must pay attention to the compensation. Without C1, it can be shown that the output impedance becomes

$$Z_O = \frac{R1'R3(R1+R2)}{R1(R2'+R3')-R1'(R2+R3)} \quad (6)$$

If the resistors are perfectly matched, Z_O is infinite, which is desirable, and the resistors behave as an ideal current source. On the other hand, if they are not matched, Z_O can be either positive or negative. The latter can cause oscillation. As a result, C1 is needed to prevent the oscillation. For critical applications, C1 could be found empirically but typically falls in the range of a few picofarads.

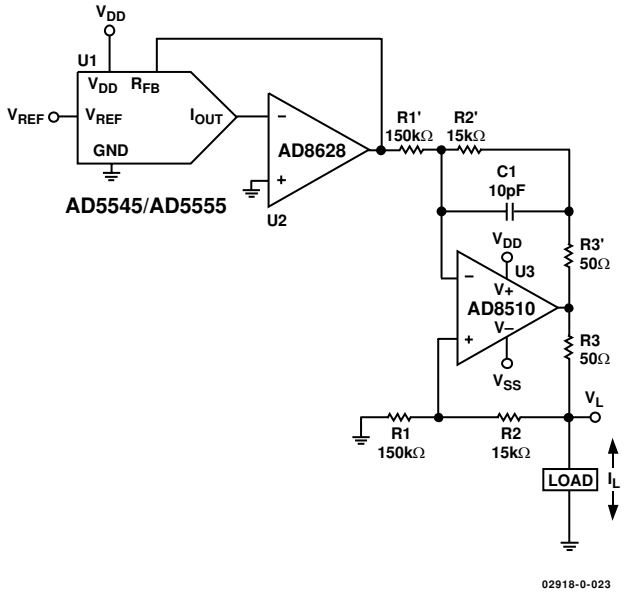

Figure 23. Programmable Current Source with Bidirectional Current Control and High Voltage Compliance Capabilities

DAC WITH PROGRAMMABLE INPUT REFERENCE RANGE

Because high voltage references can be costly, users may consider using one of the DACs, a digital potentiometer, and a low voltage reference to form a single-channel DAC with a programmable input reference range. This approach optimizes the programmable range as well as facilitates future system upgrades with just software changes. Figure 24 shows this implementation. $V_{REF}AB$ is in the feedback network, therefore,

$$V_{REF}AB = V_{REF} \times \left(1 + \frac{R_{WB}}{R_{WA}}\right) - \left(-V_{REF\_AB} \times \frac{D_A}{2^N} \times \frac{R_{WB}}{R_{WA}}\right) \quad (7)$$

where:
$V_{REF}AB$ = reference voltage of $V_{REF}A$ and $V_{REF}B$
V_{REF} = external reference voltage
D_A = DAC A digital code in decimal
N = number of bits of DAC

R_{WB} and R_{WA} are digital potentiometer 128-step programmable resistances and are given by

$$R_{WB} \approx \frac{D_C}{128} R_{AB} \quad (8)$$

$$R_{WA} \approx \frac{128 - D_C}{128} R_{AB} \quad (9)$$

$$\frac{R_{WB}}{R_{WA}} \approx \frac{D_C}{128 - D_C} \quad (10)$$

where D_C = digital potentiometer digital code in decimal ($0 \le D_C \le 127$).

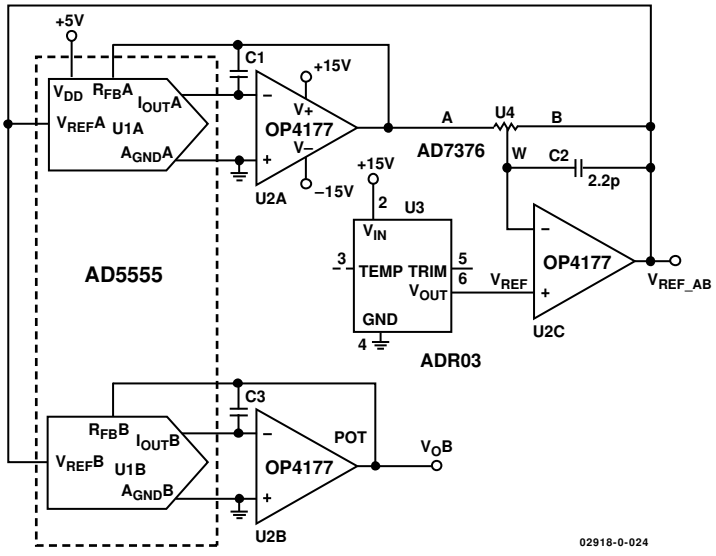

Figure 24. DAC with Programmable Input Reference Range

By putting Equations 7 through 10 together, the following results:

$$V_{REF}AB = V_{REF} \times \frac{\left(1 + \frac{D_C}{128 - D_C}\right)}{1 - \frac{D_A}{2^N} \times \frac{D_C}{128 - D_C}} \quad (11)$$

Table 9 shows a few examples of $V_{REF}AB$ of the 14-bit AD5555.

Table 9. $V_{REF}AB$ vs. D_B and D_C of the AD5555

D_C	D_A	$V_{REF}AB$
0	X	V_{REF}
32	0	1.33 V_{REF}
32	8192	1.6 V_{REF}
64	0	2 V_{REF}
64	8192	4 V_{REF}
96	0	4 V_{REF}
96	8192	−8 V_{REF}

The output of DAC B is, therefore,

$$V_{OB} = -V_{REF}AB \frac{D_B}{2^N} \quad (12)$$

where D_B is the DAC B digital code in decimal.

The accuracy of $V_{REF}AB$ is affected by the matching of the input and feedback resistors and, therefore, a digital potentiometer is used for U4 because of its inherent resistance matching. The AD7376 is a 30 V or ±15 V, 128-step digital potentiometer. If 15 V or ±7.5 V is adequate for the application, a 256-step AD5260 digital potentiometer can be used instead.

REFERENCE SELECTION

When selecting a reference for use with the AD55xx series of current output DACs, pay attention to the output voltage, temperature coefficient specification of the reference. Choosing a precision reference with a low output temperature coefficient minimizes error sources. Table 10 lists some of the references available from Analog Devices, Inc., that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. Because of the code-dependent output resistance of the DAC, the input offset voltage of an op amp is multiplied by the variable gain of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed upon the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, can cause the DAC to be nonmonotonic.

The input bias current of an op amp also generates an offset at the voltage output because of the bias current flowing in the feedback resistor, R_{FB}.

Common-mode rejection of the op amp is important in voltage-switching circuits because it produces a code-dependent error at the voltage output of the circuit.

Provided that the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage-switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, minimize capacitance at the V_{REF} node (the voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

Analog Devices offers a wide range of amplifiers for both precision dc and ac applications, as listed in Table 11 and Table 12.

Table 10. Suitable Analog Devices Precision References

Part No.	Output Voltage (V)	Initial Tolerance (%)	Maximum Temperature Drift (ppm/°C)	I_{SS} (mA)	Output Noise (µV p-p)	Package(s)
ADR01	10	0.05	3	1	20	SOIC-8
ADR01	10	0.05	9	1	20	TSOT-5, SC70-5
ADR02	5.0	0.06	3	1	10	SOIC-8
ADR02	5.0	0.06	9	1	10	TSOT-5, SC70-5
ADR03	2.5	0.1	3	1	6	SOIC-8
ADR03	2.5	0.1	9	1	6	TSOT-5, SC70-5
ADR06	3.0	0.1	3	1	10	SOIC-8
ADR06	3.0	0.1	9	1	10	TSOT-5, SC70-5
ADR420	2.048	0.05	3	0.5	1.75	SOIC-8, MSOP-8
ADR421	2.50	0.04	3	0.5	1.75	SOIC-8, MSOP-8
ADR423	3.00	0.04	3	0.5	2	SOIC-8, MSOP-8
ADR425	5.00	0.04	3	0.5	3.4	SOIC-8, MSOP-8
ADR431	2.500	0.04	3	0.8	3.5	SOIC-8, MSOP-8
ADR435	5.000	0.04	3	0.8	8	SOIC-8, MSOP-8
ADR391	2.5	0.16	9	0.12	5	TSOT-5
ADR395	5.0	0.10	9	0.12	8	TSOT-5

Table 11. Suitable Analog Devices Precision Op Amps

Part No.	Supply Voltage (V)	V_{OS} Maximum (µV)	I_B Maximum (nA)	0.1 Hz to 10 Hz Noise (µV p-p)	Supply Current (µA)	Package(s)
OP97	±2 to ±20	25	0.1	0.5	600	SOIC-8, PDIP-8
OP1177	±2.5 to ±15	60	2	0.4	500	MSOP-8, SOIC-8
AD8675	±5 to ±18	75	2	0.1	2300	MSOP-8, SOIC-8
AD8671	±5 to ±15	75	12	0.077	3000	MSOP-8, SOIC-8
ADA4004-1	±5 to ±15	125	90	0.1	2000	SOIC-8, SOT-23-5
AD8603	1.8 to 5	50	0.001	2.3	40	TSOT-5
AD8607	1.8 to 5	50	0.001	2.3	40	MSOP-8, SOIC-8
AD8605	2.7 to 5	65	0.001	2.3	1000	WLCSP-5, SOT-23-5
AD8615	2.7 to 5	65	0.001	2.4	2000	TSOT-5
AD8616	2.7 to 5	65	0.001	2.4	2000	MSOP-8, SOIC-8

Table 12. Suitable Analog Devices High Speed Op Amps

Part No.	Supply Voltage (V)	BW @ ACL (MHz)	Slew Rate (V/µs)	V_{OS} (Max) (µV)	I_B (Max) (nA)	Package(s)
AD8065	5 to 24	145	180	1500	0.006	SOIC-8, SOT-23-5
AD8066	5 to 24	145	180	1500	0.006	SOIC-8, MSOP-8
AD8021	5 to 24	490	120	1000	10,500	SOIC-8, MSOP-8
AD8038	3 to 12	350	425	3000	750	SOIC-8, SC70-5
ADA4899-1	5 to 12	600	310	35	100	LFCSP-8, SOIC-8
AD8057	3 to 12	325	1000	5000	500	SOT-23-5, SOIC-8
AD8058	3 to 12	325	850	5000	500	SOIC-8, MSOP-8
AD8061	2.7 to 8	320	650	6000	350	SOT-23-5, SOIC-8
AD8062	2.7 to 8	320	650	6000	350	SOIC-8, MSOP-8
AD9631	±3 to ±6	320	1300	10,000	7000	SOIC-8, PDIP-8

EVALUATION BOARD FOR THE AD5545

The EVAL-AD5545SDZ is used in conjunction with an SDP1Z system demonstration platform board available from Analog Devices, which is purchased separately from the evaluation board. The USB-to-SPI communication to the AD5545 is completed using this Blackfin®-based demonstration board.

SYSTEM DEMONSTRATION PLATFORM

The system demonstration platform (SDP) is a hardware and software evaluation tool for use in conjunction with product evaluation boards. The SDP board is based on the Blackfin ADSP-BF527 processor with USB connectivity to the PC through a USB 2.0 high speed port. For more information about this device, see the system demonstration platform web page.

OPERATING THE EVALUATION BOARD

The evaluation board requires ±12 V and +5 V supplies. The +12 V V_{DD} and −12 V V_{SS} are used to power the output amplifier, and the +5 V is used to power the DAC (DVDD).

Figure 25. Evaluation Board Software – Device Selection Window

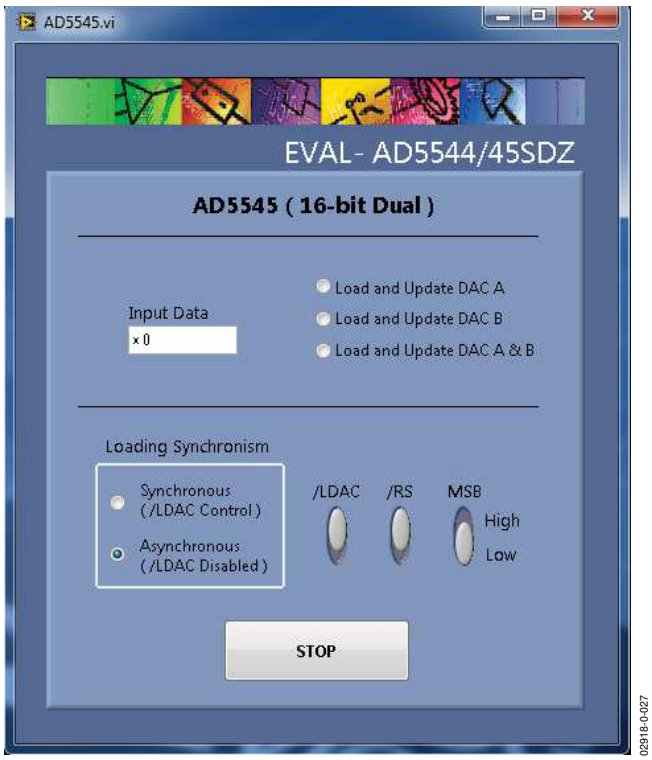

Figure 26. Evaluation Board Software—AD5545 Dual DAC

EVALUATION BOARD SCHEMATICS

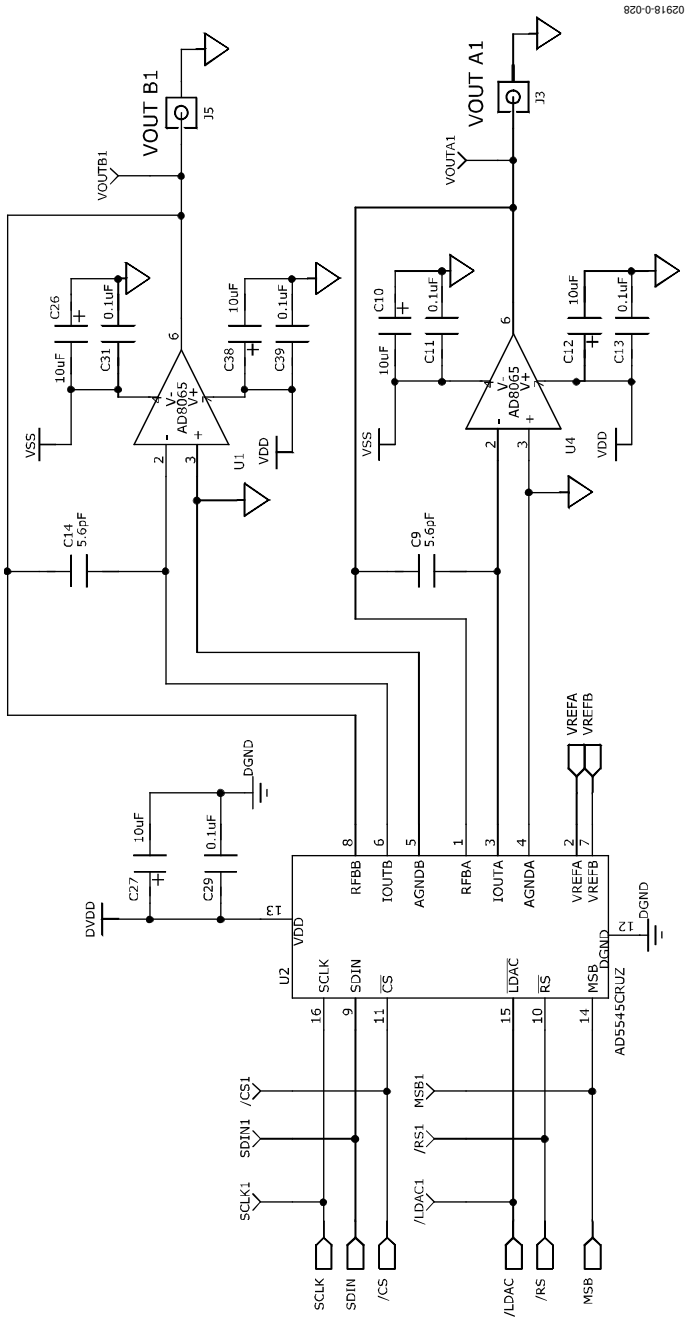

Figure 27. EVAL-AD5545SDZ Schematic Part A

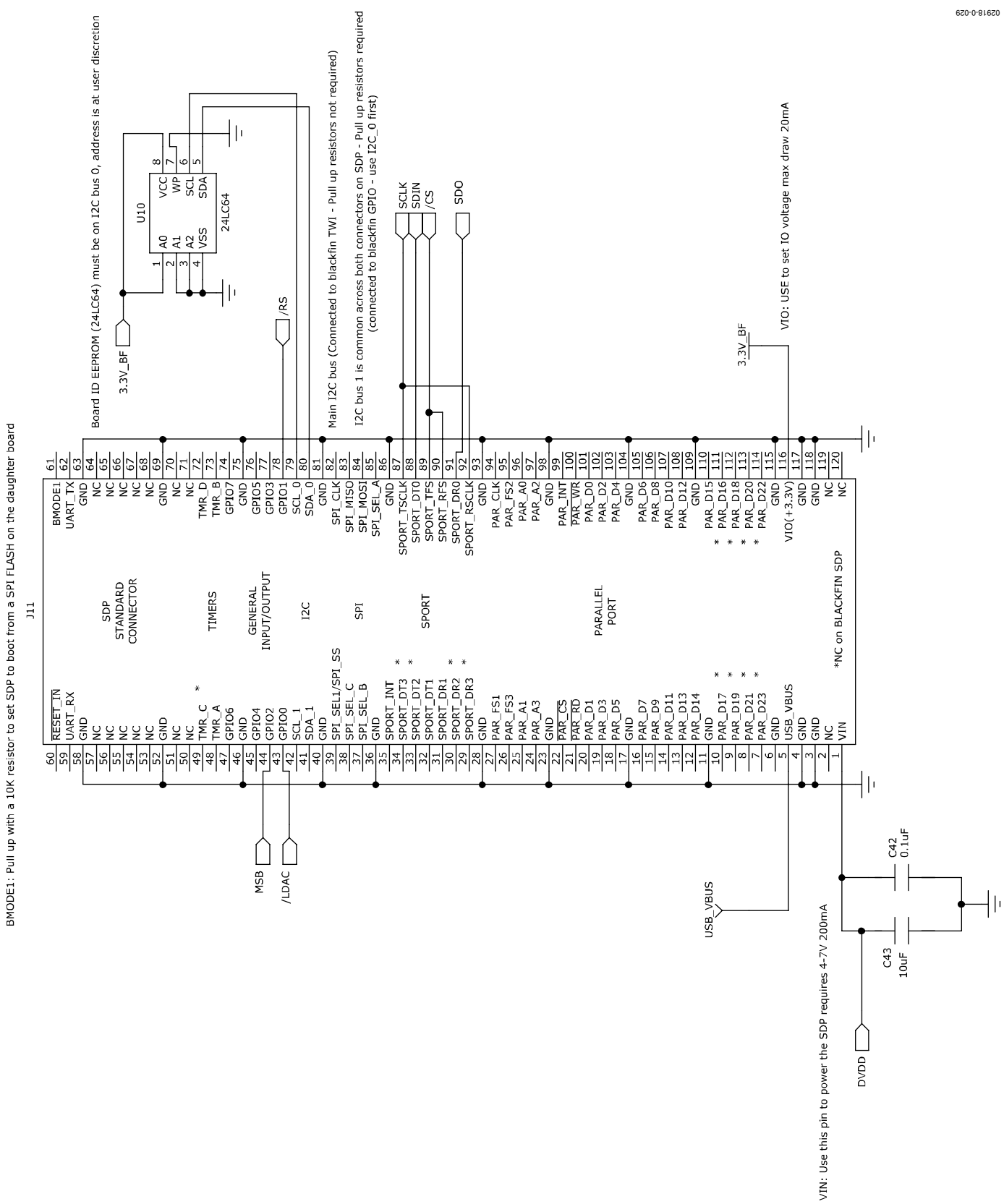

Figure 28. EVAL-AD5545SDZ Schematic Part B

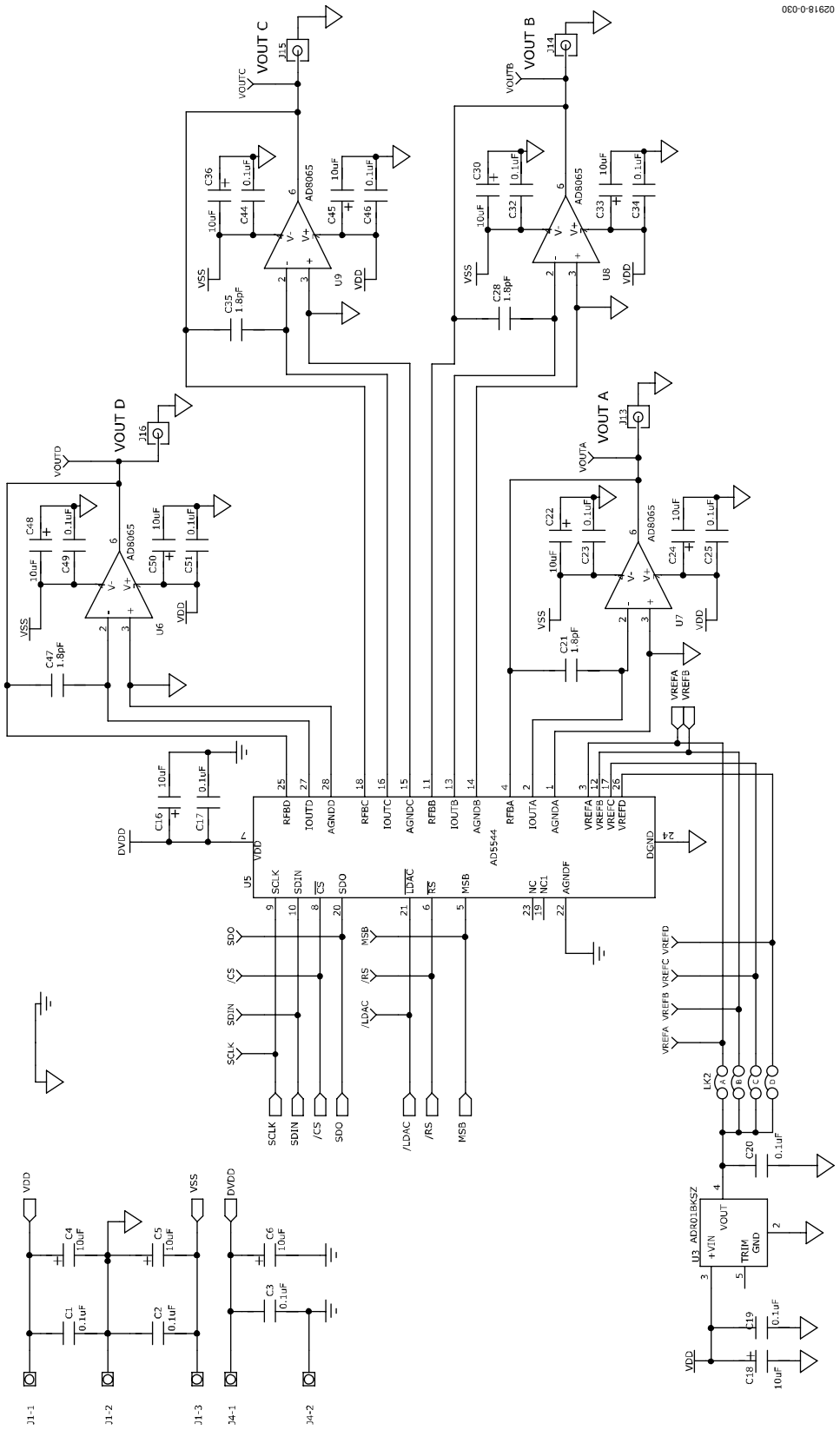

Figure 29. EVAL-AD5545SDZ Schematic Part B

EVALUATION BOARD LAYOUT

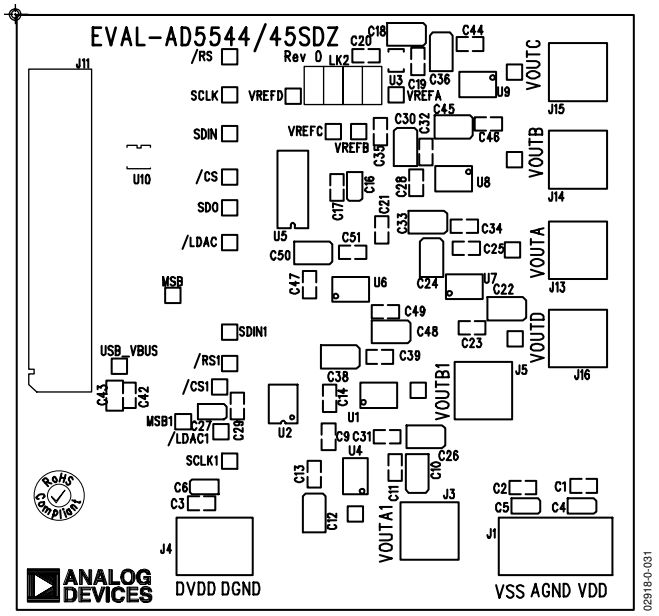

Figure 30. Silkscreen

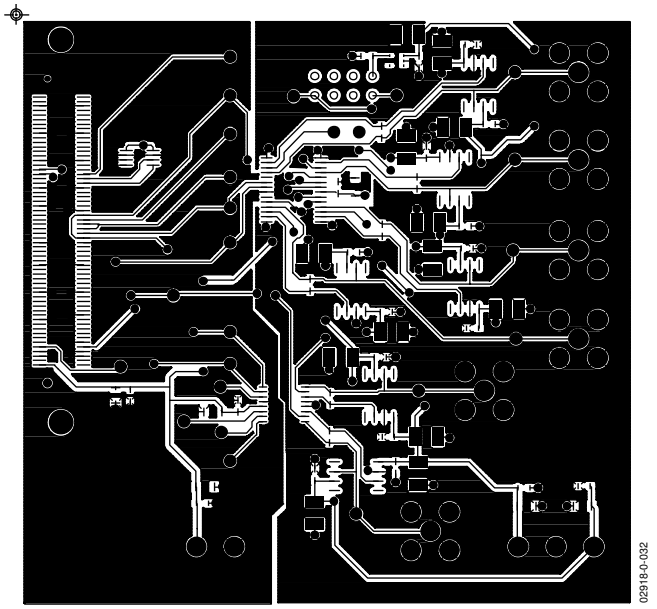

Figure 31. Component Side

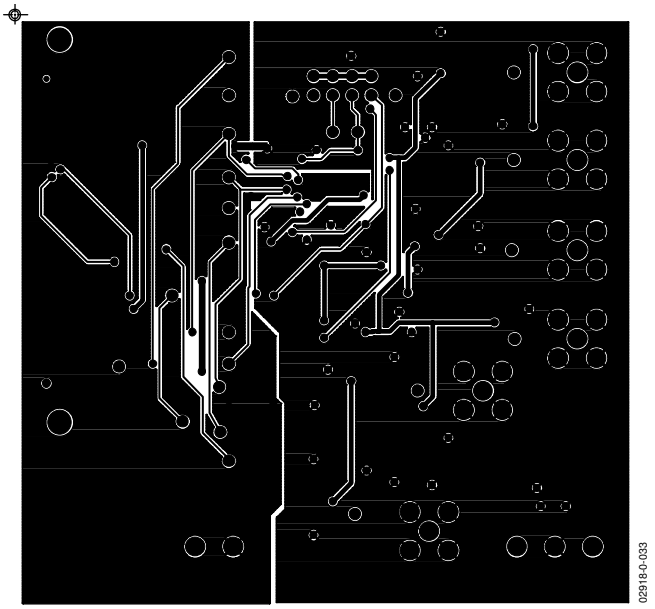

Figure 32. Solder Side

OUTLINE DIMENSIONS

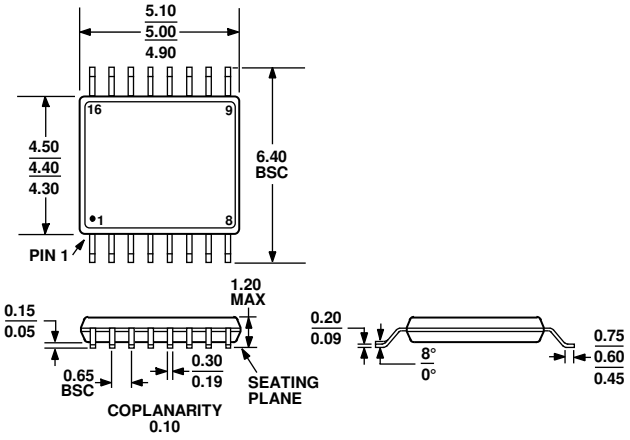

Figure 33. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	INL LSB	DNL LSB	Resolution (Bits)	Temperature Range	Package Description	Package Option	Ordering Qty
AD5545BRUZ	±2	±1	16	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5545BRUZ-REEL7	±2	±1	16	−40°C to +85°C	16-Lead TSSOP	RU-16	1000
AD5545CRUZ	±1	±1	16	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5545CRUZ-REEL7	±1	±1	16	−40°C to +85°C	16-Lead TSSOP	RU-16	1000
AD5555CRU	±1	±1	14	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5555CRUZ	±1	±1	14	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5555CRUZ-REEL7	±1	±1	14	−40°C to +85°C	16-Lead TSSOP	RU-16	1000
EV-AD5544/45SDZ				Evaluation Board			

[1] The AD5545/AD5555 contain 3131 transistors. The die size measures 71 mil. × 96 mil., 6816 sq. mil.
[2] Z = RoHS Compliant Part.