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1.2 A Programmable Device Power Supply with Integrated 16-Bit Level Setting DACs

Data Sheet **AD5560**

FEATURES

- Programmable device power supply (DPS)
  - FV, MI, MV, FNMV functions
- 5 internal current ranges (on-chip R_{SENSE})
  - ±5 µA, ±25 µA, ±250 µA, ±2.5 mA, ±25 mA
- 2 external high current ranges (external R_{SENSE})
  - EXTFORCE1: ±1.2 A maximum
  - EXTFORCE2: ±500 mA maximum
- Integrated programmable levels
  - All 16-bit DACs: force DAC, comparator DACs, clamp DACs, offset DAC, OSD DAC, DGS DAC
- Programmable Kelvin clamp and alarm
- Offset and gain correction registers on-chip
- Ramp mode on force DAC for power supply slewing
- Programmable slew rate feature, 1 V/µs to 0.3 V/µs
- DUTGND Kelvin sense and alarm
- 25 V FV span with asymmetrical operation within −22 V/+25 V
- On-chip comparators
- Gangable for higher current
- Guard amplifier
- System PMU connections
- Current clamps
- Die temperature sensor and shutdown feature
- On-chip diode thermal array
- Diagnostic register allows access to internal nodes
- Open-drain alarm flags (temperature, current clamp, Kelvin alarm)
- SPI-/MICROWIRE-/DSP-compatible interface
- 64-lead (10 mm × 10 mm) TQFP with exposed pad (on top)
- 72-ball (8 mm × 8 mm) flip-chip BGA

APPLICATIONS

- Automatic test equipment (ATE)
  - Device power supply

GENERAL DESCRIPTION

The AD5560 is a high performance, highly integrated device power supply consisting of programmable force voltages and measure ranges. This part includes the required DAC levels to set the programmable inputs for the drive amplifier, as well as clamping and comparator circuitry. Offset and gain correction is included on-chip for DAC functions. A number of programmable measure current ranges are available: five internal fixed ranges and two external customer-selectable ranges (EXTFORCE1 and EXTFORCE2) that can supply currents up to ±1.2 A and ±500 mA, respectively. The voltage range possible at this high current level is limited by headroom and the maximum power dissipation. Current ranges in excess of ±1.2 A or at high current and high voltage combinations can be achieved by paralleling or ganging multiple DPS devices. Open-drain alarm outputs are provided in the event of overcurrent, overtemperature, or Kelvin alarm on either the SENSE or DUTGND line.

The DPS functions are controlled via a simple 3-wire serial interface compatible with SPI, QSPI™, MICROWIRE™, and DSP interface standards running at clock speeds of up to 50 MHz.

Rev. E

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AD5560* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

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EVALUATION KITS

- AD5560 Evaluation Board

DOCUMENTATION

Data Sheet

- AD5560: 1.2 A Programmable Device Power Supply with Integrated 16-Bit Level Setting DACs Data Sheet

User Guides

- User Guide for the AD5560 Device Power Supply (DPS) with DACs

REFERENCE DESIGNS

- CN0130

DESIGN RESOURCES

- AD5560 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD5560 EngineerZone Discussions.

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FUNCTIONAL BLOCK DIAGRAM

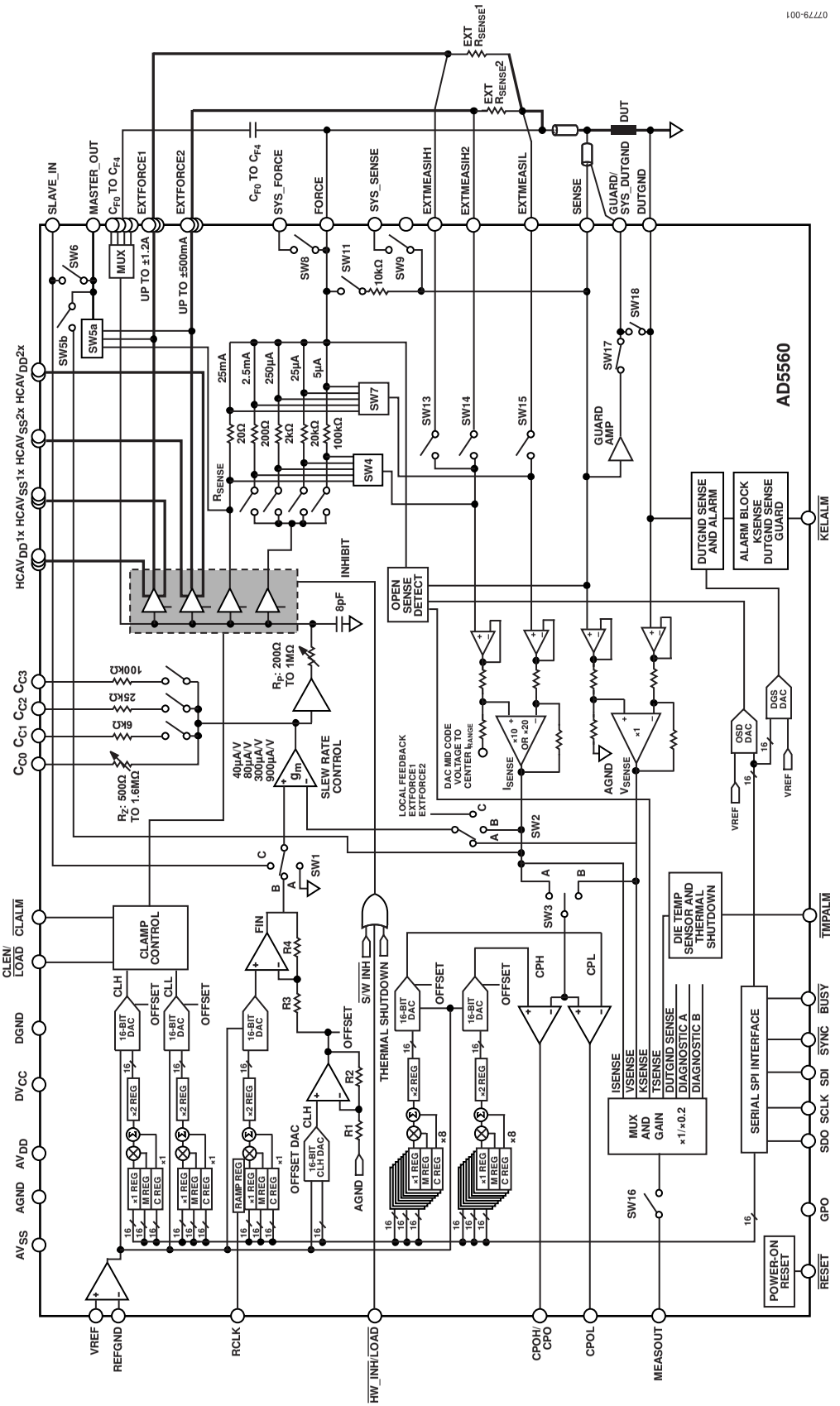

Figure 1.

SPECIFICATIONS

$HCAV_{DD}x \le (AV_{SS} + 33\ V)$, $HCAV_{DD}x \le AV_{DD}$, $HCAV_{SS}x \ge AV_{SS}$, $AV_{DD} \ge 8\ V$, $AV_{SS} \le -5\ V$, $|AV_{DD} - AV_{SS}| \ge 16\ V$ and $\le 33\ V$, DV_{CC} = 2.3 V to 5.5 V, V_{REF} = 5 V, gain (m), offset (c), and DAC offset registers are at default values; AGND = DGND = 0 V; T_J = 25°C to 90°C, maximum specifications, unless otherwise noted. FSV is full-scale voltage, FSVR is full-scale voltage range, FSC is full-scale current, FSCR is full-scale current range.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FORCE VOLTAGE					
Force Output Voltage[1]					
EXTFORCE1	AV_{SS} + 2.25		AV_{DD} − 2.25	V	Allow ±500 mV for external R_{SENSE} voltage drop
	$HCAV_{SS}1x$ + 1.75		$HCAV_{SS}1x$ − 1.75	V	Allow ±500 mV for external R_{SENSE} voltage drop
	$HCAV_{SS}1x$ + 1.25		$HCAV_{DD}1x$ − 1.25	V	Allow ±500 mV for external R_{SENSE} voltage drop; reduced headroom/footroom, clamps must be enabled[2]
EXTFORCE2	AV_{SS} + 2.25		AV_{DD} − 2.25	V	Allow ±500 mV for external R_{SENSE} voltage drop
	$HCAV_{SS}2x$ + 1.75		$HCAV_{DD}2x$ − 1.75	V	Allow ±500 mV for external R_{SENSE} voltage drop
	$HCAV_{SS}2x$ + 1.25		$HCAV_{DD}2x$ − 1.25	V	Allow ±500 mV for external R_{SENSE} voltage drop; reduced headroom/footroom, clamps must be enabled[2]
FORCE	AV_{SS} + 2.75		AV_{DD} − 2.75	V	Internal current ranges, includes ±500 mV for internal R_{SENSE} voltage drop
Headroom/Footroom[1]	−2.75		+2.75	V	Internal current ranges to AV_{DD}/AV_{SS}, includes ±500 mV for internal R_{SENSE} voltage drop.
Headroom/Footroom[1]	−2.25		+2.25	V	External current ranges, EXTFORCE1/ EXTFORCE2 to $HCAV_{DD}x$ and $HCAV_{SS}x$ supplies; includes ±500 mV for external R_{SENSE} voltage drop.\
Force Output Voltage Span	−22		+25	V	May be a skewed range but within headroom requirements and maximum power dissipation for current range
Forced Voltage Linearity Error	−2		+2	mV	
Forced Voltage Offset Error	−50		+50	mV	Uncalibrated, use c register to calibrate, measured at midscale
Forced Voltage Offset Error Tempco[1]		27		µV/°C	Standard deviation = 23 µV/°C
Forced Voltage Gain Error	−25		+25	mV	Uncalibrated, use m register to calibrate
Forced Voltage Gain Error Tempco[1]		4		ppm/°C	Standard deviation = 3 ppm/°C
Short-Circuit Current Limit[3]					Clamps off
EXTFORCE1	−3.5	±2.7	+3.5	A	Positive and negative dc short-circuit current
EXTFORCE2	−1.25	±0.9	+1.25	A	Positive and negative dc short-circuit current
FORCE	−75	±50	+75	mA	±25 mA range, positive and negative dc short-circuit current
	−20	±10	+20	mA	All other ranges, positive and negative dc short-circuit current
Active C_{Fx} Buffer	−64		+64	mA	
DC Load Regulation[1]	−1		+1	mV	EXTFORCE1 range, ±1 A load current change
	−0.4		+0.4	mV	EXTFORCE2 range, ±0.5 A load current change
Load Transient Response[1]		70		mV	1.2 A load step into 100 µF DUT capacitance (10 mΩ ESR), autocompensation mode
		140		mV	1.2 A load step into 30 µF DUT capacitance (10 mΩ ESR), autocompensation mode
NSD[1]		350		nV/√Hz	Measured at 1 kHz, at output of FORCE
MEASURE CURRENT RANGES					Sense resistors are trimmed to within 1%, nominal ±500 mV V_{RSENSE}
Internal Sense Resistors[1]		100		kΩ	±5 µA current range
		20		kΩ	±25 µA current range
		2		kΩ	±250 µA current range
		200		Ω	±2.5 mA current range
		20		Ω	±25 mA current range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Measure Current Ranges					Specified current ranges with V_{REF} = 5 V and MI gain = 20, or with V_{REF} = 2.5 V and MI gain = 5
		±5		µA	Set using internal sense resistor
		±25		µA	Set using internal sense resistor
		±250		µA	Set using internal sense resistor
		±2.5		mA	Set using internal sense resistor
		±25		mA	Set using internal sense resistor
		±500		mA	EXTFORCE2, set by user with external sense resistor, limited by headroom requirements and maximum power dissipation
		±1200		mA	EXTFORCE1, set by user with external sense resistor, limited by headroom requirements and maximum power dissipation
MEASURE CURRENT					All offset DAC/supply combinations settings, all gain settings are measure current = (I_{DUT} × R_{SENSE} × MI gain), unless otherwise noted
Differential Input Voltage Range[1]	−0.64		+0.64	V	Maximum voltage across R_{SENSE}, MI gain = 20
	−0.7		+0.7	V	Maximum voltage across R_{SENSE}, MI gain = 10
Output Voltage Span[1]		25		V	Measure current block alone (internal node)
Offset Error	−1		+1	% FSC	At 0 A, MI gain = 20, MEASOUT gain = 1
Offset Error Tempco[1]		−1		ppm of FSC/°C	Standard deviation = 13 ppm/°C
Offset Error	−1.5		+1.5	% FSC	At 0 A, MI gain = 10, MEASOUT gain = 1
Offset Error Tempco[1]		−1		ppm of FSC/°C	Standard deviation = 13 ppm/°C
Offset Error	−1.5		+1.5	% FSC	At 0 A, MI gain = 20, MEASOUT gain = 0.2
Offset Error Tempco[1]		3		ppm of FSC/°C	Standard deviation = 13 ppm/°C
Offset Error	−3		+3	% FSC	At 0 A, MI gain = 10, MEASOUT gain = 0.2
Offset Error Tempco[1]		8		ppm of FSC/°C	Standard deviation = 15 ppm/°C
Gain Error	−2		+2	% FSC	Internal current ranges, all gain settings
Gain Error[1]	−1		+1	% FSC	External current ranges, excluding R_{SENSE}
Gain Error Tempco[1]		20		ppm/°C	Standard deviation = 5 ppm/°C
MEASOUT Gain = 1					All supply conditions
Linearity Error	−0.01		+0.01	% FSCR	MI gain = 20 and 10
MEASOUT Gain = 0.2					Nominal supply (±16.5 V, 0x8000 offset DAC)
Linearity Error	−0.06		+0.06	% FSCR	MI gain = 20
Linearity Error	−0.05		+0.05	% FSCR	MI gain = 10
MEASOUT Gain = 0.2					Low supply (−25 V/+8 V, 0xD4EB offset DAC)
Linearity Error	−0.125		+0.125	% FSCR	MI gain = 20
Linearity Error	−0.175		+0.175	% FSCR	MI gain = 10
MEASOUT Gain = 0.2					High supply (−5 V/+28 V, 0xD1D offset DAC)
Linearity Error	−0.0875		+0.0875	% FSCR	MI gain = 20
Linearity Error	−0.1		+0.1	% FSCR	MI gain = 10
Common-Mode Error	−0.005		+0.005	%FSVR/V	% of FS change at measure output per volts change in DUT voltage
NSD[1]		900		nV/√Hz	MI gain = 20, MEASOUT gain = 1, measured at MEASOUT at 1 kHz, inputs grounded
		550		nV/√Hz	MI gain = 10, MEASOUT gain = 1, measured at MEASOUT at 1 kHz, inputs grounded
		170		nV/√Hz	MI gain = 20, MEASOUT gain = 0.2, measured at MEASOUT at 1 kHz, inputs grounded
		110		nV/√Hz	MI gain = 10, MEASOUT gain = 0.2, measured at MEASOUT at 1 kHz, inputs grounded
MEASURE VOLTAGE					MEASOUT Gain 1 and MEASOUT Gain 0.2
Measure Voltage Range[1]	AV_{SS} + 2.75		AV_{DD} − 2.75	V	All voltage ranges
Gain Error	−0.1		+0.1	% FS	
Gain Error Tempco[1]		3		ppm/°C	Standard deviation = 2 ppm/°C
MEASOUT Gain = 1					
Linearity Error	−2		+2	mV	
Offset Error	−12		+12	mV	
Offset Error Tempco[1]		2		µV/°C	Standard deviation = 12 µV/°C
NSD[1]		100		nV/√Hz	At 1 kHz, at MEASOUT, inputs grounded

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MEASOUT Gain = 0.2					
Linearity Error	−5.5		+5.5	mV	Referred to MV input, nominal supply (±16.5 V, 0x8000 offset DAC)
	−9		+24	mV	Referred to MV input, low supply (−25 V/+8 V, 0xD4EB offset DAC)
	−4		+13	mV	Referred to MV input, high supply (−5 V/+28 V, 0xD1D offset DAC)
Offset Error	−30		+20	mV	Referred to MV output
Offset Error Tempco[1]		10		µV/°C	Standard deviation = 12 µV/°C, referred to MV output
NSD[1]		50		nV/√Hz	At 1 kHz, at MEASOUT, inputs grounded
COMBINED LEAKAGE					Includes SYS_SENSE, SYS_FORCE, EXTFORCE1, EXTFORCE2, EXTMEASIH1, EXTMEASIH2, EXTMEASIL, FORCE, and SENSE; measured with $\overline{PD}$ = 1, $\overline{SW\text{-}INH}$ = 0 (power up and tristate)
Leakage Current	−37.5		+37.5	nA	
	−30		+30	nA	T_J = 25°C to 70°C
Leakage Current Tempco[1]		±0.1	±0.4	nA/°C	
SENSE INPUT					
Leakage Current	−2.5		+2.5	nA	Measured with $\overline{PD}$ = 1, $\overline{SW\text{-}INH}$ = 0 (power-up and tristate)
Leakage Current Tempco[1]		±0.01		nA/°C	
Pin Capacitance[1]		10		pF	
EXTMEASIH1, EXTMEASIH2, EXTMEASIL					
Leakage Current	−2.5		+2.5	nA	Measured with $\overline{PD}$ = 1, $\overline{SW\text{-}INH}$ = 0 (power-up and tristate)
Leakage Current Tempco[1]		±0.01		nA/°C	
Pin Capacitance[1]		5		pF	
FORCE OUTPUT, FORCE					
Maximum Current Drive[1]	−30		+30	mA	
Leakage Current	−10		+10	nA	Measured with $\overline{PD}$ = 1, $\overline{SW\text{-}INH}$ = 0 (power-up and tristate)
Leakage Current Tempco[1]		±0.03		nA/°C	
Pin Capacitance[1]		120		pF	
EXTFORCE1 OUTPUTS					
Maximum Current Drive[1]	−1200		+1200	mA	Set with external sense resistor, limited by headroom and power dissipation
Leakage Current	−7.5		+7.5	nA	Measured with $\overline{PD}$ = 1, $\overline{SW\text{-}INH}$ = 0 (power-up and tristate)
Leakage Current Tempco[1]		±0.03	±0.06	nA/°C	
Pin Capacitance[1]		275		pF	
EXTFORCE2 OUTPUTS					
Maximum Current Drive[1]	−500		+500	mA	Set with external sense resistor, limited by headroom and power dissipation
Leakage Current	−5		+5	nA	Measured with $\overline{PD}$ = 1, $\overline{SW\text{-}INH}$ = 0 (power-up and tristate)
Leakage Current Tempco[1]		±0.02	±0.05	nA/°C	
Pin Capacitance[1]		100		pF	
SYS_SENSE					
Voltage Range	AV_{SS}		AV_{DD}	V	
Leakage Current	−2.5		+2.5	nA	SYS_SENSE high-Z, force amplifier inhibited
Leakage Current Tempco[1]		±0.005	±0.025	nA/°C	
Path On Resistance			280	Ω	AV_{DD} = 16.5 V, AV_{SS} = −16.5 V
Pin Capacitance[1]		5		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYS_FORCE					
Voltage Range	AV_{SS}		AV_{DD}	V	
Current Carrying Capability[1]	−25		+25	mA	
Leakage Current	−2.5		+2.5	nA	SYS_FORCE high-Z, force amplifier inhibited
Leakage Current Tempco[1]		±0.005	±0.025	nA/°C	
Path On Resistance			35	Ω	AV_{DD} = 16.5 V, AV_{SS} = −16.5 V
Pin Capacitance[1]		5		pF	
SYS_DUTGND					
Voltage Range	AV_{SS}		AV_{DD}	V	
Path On Resistance		300	400	Ω	AV_{DD} = 16.5 V, AV_{SS} = −16.5 V
CURRENT CLAMP					
Clamp Accuracy	Programmed clamp value		Programmed clamp value + 10	% of FS	MI gain = 20, with clamp separation of 2 V, and 1 V separation from AGND/0 A
	Programmed clamp value		Programmed clamp value + 20	% of FS	MI gain = 10, with clamp separation of 2 V, and 1 V separation from AGND/0 A
VCLL to VCLH[1]	2			V	10% of FSCR (MI gain = 20), 20% of FSCR (MI gain = 10), restriction to prevent both clamps activating together
VCLL to 0 A[1]	1			V	5% of FSCR (MI gain = 20), 10% of FSCR (MI gain = 10), restriction to avoid impinging on FV before programmed level
VCLH to 0 A[1]	1			V	5% of FSCR (MI gain 20), 10% of FSCR (MI gain = 10), restriction to avoid impinging on FV before programmed level
Clamp Activation Response Time[1]		20	100	µs	Measured from $\overline{BUSY}$ going low to visible clamping
Clamp Recovery[1]		2	5	µs	Measured from $\overline{BUSY}$ going low to visible recovery
Alarm Delay [1]		50		µs	Time for $\overline{CLALM}$ to flag
FORCE AMPLIFER					
Slew Rate[1]		1		V/µs	Fastest slew rate, controlled via serial interface
		0.312		V/µs	Slowest slew rate, controlled via serial interface
Maximum Stable Load Capacitance[1]			160	µF	
Voltage Overshoot/Undershoot[1]			5	%	Of programmed value (≥1 V)
SETTLING TIME (FORCE AMPLIFER)	Compensation Register 1 = 0x4880 (229 nF to 380 nF, ESR 74 to 140 mΩ)				To within 10 mV of programmed value
FV (1200 mA EXTFORCE1 Range)[1]		16	25	µs	3.7 V step, R_{DUT} = 2.4 Ω, C_{DUT} = 0.22 µF, full dc load
FV (900 mA EXTFORCE1 Range)[1]		18	30	µs	8 V step, R_{DUT} = 8.8 Ω, C_{DUT} = 0.22 µF, full dc load
FV (500 mA EXTFORCE2 Range)[1]		34	53	µs	15 V step, R_{DUT} = 30 Ω, C_{DUT} = 0.22 µF, full dc load
FV (300 mA EXTFORCE2 Range)[1]		25	50	µs	10 V step, R_{DUT} = 33.3 Ω, C_{DUT} = 0.22 µF, full dc load
FV (25 mA Range)[1, 3]		125	180	µs	20 V step, R_{DUT} = 800 Ω, C_{DUT} = 0.22 µF, full dc load
FV (2.5 mA Range)[1, 3]		300	500	µs	10 V step, R_{DUT} = 4 kΩ, C_{DUT} = 0.22 µF, full dc load
FV (250 µA Range)[1, 3]		300	500	µs	10 V step, R_{DUT} = 40 kΩ, C_{DUT} = 0.22 µF, full dc load
FV (25 µA Range)[1, 3]		400	600	µs	10 V step, R_{DUT} = 400 kΩ, C_{DUT} = 0.22 µF, full dc load
FV (5 µA Range)[1, 3]		20	40	µs	1 V step, R_{DUT} = 200 kΩ, C_{DUT} = 0.22 µF, full dc load
	Compensation Register 1 = 0x8880 (1.7 µF to 2.9 µF, ESR 74 to 140 mΩ)				
FV (180 mA EXTFORCE1 Range)[1]		16	25	µs	3 V step, C_{DUT} = 2.2 µF, full dc load
FV (100 mA EXTFORCE2 Range)[1]		60	80	µs	8 V step, C_{DUT} = 2.2 µF, full dc load
	Compensation Register 1 = 0xB880 (7.9µF to 13 µF, ESR 74 to 140 mΩ)				
FV (180 mA EXTFORCE1 Range)[1]		55	70	µs	3 V step, C_{DUT} = 10 µF, full dc load
FV (100 mA EXTFORCE2 Range)[1]		210	260	µs	8 V step, C_{DUT} = 10 µF, full dc load
	Compensation Register 1 = 0xC880 (13 µF to 22 µF, ESR 74 to 140 mΩ)				
FV (180 mA EXTFORCE1 Range)[1]		65	80	µs	3 V step, C_{DUT} = 20 µF, full dc load
FV (100 mA EXTFORCE2 Range)[1]		310	370	µs	8 V step, C_{DUT} = 20 µF, full dc load

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SETTLING TIME (FV, MEASURE CURRENT)	Compensation Register 1 = 0x4880 (229 nF to 380 nF, ESR 74 to 140 mΩ)				To within 10 mV of programmed value
MI (1200 mA EXTFORCE1 Range)[1]		30	40	µs	3.7 V step, R_{DUT} = 2.4 Ω, C_{DUT} = 0.22 µF, full dc load
MI (900 mA EXTFORCE1 Range)[1]		32	42	µs	8 V step, R_{DUT} = 8.8 Ω, C_{DUT} = 0.22 µF, full dc load
MI (500 mA EXTFORCE2 Range)[1]		69	95	µs	15 V step, R_{DUT} = 30 Ω, C_{DUT} = 0.22 µF, full dc load
MI (300 mA EXTFORCE2 Range)[1]		70	100	µs	10 V step, R_{DUT} = 33.3 Ω, C_{DUT} = 0.22 µF, full dc load
MI (25 mA Range)[1, 3]		650		µs	20 V step, R_{DUT} = 800 Ω, C_{DUT} = 0.22 µF, full dc load
MI (2.5 mA Range)[1, 3]		6400		µs	10 V step, R_{DUT} = 4 kΩ, C_{DUT} = 0.22 µF, full dc load
MI Buffer Alone[1]		10	15	µs	0.5 V step using MEASOUT high-Z to within 10 mV of final value
SETTLING TIME (FV, MEASURE VOLTAGE)	Compensation Register 1 = 0x4880 (229 nF to 380 nF, ESR 74 to 140 mΩ)				To within 10 mV of programmed value
MV (1200 mA Range)[1]		16		µs	3.7 V step, R_{DUT} = 2.4 Ω, C_{DUT} = 0.22 µF, full dc load
MV (900 mA Range)[1]		20		µs	8 V step, R_{DUT} = 8.8 Ω, C_{DUT} = 0.22 µF, full dc load
MV (500 mA Range)[1]		34		µs	15 V step, R_{DUT} = 30 Ω, C_{DUT} = 0.22 µF, full dc load
MV (300 mA Range)[1]		25		µs	10 V step, R_{DUT} = 33.3 Ω, C_{DUT} = 0.22 µF, full dc load
MV (25 mA Range)[1, 3]		125	180	µs	20 V step, R_{DUT} = 800 Ω, C_{DUT} = 0.22 µF, full dc load
MV (2.5 mA Range)[1, 3]		300	500	µs	10 V step, R_{DUT} = 4 kΩ, C_{DUT} = 0.22 µF, full dc load
MV (250 µA Range)[1, 3]		300	500	µs	10 V step, R_{DUT} = 40 kΩ, C_{DUT} = 0.22 µF, full dc load
MV Buffer Alone[1]		2	5	µs	10 V step using MEASOUT high-Z to within 10 mV of final value
SETTLING TIME (FV) SAFE MODE					To within 100 mV of programmed value
FV (1200 mA EXTFORCE1 Range[1]		25		µs	3.7 V step, R_{DUT} = 3.1 Ω, C_{DUT} = 0.22 µF, full dc load
FV (180 mA EXTFORCE1 Range)[1]		303		µs	3 V step, R_{DUT} = 16 Ω, C_{DUT} = 0. 22 µF to 20 µF, full dc load
FV (100 mA EXTFORCE2 Range)[1]		660		µs	8 V step, R_{DUT} = 33.3 Ω, C_{DUT} = 0. 22 µF to 20 µF, full dc load
FV (25 mA Range)[1, 3]		760	1000	µs	20 V step, R_{DUT} = 400 Ω, C_{DUT} = 0.22 µF, full dc load
SWITCHING TRANSIENTS					
Range Change Transient[1]			0.5	% of FV	C_{DUT} = 10 µF, changing from higher to adjacent lower ranges (except EXTFORCE1 to EXTFORCE2)
	20			mV	C_{DUT} = 10 µF, changing from lower (5 µA) to higher range (EXTFORCE1)
			0.5	% of FV	C_{DUT} = 100 µF, changing between all ranges
DAC SPECIFICATIONS					
Force/Comparator/Offset DACs					
Resolution		16		Bits	
Voltage Output Span	−22		+25	V	V_{REF} = 5 V, minimum and maximum values set by offset DAC
Differential Nonlinearity[1]	−1		+1	LSB	Guaranteed monotonic
Offset DAC					
Gain Error	−20		+20	mV	
Clamp DAC					CLL < CLH
Resolution		16		Bits	
Voltage Output Span	−22		+25	V	V_{REF} = 5 V, minimum and maximum values set by offset DAC
Differential Nonlinearity[1]	−1		+1	LSB	Guaranteed monotonic
OSD DAC					
Resolution		16		Bits	
Voltage Output Span	0.62		5	V	V_{REF} = 5 V
Differential Nonlinearity[1]	−2		+2	LSB	
DGS DAC					
Resolution		16		Bits	
Voltage Output Span	0		5	V	V_{REF} = 5 V
Differential Nonlinearity[1]	−2		+2	LSB	
Comparator DAC Dynamic					
Output Voltage Settling Time[1]		3.5	6	µs	1 V change to 1 LSB
Slew Rate[1]		1		V/µs	
Digital-to-Analog Glitch Energy[1]		10		nV-s	
Glitch Impulse Peak Amplitude[1]		40		mV	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUT					
VREF DC Input Impedance	1			MΩ	Typically 100 MΩ
VREF Input Current	−10		+10	μA	Per input; typically ±30 nA
VREF Range[1]	2		5	V	
COMPARATOR					Measured directly at comparator; does not include measure block errors
Error	−7		+7	mV	Uncalibrated
VOLTAGE COMPARATOR					With respect to the measured voltage
Propagation Delay[1]		0.25		μs	
Error[1]	−12		+12	mV	Uncalibrated
CURRENT COMPARATOR					
Propagation Delay[1]		0.25	1	μs	
Error[1]	−1.5		+1.5	%	Of programmed current range, uncalibrated
MEASURE OUTPUT, MEASOUT					
Measure Output Voltage Span[1]	−12.81		+12.81	V	MEASOUT gain = 1, V_{REF} = 5 V, offset DAC = 0x8000
Measure Output Voltage Span[1]	−6.405		+6.405	V	MEASOUT gain = 1, V_{REF} = 2.5 V
Measure Output Voltage Span[1]	0		5.125	V	MEASOUT gain = 0.2, V_{REF} = 5 V, offset DAC = 0x8000
Measure Output Voltage Span[1]	0		2.56	V	MEASOUT gain = 0.2, V_{REF} = 2.5 V
Measure Pin Output Impedance			115	Ω	
Output Leakage Current	−100		+100	nA	When $\overline{HW\_INH}$ is low
Output Capacitance[1]		5		pF	
Short-Circuit Current[1]	−10		+10	mA	
OPEN-SENSE DETECT/CLAMP/ALARM					
Measurement Accuracy	−200		+200	mV	
Clamp Accuracy		600	900	mV	
Alarm Delay[1]		50		μs	
DUTGND					
Voltage Range[1]	−1		+1	V	
Pull-Up Current		+50	+70	μA	Pull-up for purpose of detecting open circuit on DUTGND, can be disabled
Leakage Current	−1		+1	μA	When pull-up disabled, DGS DAC = 0x3333 (1 V with V_{REF} = 5 V); if DUTGND voltage is far away from one of comparator thresholds, more leakage may be present
Trip Point Accuracy	−30		+10	mV	
Alarm Delay[1]		50		μs	
GUARD AMPLIFIER					
Voltage Range[1]	AV_{SS} + 2.25		AV_{DD} − 2.25	V	
Voltage Span[1]			25	V	
Output Offset	−10		+10	mV	
Short-Circuit Current[1]	−20		+20	mA	
Load Capacitance[1]			100	nF	
Output Impedance		100		Ω	
Alarm Delay[1]		200		μs	If it moves 100 mV away from input level
DIE TEMPERATURE SENSOR					
Accuracy[1]	−10		+10	%	Relative to a temperature change
Output Voltage at 25°C		1.54		V	
Output Scale Factor[1]		4.7		mV/°C	
Output Voltage Range[1]	1		2	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPI INTERFACE LOGIC					
Logic Inputs					
Input High Voltage, V_{IH}	1.7/2.0			V	(2.3 V to 2.7 V)/(2.7 V to 5.5 V) JEDEC-compliant input levels
Input Low Voltage, V_{IL}			0.7/0.8	V	(2.3 V to 2.7 V)/(2.7 V to 5.5 V) JEDEC-compliant input levels
Input Current, I_{INH}, I_{INL}	−1		+1	µA	
Input Capacitance, C_{IN}[1]			10	pF	
CMOS Logic Outputs					SDO, CPOL, CPOH, GPO, CPO
Output High Voltage, V_{OH}	DV_{CC} − 0.4			V	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
Tristate Leakage Current	−1		+1	µA	SDO, CPOL, CPOH, CPO
Output Capacitance[1]	10	10	10	pF	SDO, CPOL, CPOH, CPO
Open-Drain Logic Outputs					$\overline{BUSY}$, $\overline{TMPALM}$, $\overline{CLALM}$, $\overline{KELALM}$
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA, C_L = 50 pF, R_{PULLUP} = 1 kΩ
Output Capacitance[1]			10	pF	
POWER SUPPLIES					
$HCAV_{DD}1x$	4		28	V	$\lvert HCAV_{DD}x - HCAV_{SS}x \rvert$ < 33 V, $HCAV_{SS}x \geq AV_{SS}$, $HCAV_{DD}x \leq AV_{DD}$
$HCAV_{SS}1x$	−25		−5	V	
$HCAV_{DD}2x$	4		28	V	$\lvert HCAV_{DD}x - HCAV_{SS}x \rvert$ < 33 V, $HCAV_{SS}x \geq AV_{SS}$, $HCAV_{DD}x \leq AV_{DD}$
$HCAV_{SS}2x$	−25		−5	V	
AV_{DD}	8		28	V	$\lvert AV_{DD} - AV_{SS} \rvert$ < 33 V
AV_{SS}	−25		−5	V	
DV_{CC}	2.3		5.5	V	
AI_{DD}[4]			30	mA	All ranges
AI_{SS}[4]	−30			mA	All ranges
DI_{CC}			3	mA	
AI_{DD}[4]			27	mA	Channel inhibited/tristate, $\overline{HW\_INH}$ or $\overline{SW\text{-}INH}$ low
AI_{SS}[4]	−27			mA	Channel inhibited/tristate, $\overline{HW\_INH}$ or $\overline{SW\text{-}INH}$ low
					$HCAV_{DD}x$ and $HCAV_{SS}x$ supply currents shown are excluding load currents; however, for power budget calculations, the supply currents here are consumed by the load
$HCAI_{DD}1$			20	mA	When enabled, excluding load conditions
$HCAI_{DD}1$			0.5	mA	When disabled
$HCAI_{SS}1$	−20			mA	When enabled, excluding load condition
$HCAI_{SS}1$	−0.5			mA	When disabled
$HCAI_{DD}2$			15	mA	When enabled, excluding load conditions
$HCAI_{DD}2$			0.25	mA	When disabled
$HCAI_{SS}2$	−15			mA	When enabled, excluding load conditions
$HCAI_{SS}2$	−0.25			mA	When disabled
POWER-DOWN CURRENTS					Supply currents on power-up or during a power-down condition
$HCAI_{DD}$			250	µA	
$HCAI_{SS}$	−250			µA	
$HCAI_{DD}$			250	µA	
$HCAI_{SS}$	−250			µA	
AI_{DD}			5	mA	
AI_{SS}	−5			mA	
DI_{CC}			3	mA	
Maximum Power Dissipation					
EXTFORCE1			10	W	
EXTFORCE2			5	W	
Power-Up Overshoot[1]			5	%	Of programmed value

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Power Supply Sensitivity[1]					DC to 1 kHz
ΔForced Voltage/ΔAV_{DD}		−65		dB	−30 dB at 100 kHz
ΔForced Voltage/ΔAV_{SS}		−65		dB	−25 dB at 100 kHz
ΔForced Voltage/$\Delta HCAV_{DD}x$		−90		dB	−60 dB at 100 kHz
ΔForced Voltage/$\Delta HCAV_{SS}x$		−90		dB	−62 dB at 100 kHz
ΔMeasured Current/ΔAV_{DD}		−50		dB	−25 dB at 100 kHz
ΔMeasured Current/ΔAV_{SS}		−43		dB	−20 dB at 100 kHz
ΔMeasured Current/$\Delta HCAV_{DD}x$		−90		dB	−60 dB at 100 kHz
ΔMeasured Current/$\Delta HCAV_{SS}x$		−90		dB	−60 dB at 100 kHz
ΔMeasured Voltage/ΔAV_{DD}		−65		dB	−30 dB at 100 kHz
ΔMeasured Voltage/ΔAV_{SS}		−65		dB	−25 dB at 100 kHz
ΔMeasured Voltage/$\Delta HCAV_{DD}x$		−90		dB	−60 dB at 100 kHz
ΔMeasured Voltage/$\Delta HCAV_{SS}x$		−90		dB	−65 dB at 100 kHz
ΔForced Voltage/ΔDV_{CC}		−80		dB	−46 dB at 100 kHz
ΔMeasured Current/ΔDV_{CC}		−80		dB	−36 dB at 100 kHz
ΔMeasured Voltage/ΔDV_{CC}		−80		dB	−46 dB at 100 kHz

[1] Guaranteed by design and characterization, not subject to production test.
[2] Programmable clamps must be enabled if taking advantage of reduced headroom/footroom.
[3] Clamps disabled.
[4] Not including internal pull-up current between AVDD/AVSS and HCAVDDx/HCAVSSx pins.

TIMING CHARACTERISTICS

$HCAV_{DD}x \le AV_{SS} + 33$ V, $HCAV_{SS}x \ge AV_{SS}$, $AV_{DD} \ge 8$ V, $AV_{SS} \le -5$ V, $|AV_{DD} - AV_{SS}| \ge 16$ V and ≤ 33 V, $V_{REF} = 5$ V (T_J = 25°C to 90°C, maximum specifications, unless otherwise noted).

Table 2. SPI Interface

Parameter[1, 2, 3]	DV_{CC} = 2.3 V to 2.7 V	DV_{CC} = 2.7 V to 3.3 V	DV_{CC} = 4.5 V to 5.5 V	Unit	Description
t_{UPDATE}	600	600	600	ns max	Channel update cycle time
t_1	25	20	20	ns min	SCLK cycle time; 60/40 duty cycle
t_2	10	8	8	ns min	SCLK high time
t_3	10	8	8	ns min	SCLK low time
t_4	10	10	10	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	15	15	15	ns min	Minimum $\overline{SYNC}$ high time
t_6	5	5	5	ns min	24th SCLK falling edge to $\overline{SYNC}$ rising edge
t_7	5	5	5	ns min	Data setup time
t_8	4.5	4.5	4.5	ns min	Data hold time
t_9[4]	40	35	30	ns max	$\overline{SYNC}$ rising edge to $\overline{BUSY}$ falling edge
t_{10}	1.5	1.5	1.5	µs max	$\overline{BUSY}$ pulse width low for DAC x1 write
	280	280	280	ns max	$\overline{BUSY}$ pulse width low for other register write
t_{11}	25	20	10	ns min	$\overline{RESET}$ pulse width low
t_{12}	400	400	400	µs max	$\overline{RESET}$ time indicated by $\overline{BUSY}$ low
t_{13}	250	250	250	ns min	Minimum $\overline{SYNC}$ high time in readback mode
t_{14}[5, 6]	45	35	25	ns max	SCLK rising edge to SDO valid
t_{15}	30	30	30	ns max	$\overline{SYNC}$ rising edge to SDO high-Z
$\overline{LOAD}$ TIMING					
t_{16}	20	20	20	ns min	$\overline{LOAD}$ pulse width low
t_{17}	150	150	150	ns min	$\overline{BUSY}$ rising edge to force output response time
t_{18}	0	0	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LOAD}$ falling edge
t_{19}	150	150	150	ns min	$\overline{LOAD}$ rising edge to FORCE output response time
	150	150	150	ns min	$\overline{LOAD}$ rising edge to current range response

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 4 and Figure 5.
[4] This is measured with the load circuit shown in Figure 2.
[5] This is measured with the load circuit shown in Figure 3.
[6] Longer SCLK cycle time is required for correct operation of readback mode; consult timing diagrams and timing specifications.

TIMING DIAGRAMS

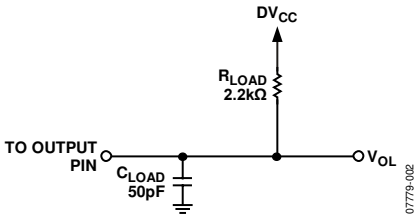

Figure 2. Load Circuit for Open Drain

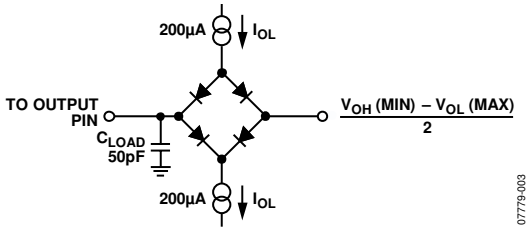

Figure 3. Load Circuit for CMOS

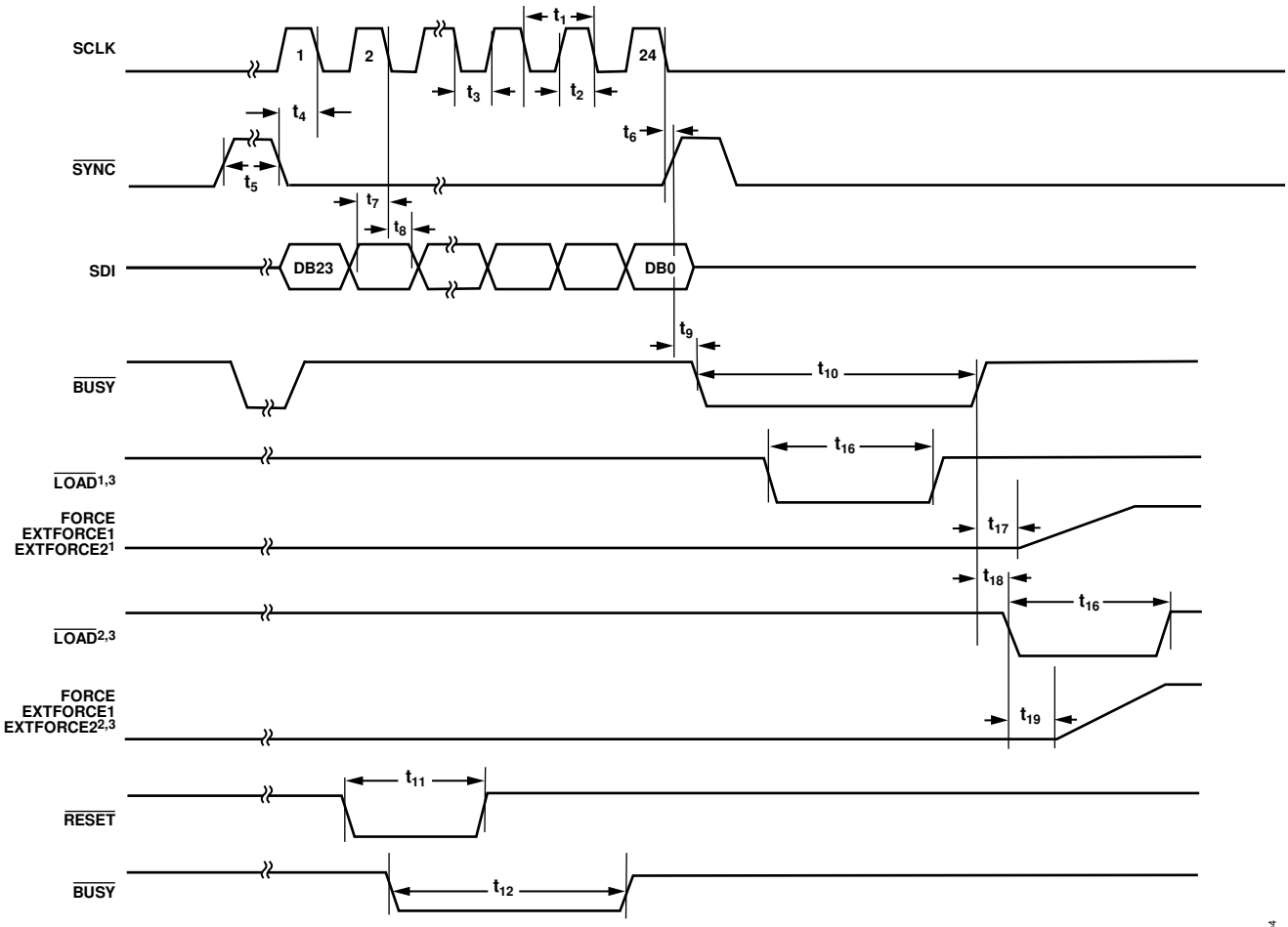

Figure 4. SPI Write Timing

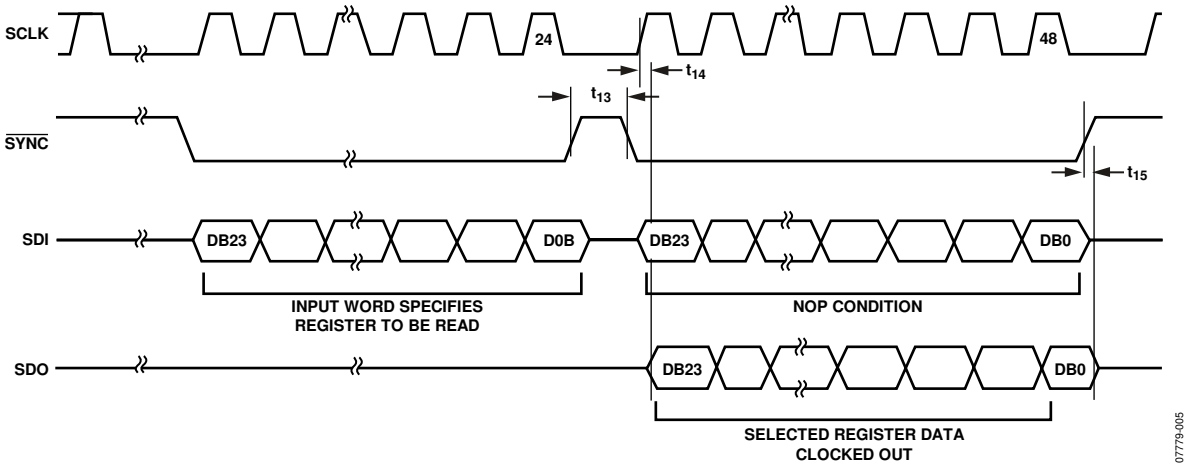

Figure 5. SPI Read Timing

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
AV_{DD} to AV_{SS}	34 V
AV_{DD} to AGND	−0.3 V to +34 V
AV_{SS} to AGND	−34 V to +0.3 V
$HCAV_{DD}x$ to $HCAV_{SS}x$	34 V
$HCAV_{DD}x$ to AGND	−0.3 V to +34 V
$HCAV_{SS}x$ to AGND	−34 V to +0.3 V
$HCAV_{DD}x$ to AV_{SS}	−0.3 V to AV_{SS} + 34 V
$HCAV_{DD}x$ to AV_{DD}	−0.3 V to AV_{DD} + 0.3 V
$HCAV_{SS}x$ to AV_{SS}	+0.3 V to AV_{SS} − 0.3 V
DV_{CC} to DGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
REFGND to AGND	−0.3 V to +0.3 V
Digital Inputs to DGND	−0.3 V to DV_{CC} + 0.3 V
Analog Inputs to AGND	AV_{SS} − 0.3 V to AV_{DD} + 0.3 V
EXTFORCE1 and EXTFORCE2 to AGND[1]	AV_{DD} − 28 V
Storage Temperature	−65°C to +125°C
Operating Junction Temperature	25°C to 90°C
Reflow Profile	J-STD 20 (JEDEC)
Junction Temperature	150°C max
Power Dissipation	10 W max (EXTFORCE1 stage)
	5 W max (EXTFORCE2 stage)
ESD	
HBM	1500 V
FICDM	500 V

[1] When an EXTFORCE1 or EXTFORCE2 stage is enabled and the supply differential $|AV_{DD} - AV_{SS}| > 28$ V, take care to ensure that these pins are not directly shorted to AV_{SS} voltage at any time because this can cause damage to the device.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

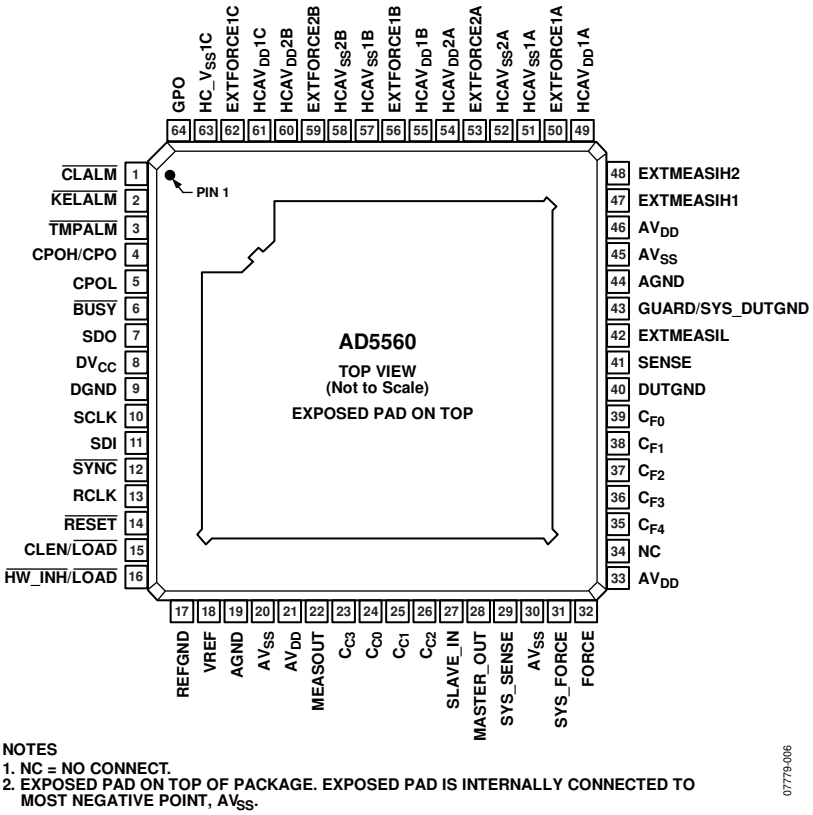

Figure 6. TQFP_EP Pin Configuration

Table 4. TQFP_EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{CLALM}}$	Clamp Alarm Output. Open-drain output, active low; this pin can be programmed to be either latched or unlatched.
2	$\overline{\text{KELALM}}$	Kelvin Alarm Pin for SENSE and DUTGND, Open-Drain Active Low. This pin can be programmed to be either latched or unlatched.
3	$\overline{\text{TMPALM}}$	Temperature Alarm Flag. Open-drain output, active low; this pin can be programmed to be either latched or unlatched.
4	CPOH/CPO	Comparator High Output (CPOH) or Window Comparator Output (CPO).
5	CPOL	Comparator Low Output.
6	$\overline{\text{BUSY}}$	Open-Drain Active Low Output. This pin indicates the status of the calibration engine for the DAC channels.
7	SDO	Serial Data Output. This pin is used for reading back DAC and DPS register information for diagnostic purposes.
8	DV_{CC}	Digital Supply Voltage.
9	DGND	Digital Ground Reference Point.
10	SCLK	Clock Input, Active Falling Edge.
11	SDI	Serial Data Input.
12	$\overline{\text{SYNC}}$	Frame Sync, Active Low.
13	RCLK	Ramp Clock Logic Input. If the ramp function is used, a clock signal of 833 kHz maximum should be applied to this input to drive the ramp circuitry. Tie RCLK low if it is unused.
14	$\overline{\text{RESET}}$	Logic Input. This pin is used to reset all internal nodes on the device to their power-on reset value.
15	CLEN/$\overline{\text{LOAD}}$	Clamp Enable. This input allows the user to enable or disable the clamp circuitry. This pin can be configured as a $\overline{\text{LOAD}}$ function to allow synchronization of multiple devices. Either CLEN or $\overline{\text{HW\_INH}}$ can be chosen as $\overline{\text{LOAD}}$ input (see the system control register, Address 0x1).
16	$\overline{\text{HW\_INH}}$/$\overline{\text{LOAD}}$	Hardware Inhibit Input to Disable Force Amplifier. This pin can be configured as a $\overline{\text{LOAD}}$ function to allow synchronization of multiple devices. Either CLEN or $\overline{\text{HW\_INH}}$ can be chosen as a $\overline{\text{LOAD}}$ input (see the system control register, Address 0x1).
17	REFGND	Accurate Ground Reference for Applied Voltage Reference.

Pin No.	Mnemonic	Description
18	VREF	Reference Input for DAC Channels, Input Range 2 V to 5 V.
19, 44	AGND	Analog Ground.
20, 30, 45	AV_{SS}	Negative Analog Supply Voltage. These pins supply DACs and other high voltage circuitry, such as measure blocks.
21, 33, 46	AV_{DD}	Positive Analog Supply Voltage. These pins supply DACs and other high voltage circuitry, such as measure blocks.
22	MEASOUT	Multiplexed DUT voltage sense, DUT current sense, Kelvin sense, or temperature output; refer to AGND.
23	C_{C3}	Compensation Capacitor Input 3.
24	C_{C0}	Compensation Capacitor Input 0.
25	C_{C1}	Compensation Capacitor Input 1.
26	C_{C2}	Compensation Capacitor Input 2.
27	SLAVE_IN	Slave Input When Ganging Multiple DPS Devices.
28	MASTER_OUT	Master Output When Ganging Multiple DPS Devices.
29	SYS_SENSE	External Sense Signal Output.
31	SYS_FORCE	External Force Signal Input.
32	FORCE	Output Force Pin for Internal Current Ranges.
34	NC	No Connect.
35	C_{F4}	Feedforward Capacitor 4.
36	C_{F3}	Feedforward Capacitor 3.
37	C_{F2}	Feedforward Capacitor 2.
38	C_{F1}	Feedforward Capacitor 1.
39	C_{F0}	Feedforward Capacitor 0.
40	DUTGND	Device Under Test Ground.
41	SENSE	Input Sense Line.
42	EXTMEASIL	Low Side Measure Current Line for External High Current Ranges.
43	GUARD/SYS_DUTGND	Guard Amplifier Output Pin or System Device Under Test Ground Pin. See the DPS Register 2 in Table 19 for addressing details.
47	EXTMEASIH1	Input High Measure Line for External High Current Range 1.
48	EXTMEASIH2	Input High Measure Line for External High Current Range 2.
49, 55, 61	$HCAV_{DD}1A$, $HCAV_{DD}1B$, $HCAV_{DD}1C$	High Current Positive Analog Supply Voltage, for EXTFORCE1 Range.
50, 56, 62	EXTFORCE1A, EXTFORCE1B, EXTFORCE1C	Output Force. This pin is used for high Current Range 1, up to a maximum of ±1.2 A.
51, 57, 63	$HCAV_{SS}1A$, $HCAV_{SS}1B$, $HCAV_{SS}1C$	High Current Negative Analog Supply Voltage, for EXTFORCE1 Range.
52, 58	$HCAV_{SS}2A$, $HCAV_{SS}2B$	High Current Negative Analog Supply Voltage, for EXTFORCE2 Range.
53, 59	EXTFORCE2A, EXTFORCE2B	Output Force. This pin is used for high Current Range 2, up to a maximum of ±500 mA.
54, 60	$HCAV_{DD}2A$, $HCAV_{DD}2B$	High Current Positive Analog Supply Voltage, for EXTFORCE2 Range.
64	GPO	Extra Logic Output Bit. Ideal for external functions such as switching out a decoupling capacitor at DUT.
65	EP	The exposed pad is internally connected to AV_{SS}.

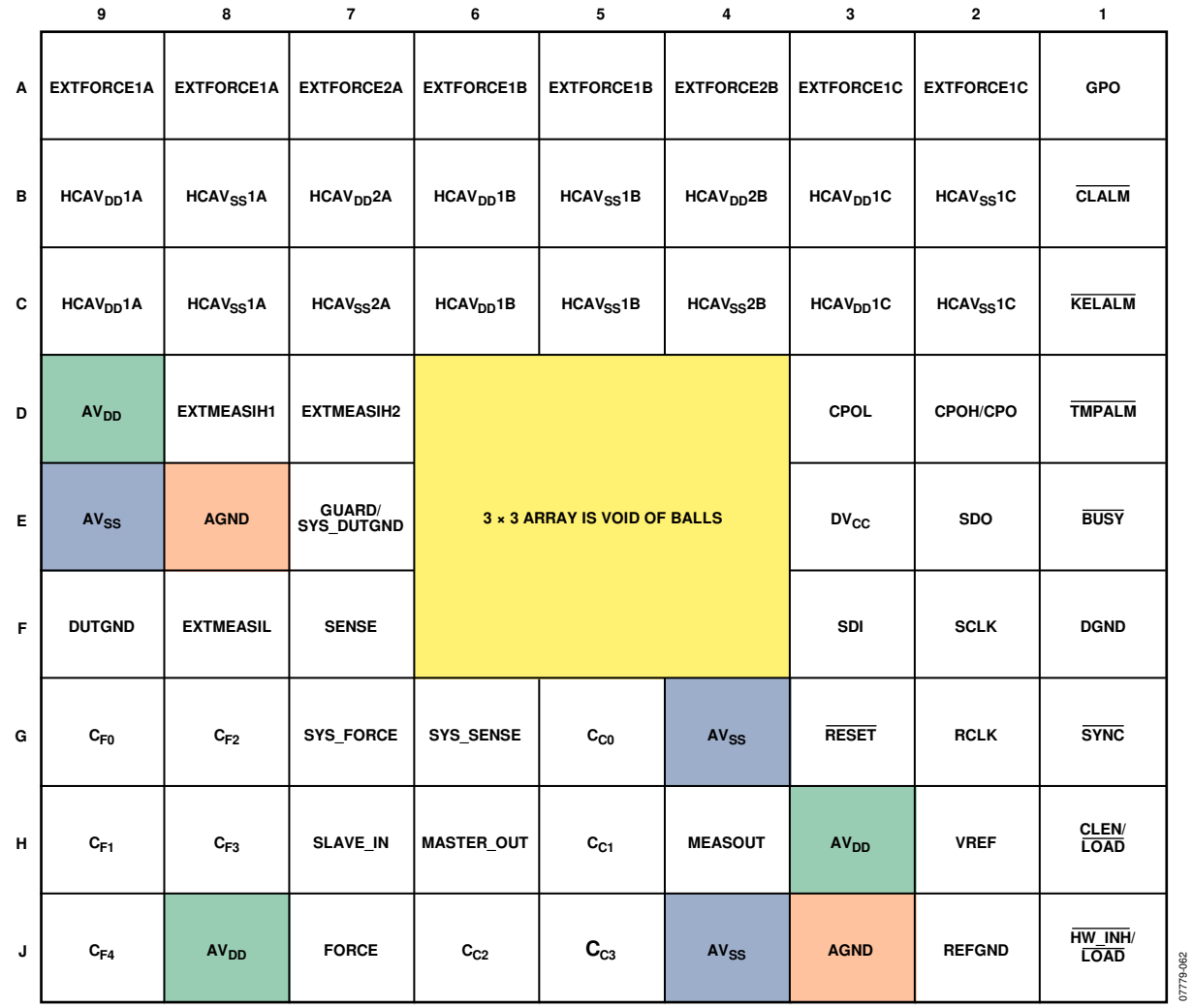

Figure 7. Flip-Chip BGA Pin Configuration, Bottom Side (BGA Balls Are Visible)

Table 5. Flip-Chip BGA Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	GPO	Extra Logic Output Bit. Ideal for external functions such as switching out a decoupling capacitor at DUT.
A2, A3	EXTFORCE1C	Output Force. These pins are used for high Current Range 1, up to a maximum of ±1.2 A.
A4	EXTFORCE2B	Output Force. This pin is used for high Current Range 2, up to a maximum of ±500 mA.
A5, A6	EXTFORCE1B	Output Force. These pins are used for high Current Range 1, up to a maximum of ±1.2 A.
A7	EXTFORCE2A	Output Force. This pin is used for high Current Range 2, up to a maximum of ±500 mA.
A8, A9	EXTFORCE1A	Output Force. These pins are used for high Current Range 1, up to a maximum of ±1.2 A.
B1	$\overline{\text{CLALM}}$	Clamp Alarm Output. Open-drain output, active low; this pin can be programmed to be either latched or unlatched.
B2, C2	$HCAV_{SS}1C$	High Current Negative Analog Supply Voltage for EXTFORCE1 Range.
B3, C3	$HCAV_{DD}1C$	High Current Positive Analog Supply Voltage for EXTFORCE1 Range.
B4	$HCAV_{DD}2B$	High Current Positive Analog Supply Voltage for EXTFORCE2 Range.
B5, C5	$HCAV_{SS}1B$	High Current Negative Analog Supply Voltage for EXTFORCE1 Range.
B6, C6	$HCAV_{DD}1B$	High Current Positive Analog Supply Voltage for EXTFORCE1 Range.
B7	$HCAV_{DD}2A$	High Current Positive Analog Supply Voltage for EXTFORCE2 Range.
B8, C8	$HCAV_{SS}1A$	High Current Negative Analog Supply Voltage for EXTFORCE1 Range.
B9, C9	$HCAV_{DD}1A$	High Current Positive Analog Supply Voltage for EXTFORCE1 Range.
C1	$\overline{\text{KELALM}}$	Kelvin Alarm Pin for SENSE and DUTGND, Open-Drain Active Low. This pin can be programmed to be either latched or unlatched.
C4	$HCAV_{SS}2B$	High Current Negative Analog Supply Voltage for EXTFORCE2 Range.
C7	$HCAV_{SS}2A$	High Current Negative Analog Supply Voltage for EXTFORCE2 Range.

Pin No.	Mnemonic	Description
D1	$\overline{\text{TMPALM}}$	Temperature Alarm Flag. Open-drain output, active low; this pin can be programmed to be either latched or unlatched.
D2	CPOH/CPO	Comparator High Output (CPOH) or Window Comparator Output (CPO).
D3	CPOL	Comparator Low Output.
D7	EXTMEASIH2	Input High Measure Line for External High Current Range 2.
D8	EXTMEASIH1	Input High Measure Line for External High Current Range 1.
D9,H3, J8	AV_{DD}	Positive Analog Supply Voltage. These pins supply DACs and other high voltage circuitry, such as measure blocks.
E1	$\overline{\text{BUSY}}$	Open-Drain Active Low Output. This pin indicates the status of the calibration engine for the DAC channels.
E2	SDO	Serial Data Output. This pin is used for reading back DAC and DPS register information for diagnostic purposes.
E3	DV_{CC}	Digital Supply Voltage.
E7	GUARD/SYS_DUTGND	Guard Amplifier Output Pin or System Device Under Test Ground Pin. See the DPS Register 2 in Table 19 for addressing details.
E8	AGND	Analog Ground.
E9, G4, J4	AV_{SS}	Negative Analog Supply Voltage. These pins supply DACs and other high voltage circuitry, such as measure blocks.
F1	DGND	Digital Ground Reference Point.
F2	SCLK	Clock Input, Active Falling Edge.
F3	SDI	Serial Data Input.
F7	SENSE	Input Sense Line.
F8	EXTMEASIL	Low Side Measure Current Line for External High Current Ranges.
F9	DUTGND	Device Under Test Ground.
G1	$\overline{\text{SYNC}}$	Frame Sync, Active Low.
G2	RCLK	Ramp Clock Logic Input. If the ramp function is used, a clock signal of 833 kHz maximum should be applied to this input to drive the ramp circuitry. Tie RCLK low if it is unused.
G3	$\overline{\text{RESET}}$	Logic Input. This pin is used to reset all internal nodes on the device to their power-on reset value.
G5	C_{C0}	Compensation Capacitor Input 0.
G6	SYS_SENSE	External Sense Signal Output.
G7	SYS_FORCE	External Force Signal Input.
G8	C_{F2}	Feedforward Capacitor 2.
G9	C_{F0}	Feedforward Capacitor 0.
H1	CLEN/$\overline{\text{LOAD}}$	Clamp Enable. This input allows the user to enable or disable the clamp circuitry. This pin can be configured as a $\overline{\text{LOAD}}$ function to allow synchronization of multiple devices. Either CLEN or $\overline{\text{HW\_INH}}$ can be chosen as $\overline{\text{LOAD}}$ input (see the system control register, Address 0x1).
H2	VREF	Reference Input for DAC Channels, Input Range is 2 V to 5 V.
H4	MEASOUT	Multiplexed DUT voltage sense, DUT current sense, Kelvin sense, or temperature output; refer to AGND.
H5	C_{C1}	Compensation Capacitor Input 1.
H6	MASTER_OUT	Master Output When Ganging Multiple DPS Devices.
H7	SLAVE_IN	Slave Input When Ganging Multiple DPS Devices.
H8	C_{F3}	Feedforward Capacitor 3.
H9	C_{F1}	Feedforward Capacitor 1.
J1	$\overline{\text{HW\_INH}}$/$\overline{\text{LOAD}}$	Hardware Inhibit Input to Disable Force Amplifier. This pin can be configured as a $\overline{\text{LOAD}}$ function to allow synchronization of multiple devices. Either CLEN or $\overline{\text{HW\_INH}}$ can be chosen as a $\overline{\text{LOAD}}$ input (see the system control register, Address 0x1).
J2	REFGND	Accurate Ground Reference for Applied Voltage Reference.
J3	AGND	Analog Ground.
J5	C_{C3}	Compensation Capacitor Input 3.
J6	C_{C2}	Compensation Capacitor Input 2.
J7	FORCE	Output Force Pin for Internal Current Ranges.
J9	C_{F4}	Feedforward Capacitor 4.

TYPICAL PERFORMANCE CHARACTERISTICS

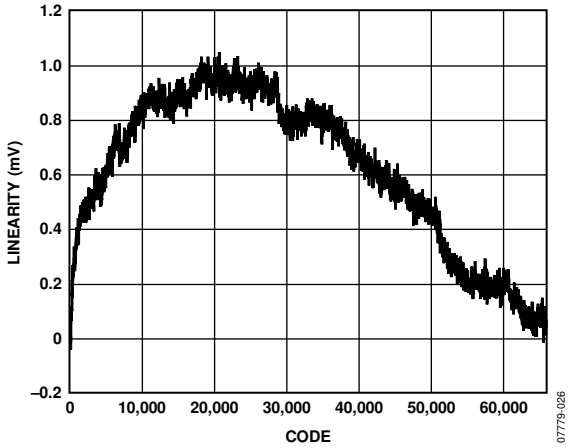

Figure 8. Force Voltage Linearity vs. Code, V_{REF} = 5 V, No Load

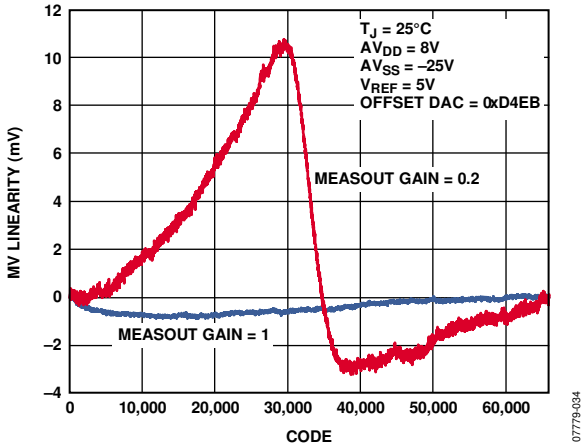

Figure 11. Measure Voltage Linearity vs. Code (MEASOUT Gain 1, MEASOUT Gain = 0.2, Negative Skew Supply)

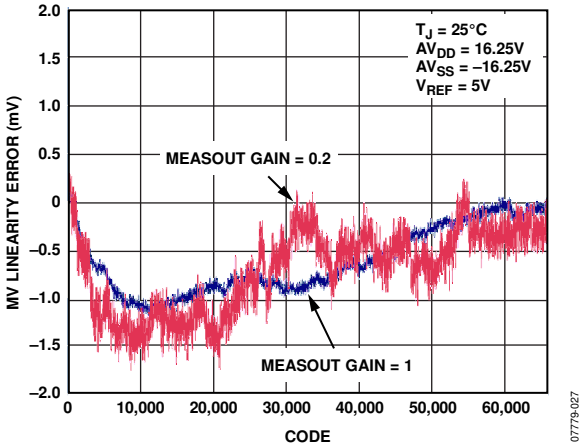

Figure 9. Measure Voltage Linearity vs. Code (MEASOUT Gain = 1, MEASOUT Gain = 0.2, Nominal Supplies)

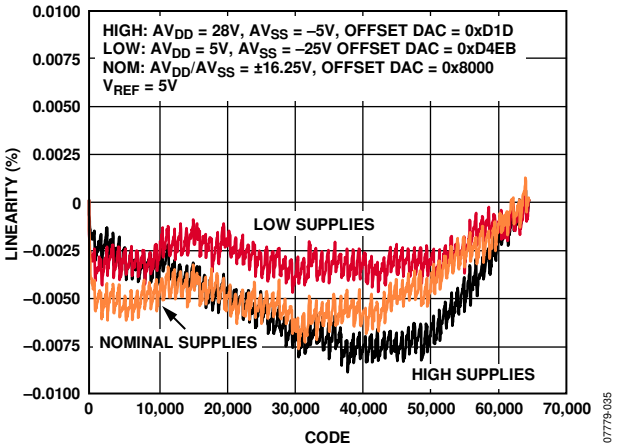

Figure 12. Measure Current Linearity vs. Code (MEASOUT Gain = 1, MI Gain = 20), T_J = 25°C

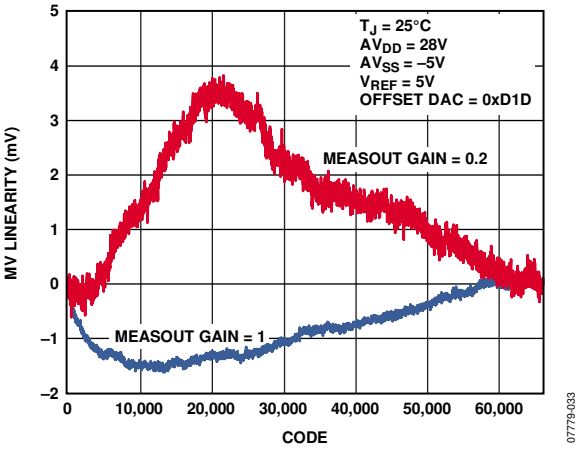

Figure 10. Measure Voltage Linearity vs. Code (MEASOUT Gain = 1, MEASOUT Gain = 0.2, Positive Skew Supply)

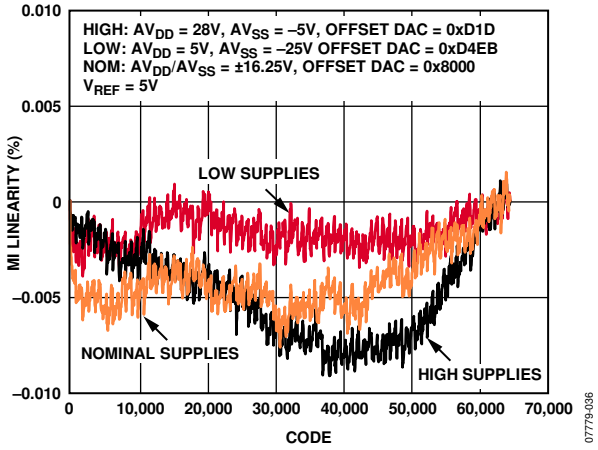

Figure 13. Measure Current Linearity vs. Code (MEASOUT Gain = 1, MI Gain = 10)

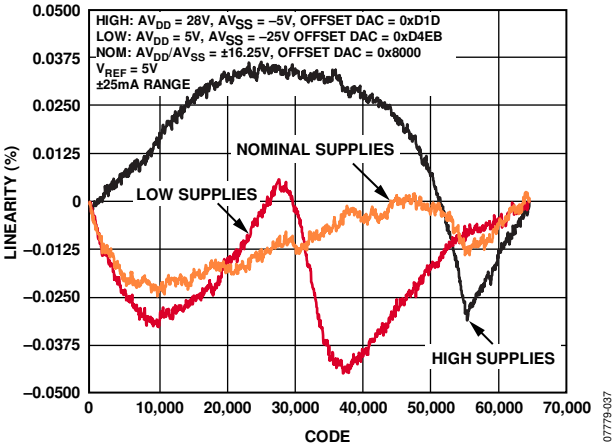

Figure 14. Measure Current Linearity vs. Code (MEASOUT Gain = 0.2, MI Gain = 20)

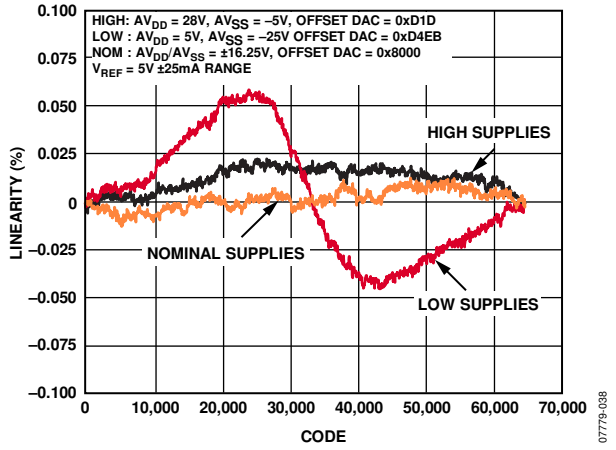

Figure 15. Measure Current Linearity vs. Code (MEASOUT Gain = 0.2, MI Gain = 10)

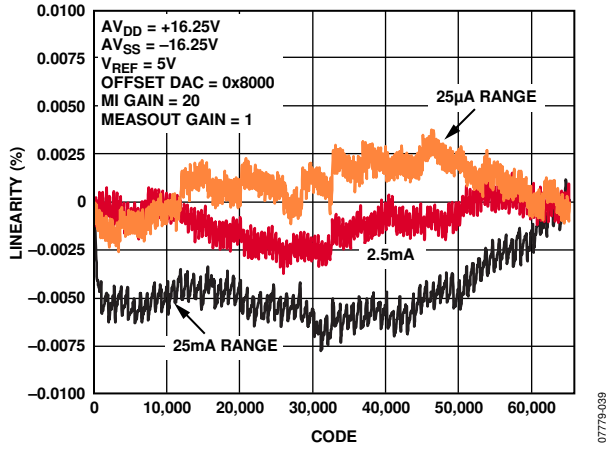

Figure 16. Measure Current Linearity vs. I_{RANGE} (MEASOUT Gain = 1, MI Gain = 20)

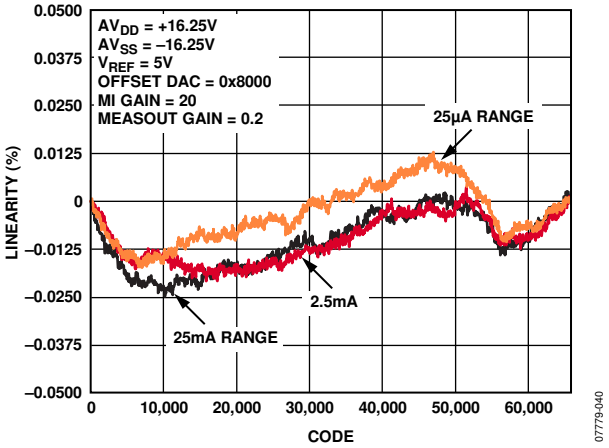

Figure 17. Measure Current Linearity vs. I_{RANGE} (MEASOUT Gain = 0.2, MI Gain = 20)

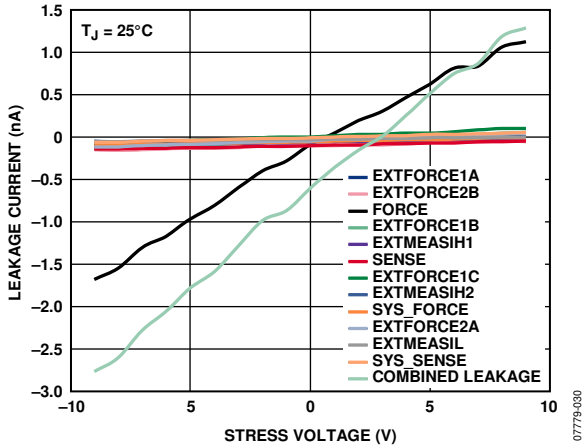

Figure 18. Leakage Current vs. Stress Voltage (Force and Combined Leakage)

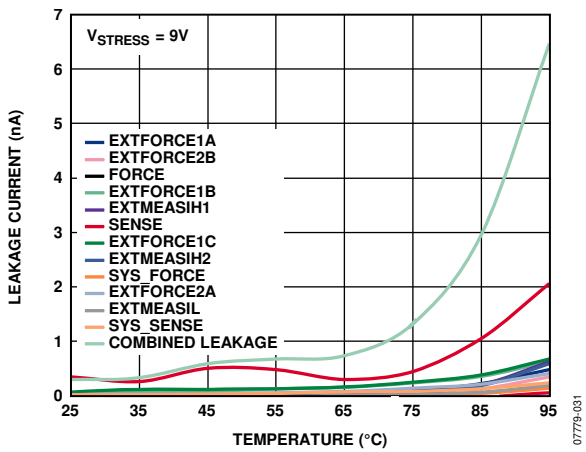

Figure 19. Leakage Current vs. Temperature (Force and Combined Leakage), V_{STRESS} = 9 V

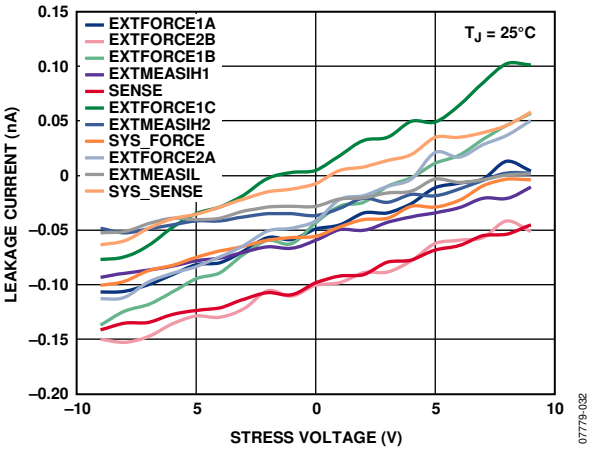

Figure 20. Leakage Current vs. Stress Voltage

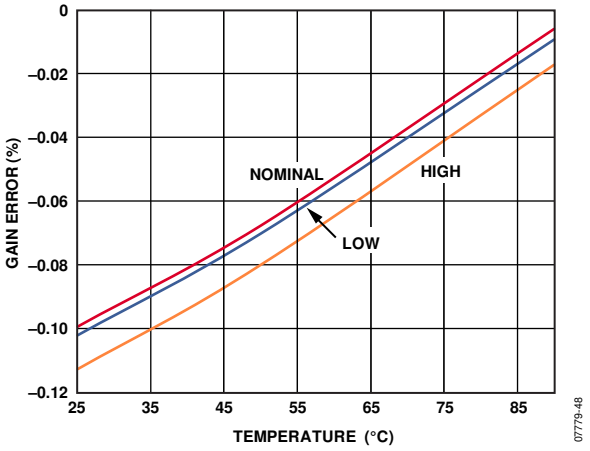

Figure 23. MI Positive Gain Error vs. Temperature, MI Gain = 20, MEASOUT Gain = 1

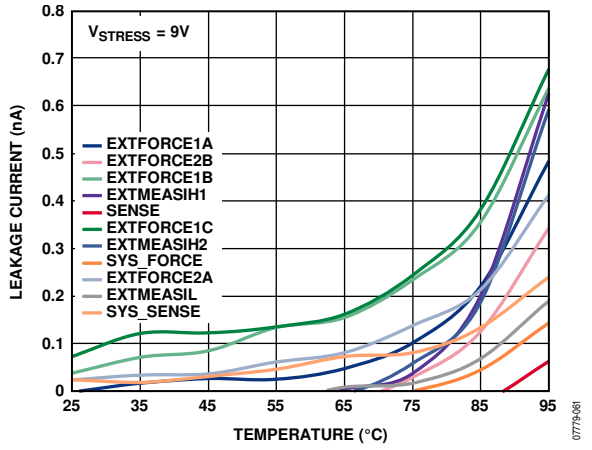

Figure 21. Leakage Current vs. Temperature, V_{STRESS} = 9 V

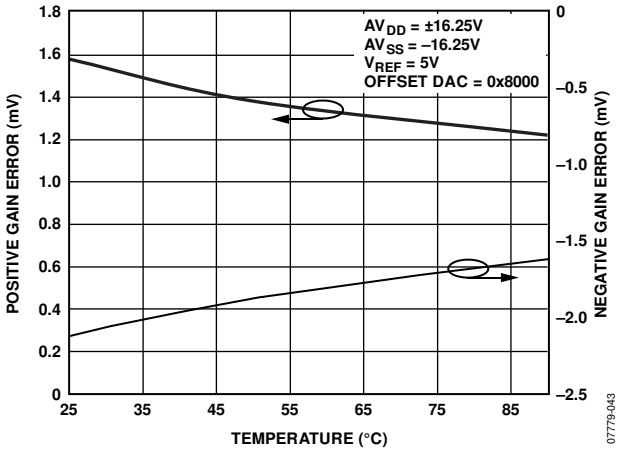

Figure 24. FV Gain Error vs. Temperature

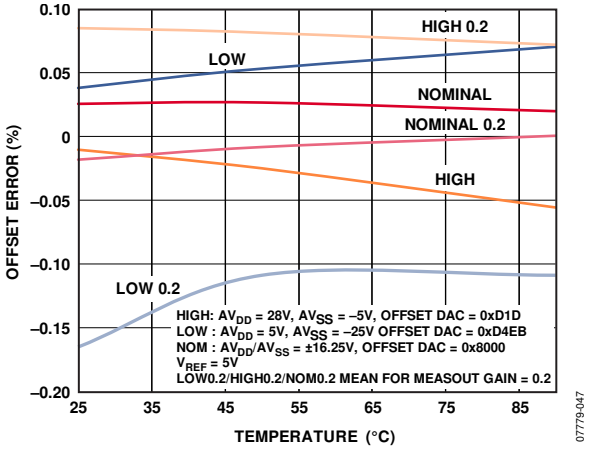

Figure 22. MI Offset Error vs. Temperature, MI Gain = 20, MEASOUT Gain = 1 and 0.2

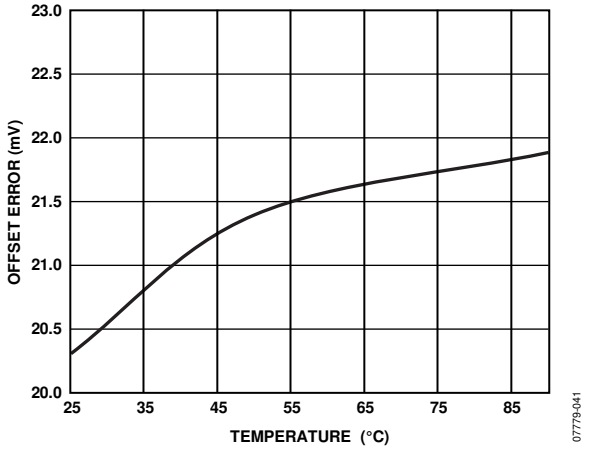

Figure 25. FV Offset Error vs. Temperature

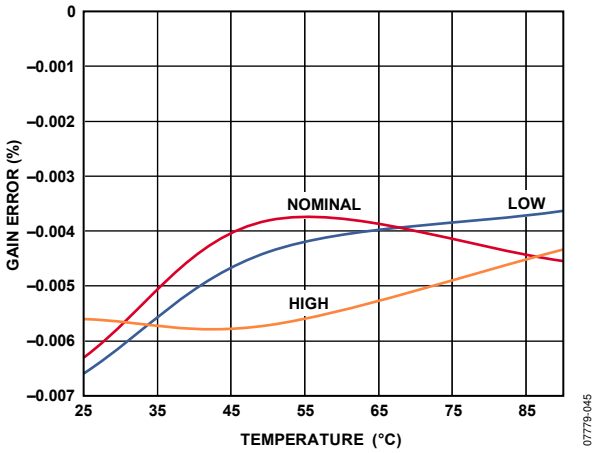

Figure 26. MV Gain Error vs. Temperature, MEASOUT Gain = 1

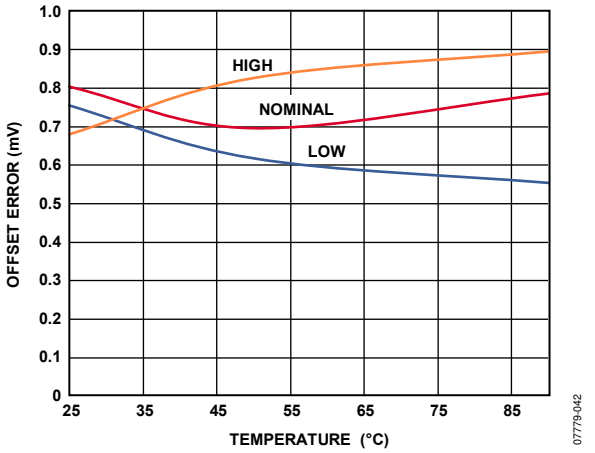

Figure 27. MV Offset Error vs. Temperature, MEASOUT Gain = 1

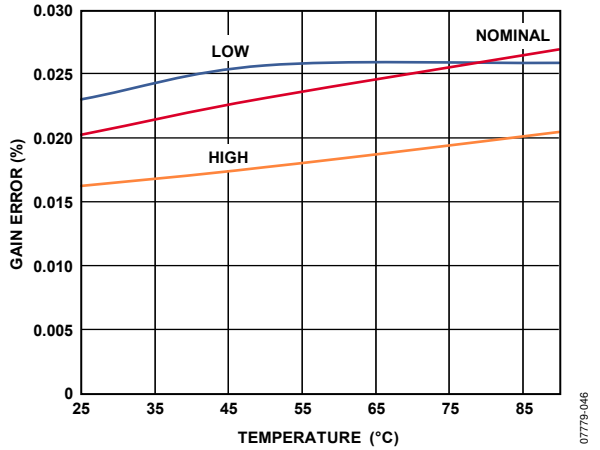

Figure 28. MV Gain Error vs. Temperature, MEASOUT Gain = 0.2

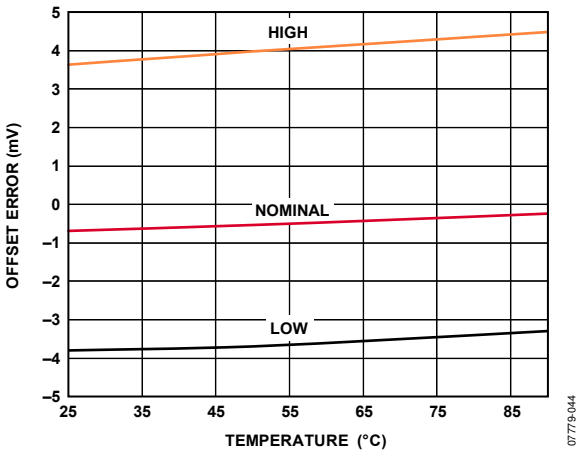

Figure 29. MV Offset Error vs. Temperature, MEASOUT Gain = 0.2

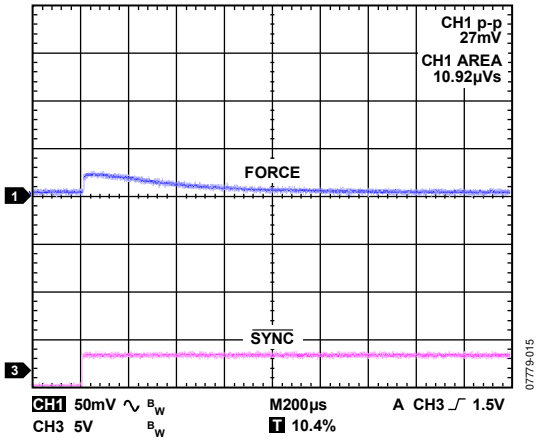

Figure 30. Range Change 2.5 mA to 25 mA, Safe Mode, 2.5 mA I_{LOAD}, 10 µF Load

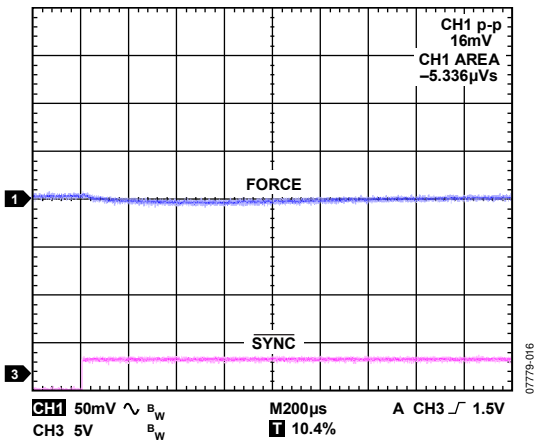

Figure 31. Range Change 25 mA to 2.5 mA, Safe Mode, 2.5 mA I_{LOAD}, 10 µF Load

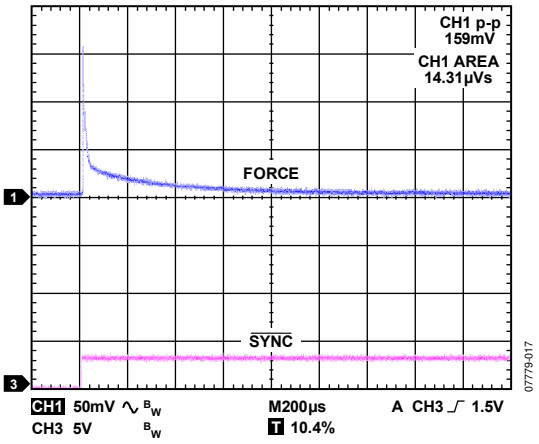

Figure 32. Range Change 25 mA to EXTFORCE2, Safe Mode, 25 mA I_{LOAD}, 10 µF Load

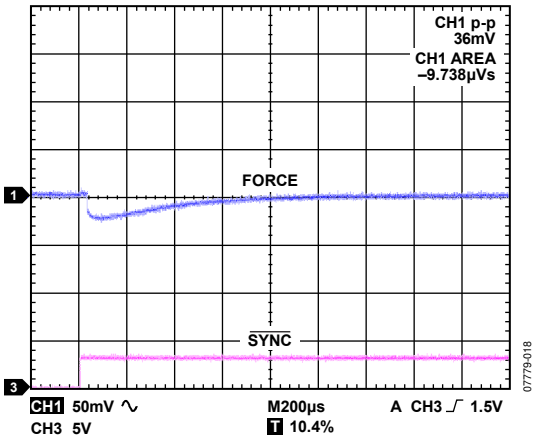

Figure 33. Range Change EXTFORCE2 to 25 mA, Safe Mode, 25 mA I_{LOAD}, 10 µF Load

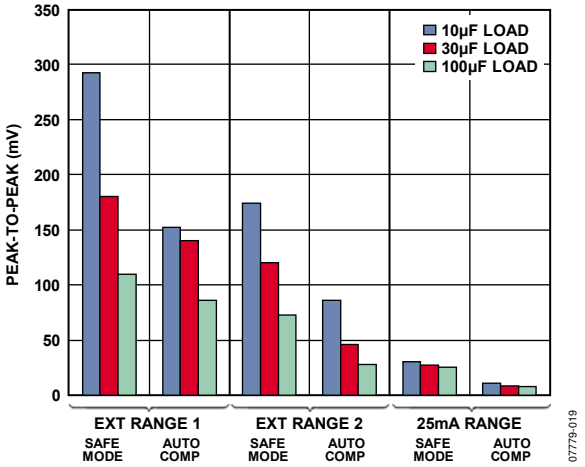

Figure 34. Kick/Droop Response vs. I_{RANGE}, Compensation, and C_{LOAD}, 10% to 90% to 10% I_{LOAD} Change

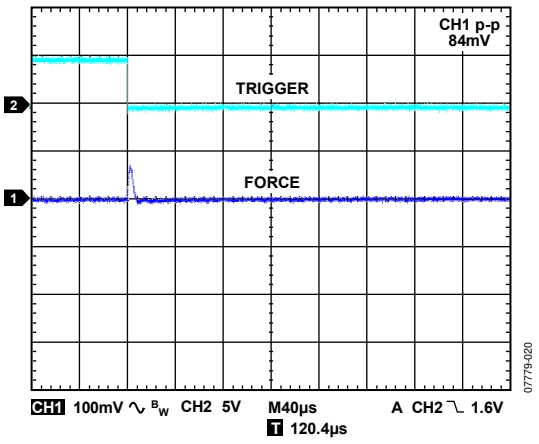

Figure 35. Autocompensation Mode 90% to 10% I_{LOAD} Change, EXTFORCE2 Range, 10 µF Load

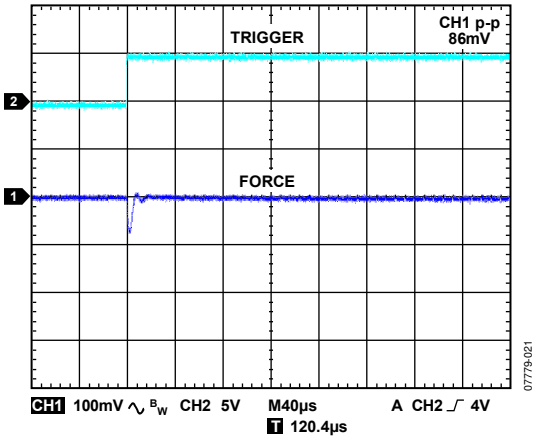

Figure 36. Autocompensation Mode 10% to 90% I_{LOAD} Change, EXTFORCE2 Range, 10 µF Load

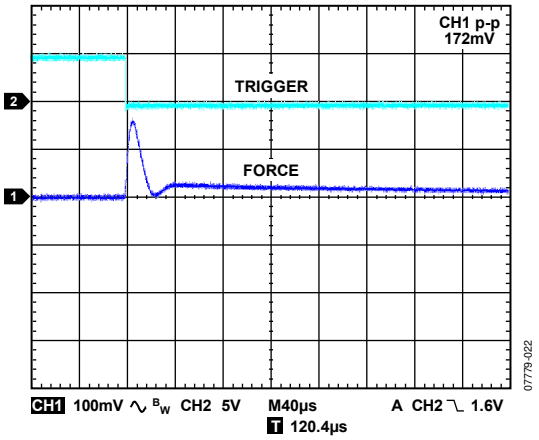

Figure 37. Safe Mode 80% to 10%, EXTFORCE2 Range, 10 µF Load