**ANALOG DEVICES**

# 16 Input, 16 Output Analog I/O Port with Integrated Amplifiers

# AD5590

## FEATURES

- **Input channels**
  - **12-bit successive approximation ADC**
  - **16 inputs with sequencer**
  - **Fast throughput rate: 1 MSPS**
  - **Wide input bandwidth: 70 dB SNR at $f_{IN}$ = 50 kHz**
- **Output channels**
  - **16 outputs with 12-bit DACs**
  - **On-chip 2.5 V reference**
  - **Hardware $\overline{\text{LDAC}}$ and $\overline{\text{LDAC}}$ override function**
  - **$\overline{\text{CLR}}$ function to programmable code**
  - **Rail-to-rail operation**
- **Operational amplifiers**
- **Offset voltage: 2.2 mV maximum**
- **Low input bias current: 1 pA maximum**
- **Single supply operation**
- **Low noise: 22 nV/√Hz**
- **Unity gain stable**
- **Flexible serial interface**
  - **SPI-/QSPI-/MICROWIRE-/DSP-compatible**
- **−40°C to +85°C operation**
- **Available in 80-ball CSP_BGA package**

## APPLICATIONS

- **Optical line cards**
- **Base stations**
- **General-purpose analog I/O**
- **Monitoring and control**

## FUNCTIONAL BLOCK DIAGRAM

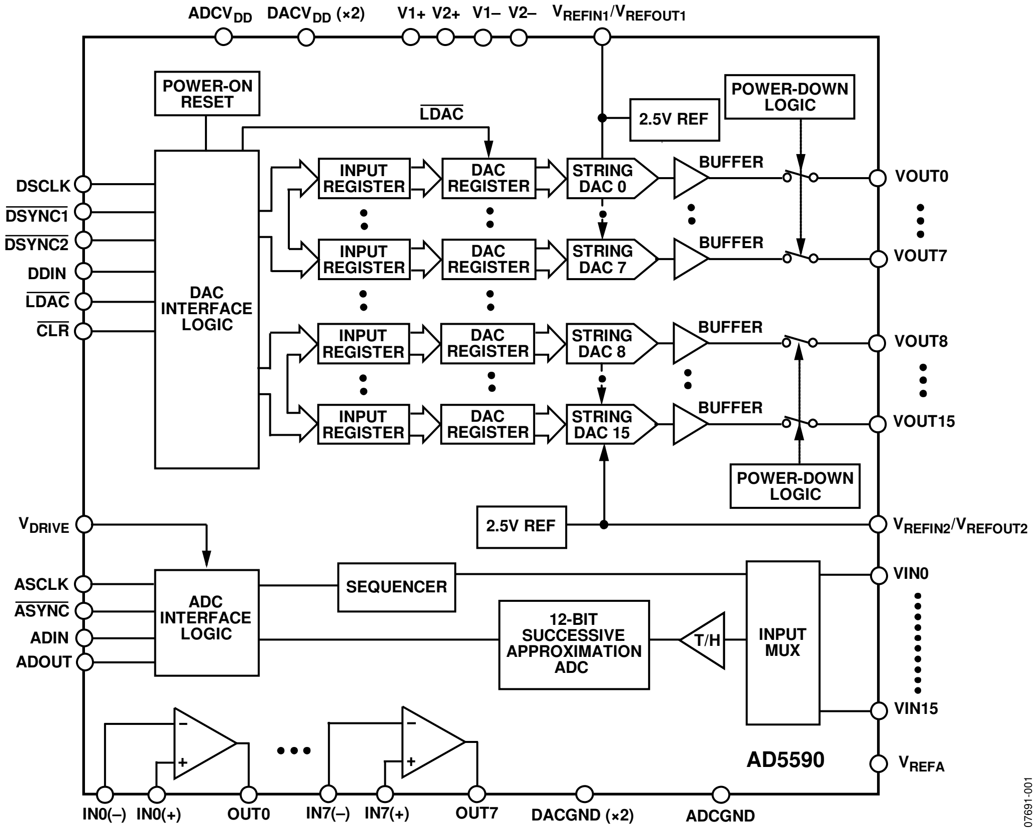

*Figure 1.*

**Rev. A**

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- AD5590 Evaluation Board

## DOCUMENTATION

**Data Sheet**

- AD5590: 16 Input, Output Analog I/O Port wth Integrated Amplifiers Data Sheet

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- AD5590 Software Evaluation

## REFERENCE MATERIALS

**Solutions Bulletins & Brochures**

- Digital to Analog Converters ICs Solutions Bulletin

**Technical Articles**

- MS-2210: Designing Power Supplies for High Speed ADC

## DESIGN RESOURCES

- AD5590 Material Declaration
- PCN-PDN Information
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# TABLE OF CONTENTS

## REVISION HISTORY

**7/11—Rev. 0 to Rev. A**

Changes to Features Section and Figure 1 ..... 1
Changes to VOUT10 Pin Number in Table 10 ..... 13

**10/08—Revision 0: Initial Version**

# GENERAL DESCRIPTION

The AD5590 is a 16-channel input and 16-channel output analog I/O port with eight uncommitted amplifiers, operating from a single 4.5 V to 5.25 V supply. The AD5590 comprises 16 input channels multiplexed into a 1 MSPS, 12-bit successive approximation ADC with a sequencer to allow a preprogrammed selection of channels to be converted sequentially. The ADC contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 1 MHz.

The conversion process and data acquisition are controlled using $\overline{\text{ASYNC}}$ and the serial clock signal, allowing the device to easily interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{\text{ASYNC}}$ and conversion is also initiated at this point. There are no pipeline delays associated with the ADC. By setting the relevant bits in the control register, the analog input range for the ADC can be selected to be a 0 V to $V_{REFA}$ input or a 0 V to 2 × $V_{REFA}$ with either straight binary or twos complement output coding. The conversion time is determined by the ASCLK frequency because it is also used as the master clock to control the conversion.

The DAC section of the AD5590 comprises sixteen 12-bit DACs divided into two groups of eight. Each group has an on-chip reference. The on-board references are off at power-up, allowing the use of external references. The internal references are enabled via a software write.

The AD5590 incorporates a power-on reset circuit that ensures that the DAC outputs power up to 0 V and remain powered up at this level until a valid write takes place. The DAC contains a power-down feature that reduces the current consumption of the device and provides software-selectable output loads while in power-down mode for any or all DAC channels. The outputs of all DACs can be updated simultaneously using the $\overline{\text{LDAC}}$ function, with the added functionality of user-selectable DAC channels to simultaneously update. There is also an asynchronous $\overline{\text{CLR}}$ that updates all DACs to a user-programmable code: zero scale, midscale, or full scale.

The AD5590 contains eight low noise, single-supply amplifiers. These amplifiers can be used for signal conditioning for the ADCs, DACs, or other independent circuitry, if required.

# SPECIFICATIONS

## ADC SPECIFICATIONS

$ADCV_{DD} = V_{DRIVE}$ = 2.7 V to 5.25 $V_{REFA}$ = 2.5 V, $f_{SCLK}$[1] = 20 MHz, $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments[2] |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | $f_{IN}$ = 50 kHz sine wave, $f_{SCLK}$ = 20 MHz |
| Signal-to-(Noise + Distortion) (SINAD)[3] | 68.5 | 70 | | dB | @ 5 V |
| | | 70.5 | | dB | @ 3 V |
| Signal-to-Noise Ratio (SNR)[3] | 69 | 70 | | dB | @ 5 V |
| | | 70.5 | | dB | @ 3 V |
| Total Harmonic Distortion (THD)[3] | −74 | −82 | | dB | @ 5 V |
| | | −82 | | dB | @ 3 V |
| Peak Harmonic or Spurious Noise (SFDR)[3] | −75 | −86 | | dB | @ 5 V |
| | | −80 | | dB | @ 3 V |
| Intermodulation Distortion (IMD)[3, 4] | | | | | fa = 40.1 kHz, fb = 41.5 kHz |
| Second-Order Terms | | −85 | | dB | |
| Third-Order Terms | | −85 | | dB | |
| Aperture Delay[4] | | 10 | | ns | |
| Aperture Jitter[4] | | 50 | | ps | |
| Channel-to-Channel Isolation[3, 4] | | −82 | | dB | $f_{IN}$ = 400 kHz |
| Full Power Bandwidth[4] | | 8.2 | | MHz | @ 3 dB |
| | | 1.6 | | MHz | @ 0.1 dB |
| DC ACCURACY[3] | | | | | |
| Resolution | | 12 | | Bits | |
| Integral Nonlinearity | −1 | | +1 | LSB | |
| Differential Nonlinearity | −1 | | +1.5 | LSB | Guaranteed no missing codes to 12 bits |
| 0 V to $V_{REFA}$ Input Range | | | | | Straight binary output coding |
| Offset Error | −10 | ±0.6 | +10 | LSB | |
| Offset Error Match | | | 3.5 | LSB | |
| Gain Error | −2 | | +2 | LSB | |
| Gain Error Match | −0.8 | | +0.8 | LSB | |
| 0 V to 2 × $V_{REFA}$ Input Range | | | | | $-V_{REFA}$ to $+V_{REFA}$ biased about $V_{REFA}$ with twos complement output coding offset |
| Positive Gain Error | −2 | | +2 | LSB | |
| Positive Gain Error Match | −0.8 | | +0.8 | LSB | |
| Zero-Code Error | −8 | ±0.6 | +8 | LSB | |
| Zero-Code Error Match | | | 2 | LSB | |
| Negative Gain Error | −1 | | +1 | LSB | |
| Negative Gain Error Match | −0.8 | | +0.8 | LSB | |
| ANALOG INPUT | | | | | |
| Input Voltage Ranges | | 0 to $V_{REFA}$ | | V | Range bit set to 1 |
| | | 0 to 2 × $V_{REFA}$ | | V | Range bit set to 0, $ADCV_{DD}/V_{DRIVE}$ = 4.75 V to 5.25 V for 0 V to 2 × $V_{REFAS}$ |
| DC Leakage Current | −1 | | +1 | µA | |
| Input Capacitance[4] | | 20 | | pF | |
| REFERENCE INPUT | | | | | |
| $V_{REFA}$ Input Voltage | | 2.5 | | V | ±1% specified performance |
| DC Leakage Current | −1 | | +1 | µA | |
| $V_{REFA}$ Input Impedance[4] | | 36 | | kΩ | $f_{SAMPLE}$ = 1 MSPS |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments[2] |
|---|---|---|---|---|---|
| LOGIC INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | $0.7 \times V_{DRIVE}$ | | | V | |
| Input Low Voltage, $V_{INL}$ | | | $0.3 \times V_{DRIVE}$ | V | |
| Input Current, $I_{IN}$ | −1 | | +1 | µA | Typically 10 nA |
| Input Capacitance, $C_{IN}$[1, 4] | | | 10 | pF | |
| LOGIC OUTPUTS | | | | | |
| Output High Voltage, $V_{OH}$ | $V_{DRIVE} - 0.2$ | | | V | $I_{SOURCE}$ = 200 µA; $V_{DD}$ = 2.7 V to 5.25 V |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = 200 µA |
| Floating State Leakage Current | | ±10 | | µA | weak/$\overline{\text{TRI}}$ bit set to 0 |
| Floating State Output Capacitance[4] | | 10 | | pF | weak/$\overline{\text{TRI}}$ bit set to 0 |
| Output Coding | | Straight (Natural) Binary | | | coding bit set to 1 |
| | | Twos Complement | | | coding bit set to 0 |
| CONVERSION RATE[4] | | | | | |
| Conversion Time | | | 800 | ns | 16 ASCLK cycles, ASCLK = 20 MHz |
| Track-and-Hold Acquisition Time[3] | | | 300 | ns | Sine wave input |
| | | | 300 | ns | Full-scale step input |
| Throughput Rate | | | 1 | MSPS | @ 5 V (see the Serial Interface section) |
| POWER REQUIREMENTS | | | | | |
| $ADCV_{DD}$ | 2.7 | | 5.25 | V | |
| $V_{DRIVE}$ | 2.7 | | 5.25 | V | |
| $I_{DRIVE}$ | | | 0.15 | µA | |
| $I_{DD}$[5] | | | | | Digital inputs = 0 V or $V_{DRIVE}$ |
| Normal Mode, Static | | 750 | | µA | $V_{DD}$ = 4.75 V to 5.25 V, ASCLK on or off |
| Normal Mode, Operational ($f_S$ = Maximum Throughput) | | | 2.5 | mA | $V_{DD}$ = 4.75 V to 5.25 V, $f_{SCLK}$ = 20 MHz |
| Autostandby Mode | | 1.55 | | mA | $f_{SAMPLE}$ = 500 kSPS |
| | | | 100 | µA | Static |
| Autoshutdown Mode | | 960 | | µA | $f_{SAMPLE}$ = 250 kSPS |
| | | | 0.5 | µA | Static |
| Full Shutdown Mode | | 0.02 | 0.5 | µA | ASCLK on or off |
| Power Dissipation | | | | | |
| Normal Mode, Operational | | | 12.5 | mW | $ADCV_{DD}$ = 5 V, $f_{SCLK}$ = 20 MHz |
| Autostandby Mode, Static | | | 500 | µW | $ADCV_{DD}$ = 5 V |
| Autoshutdown Mode, Static | | | 2.5 | µW | $ADCV_{DD}$ = 5 V |
| Full Shutdown Mode | | | 2.5 | µW | $ADCV_{DD}$ = 5 V |

[1] Specifications apply for $f_{SCLK}$ up to 20 MHz. For serial interfacing requirements, see the Timing Specifications section.
[2] Temperature range: −40°C to +85°C.
[3] See the Terminology section.
[4] Guaranteed by design and characterization. Not production tested.
[5] See the ADC Power vs. Throughput Rate section.

## DAC SPECIFICATIONS

DACV$_{DD}$ = 4.5 V to 5.25 V, R$_{L}$ = 2 kΩ to DACGND, C$_{L}$ = 200 pF to DACGND, V$_{REFIN1}$ = V$_{REFIN1}$ = DACV$_{DD}$. All specifications T$_{MIN}$ to T$_{MAX}$, unless otherwise noted.

**Table 2.**

| Parameter | Min | Typ | Max | Unit | Conditions/Comments[1] |
|---|---|---|---|---|---|
| STATIC PERFORMANCE[2] | | | | | |
| Resolution | 12 | | | Bits | |
| Integrated Nonlinearity (INL) | −3 | ±0.5 | +3 | LSB | See Figure 6 |
| Differential Nonlinearity (DNL) | −0.25 | | +0.25 | LSB | Guaranteed monotonic by design; see Figure 7 |
| Zero-Code Error | | 1 | 12 | mV | All 0s loaded to DAC register; see Figure 11 |
| Zero-Code Error Drift[3] | | ±2 | | μV/°C | |
| Full-Scale Error | −1 | −0.2 | | % FSR | All 1s loaded to DAC register |
| Gain Error | −1 | | +1 | % FSR | |
| Gain Temperature Coefficient[3] | | ±2.5 | | ppm | Of FSR/°C |
| Offset Error | −11 | ±5 | +11 | mV | |
| DC Power Supply Rejection Ratio[3] | | −80 | | dB | DACV$_{DD}$ ± 10% |
| DC Crosstalk[3] | | | | | |
| External Reference | | 10 | | μV | Due to full-scale output change, R$_{L}$ = 2 kΩ to DACGND or DACV$_{DD}$ |
| | | 5 | | μV/mA | Due to load current change |
| | | 10 | | μV | Due to powering down (per channel) |
| Internal Reference | | 25 | | μV | Due to full-scale output change, R$_{L}$ = 2 kΩ to DACGND or DACV$_{DD}$ |
| | | 10 | | μV/mA | Due to load current change |
| OUTPUT CHARACTERISTICS[3] | | | | | |
| Output Voltage Range | 0 | | DACV$_{DD}$ | V | |
| Capacitive Load Stability | | 2 | | nF | R$_{L}$ = ∞ |
| | | 10 | | nF | R$_{L}$ = 2 kΩ |
| DC Output Impedance | | 0.5 | | Ω | |
| Short-Circuit Current | | 30 | | mA | DACV$_{DD}$ = 5 V |
| Power-Up Time | | 4 | | μs | Coming out of power-down mode, DACV$_{DD}$ = 5 V |
| REFERENCE INPUTS | | | | | |
| Reference Current | | 40 | 50 | μA | V$_{REFINx}$ = DACV$_{DD}$ = 5.5 V (per DAC channel) |
| Reference Input Range | 0 | | DACV$_{DD}$ | V | |
| Reference Input Impedance[3] | | 14.6 | | kΩ | |
| REFERENCE OUTPUT | | | | | |
| Output Voltage | 2.495 | | 2.505 | V | At ambient |
| Reference Temperature Coefficient[3] | | ±10 | | ppm/°C | |
| Reference Output Impedance[3] | | 7.5 | | kΩ | |
| LOGIC INPUTS | | | | | |
| Input Current | −3 | | +3 | μA | All digital inputs |
| Input Low Voltage, V$_{INL}$ | | | 0.8 | V | DACV$_{DD}$ = 5 V |
| Input High Voltage, V$_{INH}$ | 2 | | | V | DACV$_{DD}$ = 5 V |
| Pin Capacitance[3] | | 5 | | pF | |

| Parameter | Min | Typ | Max | Unit | Conditions/Comments[1] |
|---|---|---|---|---|---|
| POWER REQUIREMENTS | | | | | |
| $DACV_{DD}$ | 4.5 | | 5.5 | V | All digital inputs at 0 or $DACV_{DD}$, DAC active, excludes load current |
| $I_{DD}$ (Normal Mode)[4] | | | | | $V_{IH} = DACV_{DD} = 4.5$ V to 5.5 V, $V_{IL}$ = DACGND |
| | | 2.6 | 3.2 | mA | Internal reference off |
| | | 4 | 5 | mA | Internal reference on |
| $DACI_{DD}$ (All Power-Down Modes)[5] | | | | | |
| $DACV_{DD}$ | | 0.8 | 2 | µA | $V_{IH} = DACV_{DD} = 4.5$ V to 5.5 V, $V_{IL}$ = DACGND |

[1] Temperature range is −40°C to +85°C, typical at 25°C.
[2] Linearity calculated using a reduced code range of Code 32 to Code 4064. Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All sixteen DACs powered down.

### DAC AC Characteristics

$DACV_{DD} = 4.5$ V to 5.25 V, $R_L = 2$ kΩ to DACGND, $C_L = 200$ pF to DACGND, $V_{REFIN1} = V_{REFIN1} = DACV_{DD}$. All specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 3.**

| Parameter[1, 2] | Min | Typ | Max | Unit | Conditions/Comments[3] |
|---|---|---|---|---|---|
| Output Voltage Settling Time | | 6 | 10 | µs | ¼ to ¾ scale settling to ±2 LSB |
| Slew Rate | | 1.5 | | V/µs | |
| Digital-to-Analog Glitch Impulse | | 4 | | nV-sec | 1 LSB change around major carry (see Figure 17) |
| Digital Feedthrough | | 0.1 | | nV-sec | |
| Reference Feedthrough | | −90 | | dB | $V_{REFIN1} = V_{REFIN2} = 2$ V ± 0.1 V p-p, frequency = 10 Hz to 20 MHz |
| Digital Crosstalk | | 0.5 | | nV-sec | |
| Analog Crosstalk | | 2.5 | | nV-sec | |
| DAC-to-DAC Crosstalk | | 3 | | nV-sec | |
| Multiplying Bandwidth | | 340 | | kHz | $V_{REFIN1} = V_{REFIN2} = 2$ V ± 0.2 V p-p |
| Total Harmonic Distortion | | −80 | | dB | $V_{REFIN1} = V_{REFIN2} = 2$ V ± 0.1 V p-p, frequency = 10 kHz |
| Output Noise Spectral Density | | 120 | | nV/√Hz | DAC Code = 0x8400, 1 kHz |
| | | 100 | | nV/√Hz | DAC Code = 0x8400, 10 kHz |
| Output Noise | | 15 | | µV p-p | 0.1 Hz to 10 Hz |

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +85°C, typical at 25°C.

## OPERATIONAL AMPLIFIER SPECIFICATIONS

Electrical characteristics @ $V_{SY}$ = 5 V, $V_{CM}$ = $V_{SY}/2$, $T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | | 0.4 | 2.2 | mV | $-0.3\text{ V} < V_{CM} < +5.3\text{ V}$ |
| | | | | 2.2 | mV | $-40°\text{C} < T_A < +85°\text{C}$, $-0.3\text{ V} < V_{CM} < +5.2\text{ V}$ |
| Offset Voltage Drift[1] | $\Delta V_{OS}/\Delta T$ | | 1 | 4.5 | µV/°C | $-40°\text{C} < T_A < +85°\text{C}$ |
| Input Bias Current[1] | $I_B$ | | 0.2 | 1 | pA | |
| | | | | 110 | pA | $-40°\text{C} < T_A < +85°\text{C}$ |
| Input Offset Current[1] | $I_{OS}$ | | 0.1 | 0.5 | pA | |
| | | | | 50 | pA | $-40°\text{C} < T_A < +85°\text{C}$ |
| Common-Mode Rejection Ratio | CMRR | | 95 | | dB | $0\text{ V} < V_{CM} < 5\text{ V}$ |
| | | 68 | | | dB | $-40°\text{C} < T_A < +85°\text{C}$ |
| Large Signal Voltage Gain | $A_{VO}$ | 235 | 400 | | V/mV | $R_L = 10\text{ k}\Omega$, $0.5\text{ V} < V_{OUT} < 4.5\text{ V}$ |
| Input Capacitance[1] | $C_{DIFF}$ | | 2 | | pF | |
| | $C_{CM}$ | | 7 | | pF | |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | $V_{OH}$ | 4.95 | 4.98 | | V | $I_L = 1\text{ mA}$ |
| | | 4.9 | | | V | −40°C to +85°C |
| | | | 4.7 | | V | $I_L = 10\text{ mA}$ |
| | | 4.50 | | | V | −40°C to +85°C |
| Output Voltage Low | $V_{OL}$ | | 20 | 30 | mV | $I_L = 1\text{ mA}$ |
| | | | | 50 | mV | −40°C to +85°C |
| | | | 190 | 275 | mV | $I_L = 10\text{ mA}$ |
| | | | | 335 | mV | −40°C to +85°C |
| Short-Circuit Current[1] | $I_{SC}$ | | ±80 | | mA | |
| Closed-Loop Output Impedance[1] | $Z_{OUT}$ | | 15 | | Ω | $f = 10\text{ kHz}$, $A_V = 1$ |
| POWER SUPPLY | | | | | | |
| Power Supply Span (V+ to V−) | | | 5 | | V | |
| Power Supply Rejection Ratio | PSRR | 67 | 94 | | dB | $1.8\text{ V} < V_{SY} < 5\text{ V}$ |
| | | 64 | | | dB | $-40°\text{C} < T_A < +85°\text{C}$ |
| Supply Current per Amplifier | $I_{SY}$ | | 38 | | µA | $V_{OUT} = V_{SY}/2$ |
| | | | 50 | 60 | µA | $-40°\text{C} < T_A < +85°\text{C}$ |
| DYNAMIC PERFORMANCE[1] | | | | | | |
| Slew Rate | SR | | 0.1 | | V/µs | $R_L = 10\text{ k}\Omega$ |
| Settling Time 0.1% | $t_S$ | | 23 | | µs | G = ±1, 2 V step, $C_L = 20\text{ pF}$, $R_L = 1\text{ k}\Omega$ |
| Gain Bandwidth Product | GBP | | 400 | | kHz | $R_L = 100\text{ k}\Omega$ |
| | | | 350 | | kHz | $R_L = 10\text{ k}\Omega$ |
| Phase Margin | $Ø_O$ | | 70 | | Degrees | $R_L = 10\text{ k}\Omega$, $R_L = 100\text{ k}\Omega$, $C_L = 20\text{ pF}$ |
| NOISE PERFORMANCE[1] | | | | | | |
| Peak-to-Peak Noise | | | 2.3 | 3.5 | µV | |
| Voltage Noise Density | $e_n$ | | 25 | | nV/√Hz | f = 1 kHz |
| | | | 22 | | nV/√Hz | f = 10 kHz |
| Current Noise Density | $i_n$ | | 0.05 | | pA/√Hz | f = 1 kHz |

[1] Guaranteed by design and characterization. Not production tested.

## TIMING SPECIFICATIONS

### ADC Timing Characteristics

$ADCV_{DD}$ = 2.7 V to 5.25 V, $V_{DRIVE} \le ADCV_{DD}$, $V_{REFA}$ = 2.5 V; All specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 5.**

| Parameter[1] | Limit at $T_{MIN}$, $T_{MAX}$; $ADCV_{DD}$ = 5 V | Unit | Conditions/Comments |
|---|---|---|---|
| $f_{SCLK}$[2] | 10 | kHz min | |
| | 20 | MHz min | |
| $t_{CONVERT}$ | 16 × $t_{ASCLK}$ | MHz max | |
| $t_{QUIET}$ | 50 | ns min | |
| $t_2$ | 10 | ns min | $\overline{\text{ASYNC}}$ to ASCLK setup time |
| $t_3$[3] | 14 | ns max | Delay from $\overline{\text{ASYNC}}$ until ADOUT three-state disabled |
| $t_3b$[4] | 20 | ns min | Data hold time |
| $t_4$[3] | 40 | ns max | Data access time after ASCLK falling edge |
| $t_5$ | 0.4 × $t_{ASCLK}$ | ns min | ASCLK low pulse width |
| $t_6$ | 0.4 × $t_{ASCLK}$ | ns min | ASCLK high pulse width |
| $t_7$ | 15 | ns min | ASCLK to ADOUT valid hold time |
| $t_8$[5] | 15/50 | ns min/max | ASCLK falling edge to ADOUT high impedance |
| $t_9$ | 20 | ns min | ADIN setup time prior to ASCLK falling edge |
| $t_{10}$ | 5 | ns min | ADIN Hold time prior to ASCLK falling edge |
| $t_{11}$ | 20 | ns min | 16th ASCLK falling edge to $\overline{\text{ASYNC}}$ high |
| $t_{12}$ | 1 | µs max | Power-up time from full power-down/autoshutdown/ autostandby modes |

[1] Guaranteed by design and characterization. Not production tested. All input signals are specified with tr = tf = 5 ns (10% to 90% of $ADCV_{DD}$) and timed from a voltage level of 1.6 V.

[2] Maximum ASCLK frequency is 50 MHz at $ADCV_{DD}$ = 2.7 V to 5.5 V. Guaranteed by design and characterization; not production tested.

[3] Measured with the load circuit of Figure 3 and defined as the time required for the output to cross 0.4 V or 0.7 × $V_{DRIVE}$.

[4] $t_3b$ represents a worst-case figure for having ADD3 available on the ADOUT line, that is, if the ADC goes back into three-state at the end of a conversion and some other device takes control of the bus between conversions, the user needs to wait a maximum time of $t_3b$ before having ADD3 valid on the ADOUT line. If the ADOUT line is weakly driven to ADD3 between conversions, then the user typically needs to wait 17 ns at 3 V and 12 ns at 5 V after the $\overline{\text{ASYNC}}$ falling edge before seeing ADD3 valid on ADOUT.

[5] $t_8$ is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, $t_8$, quoted in the timing characteristics, is the true bus relinquish time of the part and is independent of bus loading.

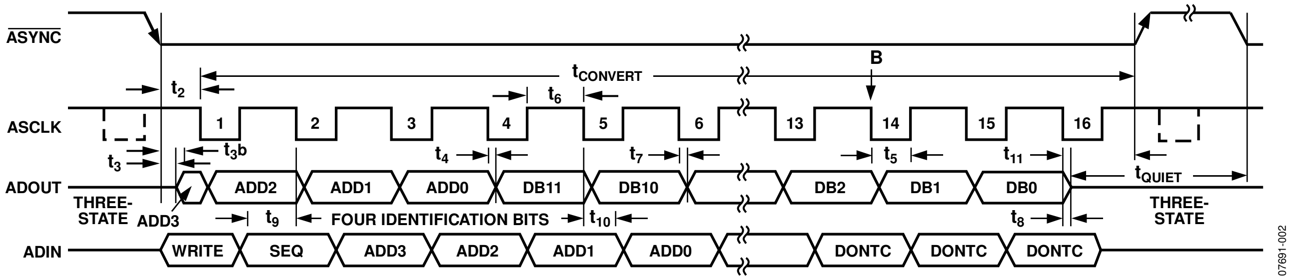


*Figure 2. ADC Timing Characteristics*

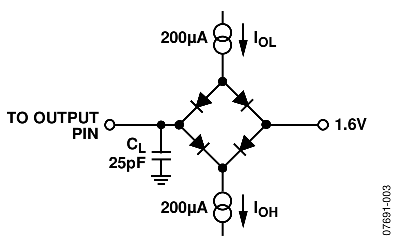


*Figure 3. Load Circuit for ADC Digital Output Timing Specifications*

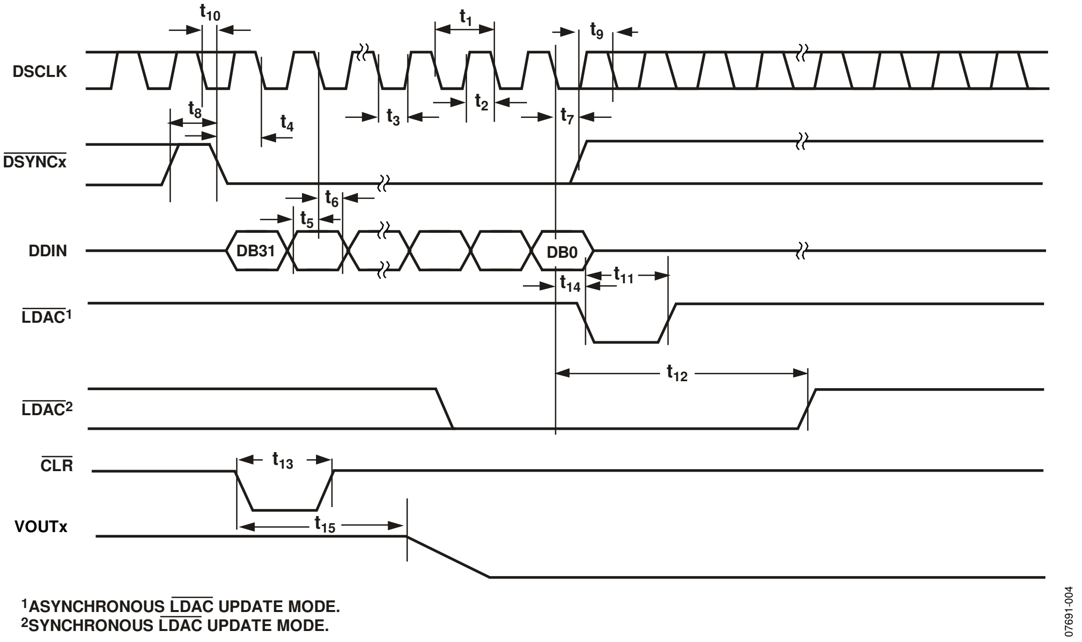
### DAC Timing Characteristics

All input signals are specified with tr = tf = 1 ns/V (10% to 90% of $V_{DD}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 4. $DACV_{DD}$ = 4.5 V to 5.5 V. All specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 6.**

| Parameter[1] | Limit at $T_{MIN}$, $T_{MAX}$; $DACV_{DD}$ = 2.7 V to 5.5 V | Unit | Conditions/Comments |
|---|---|---|---|
| $t_1$[2] | 20 | ns min | DSCLK cycle time |
| $t_2$ | 8 | ns min | DSCLK high time |
| $t_3$ | 8 | ns min | DSCLK low time |
| $t_4$ | 13 | ns min | $\overline{\text{DSYNC}}$ to DSCLK falling edge setup time |
| $t_5$ | 4 | ns min | Data setup time |
| $t_6$ | 4 | ns min | Data hold time |
| $t_7$ | 0 | ns min | DSCLK falling edge to $\overline{\text{DSYNC}}$ rising edge |
| $t_8$ | 15 | ns min | Minimum $\overline{\text{DSYNC}}$ high time |
| $t_9$ | 13 | ns min | $\overline{\text{DSYNC}}$ rising edge to DSCLK fall ignore |
| $t_{10}$ | 0 | ns min | DSCLK falling edge to $\overline{\text{DSYNC}}$ fall ignore |
| $t_{11}$ | 10 | ns min | $\overline{\text{LDAC}}$ pulse width low |
| $t_{12}$ | 15 | ns min | DSCLK falling edge to $\overline{\text{LDAC}}$ rising edge |
| $t_{13}$ | 5 | ns min | $\overline{\text{CLR}}$ pulse width low |
| $t_{14}$ | 0 | ns min | DSCLK falling edge to $\overline{\text{LDAC}}$ falling edge |
| $t_{15}$ | 300 | ns typ | $\overline{\text{CLR}}$ pulse activation time |

[1] Sample tested at 25°C to ensure compliance.
[2] Maximum DSCLK frequency is 50 MHz at $V_{DD}$ = 2.7 V to 5.5 V. Guaranteed by design and characterization; not production tested.



[1]ASYNCHRONOUS $\overline{\text{LDAC}}$ UPDATE MODE.
[2]SYNCHRONOUS $\overline{\text{LDAC}}$ UPDATE MODE.

*Figure 4. DAC Timing Characteristics*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C unless otherwise noted. $V_{DD}$ refers to DACV$_{DD}$ or ADCV$_{DD}$. GND refers to DACGND or ADCGND.

**Table 7.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| $V_{DRIVE}$ to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Op Amp Supply Voltage | 6 V |
| Op Amp Input Voltage | (V1− or V2−) − 0.3 V to (V1+ or V2+) + 0.3 V |
| Op Amp Differential Input Voltage | ±6 V |
| Op Amp Output Short-Circuit Duration to GND | Indefinite |
| Analog Input Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to +7 V |
| Digital Output Voltage to GND | −0.3 V to $V_{DD}$ +0.3 V |
| $V_{REFA}$ to GND | −0.3 V to $V_{DD}$ +0.3 V |
| $V_{REFIN}$/$V_{REFOUT}$ to GND | −0.3 V to $V_{DD}$ +0.3 V |
| Input Current to Any ADC Pin Except Supplies | ±10 mA |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature ($T_J$ max) | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a 4-layer JEDEC thermal test board for surface-mount packages.

**Table 8. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 80-Ball CSP_BGA | 40 | °C/W |

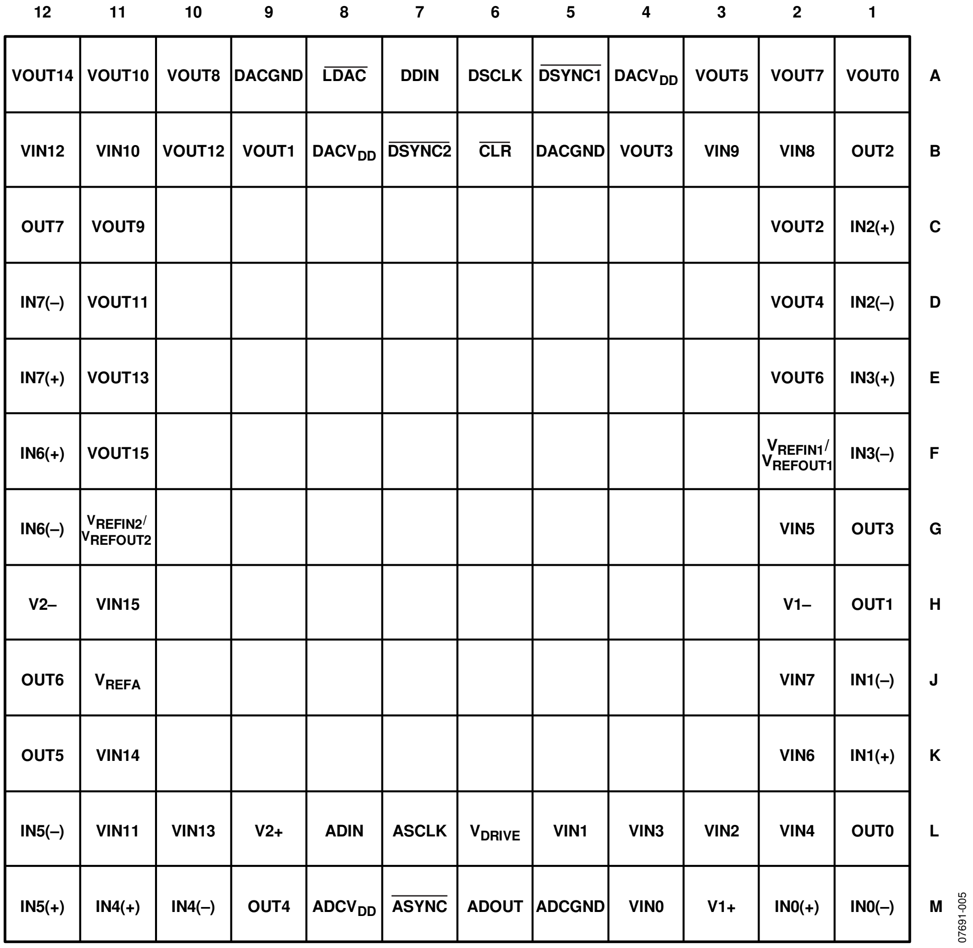
**Table 9. Junction Temperature**

| Parameter | Max | Unit | Comments |
|---|---|---|---|
| Junction Temperature[1, 2] | 130 | °C | $T_J = T_A + P_{TOTAL} \times \theta_{JA}$ |

[1] $P_{TOTAL}$ is the sum of ADC, DAC, and operational amplifier supply currents.
[2] $\theta_{JA}$ is the package thermal resistance.

## ESD CAUTION

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



| 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VOUT14 | VOUT10 | VOUT8 | DACGND | $\overline{\text{LDAC}}$ | DDIN | DSCLK | $\overline{\text{DSYNC1}}$ | $\text{DACV}_{\text{DD}}$ | VOUT5 | VOUT7 | VOUT0 | A |
| VIN12 | VIN10 | VOUT12 | VOUT1 | $\text{DACV}_{\text{DD}}$ | $\overline{\text{DSYNC2}}$ | $\overline{\text{CLR}}$ | DACGND | VOUT3 | VIN9 | VIN8 | OUT2 | B |
| OUT7 | VOUT9 | | | | | | | | | VOUT2 | IN2(+) | C |
| IN7(–) | VOUT11 | | | | | | | | | VOUT4 | IN2(–) | D |
| IN7(+) | VOUT13 | | | | | | | | | VOUT6 | IN3(+) | E |
| IN6(+) | VOUT15 | | | | | | | | | $\text{V}_{\text{REFIN1}}$/ $\text{V}_{\text{REFOUT1}}$ | IN3(–) | F |
| IN6(–) | $\text{V}_{\text{REFIN2}}$/ $\text{V}_{\text{REFOUT2}}$ | | | | | | | | | VIN5 | OUT3 | G |
| V2– | VIN15 | | | | | | | | | V1– | OUT1 | H |
| OUT6 | $\text{V}_{\text{REFA}}$ | | | | | | | | | VIN7 | IN1(–) | J |
| OUT5 | VIN14 | | | | | | | | | VIN6 | IN1(+) | K |
| IN5(–) | VIN11 | VIN13 | V2+ | ADIN | ASCLK | $\text{V}_{\text{DRIVE}}$ | VIN1 | VIN3 | VIN2 | VIN4 | OUT0 | L |
| IN5(+) | IN4(+) | IN4(–) | OUT4 | $\text{ADCV}_{\text{DD}}$ | $\overline{\text{ASYNC}}$ | ADOUT | ADCGND | VIN0 | V1+ | IN0(+) | IN0(–) | M |

*Figure 5. Pin Configuration*

**Table 10. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| M7 | $\overline{\text{ASYNC}}$ | Frame Synchronization Signal. Active low logic input. This input provides the dual function of initiating ADC conversions and also frames the serial data transfer. |
| J11 | $\text{V}_{\text{REFA}}$ | Reference Input for the ADC Block. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V ± 1% for specified performance. |
| M8 | $\text{ADCV}_{\text{DD}}$ | Power Supply Input for the ADC Block. The ADC can operate from 4.5 V to 5.25 V, and the supply should be decoupled with a 10 µF in parallel with a 0.1 µF capacitor to ADCGND. |
| M5 | ADCGND | Ground Reference Point for the ADC Block. All ADC analog/digital input/output signals and any external reference signal should be referred to this ADCGND voltage. |
| M4, L5, L3, L4, L2, G2, K2, J2, B2, B3, B11, L11, B12, L10, K11, H11 | VIN0 to VIN15 | Analog Input 0 through Analog Input 15. Sixteen single-ended analog input channels that are multiplexed into the on-chip track and hold. The analog input channel to be converted is selected by using the ADD3 through ADD0 address bits of the control register. The address bits in conjunction with the SEQ and shadow bits allow the sequence register to be programmed. The input range for all input channels can extend from 0 V to $\text{V}_{\text{REFA}}$ or 0 V to 2 × $\text{V}_{\text{REFA}}$, as selected via the range bit in the control register. Any unused input channels should be connected to GND to avoid noise pickup. |
| L8 | ADIN | ADC Data In. Logic input. Data to be written to the control register of the ADC is provided on this input and is clocked into the register on the falling edge of ASCLK (see the Accessing the ADC Block section). |
| M6 | ADOUT | Data Out. Logic output. The conversion result from the ADC block is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the ASCLK input. The data stream consists of four address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data, which is provided MSB first. The output coding can be selected as straight binary or twos complement via the coding bit in the control register. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| L7 | ASCLK | Serial Clock. Logic input. ASCLK provides the serial clock for accessing data from the ADC block. This clock input is also used as the clock source for the conversion process of the ADC. |
| L6 | $V_{DRIVE}$ | Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the serial interface of the ADC block operates. |
| A4, B8 | $DACV_{DD}$ | Power Supply Input for the DAC Block. The DAC can operate from 4.5 V to 5.25 V, and the supply should be decoupled with a 10 µF in parallel with a 0.1 µF capacitor to DACGND. The two $DACV_{DD}$ pins must be connected together. |
| A9, B5 | DACGND | Ground Reference Point for the DAC Block. All DAC analog/digital input/output signals and any external reference signal should be referred to this DACGND voltage. The two DACGND pins should be connected together. |
| A8 | $\overline{\text{LDAC}}$ | Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. Alternatively, this pin can be tied permanently low. |
| A5 | $\overline{\text{DSYNC1}}$ | Active Low Control Input. This is the frame synchronization signal for the input data of DAC channels VOUT0 to VOUT7. When $\overline{\text{DSYNC1}}$ goes low, it powers on the DSCLK and DDIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{DSYNC1}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{DSYNC1}}$ acts as an interrupt and the write sequence is ignored by the device. |
| B7 | $\overline{\text{DSYNC2}}$ | Active Low Control Input. This is the frame synchronization signal for the input data of DAC channels VOUT8 to VOUT15. When $\overline{\text{DSYNC2}}$ goes low, it powers on the DSCLK and DDIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{DSYNC2}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{DSYNC2}}$ acts as an interrupt and the write sequence is ignored by the device. |
| B6 | $\overline{\text{CLR}}$ | Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the $\overline{\text{CLR}}$ code register—zero scale, midscale, or full scale. Default setting clears the output to 0 V. |
| A7 | DDIN | DAC Data Input. This DAC has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. |
| A6 | DSCLK | DAC Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz. |
| A1, B9, C2, B4, D2, A3, E2, A2 | VOUT0 to VOUT7 | Analog Output Voltage from DAC0 to DAC7. $\overline{\text{DSYNC1}}$ is the frame synchronization signal for writing data to these DACs. The DAC is updated automatically if $\overline{\text{LDAC}}$ is low, or on the falling edge of $\overline{\text{LDAC}}$ if it is high. The output amplifiers have rail-to-rail operation. |
| A10, C11, A11, D11, B10, E11, A12, F11 | VOUT8 to VOUT15 | Analog Output Voltage from DAC8 to DAC15. $\overline{\text{DSYNC2}}$ is the frame synchronization signal for writing data to these DACs. The DAC is updated automatically if $\overline{\text{LDAC}}$ is low, or on the falling edge of $\overline{\text{LDAC}}$ if it is high. The output amplifiers have rail to rail operation. |
| F2 | $V_{REFIN1}$/ $V_{REFOUT1}$ | Reference Input/Output Pin for DAC0 to DAC7. The DACs have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input. |
| G11 | $V_{REFIN2}$/ $V_{REFOUT2}$ | Reference Input/Output Pin for DAC8 to DAC15. The DACs have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input. |
| M3 | V1+ | Positive Supply Input for the amplifier 0 to amplifier 3. The supply for these amplifiers is independent of other supplies and can be operated with a different supply if required. The pin should be decoupled to V1− with a 10 µF in parallel with a 0.1 µF capacitor. |
| H2 | V1− | Negative Supply Input for Amplifier 0 to Amplifier 3. |
| L9 | V2+ | Positive Supply Input for Amplifier 4 to Amplifier 7. The supply for these amplifiers is independent of other supplies and can be operated with a different supply if required. The pin should be decoupled to V2− with a 10 µF in parallel with a 0.1 µF capacitor. |
| H12 | V2− | Negative Supply Input for Amplifier 4 to Amplifier 7. |
| M1, J1, D1, F1, M10, L12, G12, D12 | IN0(−) to IN7(−) | Inverting Input Terminals for Operational Amplifier 0 to Amplifier 7. |
| M2, K1, C1, E1, M11, M12, F12, E12 | IN0(+) to IN7(+) | Noninverting Input Terminals for Operational Amplifier 0 to Amplifier 7. |
| L1, H1, B1, G1, M9, K12, J12, C12 | OUT0 to OUT7 | Output Terminals for Operational Amplifier 0 to Amplifier 7. |

# TYPICAL PERFORMANCE CHARACTERISTICS

## DAC

$DACV_{DD}$ and $ADCV_{DD}$ = 5 V, $V_{SY}$ = 5 V, unless otherwise noted.

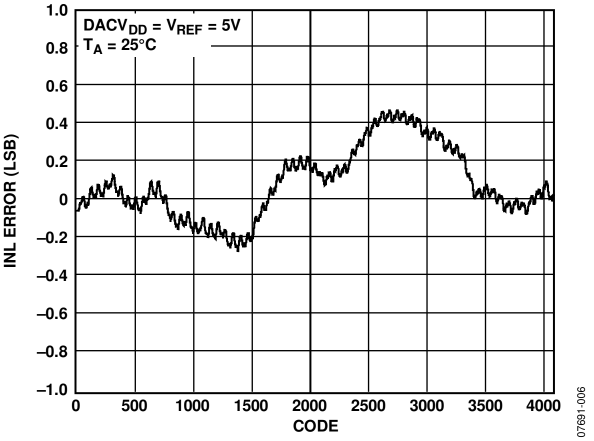


*Figure 6. DAC INL, External Reference*

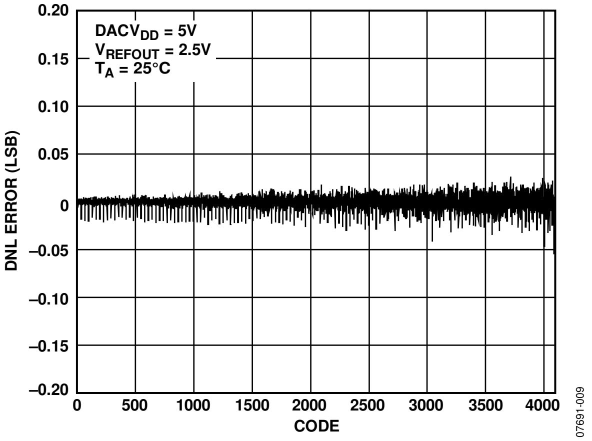


*Figure 9. DAC DNL, Internal Reference*

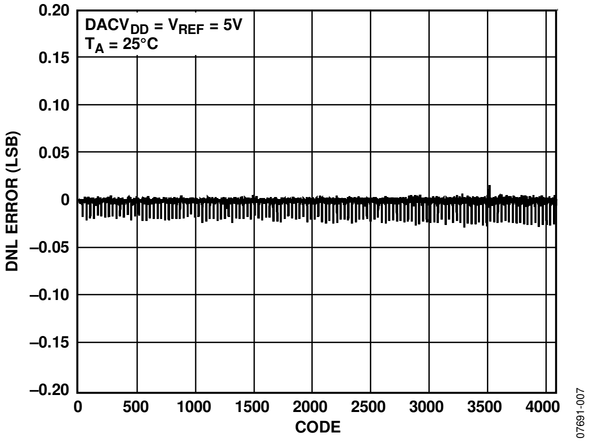


*Figure 7. DAC DNL, External Reference*

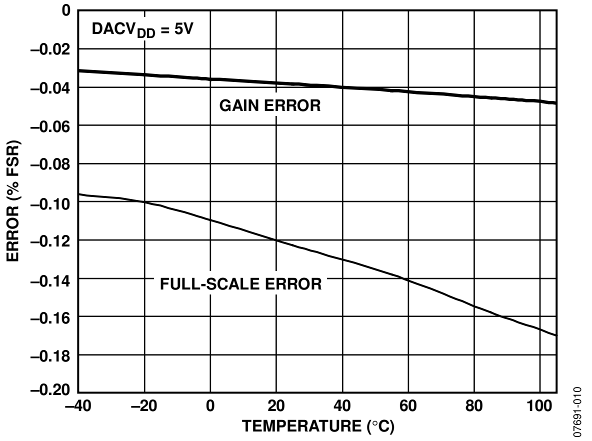


*Figure 10. DAC Gain Error and Full-Scale Error vs. Temperature*

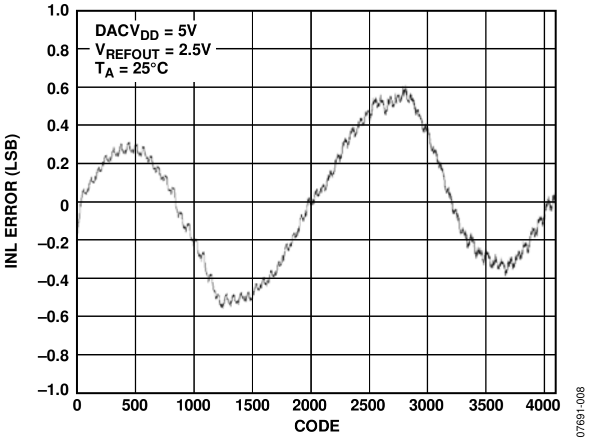


*Figure 8. DAC INL, Internal Reference*

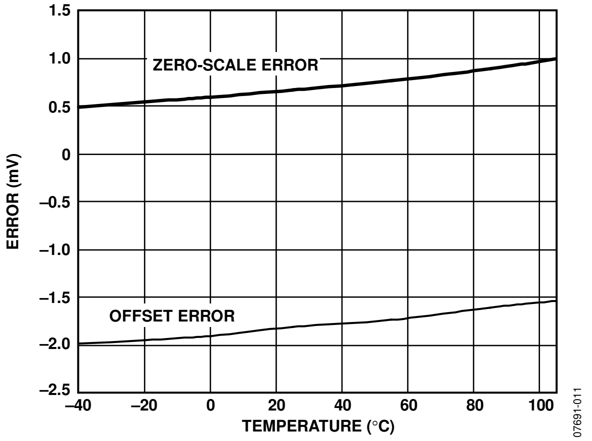


*Figure 11. DAC Zero-Scale Error and Offset Error vs. Temperature*

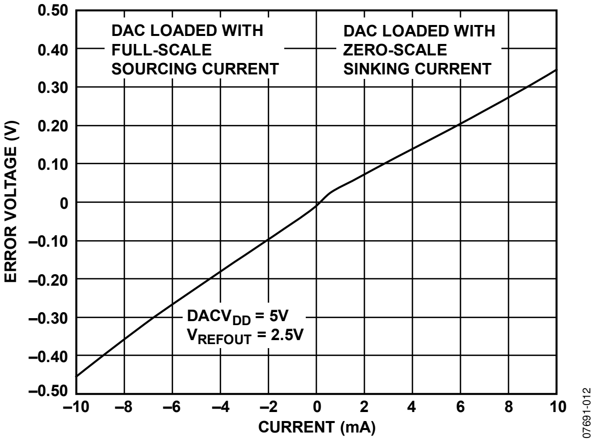


Figure 12. DAC Headroom at Rails vs. Source and Sink

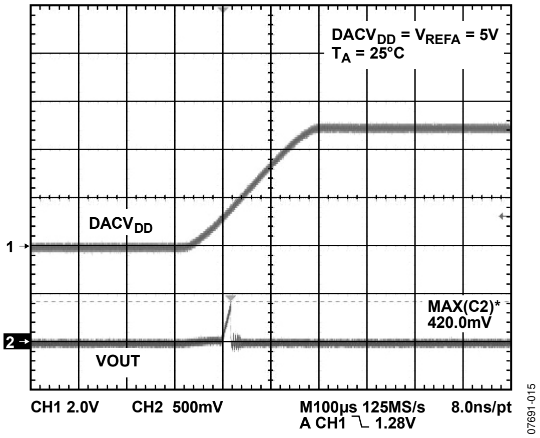


Figure 15. DAC Power-On Reset to 0 V

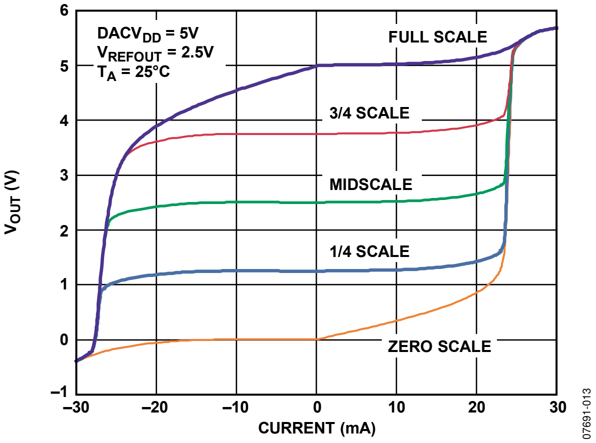


Figure 13. DAC Sink and Source Capability

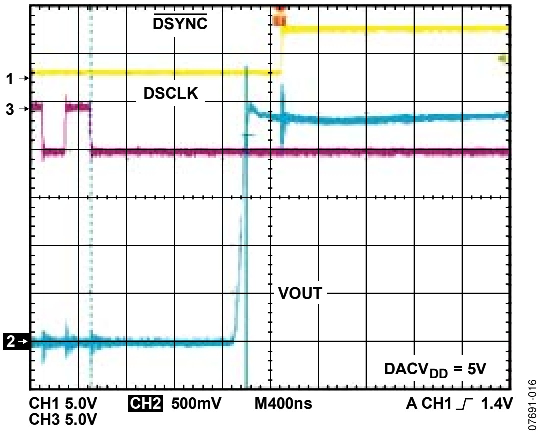


Figure 16. DAC Exiting Power-Down to Midscale

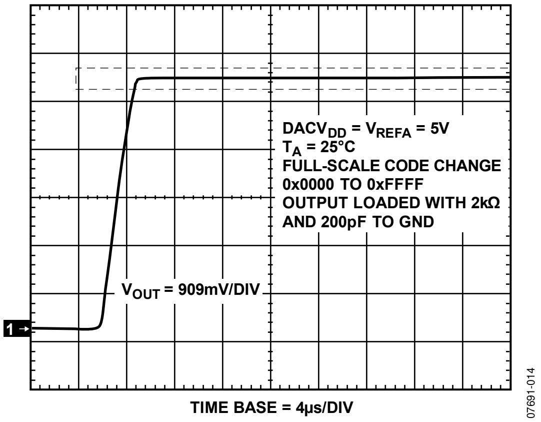


Figure 14. DAC Full-Scale Settling Time

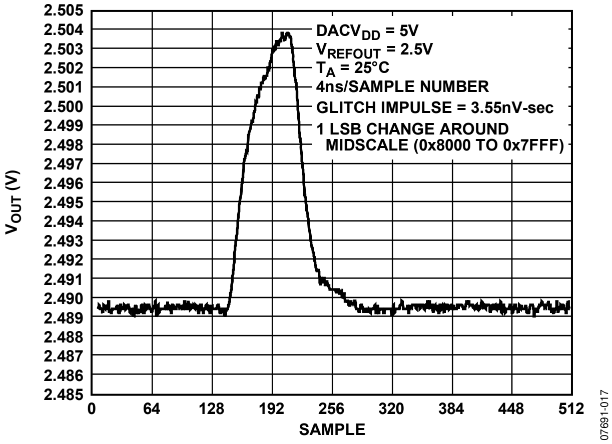


Figure 17. DAC Digital-to-Analog Glitch Impulse (Negative)

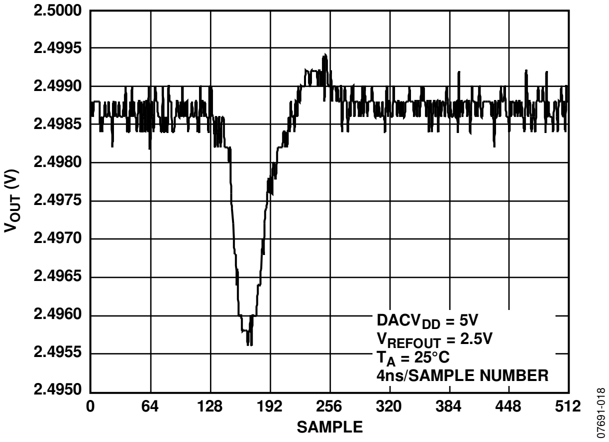


*Figure 18. DAC Analog Crosstalk*

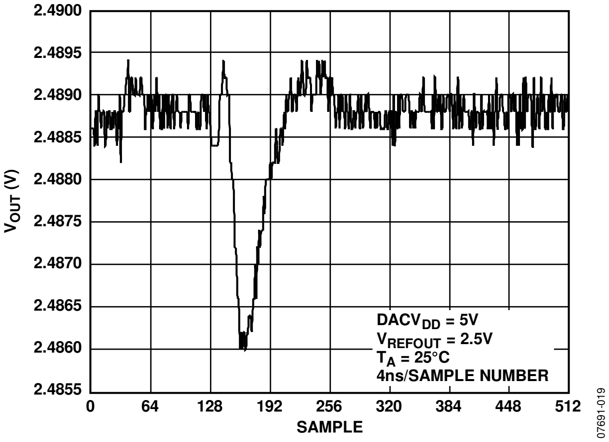


*Figure 19. DAC-to-DAC Crosstalk*

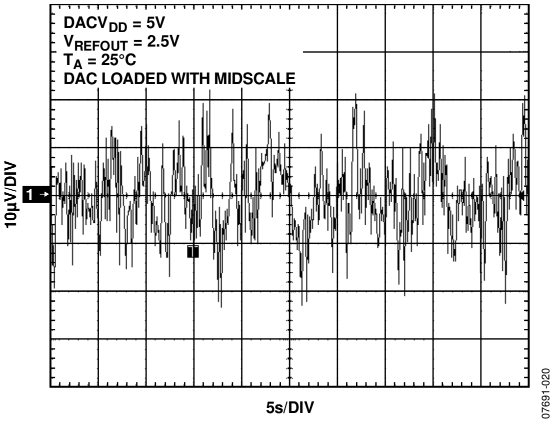


*Figure 20. 0.1 Hz to 10 Hz DAC Output Noise Plot, Internal Reference*

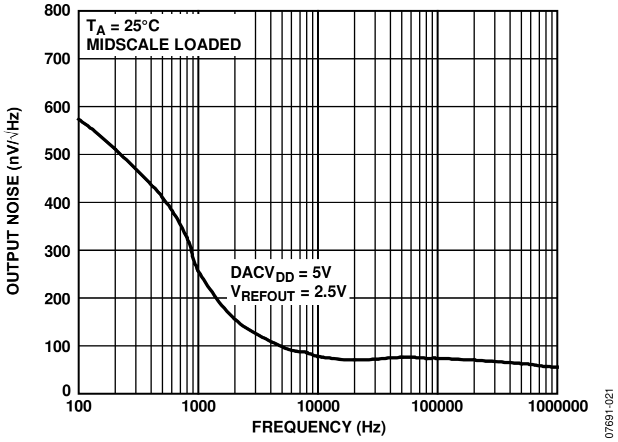


*Figure 21. DAC Noise Spectral Density, Internal Reference*

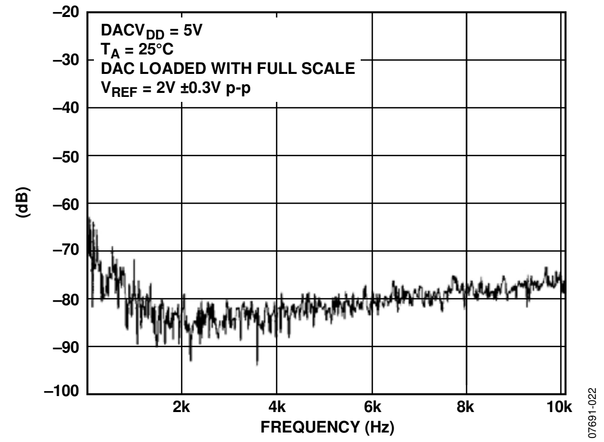


*Figure 22. DAC Total Harmonic Distortion*

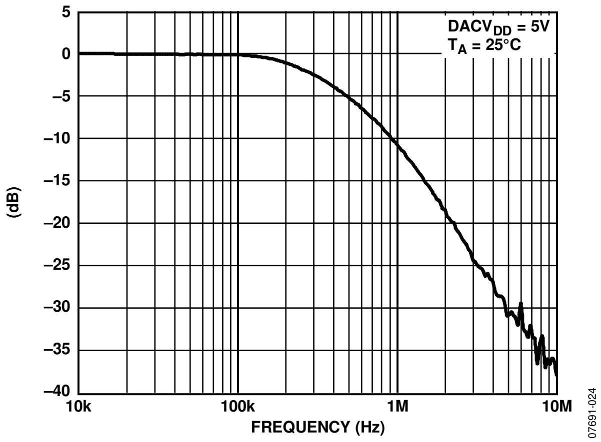


*Figure 24. DAC Multiplying Bandwidth*

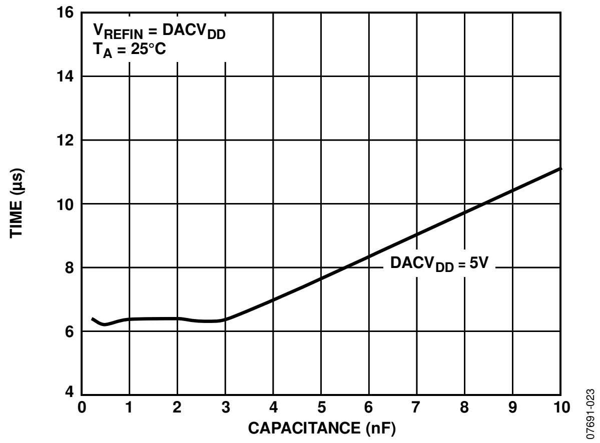


*Figure 23. DAC Settling Time vs. Capacitive Load*

## ADC

$DACV_{DD}$ and $ADCV_{DD}$ = 5 V, $V_{SY}$ = 5 V, unless otherwise noted.

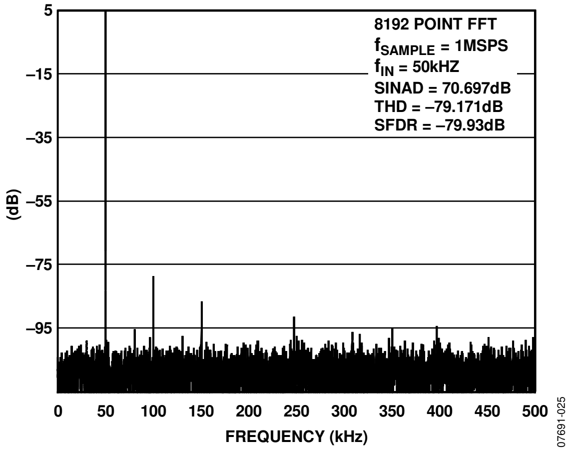


*Figure 25. ADC Dynamic Performance at 1 MSPS*

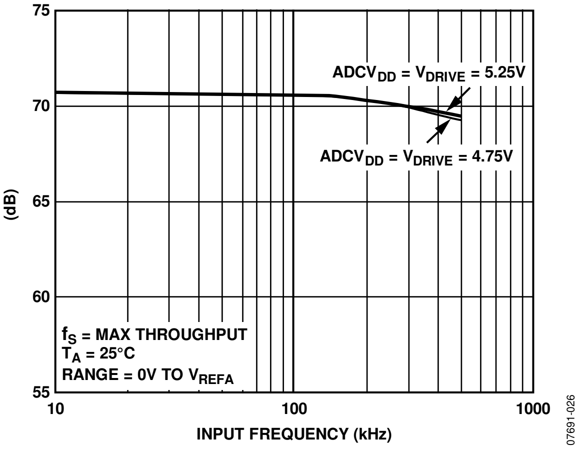


*Figure 26. ADC SINAD vs. Analog Input Frequency for Various Supply Voltages at 1 MSPS*

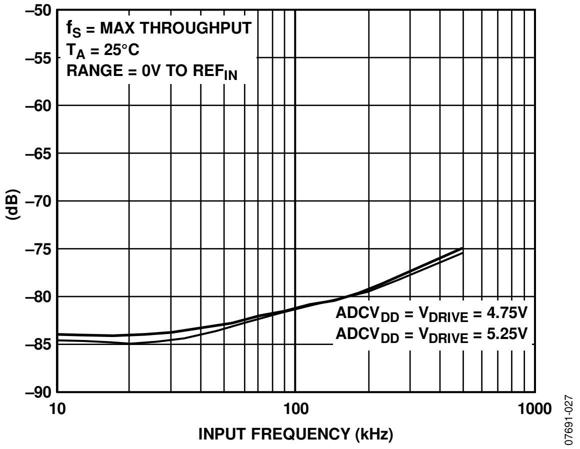


*Figure 27. THD vs. Analog Input Frequency for Various Supplies at 1 MSPS*

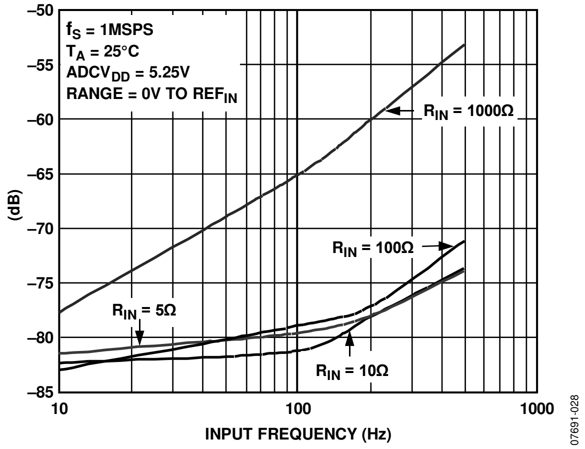


*Figure 28. ADC THD vs. Input Frequency for Various Analog Source Impedances*

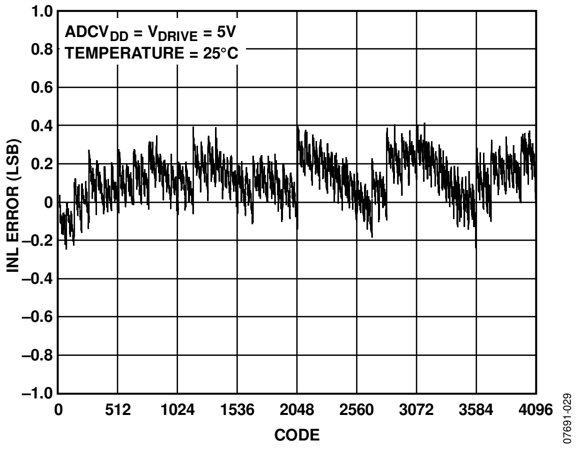


*Figure 29. ADC Typical INL*

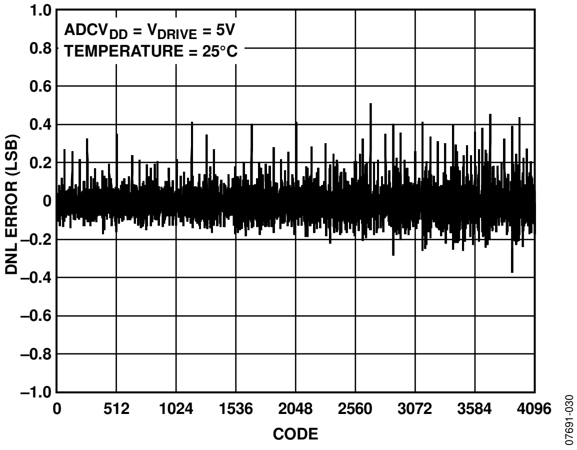


*Figure 30. ADC Typical DNL*

## AMPLIFIER

DACV$_{DD}$ and ADCV$_{DD}$ = 5 V, V$_{SY}$ = 5 V, unless otherwise noted.

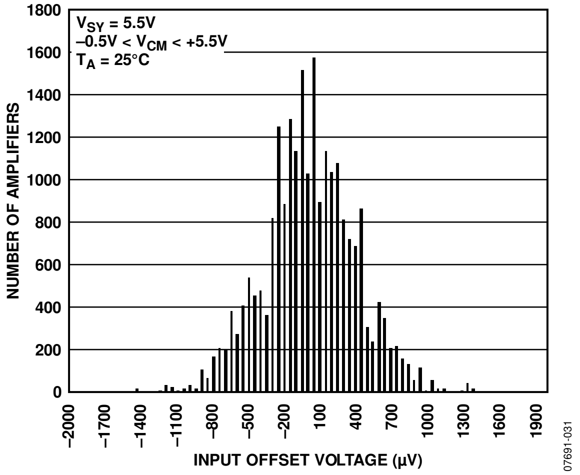


*Figure 31. Amplifier Input Offset Voltage Distribution*

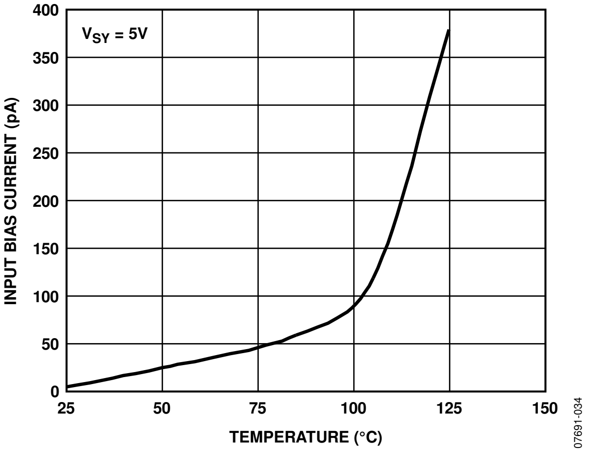


*Figure 34. Amplifier Input Bias Current vs. Temperature*

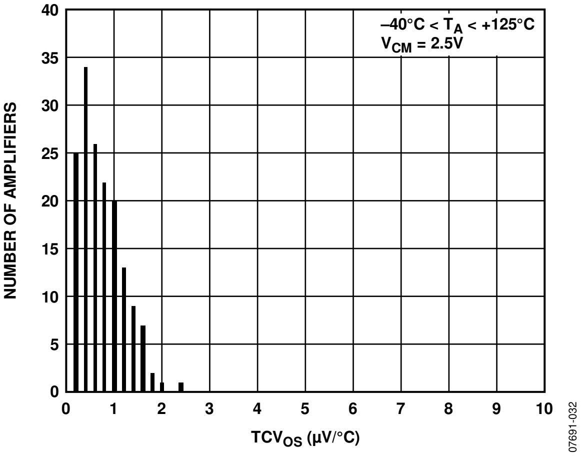


*Figure 32. Amplifier Input Offset Voltage Drift Distribution*

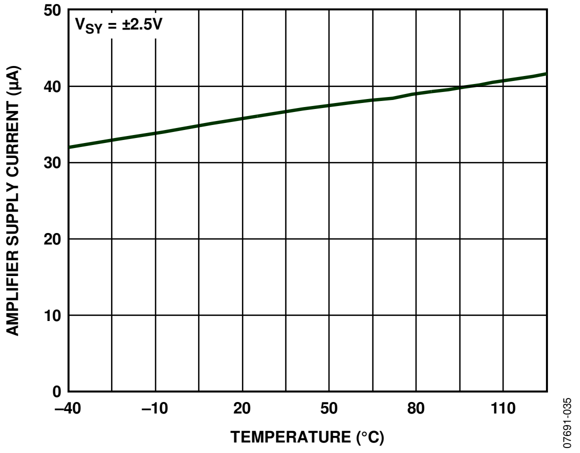


*Figure 35. Amplifier Supply Current vs. Temperature*

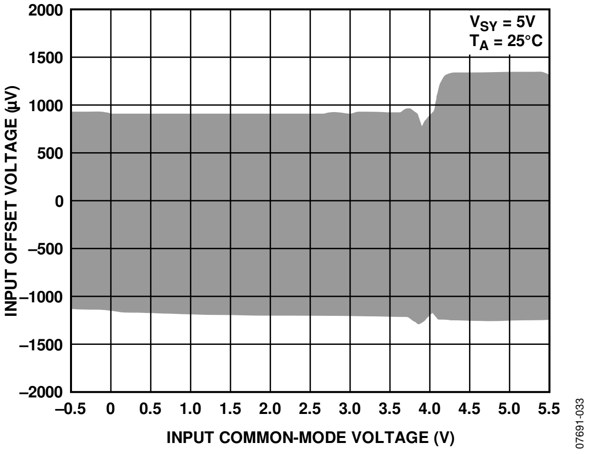


*Figure 33. Amplifier Input Offset Voltage vs. Input Common-Mode Voltage*

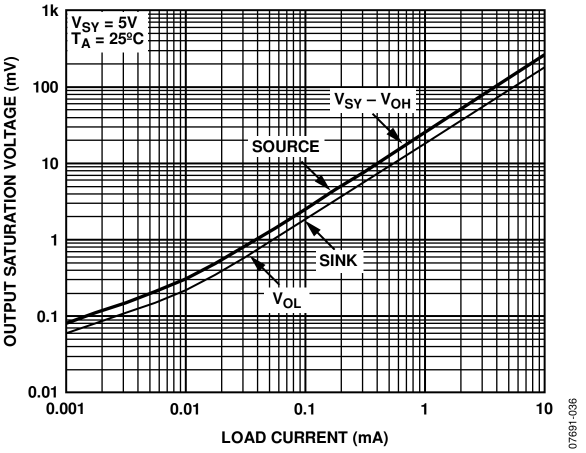


*Figure 36. Amplifier Output Saturation Voltage vs. Load Current*

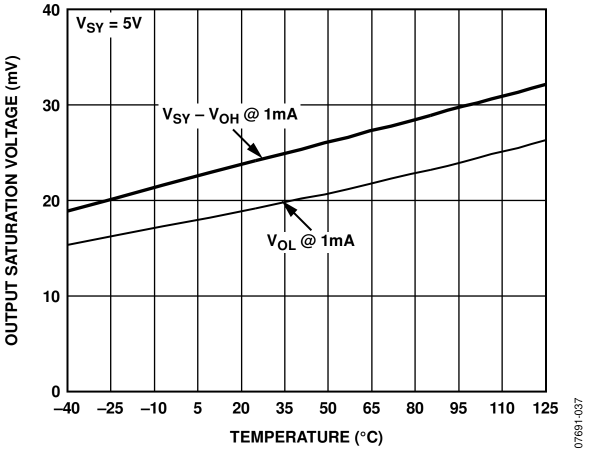


Figure 37. Amplifier Output Saturation Voltage vs. Temperature ($I_L$ = 1 mA)

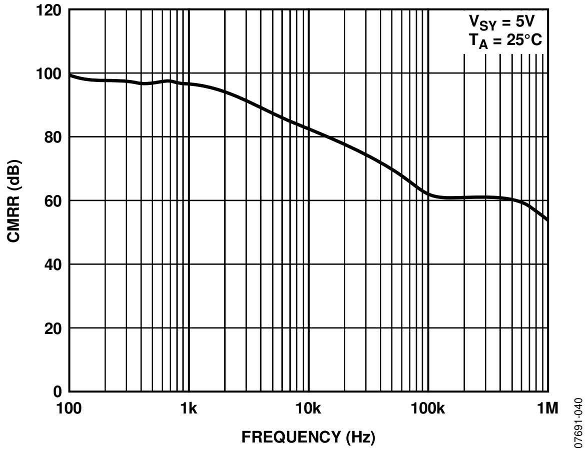


Figure 40. Amplifier CMRR vs. Frequency

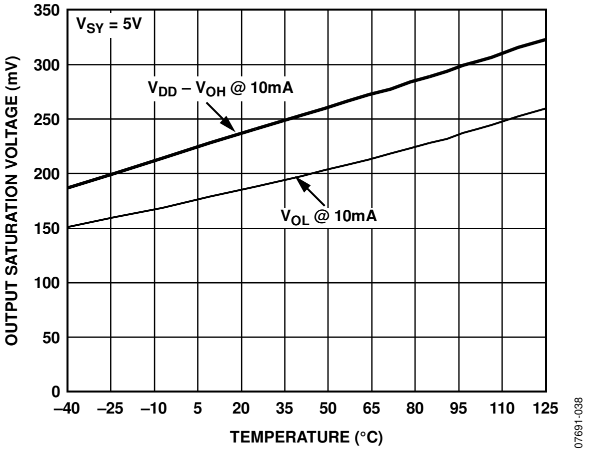


Figure 38. Amplifier Output Saturation Voltage vs. Temperature ($I_L$ = 10 mA)

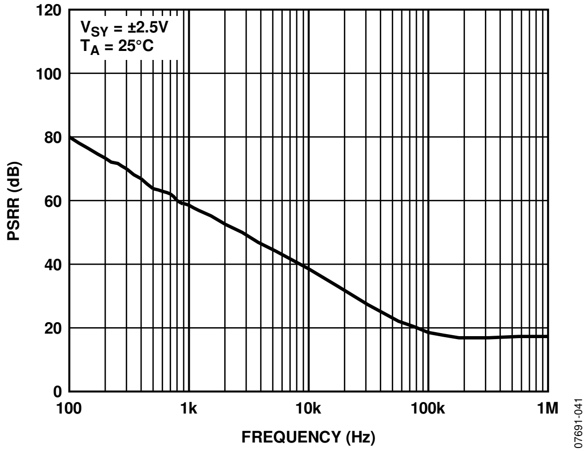


Figure 41. Amplifier PSRR vs. Frequency

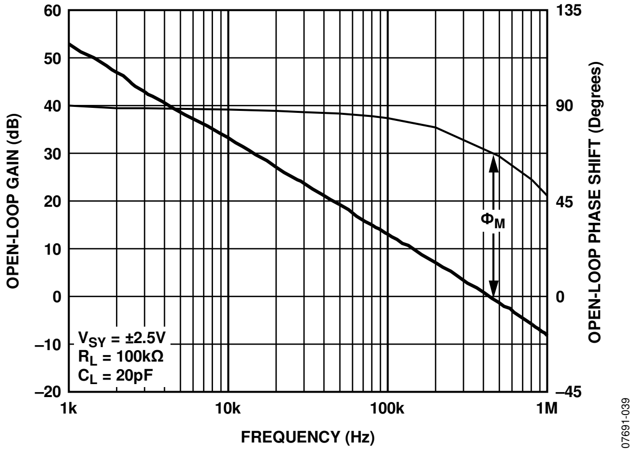


Figure 39. Amplifier Open-Loop Gain and Phase vs. Frequency

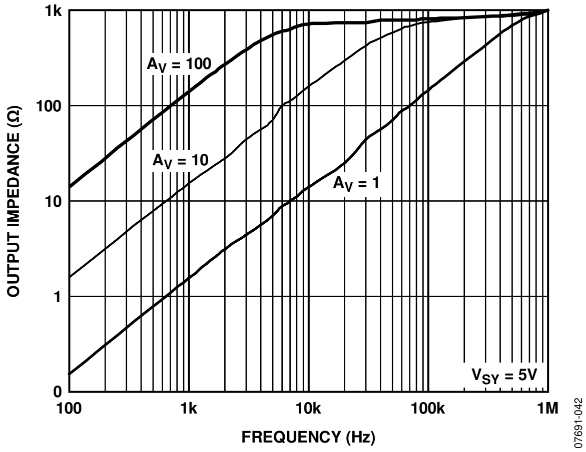


Figure 42. Amplifier Closed-Loop Output Impedance vs. Frequency

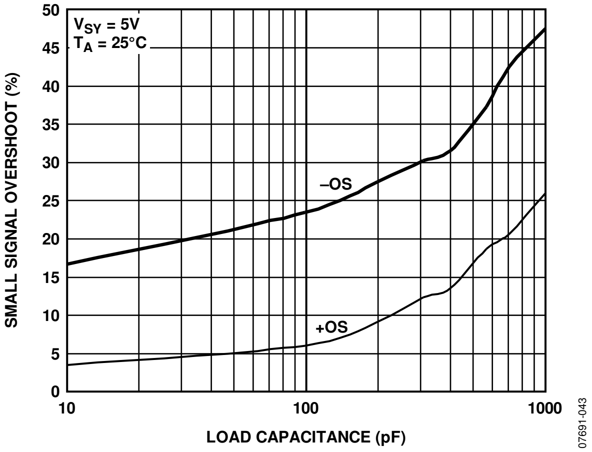


Figure 43. Small Signal Overshoot vs. Load Capacitance

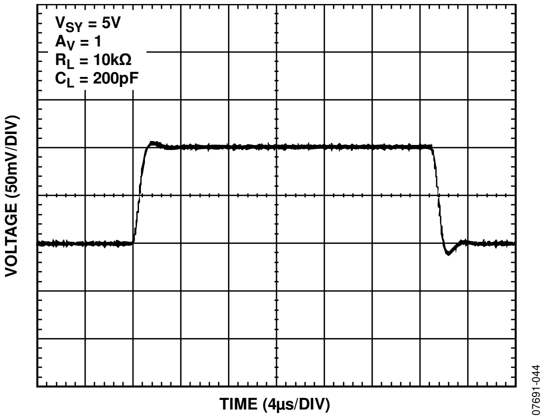


Figure 44. Amplifier Small Signal Transient Response

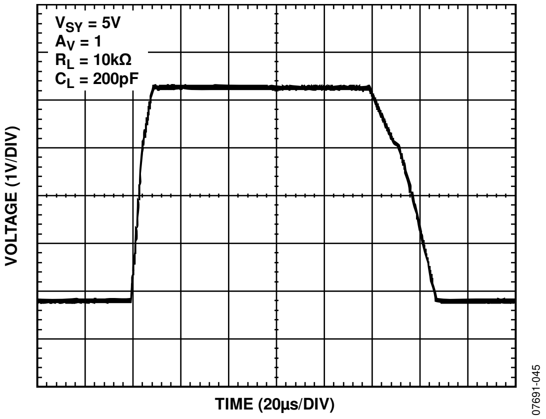


Figure 45. Amplifier Large Signal Transient Response

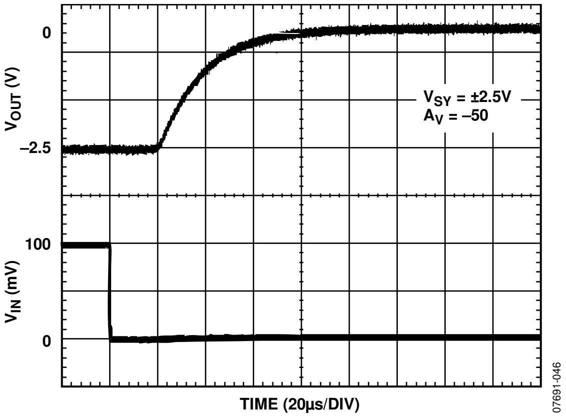


Figure 46. Amplifier Positive Overload Recovery

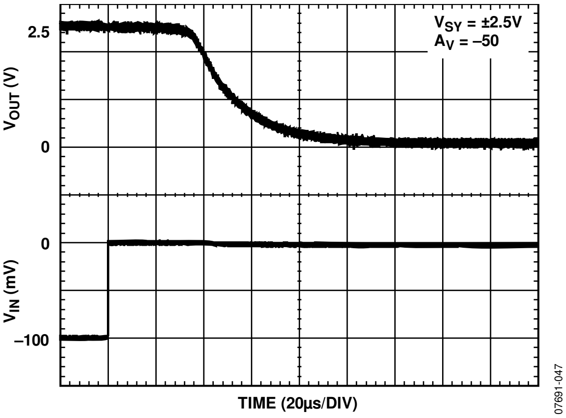


Figure 47. Amplifier Negative Overload Recovery

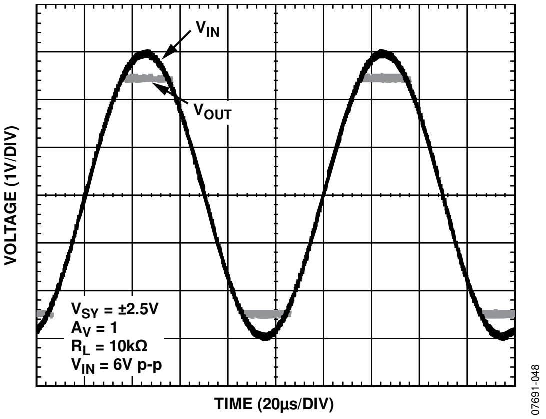


Figure 48. Amplifier, No Phase Reversal

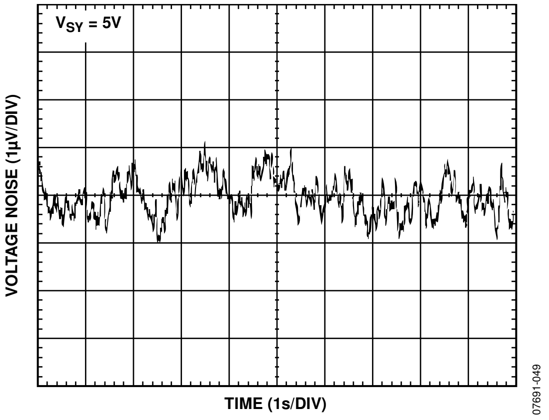


*Figure 49. Amplifier 0.1 Hz to 10 Hz Input Voltage Noise*

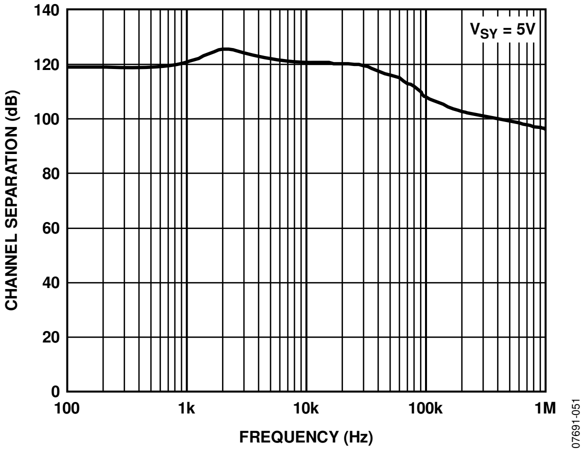


*Figure 51. Amplifier Channel Separation*

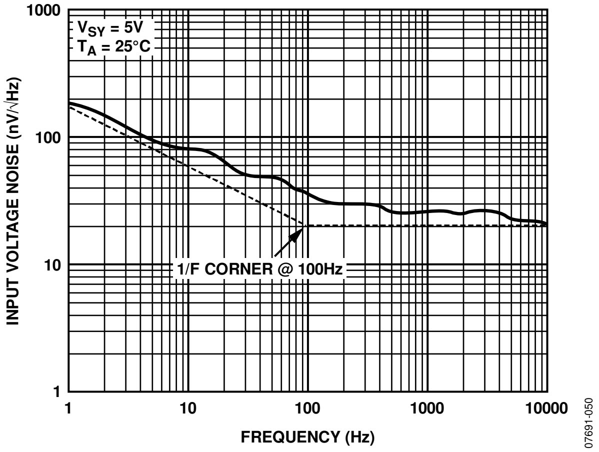


*Figure 50. Amplifier Voltage Noise Density*

# TERMINOLOGY

**DAC Integrated Nonlinearity**

For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function.

**DAC Differential Nonlinearity**

Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. The DAC is guaranteed monotonic by design.

**DAC Offset Error**

Offset error is a measure of the difference between the actual $V_{OUT}$ and the ideal $V_{OUT}$, expressed in millivolts in the linear region of the transfer function. It can be negative or positive and is expressed in millivolts.

**DAC Zero-Code Error**

Zero-code error is a measure of the output error when zero code (0x0000) is loaded into the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in millivolts.

**DAC Gain Error**

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range.

**DAC Zero-Code Error Drift**

Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in microvolts per degree Celsius.

**DAC Gain Error Drift**

Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in ppm of full-scale range per degree Celsius.

**DAC Full-Scale Error**

Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded into the DAC register. Ideally, the output should be $V_{DD}$ – 1 LSB. Full-scale error is expressed as a percentage of the full-scale range. Figure 10 shows a plot of typical full-scale error vs. temperature.

**DAC Digital-to-Analog Glitch Impulse**

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000).

**DAC DC Power Supply Rejection Ratio (PSRR)**

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in $V_{OUT}$ to a change in $DACV_{DD}$ for full-scale output of the DAC. It is measured in decibels. $V_{REFIN}$ is held at 2 V, and $DACV_{DD}$ is varied ±10%.

**DAC DC Crosstalk**

DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in microvolts.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in microvolts per milliamp.

**Reference Feedthrough**

Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, $\overline{\text{LDAC}}$ is high). It is expressed in decibels.

**DAC Digital Feedthrough**

Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device, but is measured when the DAC is not being written to ($\overline{\text{SYNC}}$ held high). It is specified in nV-sec and measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s or vice versa.

**DAC Digital Crosstalk**

Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s or vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

**DAC Analog Crosstalk**

Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s or vice versa) while keeping $\overline{\text{LDAC}}$ high, and then pulsing $\overline{\text{LDAC}}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nV-sec.

**DAC-to-DAC Crosstalk**

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s or vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-sec.

### Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

### DAC Total Harmonic Distortion (THD)

Total harmonic distortion is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in decibels.

### ADC Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

### ADC Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

### ADC Offset Error

This is the deviation of the first code transition (00…000 to 00…001) from the ideal, that is, ADCGND + 1 LSB.

### ADC Offset Error Match

This is the difference in offset error between any two channels.

### ADC Gain Error

This is the deviation of the last code transition (111…110 to 111…111) from the ideal (that is, $V_{REFA}$ − 1 LSB) after the offset error has been adjusted out.

### ADC Gain Error Match

This is the difference in gain error between any two channels.

### ADC Zero-Code Error

This applies when using the twos complement output coding option, in particular to the 2 × $V_{REFA}$ input range with−$V_{REFA}$ to +$V_{REFA}$ biased about the $V_{REFA}$ point. It is the deviation of the midscale transition (all 0s to all 1s) from the ideal $V_{IN}$ voltage, that is, $V_{REFA}$ − 1 LSB.

### ADC Zero-Code Error Match

This is the difference in ADC zero-code error between any two channels.

### ADC Positive Gain Error

This applies when using the twos complement output coding option, in particular to the 2 × $V_{REFA}$ input range with −$V_{REFA}$ to +$V_{REFA}$ biased about the $V_{REFA}$ point. It is the deviation of the last code transition (011…110 to 011…111) from the ideal (that is, +$V_{REFA}$ − 1 LSB) after the zero-code error has been adjusted out.

### ADC Positive Gain Error Match

This is the difference in ADC positive gain error between any two channels.

### ADC Negative Gain Error

This applies when using the twos complement output coding option, in particular to the 2 × $V_{REFA}$ input range with −$V_{REFA}$ to +$V_{REFA}$ biased about the $V_{REFA}$ point. It is the deviation of the first code transition (100…000 to 100…001) from the ideal (that is, −$V_{REFA}$ + 1 LSB) after the ADC zero-code error has been adjusted out.

### ADC Negative Gain Error Match

This is the difference in negative gain error between any two channels.

### ADC Channel-to-Channel Isolation

Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 400 kHz sine wave signal to all 15 nonselected input channels and determining how much that signal is attenuated in the selected channel with a 50 kHz signal. The figure is given worst case across all 16 channels for the ADC.

### ADC PSR (Power Supply Rejection)

Variations in power supply affect the full scale transition, but not the linearity of the converter. Power supply rejection is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value (see the Typical Performance Characteristics section).

### ADC Track-and-Hold Acquisition Time

The track-and-hold amplifier returns into track on the 14th ASCLK falling edge. Track-and-hold acquisition time is the minimum time required for the track-and-hold amplifier to remain in track mode for its output to reach and settle to within ±1 LSB of the applied input signal, given a step change to the input signal.

### ADC Signal-to-(Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the analog-to-digital converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal-to-(Noise+Distortion) = 6.02\,N + 1.76 \ \text{[dB]}$$

Thus, for a 12-bit converter, this is 74 dB.

### ADC Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the ADC, it is defined as

$$THD\text{[dB]} = 20 \times \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where $V_1$ is the rms amplitude of the fundamental and $V_2$, $V_3$, $V_4$, $V_5$, and $V_6$ are the rms amplitudes of the second through the sixth harmonics.