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8-Channel, 12-Bit, Configurable ADC/DAC with On-Chip Reference, SPI Interface

Data Sheet **AD5592R**

FEATURES

8-channel, configurable ADC/DAC/GPIO
Configurable as any combination of
- **8 × 12-bit DAC channels**
- **8 × 12-bit ADC channels**
- **8 × general-purpose digital input/output pins**

Integrated temperature sensor
SPI interface
Available in
- **16-ball, 2 mm × 2 mm WLCSP**
- **16-lead, 3 mm × 3 mm LFCSP**
- **16-lead TSSOP**

APPLICATIONS

Control and monitoring
General-purpose analog and digital inputs/outputs

GENERAL DESCRIPTION

The AD5592R/AD5592R-1 have eight I/Ox pins (I/O0 to I/O7) that can be independently configured as digital-to-analog converter (DAC) outputs, analog-to-digital converter (ADC) inputs, digital outputs, or digital inputs. When an I/Ox pin is configured as an analog output, it is driven by a 12-bit DAC. The output range of the DAC is 0 V to V_{REF} or 0 V to 2 × V_{REF}.

When an I/Ox pin is configured as an analog input, it is connected to a 12-bit ADC via an analog multiplexer. The input range of the ADC is 0 V to V_{REF} or 0 V to 2 × V_{REF}. The ADC has a total throughput rate of 400 kSPS. The I/Ox pins can also be configured as digital, general-purpose input or output (GPIO) pins. The state of the GPIO pins can be set or read back by accessing the GPIO write data register or the GPIO read configuration register, respectively, via a serial peripheral interface (SPI) write or read operation.

The AD5592R/AD5592R-1 have an integrated 2.5 V, 25 ppm/°C reference, which is turned off by default, and an integrated temperature indicator, which gives an indication of the die temperature. The temperature value is read back as part of an ADC read sequence.

The AD5592R/AD5592R-1 are available in 16-ball, 2 mm × 2 mm WLCSP, 16-lead, 3 mm × 3 mm LFCSP, and 16-lead TSSOP. The AD5592R/AD5592R-1 operate over a temperature range of −40°C to +105°C.

Table 1. Related Products

Part No.	Description
AD5593R	AD5592R equivalent with V_{LOGIC} and $\overline{RESET}$ pins and an I^2C interface

FUNCTIONAL BLOCK DIAGRAM

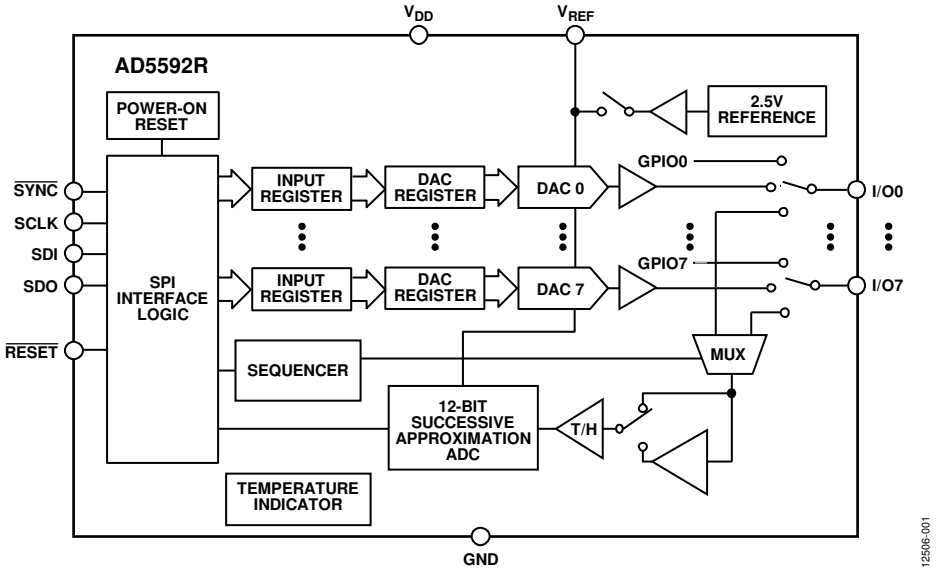

Figure 1. AD5592R Functional Block Diagram

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COMPARABLE PARTS

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EVALUATION KITS

- AD5592R Evaluation Board

DOCUMENTATION

Data Sheet

- AD5592R: 8-Channel, 12-Bit, Configurable ADC/DAC with On-Chip Reference, SPI Interface Data Sheet

User Guides

- UG-753: Evaluating the 8-Channel, 12-Bit, Configurable ADC/DAC/GPIO AD5592R with On-Chip Reference and SPI Interface
- UG-754: Evaluating the AD5592R-1 8-Channel, 12-Bit, Configurable ADC/DAC/GPIO

TOOLS AND SIMULATIONS

- AD5592R-1 Ibis Model

REFERENCE DESIGNS

- CN0229

DESIGN RESOURCES

- AD5592r Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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FUNCTIONAL BLOCK DIAGRAM (AD5592R-1)

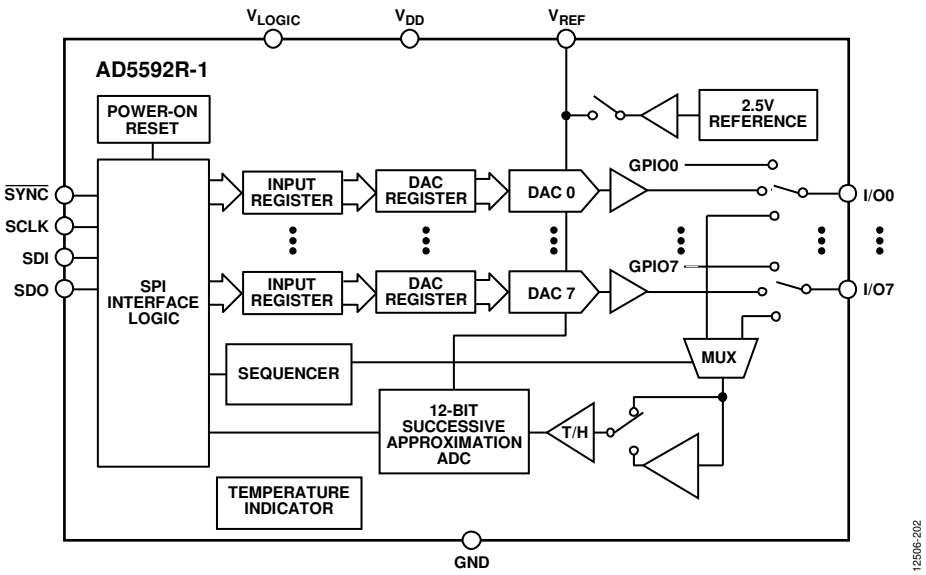

Figure 2. AD5592R-1 Functional Block Diagram

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, V_{REF} = 2.5 V (external), R_L = 2 kΩ to GND, C_L = 200 pF to GND, T_A = T_{MIN} to T_{MAX}, temperature range = −40°C to +105°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
ADC PERFORMANCE					f_{IN} = 10 kHz sine wave
Resolution		12		Bits	
Input Range	0		V_{REF}	V	When using the internal ADC buffer, there is a dead band of 0 V to 5 mV
	0		2 × V_{REF}	V	
Integral Nonlinearity (INL)	−2		+2	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	
Offset Error			±5	mV	
Gain Error			0.3	% FSR	
Throughput Rate[2]			400	kSPS	
Track Time (t_{TRACK})[2]	500			ns	
Conversion Time (t_{CONV})[2]			2	µs	
Signal-to-Noise Ratio (SNR)		69		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		67		dB	V_{DD} = 5.5 V, input range = 0 V to V_{REF}
		61		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Signal-to-Noise-and-Distortion (SINAD) Ratio		69		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		67		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		60		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Total Harmonic Distortion (THD)		−91		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		−89		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		−72		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Peak Harmonic or Spurious Noise (SFDR)		91		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		91		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		72		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Aperture Delay[2]		15		ns	V_{DD} = 3 V
		12		ns	V_{DD} = 5 V
Aperture Jitter[2]		50		ps	
Channel-to-Channel Isolation		−95		dB	f_{IN} = 5 kHz
Input Capacitance		45		pF	
Full Power Bandwidth		8.2		MHz	At 3 dB
		1.6		MHz	At 0.1 dB
DAC PERFORMANCE[3]					
Resolution		12		Bits	
Output Range	0		V_{REF}	V	
	0		2 × V_{REF}	V	
Integral Nonlinearity (INL)	−1		+1	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	
Offset Error	−3		+3	mV	
Offset Error Drift[2]		8		µV/°C	
Gain Error			±0.2	% FSR	Output range = 0 V to V_{REF}
			±0.1	% FSR	Output range = 0 V to 2 × V_{REF}
Zero Code Error		0.65	2	mV	
Total Unadjusted Error		±0.03	±0.25	% FSR	Output range = 0 V to V_{REF}
		±0.015	±0.1		Output range = 0 V to 2 × V_{REF}
Capacitive Load Stability[2]			2	nF	R_{LOAD} = ∞
			10	nF	R_{LOAD} = 1 kΩ
Resistive Load	1			kΩ	
Short-Circuit Current		25		mA	

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
DC Crosstalk[2]	−4		+4	µV	Due to single channel, full-scale output change
DC Output Impedance		0.2		Ω	
DC Power Supply Rejection Ratio (PSRR)[2]		0.15		mV/V	DAC code = midscale, V_{DD} = 3 V ± 10% or 5 V ± 10%
Load Impedance at Rails[4]		25		Ω	
Load Regulation		200		µV/mA	V_{DD} = 5 V ± 10%, DAC code = midscale, −10 mA ≤ I_{OUT} ≤ +10 mA
		200		µV/mA	V_{DD} = 3 V ± 10%, DAC code = midscale, −10 mA ≤ I_{OUT} ≤ +10 mA
Power-Up Time		7		µs	Coming out of power-down mode, V_{DD} = 5 V
AC SPECIFICATIONS					
Slew Rate		1.25		V/µs	Measured from 10% to 90% of full scale
Settling Time		6		µs	¼ scale to ¾ scale settling to 1 LSB
DAC Glitch Impulse		2		nV-sec	
DAC to DAC Crosstalk		1		nV-sec	
Digital Crosstalk		0.1		nV-sec	
Analog Crosstalk		1		nV-sec	
Digital Feedthrough		0.1		nV-sec	
Multiplying Bandwidth		240		kHz	DAC code = full scale, output range = 0 V to V_{REF}
Output Voltage Noise Spectral Density		200		nV/√Hz	DAC code = midscale, output range = 0 V to 2 × V_{REF}, measured at 10 kHz
Signal-to-Noise Ratio (SNR)		81		dB	
Peak Harmonic or Spurious Noise (SFDR)		77		dB	
Signal-to-Noise-and-Distortion (SINAD) Ratio		74		dB	
Total Harmonic Distortion (THD)		−76		dB	
REFERENCE INPUT					
V_{REF} Input Voltage	1		V_{DD}	V	
DC Leakage Current	−1		+1	µA	No I/Ox pins configured as DACs
Reference Input Impedance		12		kΩ	DAC output range = 0 V to 2 × V_{REF}
		24		kΩ	DAC output range = 0 V to V_{REF}
REFERENCE OUTPUT					
V_{REF} Output Voltage	2.495	2.5	2.505	V	At ambient
V_{REF} Temperature Coefficient		20		ppm/°C	
Capacitive Load Stability		5		µF	R_L = 2 kΩ
Output Impedance[2]		0.15		Ω	V_{DD} = 2.7 V
		0.7		Ω	V_{DD} = 5 V
Output Voltage Noise		10		µV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density		240		nV/√Hz	At ambient, f = 10 kHz, C_L = 10 nF
Line Regulation		20		µV/V	At ambient, sweeping V_{DD} from 2.7 V to 5.5 V
		10		µV/V	At ambient, sweeping V_{DD} from 2.7 V to 3.3 V
Load Regulation					
Sourcing		210		µV/mA	At ambient, −5 mA ≤ load current ≤ +5 mA
Sinking		120		µV/mA	At ambient, −5 mA ≤ load current ≤ +5 mA
Output Current Load Capability		±5		mA	V_{DD} ≥ 3 V
GPIO OUTPUT					
I_{SOURCE}, I_{SINK}		1.6		mA	
Output Voltage					
High (V_{OH})	V_{DD} − 0.2			V	I_{SOURCE} = 1 mA
Low (V_{OL})			0.4	V	I_{SOURCE} = 1 mA

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
GPIO INPUT					
Input Voltage					
High (V_{IH})	$0.7 \times V_{DD}$			V	
Low (V_{IL})			$0.3 \times V_{DD}$	V	
Input Capacitance		20		pF	
Hysteresis		0.2		V	
Input Current		±1		µA	
LOGIC INPUTS					
AD5592R Input Voltage					
High (V_{INH})	$0.7 \times V_{DD}$			V	
Low (V_{INL})			$0.3 \times V_{DD}$	V	
AD5592R-1 Input Voltage					
High (V_{INH})	$0.7 \times V_{LOGIC}$			V	
Low (V_{INL})			$0.3 \times V_{LOGIC}$	V	
Input Current (I_{IN})	−1		+1	µA	Typically 10 nA, $\overline{RESET}$ = 1 µA typical
Input Capacitance (C_{IN})			10	pF	
LOGIC OUTPUT (SDO)					
Output High Voltage (V_{OH})					
AD5592R	$V_{DD} - 0.2$			V	I_{SOURCE} = 200 µA, V_{DD} = 2.7 V to 5. 5 V
AD5592R-1	$V_{LOGIC} - 0.2$			V	I_{SOURCE} = 200 µA, V_{DD} = 2.7 V to 5. 5 V
Output Low Voltage (V_{OL})			0.4	V	I_{SINK} = 200 µA
Floating-State Output Capacitance		10		pF	
TEMPERATURE SENSOR[2]					
Resolution		12		Bits	
Operating Range	−40		+105	°C	
Accuracy		±3		°C	5 sample averaging
Track Time			5	µs	ADC buffer enabled
			20	µs	ADC buffer disabled
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD}			2.7	mA	Digital inputs = 0 V or V_{DD}, I/O0 to I/O7 configured as DACs and ADCs, internal reference on, ADC buffer on, DAC code = 0xFFF, range is 0 V to $2 \times V_{REF}$ for DACs and ADCs
Power-Down Mode			3.5	µA	
V_{DD} = 5 V (Normal Mode)		1.6		mA	I/O0 to I/O7 are DACs, internal reference, gain = 2
		1		mA	I/O0 to I/O7 are DACs, external reference, gain = 2
		2.4		mA	I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 2
		1.1		mA	I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 2
		1		mA	I/O0 to I/O7 are ADCs, internal reference, gain = 2
		0.75		mA	I/O0 to I/O7 are ADCs, external reference, gain = 2
		0.5		mA	I/O0 to I/O7 are general-purpose outputs
		0.5		mA	I/O0 to I/O7 are general-purpose inputs
		0.5		mA	I/O0 to I/O3 are general-purpose outputs, I/O4 to I/O7 are general-purpose inputs

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
V_{DD} = 3 V (Normal Mode)		1.1		mA	I/O0 to I/O7 are DACs, internal reference, gain = 1
		1		mA	I/O0 to I/O7 are DACs, external reference, gain = 1
		1.1		mA	I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 1
		0.78		mA	I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 1
		0.75		mA	I/O0 to I/O7 are ADCs, internal reference, gain = 1
		0.5		mA	I/O0 to I/O7 are ADCs, external reference, gain = 1
		0.45		mA	I/O0 to I/O7 are general-purpose outputs
		0.45		mA	I/O0 to I/O7 are general-purpose inputs
V_{LOGIC}	1.8		V_{DD}	V	AD5592R-1 only
I_{LOGIC}			3	µA	AD5592R-1 only

[1] All specifications expressed in decibels are referred to full-scale input (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise noted.
[2] Guaranteed by design and characterization; not production tested.
[3] DC specifications tested with the outputs unloaded, unless otherwise noted. Linearity calculated using a code range of 8 to 4095. There is an upper dead band of 10 mV when $V_{REF} = V_{DD}$.
[4] When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV (see Figure 33).

TIMING CHARACTERISTICS

Guaranteed by design and characterization, not production tested; all input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 3. AD5592R Timing Characteristics

Parameter	2.7 V ≤ V_{DD} < 3 V	3 V ≤ V_{DD} ≤ 5.5 V	Unit	Test Conditions/Comments
t_1	33	20	ns min	SCLK cycle time, write operation
	50	50	ns min	SCLK cycle time, read operation
t_2	16	10	ns min	SCLK high time
t_3	16	10	ns min	SCLK low time
t_4	15	10	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
	2	2	µs max	$\overline{SYNC}$ falling edge to SCLK falling edge setup time[1]
t_5	7	7	ns min	Data setup time
t_6	5	5	ns min	Data hold time
t_7	15	10	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	30	30	ns min	Minimum $\overline{SYNC}$ high time for register write operations
	60	60	ns min	Minimum $\overline{SYNC}$ high time for register read operations
t_9	0	0	ns min	$\overline{SYNC}$ rising edge to next SCLK falling edge
t_{10}	25	25	ns max	SCLK rising edge to SDO valid
t_{11}	250	250	ns min	$\overline{RESET}$ low pulse width (not shown in Figure 4)

[1] When reading an ADC conversion.

Table 4. AD5592R-1 Timing Characteristics

Parameter	1.8 V ≤ V_{LOGIC} < 3 V	3 V ≤ V_{LOGIC} ≤ 5.5 V	Unit	Test Conditions/Comments
t_1	33	20	ns min	SCLK cycle time, write operation
	50	50	ns min	SCLK cycle time, read operation
t_2	16	10	ns min	SCLK high time
t_3	16	10	ns min	SCLK low time
t_4	15	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
	2	2	µs max	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	7	7	ns min	Data setup time
t_6	5	5	ns min	Data hold time
t_7	15	10	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	30	30	ns min	Minimum $\overline{SYNC}$ high time for write operations
	60	60	ns min	Minimum $\overline{SYNC}$ high time for register read operations
t_9	0	0	ns min	$\overline{SYNC}$ rising edge to next SCLK falling edge
t_{10}	40	25	ns max	SCLK rising edge to SDO valid

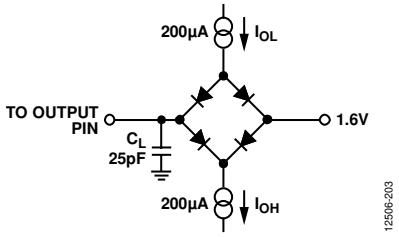

Figure 3. Load Circuit for Logic Output (SDO) Timing Specifications

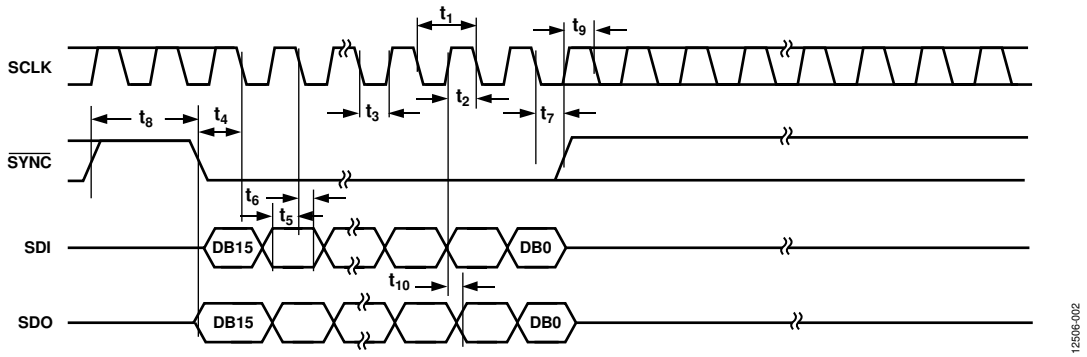

Figure 4. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to + 7 V
V_{LOGIC} to GND	−0.3 V to + 7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
AD5592R	
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
AD5592R-1	
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Ball WLCSP	60	°C/W
16-Lead LFCSP	137	°C/W
16-Lead TSSOP	112	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

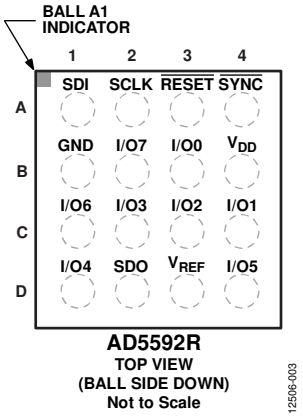

Figure 5. AD5592R 16-Ball WLCSP Pin Configuration

Table 7. AD5592R 16-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	SDI	Data In. Logic input. Data that is to be written to the DACs and control registers is provided on this input and is clocked into the register on the falling edge of SCLK.
A2	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz when writing to the DACs. SCLK has a maximum speed of 20 MHz when performing a conversion or clocking data from the AD5592R.
A3	$\overline{\text{RESET}}$	Asynchronous Reset Pin. Tie this pin high for normal operation. When this pin is brought low, the AD5592R is reset to its default configuration.
A4	$\overline{\text{SYNC}}$	Synchronization. Active low control input. $\overline{\text{SYNC}}$ is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, data is transferred in on the falling edges of the next 16 clocks.
B1	GND	Ground Reference Point for All Circuitry on the AD5592R.
B2	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. The function of this pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16). I/O7 can also be configured as a $\overline{\text{BUSY}}$ signal to indicate when an ADC conversion is taking place (see Table 30 and Table 31).
B3, C4, C3, C2, D1, D4, C1	I/O0 to I/O6	Input/Output 0 Through Input/Output 6. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16).
B4	V_{DD}	Power Supply Input. The AD5592R operates from 2.7 V to 5.5 V, and this pin must be decoupled with a 0.1 µF capacitor to GND.
D2	SDO	Data Out. Logic output. The conversion results from the ADC, register reads, and temperature sensor information are provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The MSB is placed on the SDO pin on the falling edge of $\overline{\text{SYNC}}$. Because the SCLK can idle high or low, the next bit is clocked out on the first rising edge of SCLK that follows a falling edge SCLK while $\overline{\text{SYNC}}$ is low (see Figure 4).
D3	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on this pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5592R. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.

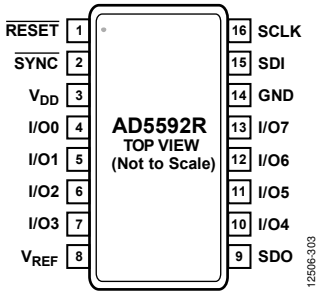

Figure 6. AD5592R 16-Lead TSSOP Pin Configuration

Table 8. AD5592R 16-Lead TSSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
15	SDI	Data In. Logic input. Data that is to be written to the DACs and control registers is provided on this input and is clocked into the register on the falling edge of SCLK.
16	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz when writing to the DACs. SCLK has a maximum speed of 20 MHz when performing a conversion or clocking data from the AD5592R.
1	$\overline{\text{RESET}}$	Asynchronous Reset Pin. Tie this pin high for normal operation. When this pin is brought low, the AD5592R is reset to its default configuration.
2	$\overline{\text{SYNC}}$	Synchronization. Active low control input. $\overline{\text{SYNC}}$ is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, data is transferred in on the falling edges of the next 16 clocks.
14	GND	Ground Reference Point for All Circuitry on the AD5592R.
13	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. The function of this pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16). I/O7 can also be configured as a $\overline{\text{BUSY}}$ signal to indicate when an ADC conversion is taking place (see Table 30 and Table 31).
4, 5, 6, 7, 10, 11, 12	I/O0 to I/O6	Input/Output 0 Through Input/Output 6. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16).
3	V_{DD}	Power Supply Input. The AD5592R operates from 2.7 V to 5.5 V, and this pin must be decoupled with a 0.1 µF capacitor to GND.
9	SDO	Data Out. Logic output. The conversion results from the ADC, register reads, and temperature sensor information are provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The MSB is placed on the SDO pin on the falling edge of $\overline{\text{SYNC}}$. Because the SCLK can idle high or low, the next bit is clocked out on the first rising edge of SCLK that follows a falling edge SCLK while $\overline{\text{SYNC}}$ is low (see Figure 4).
8	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on this pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5592R. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.

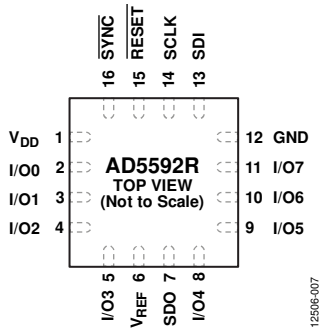

Figure 7. AD5592R 16-Lead LFCSP Pin Configuration

Table 9. AD5592R 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The AD5592R operates from 2.7 V to 5.5 V, and this pin must be decoupled with a 0.1 µF capacitor to GND.
2, 3, 4, 5, 8, 9, 10	I/O0 to I/O6	Input/Output 0 Through Input/Output 6. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16).
6	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on this pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5592R. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.
7	SDO	Data Out. Logic output. The conversion results from the ADC, register reads, and temperature sensor information are provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The MSB is placed on the SDO pin on the falling edge of $\overline{SYNC}$. Because the SCLK can idle high or low, the next bit is clocked out on the first rising edge of SCLK that follows a falling edge SCLK while $\overline{SYNC}$ is low (see Figure 4).
11	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. The function of this pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16). I/O7 can also be configured as a $\overline{BUSY}$ signal to indicate when an ADC conversion is taking place (see Table 30 and Table 31).
12	GND	Ground Reference Point for All Circuitry on the AD5592R.
13	SDI	Data In. Logic input. Data that is to be written to the DACs and control registers is provided on this input and is clocked into the register on the falling edge of SCLK.
14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz when writing to the DACs. SCLK has a maximum speed of 20 MHz when performing a conversion or clocking data from the AD5592R.
15	$\overline{RESET}$	Asynchronous Reset Pin. Tie this pin high for normal operation. When this pin is brought low, the AD5592R is reset to its default configuration.
16	$\overline{SYNC}$	Synchronization. Active low control input. $\overline{SYNC}$ is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, data is transferred in on the falling edges of the next 16 clocks.

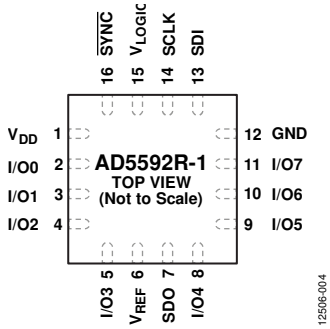

Figure 8. AD5592R-1 16-Lead LFCSP Pin Configuration

Table 10. AD5592R-1 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The AD5592R-1 operates from 2.7 V to 5.5 V, and this pin must be decoupled with a 0.1 µF capacitor to GND.
2 to 5, 8 to 10	I/O0 to I/O6	Input/Output 0 Through Input/Output 6. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16).
6	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on this pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5592R-1. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.
7	SDO	Data Out. Logic output. The conversion results from the ADC, register reads, and temperature sensor information are provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The MSB is placed on the SDO pin on the falling edge of $\overline{SYNC}$. Because the SCLK can idle high or low, the next bit is clocked out on the first rising edge of SCLK that follows a falling edge SCLK while $\overline{SYNC}$ is low (see Figure 4).
11	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. The function of this pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16). I/O7 can also be configured as a $\overline{BUSY}$ signal to indicate when an ADC conversion is taking place (see Table 30 and Table 31).
12	GND	Ground Reference Point for All Circuitry on the AD5592R-1.
13	SDI	Data In. Logic input. Data to be written to the DACs and control registers is provided on this input and is clocked into the register on the falling edge of SCLK.
14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz when writing to the DACs. SCLK has a maximum speed of 20 MHz when performing a conversion or clocking data from the AD5592R-1.
15	V_{LOGIC}	Interface Power Supply. The voltage of this pin ranges from 1.8 V to 5.5 V.
16	$\overline{SYNC}$	Synchronization. Active low control input. $\overline{SYNC}$ is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, data is transferred in on the falling edges of the next 16 clocks.

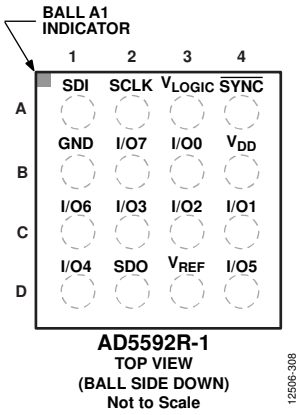

Figure 9. AD5592R-1 16-Ball WLCSP Pin Configuration

Table 11. AD5592R-1 16-Lead WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
B4	V_{DD}	Power Supply Input. The AD5592R-1 operates from 2.7 V to 5.5 V, and this pin must be decoupled with a 0.1 µF capacitor to GND.
B3, C4, C3, C2, D1, D4, C1	I/O0 to I/O6	Input/Output 0 Through Input/Output 6. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16).
D3	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on this pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5592R-1. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.
D2	SDO	Data Out. Logic output. The conversion results from the ADC, register reads, and temperature sensor information are provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The MSB is placed on the SDO pin on the falling edge of $\overline{SYNC}$. Because the SCLK can idle high or low, the next bit is clocked out on the first rising edge of SCLK that follows a falling edge SCLK while $\overline{SYNC}$ is low (see Figure 4).
B2	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. The function of this pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16). I/O7 can also be configured as a $\overline{BUSY}$ signal to indicate when an ADC conversion is taking place (see Table 30 and Table 31).
B1	GND	Ground Reference Point for All Circuitry on the AD5592R-1.
A1	SDI	Data In. Logic input. Data to be written to the DACs and control registers is provided on this input and is clocked into the register on the falling edge of SCLK.
A2	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz when writing to the DACs. SCLK has a maximum speed of 20 MHz when performing a conversion or clocking data from the AD5592R-1.
A3	V_{LOGIC}	Interface Power Supply. The voltage of this pin ranges from 1.8 V to 5.5 V.
A4	$\overline{SYNC}$	Synchronization. Active low control input. $\overline{SYNC}$ is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, data is transferred in on the falling edges of the next 16 clocks.

TYPICAL PERFORMANCE CHARACTERISTICS

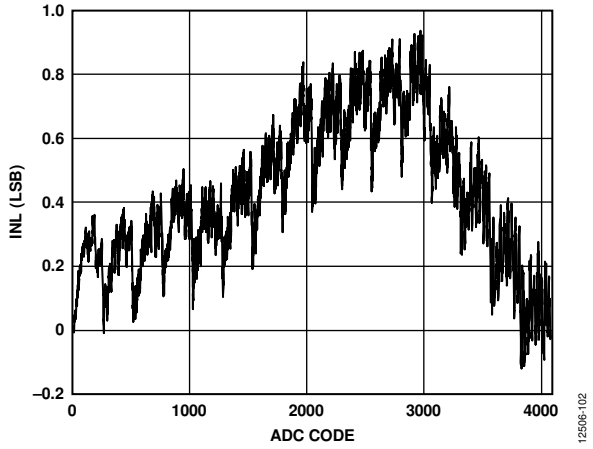

Figure 10. ADC INL, V_{DD} = 5.5 V

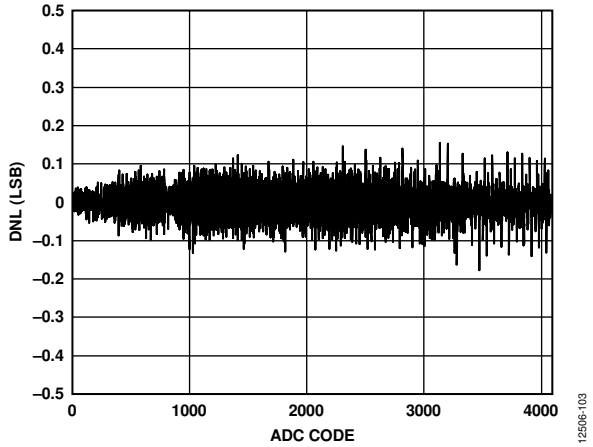

Figure 11. ADC DNL, V_{DD} = 5.5 V

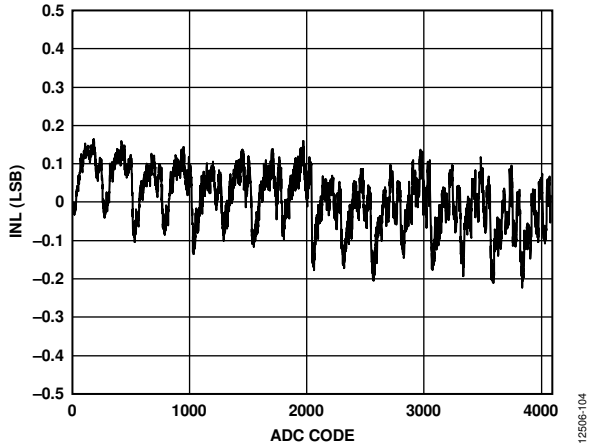

Figure 12. ADC INL, V_{DD} = 2.7 V

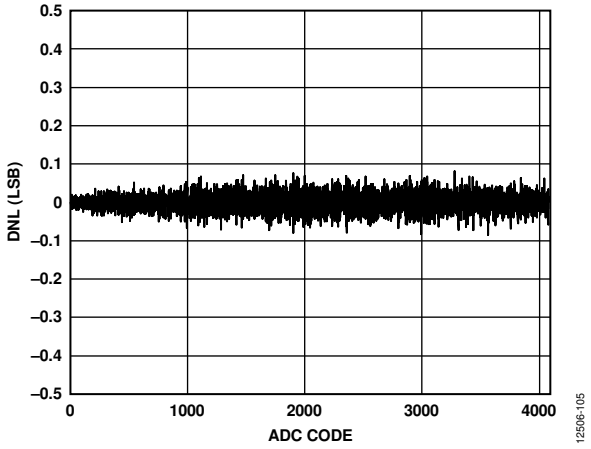

Figure 13. ADC DNL, V_{DD} = 2.7 V

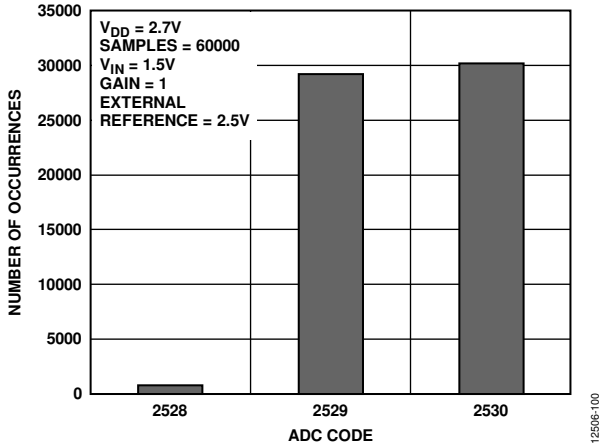

Figure 14. Histogram of ADC Codes, V_{DD} = 2.7 V

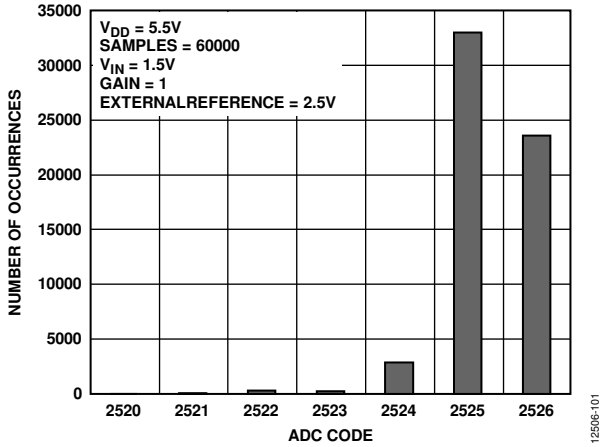

Figure 15. Histogram of ADC Codes, V_{DD} = 5.5 V

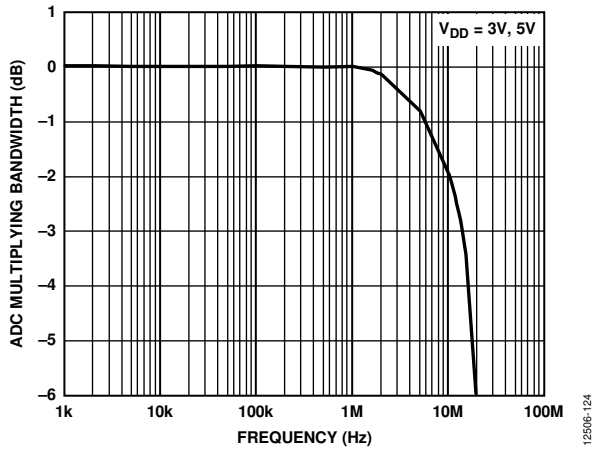

Figure 16. ADC Multiplying Bandwidth

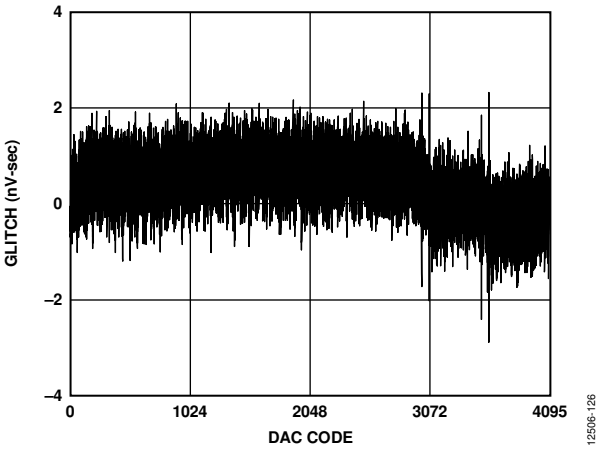

Figure 19. DAC Adjacent Code Glitch

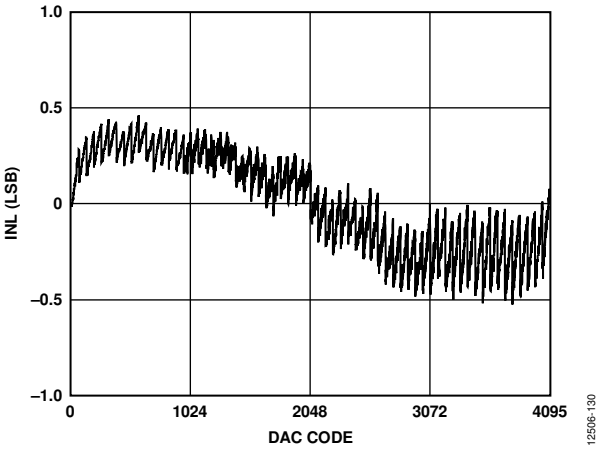

Figure 17. DAC INL

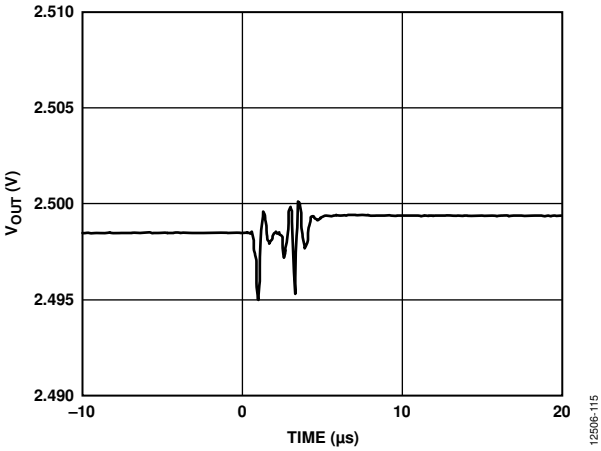

Figure 20. DAC Digital-to-Analog Glitch (Rising)

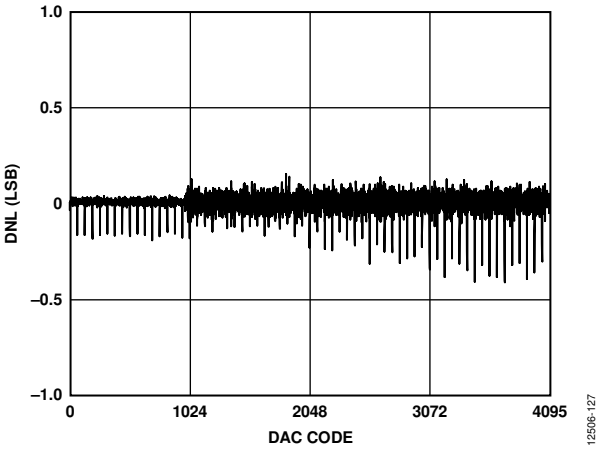

Figure 18. DAC DNL

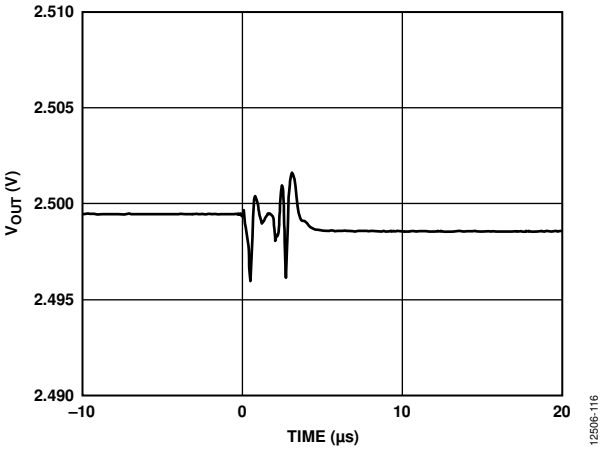

Figure 21. DAC Digital-to-Analog Glitch (Falling)

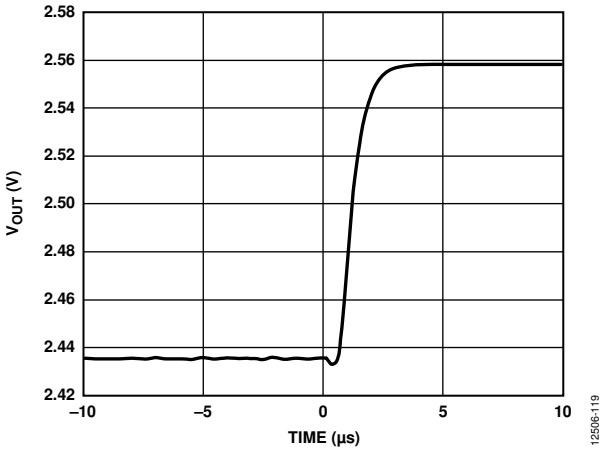

Figure 22. DAC Settling Time (100 Code Change, Rising Edge)

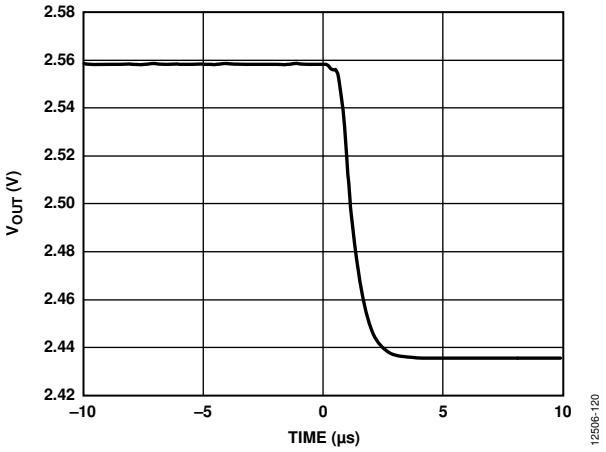

Figure 23. DAC Settling Time (100 Code Change, Falling Edge)

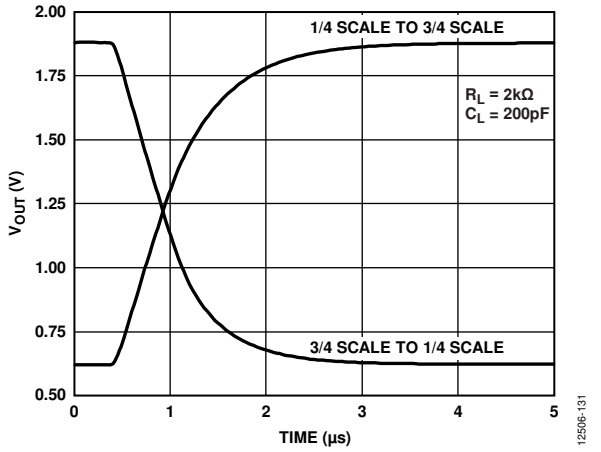

Figure 24. DAC Settling Time, Output Range = 0 V to V_{REF}

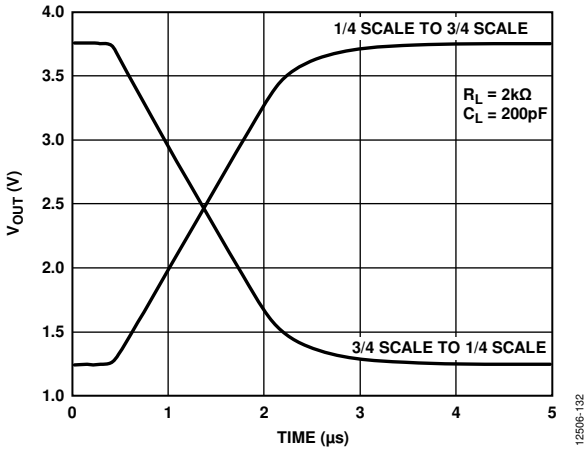

Figure 25. DAC Settling Time, Output Range = 0 V to 2 × V_{REF}

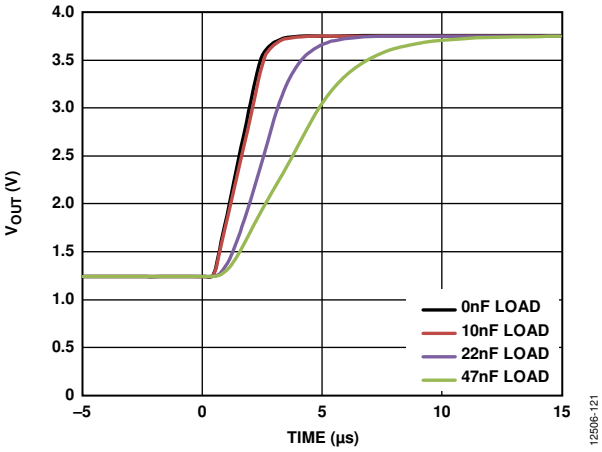

Figure 26. DAC Settling Time for Various Capacitive Loads

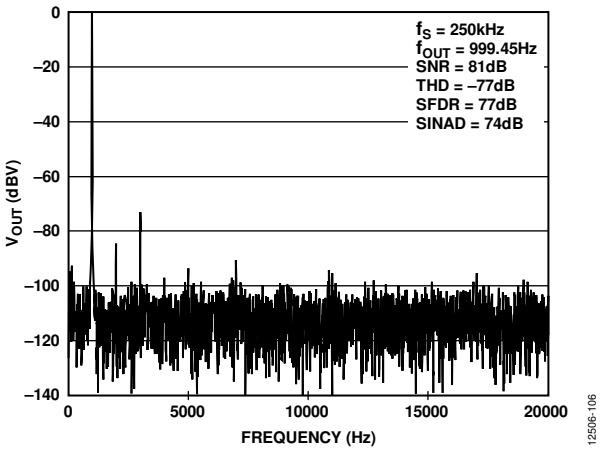

Figure 27. DAC Sine Wave Output, Output Range = 0 V to 2 × V_{REF}, Bandwidth = 0 Hz to 20 kHz

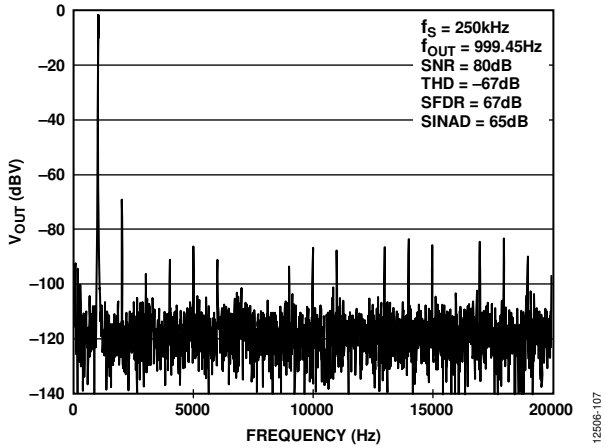

Figure 28. DAC Sine Wave Output, Output Range = 0 V to V_{REF}, Bandwidth = 0 Hz to 20 kHz

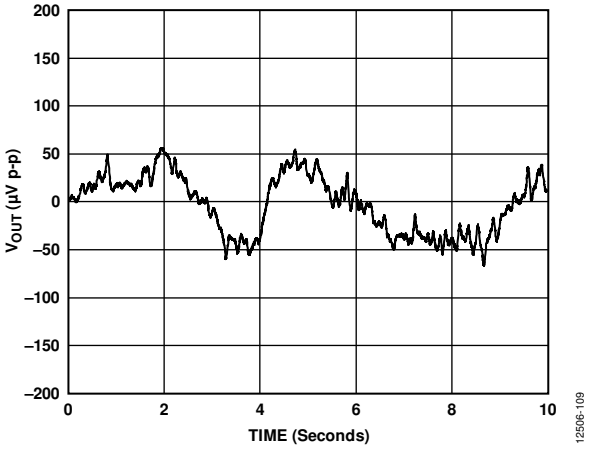

Figure 29. DAC 1/f Noise with External Reference

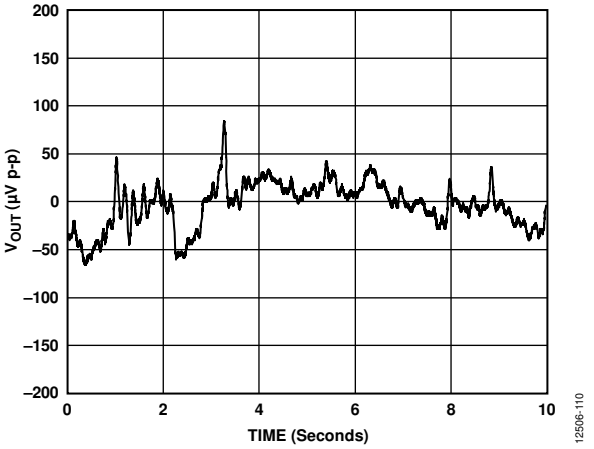

Figure 30. DAC 1/f Noise with Internal Reference

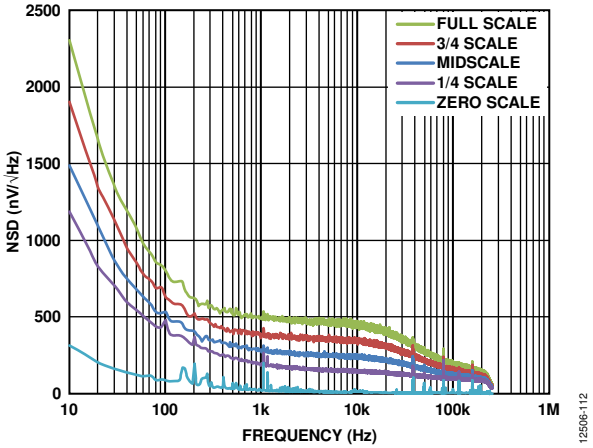

Figure 31. DAC Output Noise Spectral Density (NSD)

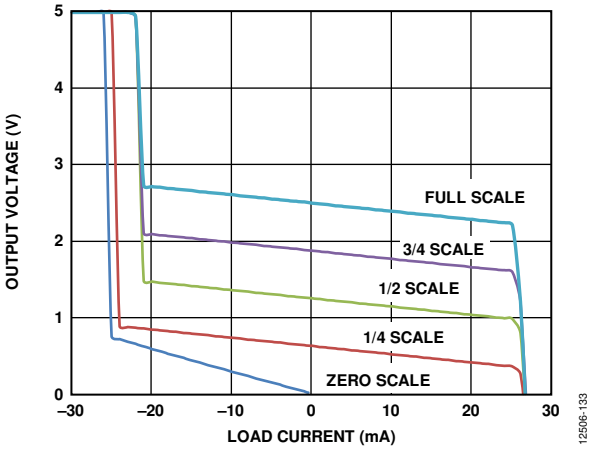

Figure 32. DAC Output Sink and Source Capability, Output Range = 0 V to V_{REF}

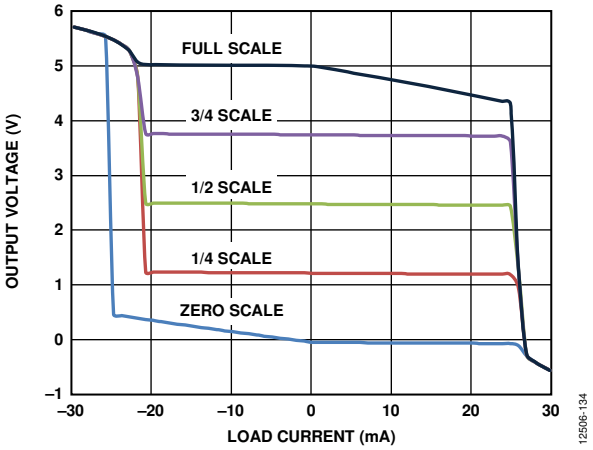

Figure 33. DAC Output Sink and Source Capability, Output Range = 0 V to 2 × V_{REF}

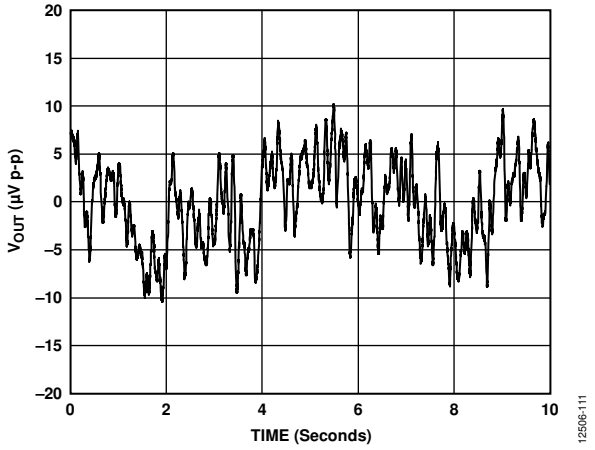

Figure 34. Internal Reference 1/f Noise

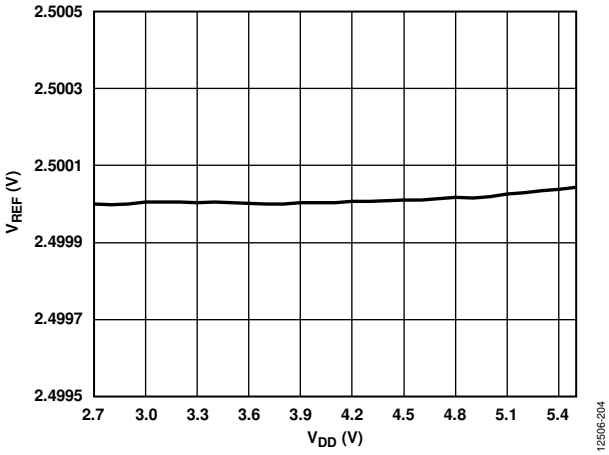

Figure 36. Reference Line Regulation

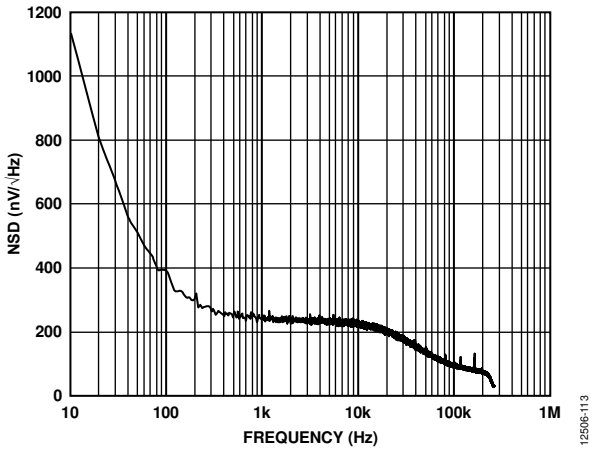

Figure 35. Reference Noise Spectral Density (NSD)

TERMINOLOGY

ADC TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The end-points of the transfer function are zero scale, a point that is 1 LSB below the first code transition, and full scale, a point that is 1 LSB above the last code transition.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
Offset error is the deviation of the first code transition (00 … 000) to (00 … 001) from the ideal, that is, AGND + 1 LSB.

Offset Error Match
Offset error match is the difference in offset error between any two channels.

Gain Error
Gain error is the deviation of the last code transition (111 … 110) to (111 … 111) from the ideal (that is, V_{REF} − 1 LSB) after the offset error has been adjusted out.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale, 5 kHz sine wave signal to all nonselected ADC input channels and determining how much that signal is attenuated in the selected channel. This specification is the worst case across all ADC channels for the AD5592R/AD5592R-1.

Track-and-Hold Acquisition Time
The track-and-hold amplifier enters hold mode on the falling edge of $\overline{\text{SYNC}}$ and returns to track mode when the conversion is complete. The track-and-hold acquisition time is the minimum time required for the track-and-hold amplifier to remain in track mode for its output to reach and settle to within ±1 LSB of the applied input signal, given a step change to the input signal.

Signal-to-Noise-and-Distortion (SINAD) Ratio
SINAD is the measured ratio of signal-to-noise-and-distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical SINAD ratio for an ideal N-bit converter with a sine wave input is given by

$$SINAD\ (\text{dB}) = 6.02N + 1.76$$

Thus, for a 12-bit converter, SINAD is 74 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD5592R/AD5592R-1, it is defined as

$$THD\ (\text{dB}) = 20 \times \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise (SFDR)
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

DAC TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 17.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 18.

Zero Code Error
Zero code error is a measurement of the output error when zero code (0x000) is loaded to the DAC register. Ideally, the output is 0 V. The zero code error is always positive in the AD5592R/AD5592R-1 because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero code error is expressed in mV.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % FSR.

Offset Error Drift
Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in μV/°C.

Gain Temperature Coefficient
Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error
Offset error is a measurement of the difference between V_{OUT} (actual) and V_{OUT} (ideal), expressed in mV, in the linear region of the transfer function. Offset error can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for a full-scale output of the DAC. It is measured in mV/V. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the rising edge of $\overline{SYNC}$.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FF to 0x800).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Noise Spectral Density
Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC maintained at midscale. It is expressed in μV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in μV/mA.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa), then executing a software LDAC (see Table 45 and Table 46), and monitoring the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth; the multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The voltage reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows:

$$TC = \left[\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(NOM)} \times Temp\ Range} \right] \times 10^6$$

where:

$V_{REF(MAX)}$ is the maximum reference output measured over the total temperature range.

$V_{REF(MIN)}$ is the minimum reference output measured over the total temperature range.

$V_{REF(NOM)}$ is the nominal reference output voltage, 2.5 V.

Temp Range is the specified temperature range of −40°C to +105°C.

THEORY OF OPERATION

The AD5592R/AD5592R-1 are 8-channel configurable analog and digital input/output ports. The AD5592R/AD5592R-1 have eight pins that can be independently configured as a 12-bit DAC output channel, a 12-bit ADC input channel, a digital input pin, or a digital output pin.

The function of each pin is determined by programming the ADC, DAC, or GPIO configuration registers as appropriate. See the Configuring the AD5592R/AD5592R-1 section and Table 16 for more information.

DAC SECTION

The AD5592R/AD5592R-1 contain eight 12-bit DACs and implement a segmented string DAC architecture with an internal output buffer. Figure 37 shows the internal block diagram of the DAC architecture.

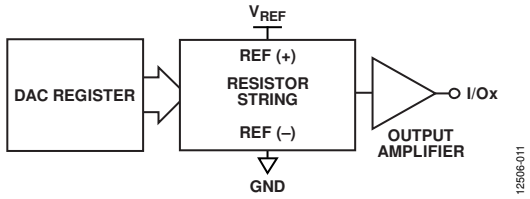

Figure 37. Internal Block Diagram of the DAC Architecture

The DAC channels have a shared gain bit that sets the output range as 0 V to V_{REF} or 0 V to 2 × V_{REF}. Because the gain bit is shared by all channels, it is not possible to set different output ranges on a per channel basis. The input coding to the DAC is straight binary. The ideal output voltage is given by

$$V_{OUT} = G \times V_{REF} \times \left(\frac{D}{2^N} \right)$$

where:
D is the decimal equivalent of the binary code (0 to 4095) that is loaded to the DAC register.
G = 1 for an output range of 0 V to V_{REF}, or G = 2 for an output range of 0 V to 2 × V_{REF}.
N = 12.

Resistor String

The simplified segmented resistor string DAC structure is shown in Figure 38. The code loaded to the DAC register determines the switch on the string that is connected to the output buffer.

Because each resistance in the string has the same value, R, the string DAC is guaranteed monotonic.

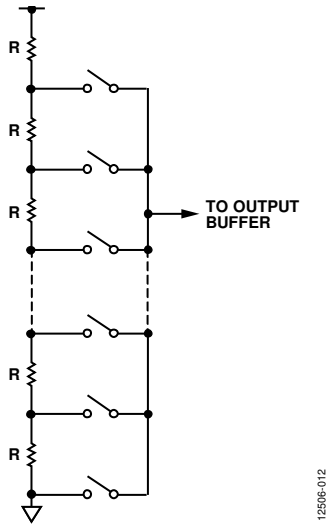

Figure 38. Simplified Resistor String Structure

Output Buffer

The output buffer is designed as an input/output rail-to-rail buffer. The output buffer can drive 2 nF capacitance with a 1 kΩ resistor in parallel. The slew rate is 1.25 V/µs with a ¼ to ¾ scale settling time of 6 µs. By default, the DAC outputs update directly after data has been written to the input register. The LDAC register is used to delay the updates until additional channels have been written to, if required. See the Readback and LDAC Mode Register section for more information.

ADC SECTION

The 12-bit, single-supply ADC is capable of throughput rates of 400 kSPS. The ADC is preceded by a multiplexer that switches selected I/Ox pins to the ADC. A sequencer is included to automatically switch the multiplexer to the next selected channel. Channels are selected for conversion by writing to the ADC sequence register. When the write to the ADC sequence register has completed, the first channel in the conversion sequence is put into track mode. Allow each channel to track the input signal for a minimum of 500 ns. The first $\overline{\text{SYNC}}$ falling edge following the write to the ADC sequence register begins the conversion of the first channel in the sequence. The next $\overline{\text{SYNC}}$ falling edge starts a conversion on the second channel in the sequence and also begins to clock the first ADC result onto the serial interface. ADC data is clocked out of the AD5592R in a 16-bit frame. D15 is 0 to indicate that the data contains ADC data, D14 to D12 is the binary representation of the ADC address, and D11 to D0 is the ADC result (see Table 12).

Each conversion takes 2 µs, and the conversion must be completed before another conversion is initiated. Only write to the AD5592R/AD5592R-1 when no conversion is taking place. I/O7 can be configured as a $\overline{\text{BUSY}}$ signal to indicate when a conversion is taking place. $\overline{\text{BUSY}}$ goes low while a conversion is in progress, and high when an ADC result is available. The ADC has an input range selection bit (Bit D5 in the general-purpose control register), which sets the input range as 0 V to V_{REF} or 0 V to 2 × V_{REF}. All input channels share the same range. The output coding of the ADC is straight binary. It is possible to set each I/Ox pin as both a DAC and an ADC. When an I/Ox pin is set as both a DAC and an ADC, the primary function is that of the DAC. If the pin is selected for inclusion in an ADC conversion sequence, the voltage on the pin is converted and made available via the serial interface, allowing the DAC voltage to be monitored.

Calculating ADC Input Current

The current flowing into the I/Ox pins configured as ADC inputs vary with the sampling rate (f_S), the voltage difference between successive channels (V_{DIFF}), and whether buffered or unbuffered mode is used. Figure 39 shows a simplified version of the ADC input structure. When a new channel is selected for conversion, the 5.8 pF capacitor must be charged or discharged of the voltage that was on the previously selected channel. The time required by the charge or discharge depends on the voltage difference between the two channels. This affects the input impedance of the multiplexer and therefore the input current flowing into the I/Ox pins. In buffered mode, Switch S1 is open and Switch S2 is closed, in which case the U1 buffer is directly driving the 23.1 pF capacitor, and its charging time is negligible. In unbuffered mode, Switch S1 is closed and Switch S2 is closed. In unbuffered mode, the 23.1 pF capacitor must be charged from the I/Ox pins, which contributes to the input current. For applications where the ADC input current is too high, an external input buffer may be required. The choice of buffer is a function of the particular application.

Calculate the input current for buffered mode as follows:

$$f_S \times C \times V_{DIFF} + 1 \text{ nA}$$

where:
f_S is the ADC sample rate in Hertz.
C is the sampling capacitance in Farads.
V_{DIFF} is the voltage change between successive channels.
1 nA is the dc leakage current associated with buffered mode.

Calculate the input current for unbuffered mode as follows:

$$f_S \times C \times V_{DIFF}$$

An example solution is as follows: for the ADC input current in buffered mode, where I/O0 = 0.5 V, I/O1 = 2 V, and f_S = 10 kHz,

$$(10{,}000 \times 5.8 \times 10^{-12} \times 1.5) + 1 \text{ nA} = 88 \text{ nA}$$

Under the same conditions, the ADC input current in unbuffered mode is as follows:

$$(10{,}000 \times 28.9 \times 10^{-12} \times 1.5) = 433.5 \text{ nA}$$

Table 12. ADC Conversion Format

MSB				LSB
D15	**D14**	**D13**	**D12**	**D11 to D0**
0	ADC address			12-bit ADC data

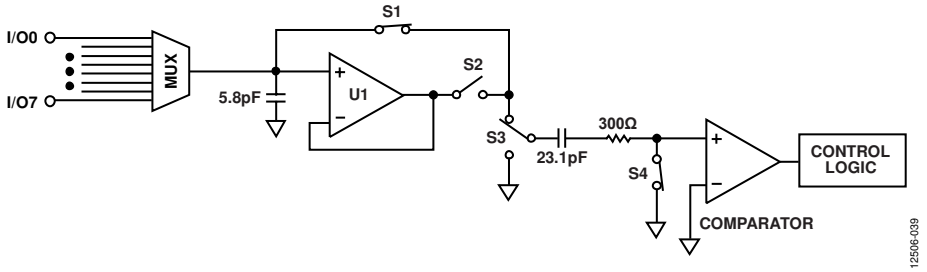

Figure 39. ADC Input Structure