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Single, 12-/14-/16-Bit *nano*DAC with 5 ppm/°C On-Chip Reference in SOT-23

Data Sheet

AD5620/AD5640/AD5660

FEATURES

- Low power, single *nano*DACs
  - AD5660: 16 bits
  - AD5640: 14 bits
  - AD5620: 12 bits
- 12-bit accuracy guaranteed
- On-chip, 1.25 V/2.5 V, 5 ppm/°C reference
- Tiny 8-lead SOT-23, MSOP, and LFCSP packages
- Power-down to 480 nA @ 5 V, 200 nA @ 3 V
- 3 V/5 V single power supply
- Guaranteed 16-bit monotonic by design
- Power-on reset to zero/midscale
- 3 power-down functions
- Serial interface with Schmitt-triggered inputs
- Rail-to-rail operation
- $\overline{\text{SYNC}}$ interrupt facility

APPLICATIONS

- Process control
- Data acquisition systems
- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
- Programmable attenuators

PRODUCT HIGHLIGHTS

1. 12-/14-/16-bit *nano*DAC—12-bit accuracy guaranteed.
2. On-chip, 1.25 V/2.5 V, 5 ppm/°C reference.
3. Available in 8-lead SOT-23, MSOP, and LFCSP packages.
4. Power-on reset to 0 V or midscale.
5. 10 µs settling time.

Table 1. Related Device

Part No.	Description
AD5662	2.7 V to 5.5 V, 16-bit DAC in SOT-23, LFCSP, and MSOP, external reference

FUNCTIONAL BLOCK DIAGRAM

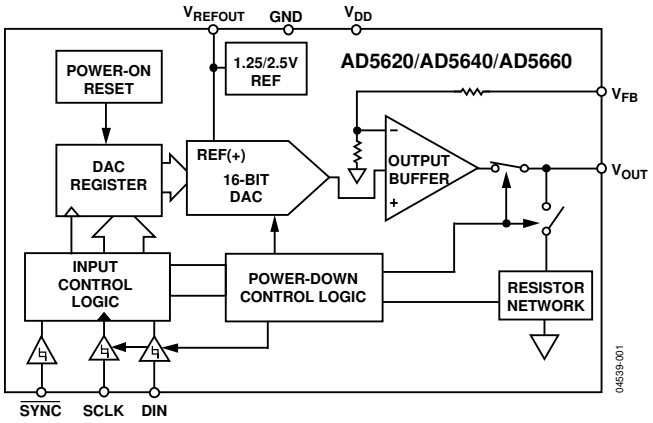

Figure 1.

GENERAL DESCRIPTION

The AD5620/AD5640/AD5660, members of the *nano*DAC™ family of devices, are low power, single, 12-/14-/16-bit, buffered voltage-out DACs and are guaranteed monotonic by design.

The AD5620/AD5640/AD5660-1 parts include an internal, 1.25 V, 5 ppm/°C reference, giving a full-scale output voltage range of 2.5 V. The AD5620/AD5640/AD5660-2-3 parts include an internal, 2.5 V, 5 ppm/°C reference, giving a full-scale output voltage range of 5 V. The reference associated with each part is available at the V_{REFOUT} pin.

The parts incorporate a power-on reset circuit to ensure that the DAC output powers up to 0 V (AD5620/AD5640/AD5660-1-2) or midscale (AD5620-3 and AD5660-3) and remains there until a valid write takes place. The parts contain a power-down feature that reduces the current consumption of the device to 480 nA at 5 V and provides software-selectable output loads while in power-down mode. The power consumption is 2.5 mW at 5 V, reducing to 1 µW in power-down mode.

The AD5620/AD5640/AD5660 on-chip precision output amplifier allows rail-to-rail output swing to be achieved. For remote sensing applications, the output amplifier's inverting input is available to the user. The AD5620/AD5640/AD5660 use a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

Rev. G

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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Updated Formatted ... Universal
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9/05—Rev. 0 to Rev. A

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7/05—Revision 0: Initial Version

SPECIFICATIONS

AD5620/AD5640/AD5660-2-3

V_{DD} = 4.5 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, C_{REFOUT} = 100 nF; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	A Grade[1]	B Grade[1]	C Grade[1]	Unit	Conditions/Comments
STATIC PERFORMANCE[2]					
AD5660					
Resolution	16	16	16	Bits min	
Relative Accuracy	±32	±16	±16	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	Guaranteed monotonic by design
AD5640					
Resolution	14	14	14	Bits min	
Relative Accuracy	±8	±4	±4	LSB max	
Differential Nonlinearity	±0.5	±0.5	±0.5	LSB max	Guaranteed monotonic by design
AD5620					
Resolution	12	12	12	Bits min	
Relative Accuracy	±6	±1	±1	LSB max	
Differential Nonlinearity	±0.25	±0.25	±0.25	LSB max	Guaranteed monotonic by design
Zero-Code Error	2	2	2	mV typ	All 0s loaded to DAC register
	10	10	10	mV max	
Offset Error	±10	±10	±10	mV max	
Full-Scale Error	−0.15	−0.15	−0.15	% FSR typ	All 1s loaded to DAC register
	±1	±1	±1	% FSR max	
Gain Error	±1.5	±1.5	±1.5	% FSR max	
Zero-Code Error Drift	±2	±2	±2	µV/°C typ	
Gain Temperature Coefficient	±2.5	±2.5	±2.5	ppm typ	Of FSR/°C
DC Power Supply Rejection Ratio	−75	−75	−75	dB typ	DAC code = midscale; V_{DD} = 5 V ± 10%
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0	0	0	V min	
	V_{DD}	V_{DD}	V_{DD}	V max	
Output Voltage Settling Time	8	8	8	µs typ	¼ to ¾ scale change settling to ±2 LSB
	10	10	10	µs max	R_L = 2 kΩ; 0 pF < C_L < 200 pF
Slew Rate	1.5	1.5	1.5	V/µs typ	¼ to ¾ scale
Capacitive Load Stability	2	2	2	nF typ	R_L = ∞
	10	10	10	nF typ	R_L = 2 kΩ
Output Noise Spectral Density	80	80	80	nV/√Hz typ	DAC code = midscale, 10 kHz
Output Noise (0.1 Hz to 10 Hz)	45	45	45	µV p-p typ	DAC code = midscale
Digital-to-Analog Glitch Impulse	5	5	5	nV-s typ	1 LSB change around major carry
Digital Feedthrough	0.1	0.1	0.1	nV-s typ	
DC Output Impedance	0.5	0.5	0.5	Ω typ	
Short-Circuit Current	30	30	30	mA typ	V_{DD} = 5 V
Power-Up Time	5	5	5	µs typ	Coming out of power-down mode; V_{DD} = 5 V
REFERENCE OUTPUT					
Output Voltage	2.495	2.495	2.495	V min	At ambient
	2.505	2.505	2.505	V max	
Reference TC[3]	±10	±10	±5	ppm/°C typ	
			±10	ppm/°C max	
Output Impedance	7.5	7.5	7.5	kΩ typ	

Parameter	A Grade[1]	B Grade[1]	C Grade[1]	Unit	Conditions/Comments
LOGIC INPUTS[3]					
Input Current	±2	±2	±2	μA max	All digital inputs
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	V_{DD} = 5 V
V_{INH}, Input High Voltage	2	2	2	V min	V_{DD} = 5 V
Pin Capacitance	3	3	3	pF typ	
POWER REQUIREMENTS					
V_{DD}	4.5	4.5	4.5	V min	All digital inputs at 0 V or V_{DD}
	5.5	5.5	5.5	V max	DAC active and excluding load current
I_{DD} (Normal Mode)					
V_{DD} = 4.5 V to 5.5 V	0.55	0.55	0.55	mA typ	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V	1	1	1	mA max	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} (All Power-Down Modes)					
V_{DD} = 4.5 V to 5.5 V	0.48	0.48	0.48	μA typ	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V	1	1	1	μA max	$V_{IH} = V_{DD}$ and V_{IL} = GND

[1] Temperature range is −40°C to +105°C, typical at +25°C.
[2] Linearity calculated using a reduced code range: AD5660 (Code 511 to Code 65024); AD5640 (Code 128 to Code 16256); AD5620 (Code 32 to Code 4064). Output unloaded. Linearity tested with V_{DD} = 5.5 V. If part is operated with a V_{DD} < 5 V, the output is clamped to V_{DD}.
[3] Guaranteed by design and characterization; not production tested.

AD5620/AD5640/AD5660-1

V_{DD}[1] = 2.7 V to 3.3 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, C_{REFOUT} = 100 nF; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	A Grade[2]	B Grade[2]	C Grade[2]	Unit	Conditions/Comments
STATIC PERFORMANCE[3]					
AD5660					
Resolution	16	16	16	Bits min	
Relative Accuracy	±32	±16	±16	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	Guaranteed monotonic by design
AD5640					
Resolution	14	14	14	Bits min	
Relative Accuracy	±8	±4	±4	LSB max	
Differential Nonlinearity	±0.5	±0.5	±0.5	LSB max	Guaranteed monotonic by design
AD5620					
Resolution	12	12	12	Bits min	
Relative Accuracy	±6	±1	±1	LSB max	
Differential Nonlinearity	±0.25	±0.25	±0.25	LSB max	Guaranteed monotonic by design
Zero-Code Error	2	2	2	mV typ	All 0s loaded to DAC register
	8	8	8	mV max	
Offset Error	±9	±9	±9	mV max	
Full-Scale Error	±0.15	±0.15	±0.15	% FSR typ	All 1s loaded to DAC register
	±0.85	±0.85	±0.85	% FSR max	
Gain Error	±0.85	±0.85	±0.85	% FSR max	
Zero-Code Error Drift	±2	±2	±2	µV/°C typ	
Gain Temperature Coefficient	±2.5	±2.5	±2.5	ppm typ	Of FSR/°C
DC Power Supply Rejection Ratio	−60	−60	−60	dB typ	DAC code = midscale; V_{DD} = 3 V ± 10%
OUTPUT CHARACTERISTICS[4]					
Output Voltage Range	0	0		V min	
	V_{DD}	V_{DD}	V_{DD}	V max	
Output Voltage Settling Time	8	8	8	µs typ	¼ to ¾ scale change settling to ±2 LSB
	10	10	10	µs max	R_L = 2 kΩ; 0 pF < C_L < 200 pF
Slew Rate	1.5	1.5	1.5	V/µs typ	¼ to ¾ scale
Capacitive Load Stability	2	2	2	nF typ	R_L = ∞
	10	10	10	nF typ	R_L = 2 kΩ
Output Noise Spectral Density	80	80	80	nV/√Hz typ	DAC code = midscale, 10 kHz
Output Noise (0.1 Hz to 10 Hz)	20	20	20	µV p-p typ	DAC code = midscale
Digital-to-Analog Glitch Impulse	5	5	5	nV-s typ	1 LSB change around major carry
Digital Feedthrough	0.1	0.1	0.1	nV-s typ	
DC Output Impedance	0.5	0.5	0.5	Ω typ	
Short-Circuit Current	30	30	30	mA typ	V_{DD} = 3 V
Power-Up Time	6	6	6	µs typ	Coming out of power-down mode; V_{DD} = 3 V
REFERENCE OUTPUT					
Output Voltage	1.247	1.247	1.247	V min	At ambient
	1.253	1.253	1.253	V max	
Reference TC[4]	±10	±10	±5	ppm/°C typ	
			±15	ppm/°C max	
Output Impedance	7.5	7.5	7.5	kΩ typ	

Parameter	A Grade[2]	B Grade[2]	C Grade[2]	Unit	Conditions/Comments
LOGIC INPUTS[4]					
Input Current	±1	±1	±1	µA max	All digital inputs
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	V_{DD} = 3 V
V_{INH}, Input High Voltage	2	2	2	V min	V_{DD} = 3 V
Pin Capacitance	3	3	3	pF max	
POWER REQUIREMENTS					
V_{DD}	2.7	2.7	2.7	V min	All digital inputs at 0 V or V_{DD}
	3.3	3.3	3.3	V max	DAC active and excluding load current
I_{DD} (Normal Mode)					
V_{DD} = 2.7 V to 3.3 V	0.55	0.55	0.55	mA typ	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.3 V	0.65	0.65	0.65	mA max	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} (All Power-Down Modes)					
V_{DD} = 2.7 V to 3.3 V	0.2	0.2	0.2	µA typ	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.3 V	0.25	0.25	0.25	µA max	$V_{IH} = V_{DD}$ and V_{IL} = GND

[1] Part is functional with V_{DD} up to 5.5 V.
[2] Temperature range is −40°C to +105°C, typical at +25°C.
[3] Linearity calculated using a reduced code range: AD5660 (Code 511 to Code 65024); AD5640 (Code 128 to Code 16256); AD5620 (Code 32 to Code 4064). Output unloaded.
[4] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2. V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

	Limit at T_{MIN}, T_{MAX}			
Parameter	**V_{DD} = 2.7 V to 3.6 V**	**V_{DD} = 3.6 V to 5.5 V**	**Unit**	**Conditions/Comments**
t_1[1]	50	33	ns min	SCLK cycle time
t_2	13	13	ns min	SCLK high time
t_3	13	13	ns min	SCLK low time
t_4	13	13	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	5	5	ns min	Data setup time
t_6	4.5	4.5	ns min	Data hold time
t_7	0	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	50	33	ns min	Minimum $\overline{SYNC}$ high time
t_9	13	13	ns min	$\overline{SYNC}$ rising edge to SCLK fall ignore
t_{10}	0	0	ns min	SCLK falling edge to $\overline{SYNC}$ fall ignore

[1] Maximum SCLK frequency is 30 MHz at V_{DD} = 3.6 V to 5.5 V and 20 MHz at V_{DD} = 2.7 V to 3.6 V.

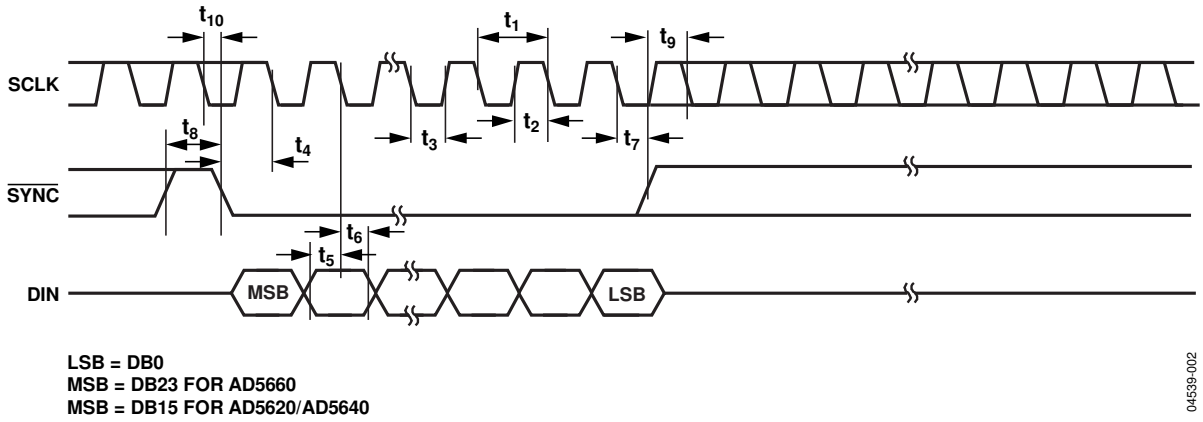


Figure 2. Serial Write Operation

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{FB} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REFOUT} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
SOT-23 Package (4-Layer Board)	
θ_{JA} Thermal Impedance	119°C/W
MSOP Package (4-Layer Board)	
θ_{JA} Thermal Impedance	141°C/W
θ_{JC} Thermal Impedance	44°C/W
LFCSP Package(4-Layer Board)	
θ_{JA} Thermal Impedance	103°C/W
θ_{JC} Thermal Impedance	44.4°C/W
Reflow Soldering Peak Temperature	
SnPb	240°C
Pb-Free	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

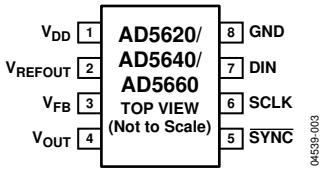


Figure 3. SOT-23 Pin Configuration

Figure 4. MSOP Pin Configuration

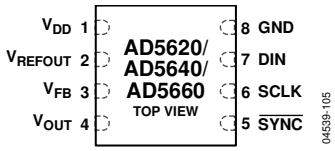


Figure 5. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. These parts can operate from 2.7 V to 5.5 V. V_{DD} should be decoupled to GND.
2	V_{REFOUT}	Reference Voltage Output.
3	V_{FB}	Feedback Connection for the Output Amplifier. V_{FB} should be connected to V_{OUT} for normal operation.
4	V_{OUT}	Analog Output Voltage from DAC. The output amplifier has rail-to-rail operation.
5	$\overline{SYNC}$	Level-Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock cycle for the AD5660 and the 16th clock cycle for AD5620/AD5640 unless $\overline{SYNC}$ is taken high before this edge. In this case, the rising edge of $\overline{SYNC}$ acts as an interrupt, and the write sequence is ignored by the DAC.
6	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.
7	DIN	Serial Data Input. The AD5660 has a 24-bit shift register, and the AD5620/AD5640 have a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
8	GND	Ground Reference Point for all Circuitry on the Part.

TYPICAL PERFORMANCE CHARACTERISTICS

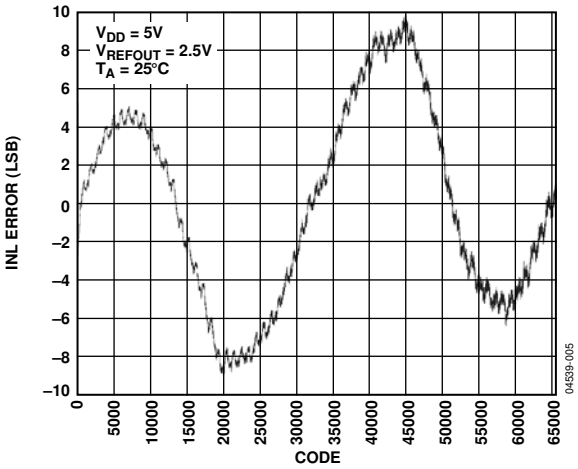


Figure 6. INL—AD5660-2/AD5660-3

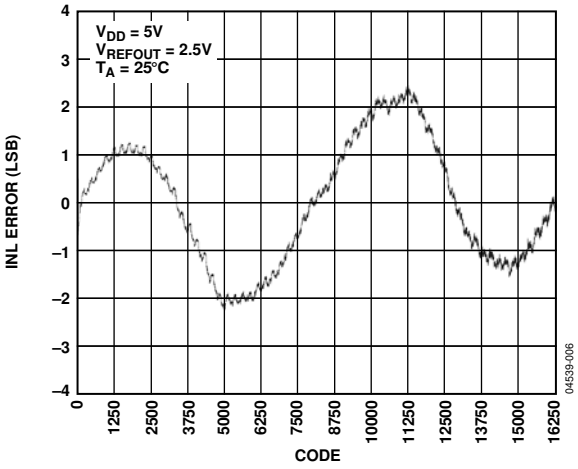


Figure 7. INL—AD5640-2/AD5640-3

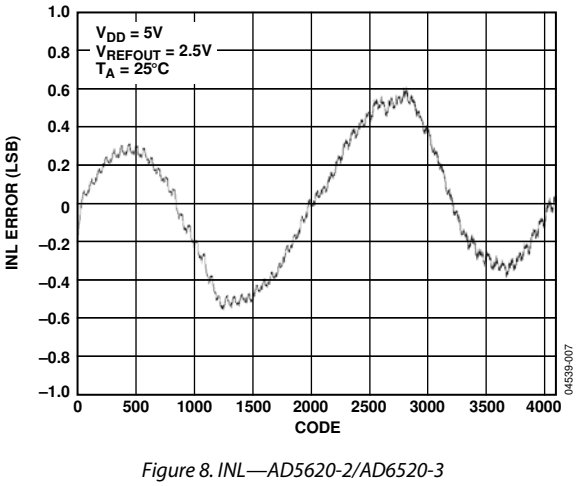


Figure 8. INL—AD5620-2/AD6520-3

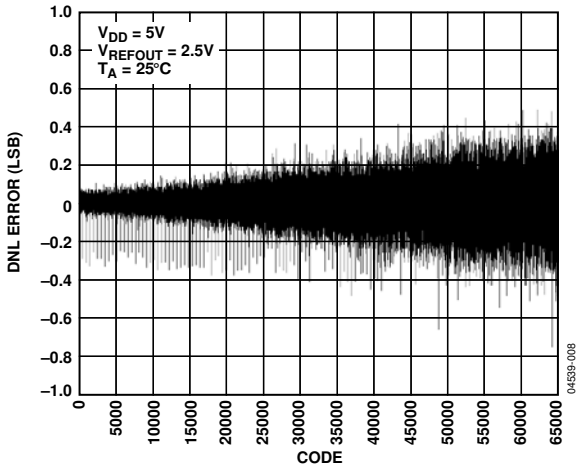


Figure 9. DNL—AD5660-2/AD5660-3

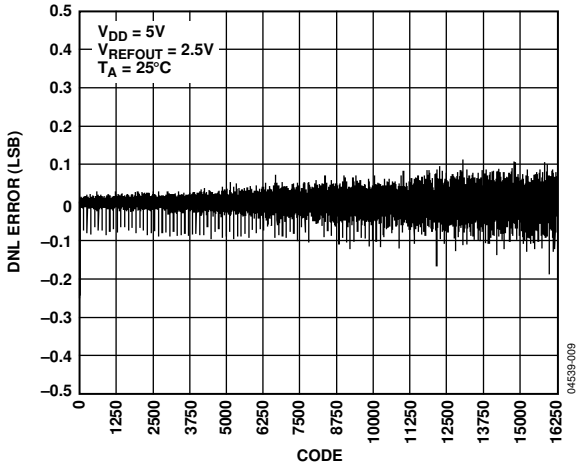


Figure 10. DNL—AD5640-2/AD5640-3

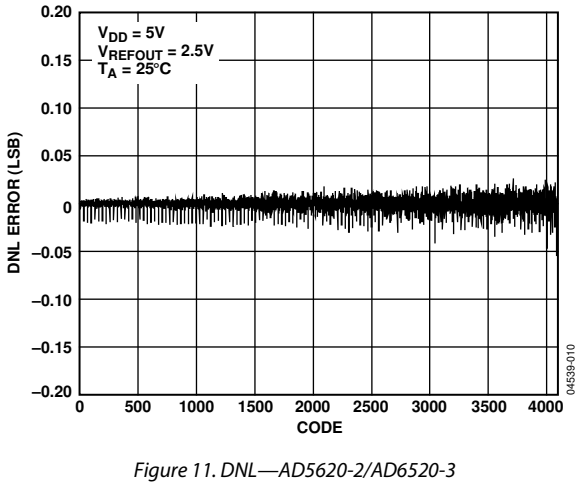


Figure 11. DNL—AD5620-2/AD6520-3

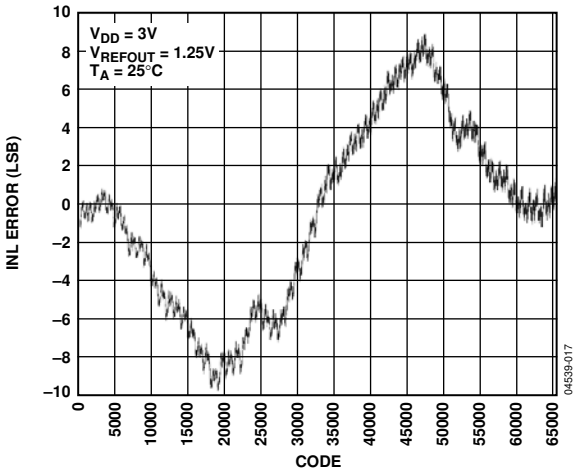


Figure 12. INL—AD5660-1

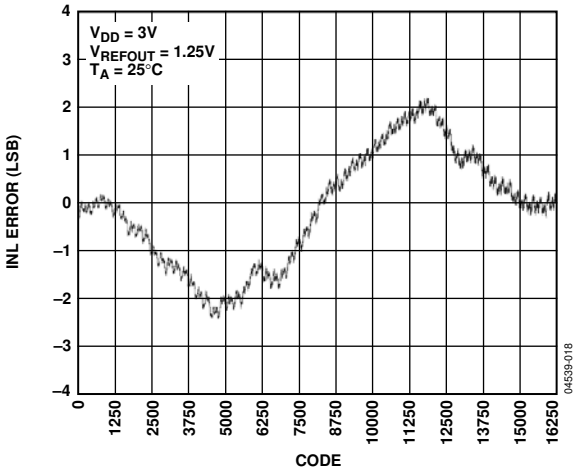


Figure 13. INL—AD5640-1

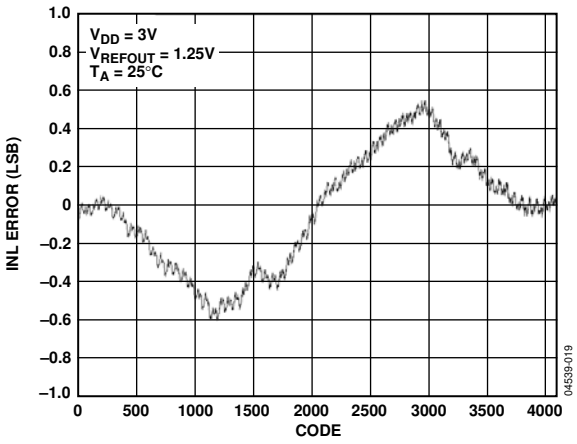


Figure 14. INL—AD5620-1

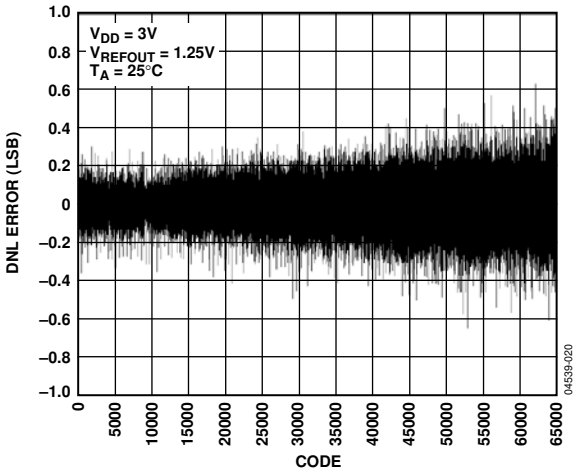


Figure 15. DNL—AD5660-1

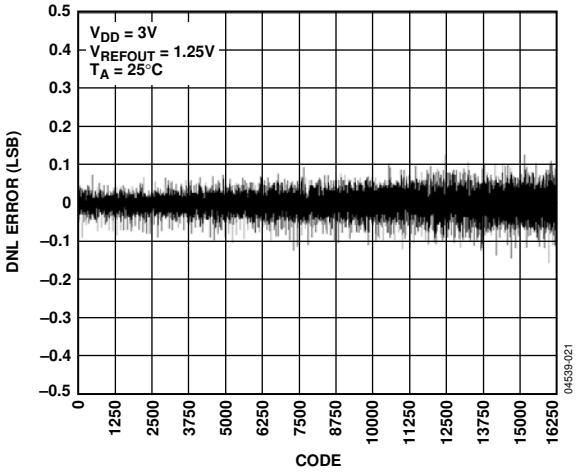


Figure 16. DNL—AD5640-1

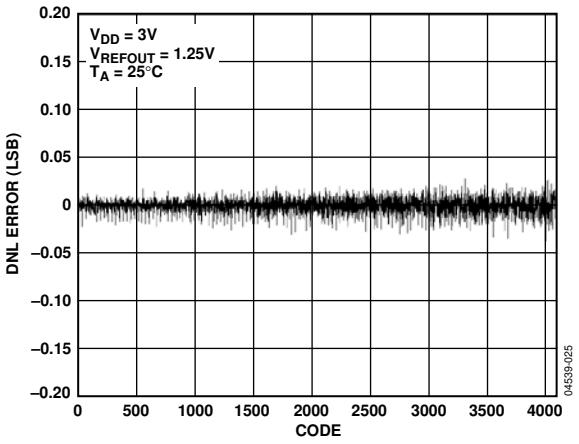


Figure 17. DNL—AD5620-1

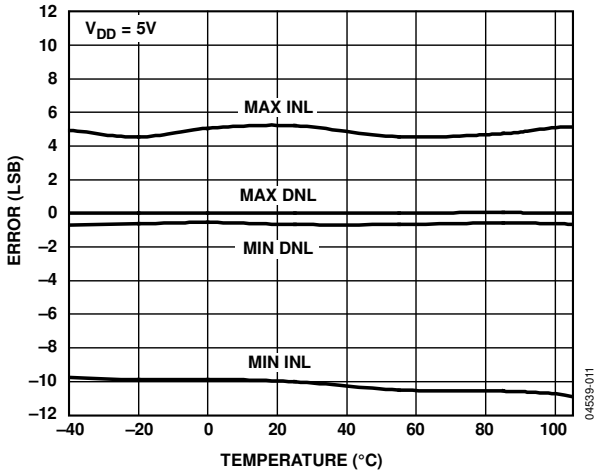


Figure 18. INL Error and DNL Error vs. Temperature

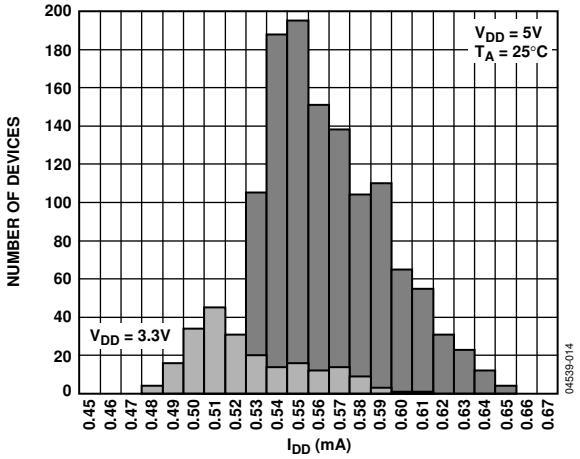


Figure 21. I_{DD} Histogram

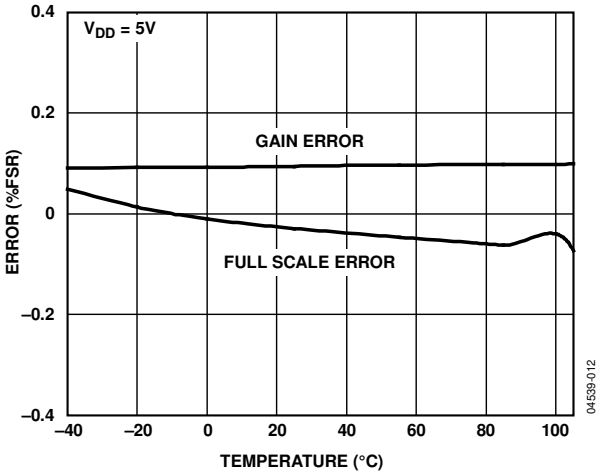


Figure 19. Gain Error and Full-Scale Error vs. Temperature

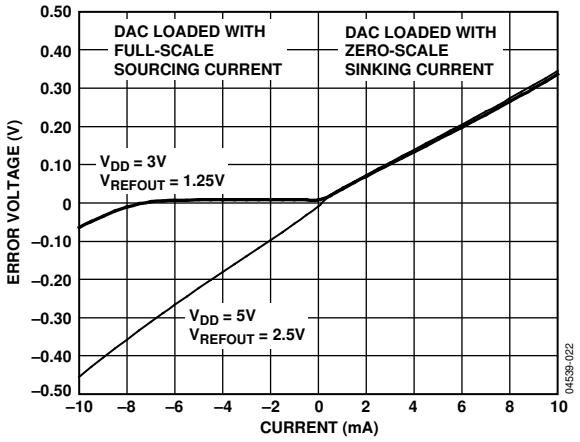


Figure 22. Headroom at Rails vs. Source and Sink

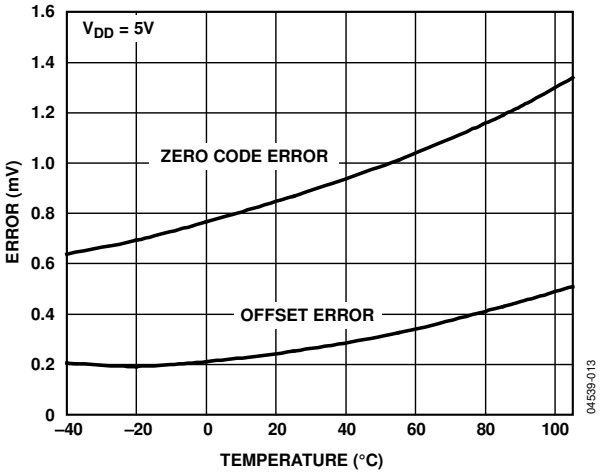


Figure 20. Zero-Code and Offset Error vs. Temperature

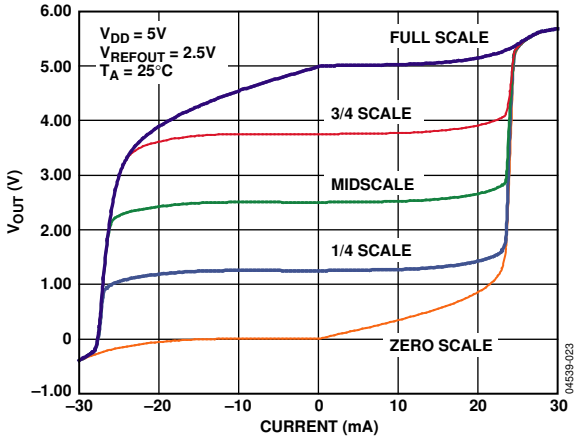


Figure 23. Source and Sink Capability—AD5660-2/AD5660-3

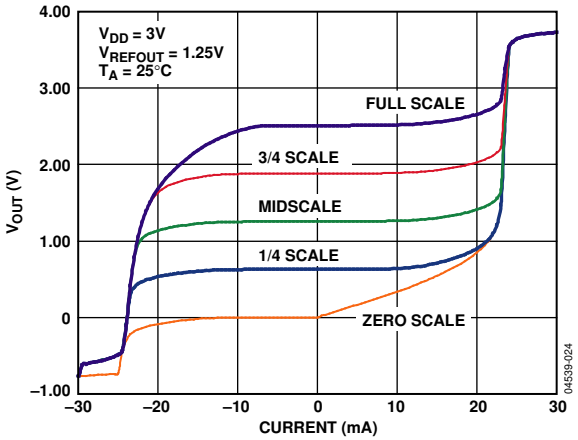


Figure 24. Source and Sink Capability—AD5660-1

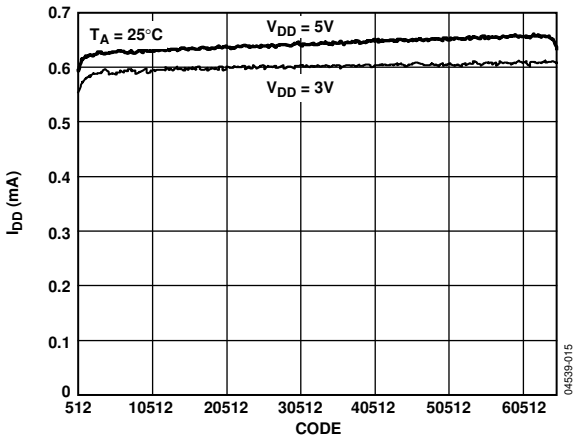


Figure 25. Supply Current vs. Code

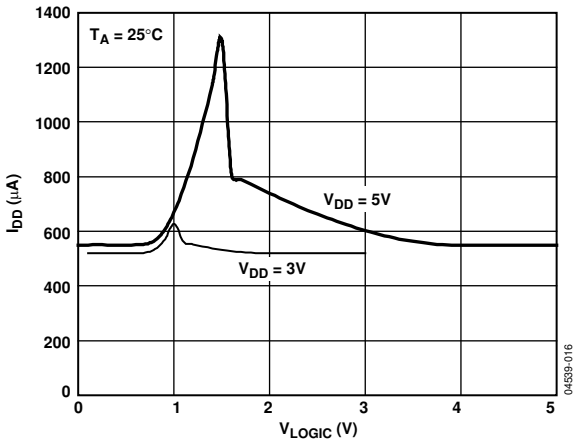


Figure 26. Supply Current vs. Logic Input Voltage

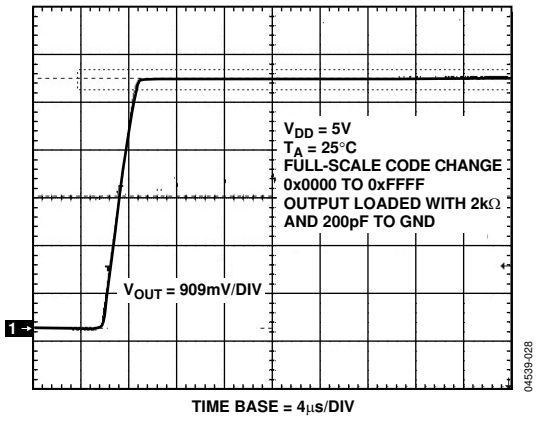


Figure 27. Full-Scale Settling Time, 5 V

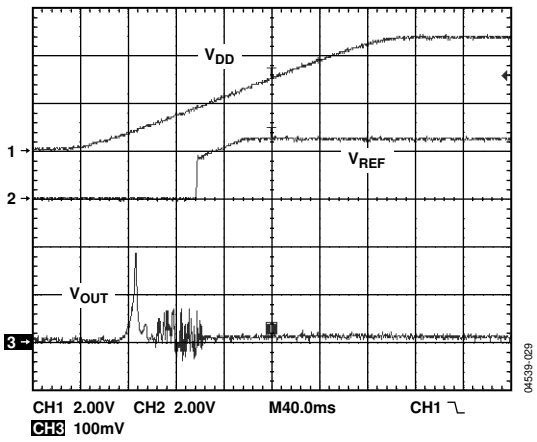


Figure 28. Power-On Reset to 0 V—AD5660-2

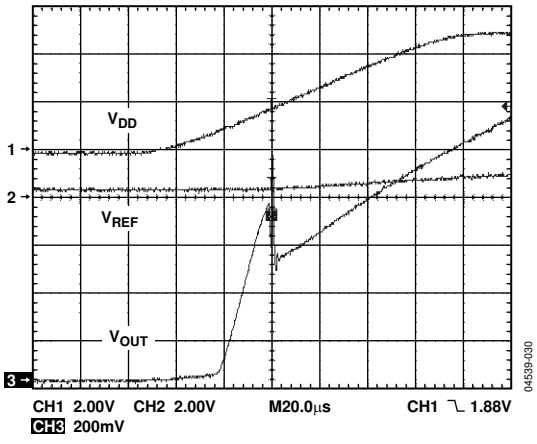


Figure 29. Power-On Reset to Midscale—AD5660-3

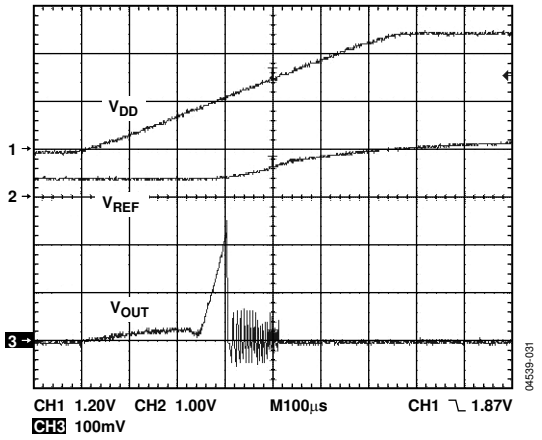


Figure 30. Power-On Reset to 0 V—AD5660-1

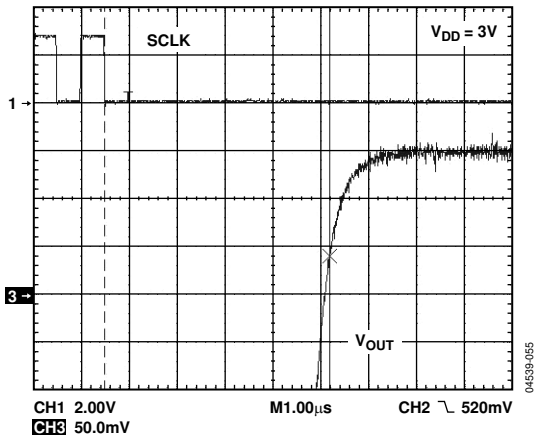


Figure 31. Exiting Power-Down to Midscale

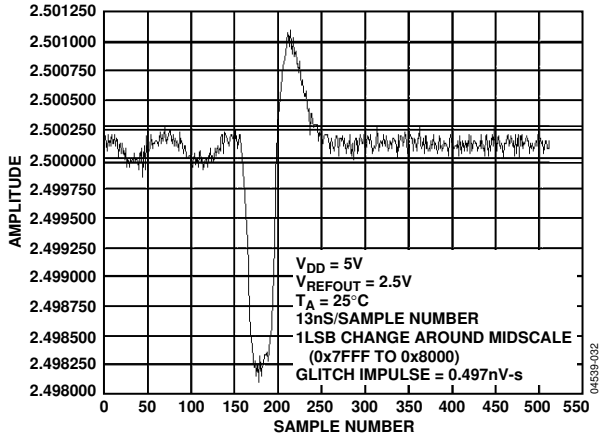


Figure 32. Digital-to-Analog Glitch Impulse—AD5660-2/AD5660-3

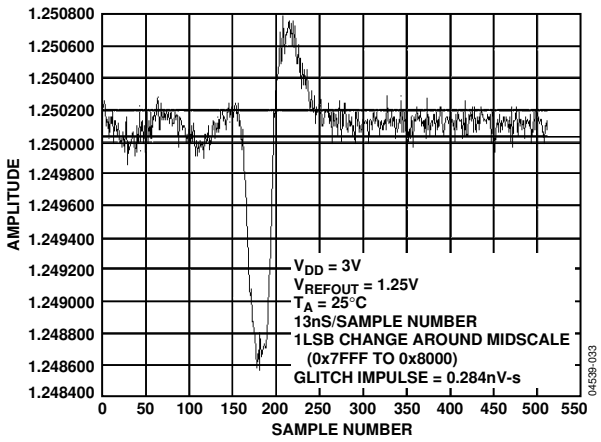


Figure 33. Digital-to-Analog Glitch Impulse—AD5660-1

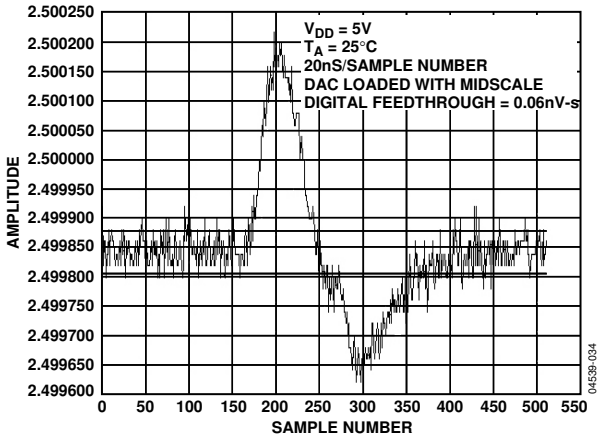


Figure 34. Digital Feedthrough

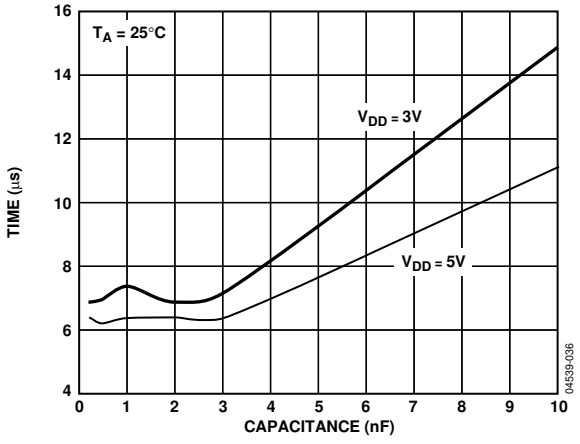


Figure 35. Settling Time vs. Capacitive Load

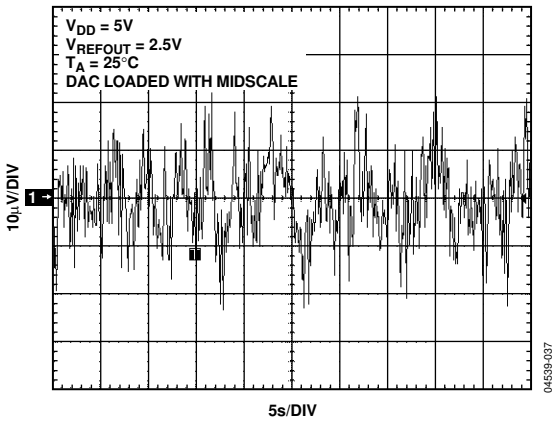


Figure 36. 0.1 Hz to 10 Hz Output Noise—AD5660-2/AD5660-3

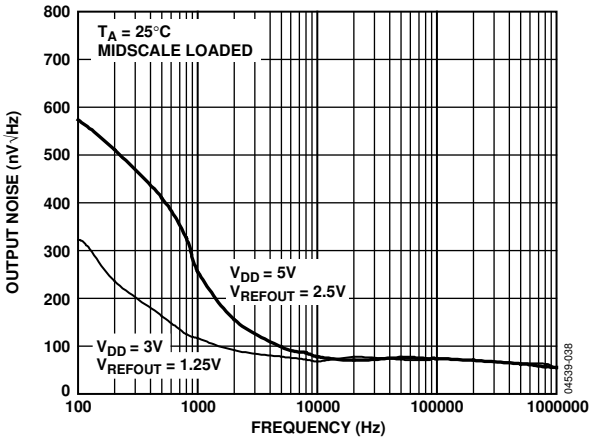


Figure 38. Noise Spectral Density

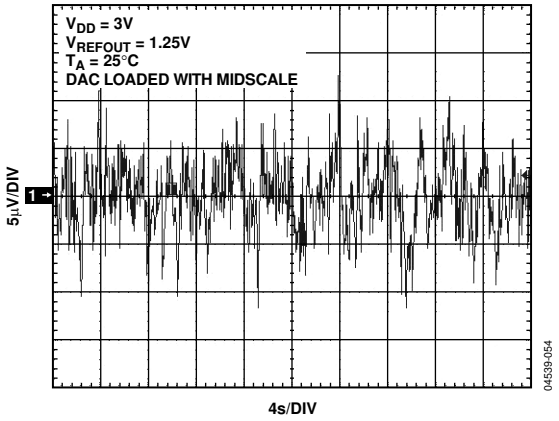


Figure 37. 0.1 Hz to 10 Hz Output Noise—AD5660-1

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Figure 6 through Figure 8 show typical INL vs. code.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Figure 9 through Figure 11 show typical DNL vs. code.

Zero-Code Error
Zero-code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5620/AD5640/AD5660, because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV. Figure 20 shows a plot of zero-code error vs. temperature.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range. Figure 19 shows a plot of full-scale error vs. temperature.

Gain Error
This is a measurement of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range.

Zero-Code Error Drift
This is a measurement of the change in zero-code error with a change in temperature. It is expressed in μV/°C.

Gain Temperature Coefficient
This is a measurement of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Offset Error
Offset error is a measurement of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5660 with Code 512 loaded into the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to the change in V_{DD} for the full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2.5 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
This indicates the amount of time for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change. It is measured from the 24th falling edge of SCLK.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 32 and Figure 33.

Digital Feedthrough
Digital feedthrough is a measurement of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s or vice versa.

Noise Spectral Density
This is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz. Figure 38 shows a plot of noise spectral density.

THEORY OF OPERATION

D/A SECTION

The AD5620/AD5640/AD5660 DACs are fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. The parts include an internal 1.25 V/2.5 V, 5 ppm/°C reference that is internally gained up by 2. Figure 39 shows a block diagram of the DAC architecture.

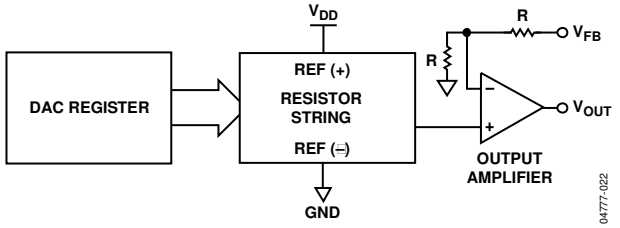


Figure 39. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = 2 \times V_{REFOUT} \times \left(\frac{D}{2^N} \right)$$

where:
D is the decimal equivalent of the binary code that is loaded to the DAC register.
0 to 4095 for AD5620 (12 bit)
0 to 16383 for AD5640 (14 bit)
0 to 65535 for AD5660 (16 bit)
N is the DAC resolution.

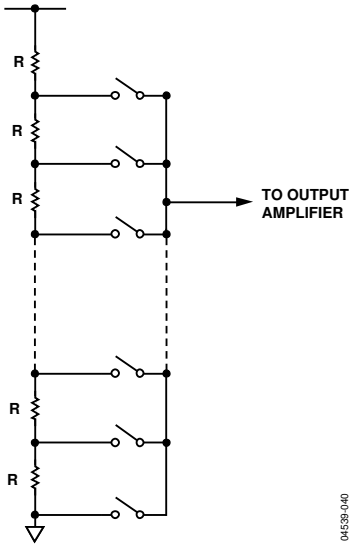


Figure 40. Resistor String

RESISTOR STRING

The resistor string section is shown in Figure 40. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

INTERNAL REFERENCE

The AD5620/AD5640/AD5660-1 parts include an internal, 1.25 V, 5 ppm/°C reference, giving a full-scale output voltage of 2.5 V. The AD5620/AD5640/AD5660-2-3 parts include an internal, 2.5 V, 5 ppm/°C reference, giving a full-scale output voltage of 5 V. The reference associated with each part is available at the V_{REFOUT} pin. A buffer is required if the reference output is used to drive external loads. It is recommended that a 100 nF capacitor is placed between the reference output and GND for reference stability.

OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. This output buffer amplifier has a gain of 2 derived from a 50 kΩ resistor divider network in the feedback path. The inverting input of the output amplifier is available to the user, allowing for remote sensing. This V_{FB} pin must be connected to V_{OUT} for normal operation. It can drive a load of 2 kΩ in parallel with 1000 pF to GND. Figure 22 shows the source and sink capabilities of the output amplifier. The slew rate is 1.5 V/μs with a ¼ to ¾ full-scale settling time of 10 μs.

SERIAL INTERFACE

The AD5620/AD5640/AD5660 have a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most DSPs.
See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the DIN line is clocked into the 16-bit shift register (AD5620/AD5640) or the 24-bit shift register (AD5660) on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the AD5620/AD5640/AD5660 compatible with high speed DSPs. On the 16th falling clock edge (AD5620/AD5640) or the 24th falling clock edge (AD5660), the last data bit is clocked in and the programmed function is executed, that is, a change in the DAC register contents and/or a change in the mode of operation is executed. At this stage, the $\overline{SYNC}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Because the $\overline{SYNC}$ buffer draws more current when V_{IN} = 2 V than it does when V_{IN} = 0.8 V, $\overline{SYNC}$ should be idled low between write sequences for even lower power operation of the parts. As is mentioned previously, however, $\overline{SYNC}$ must be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

AD5620/AD5640

The input shift register is 16 bits wide for the AD5620/AD5640 (see Figure 41 and Figure 42). The first two bits are control bits that control which mode of operation the part is in (normal mode or any of the three power-down modes). The next 14/12 bits, respectively, are the data bits. These are transferred to the DAC register on the 16th falling edge of SCLK.

AD5660

The input shift register is 24 bits wide for the AD5660 (see Figure 43). The first six bits are don't care bits. The next two are control bits that control which mode of operation the part is in (normal mode or any of the three power-down modes). For a more complete description of the various modes, see the Power-Down Modes section. The next 16 bits are the data bits. These are transferred to the DAC register on the 24th falling edge of SCLK.

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence for the AD5660, the $\overline{\text{SYNC}}$ line is kept low for at least 24 falling edges of SCLK, and the DAC is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 24th falling edge, this acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 44). Similarly, in a normal write sequence for the AD5620/AD5640, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK, and the DAC is updated on the 16th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, this acts as an interrupt to the write sequence.

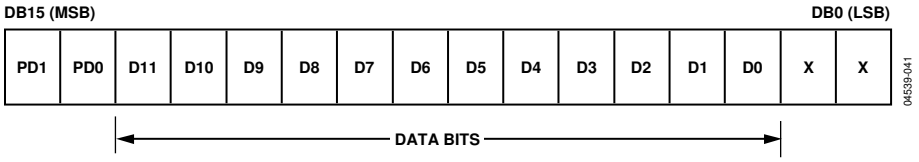


Figure 41. AD5620 Input Register Contents

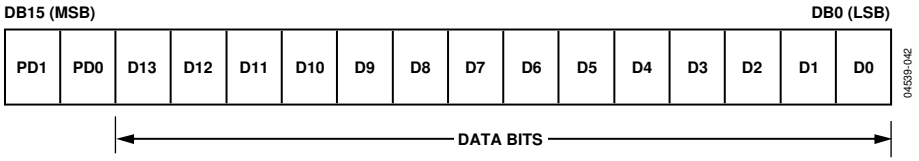


Figure 42. AD5640 Input Register Contents

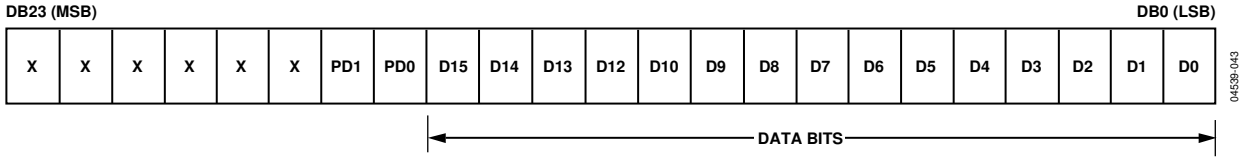


Figure 43. AD5660 Input Register Contents

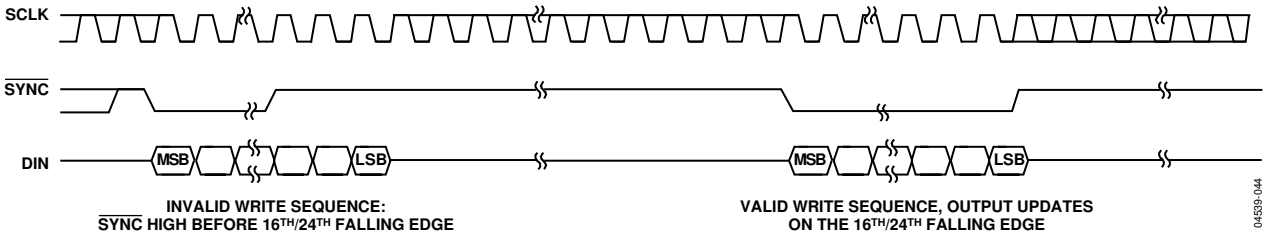


Figure 44. $\overline{\text{SYNC}}$ Interrupt Facility

POWER-ON RESET

The AD5620/AD5640/AD5660 family contains a power-on reset circuit that controls the output voltage during power-up. The AD5620/AD5640/AD5660-1-2 DAC output powers up to 0 V, and the AD5620/AD5660-3 DAC output powers up to midscale. The output remains at this level until a valid write sequence is made to the DAC, which is useful in applications where it is important to know the state of the DAC output while it is in the process of powering up.

POWER-DOWN MODES

The AD5620/AD5640/AD5660 have four separate modes of operation. These modes are software-programmable by setting two bits in the control register. Table 7 and Table 8 show how the state of the bits corresponds to the operating mode of the device.

Table 7. Modes of Operation for the AD5660

DB17	DB16	AD5660 Operating Mode
0	0	Normal operation
		Power-down modes:
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-state

Table 8. Modes of Operation for the AD5620/AD5640

DB15	DB14	AD5620/AD5640 Operating Mode
0	0	Normal operation
		Power-down modes:
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-state

When both bits are set to 0, the part works normally with its normal power consumption of 550 μA at 5 V. However, for the three power-down modes, the supply current falls to 480 nA at 5 V (200 nA at 3 V). Not only does the supply current fall, but the output stage is internally switched from the output of the amplifier to a resistor network of known values. The advantage is that the output impedance of the part is known while the part is in power-down mode. There are three options: the output is connected internally to GND through a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-stated). The output stage is shown in Figure 45.

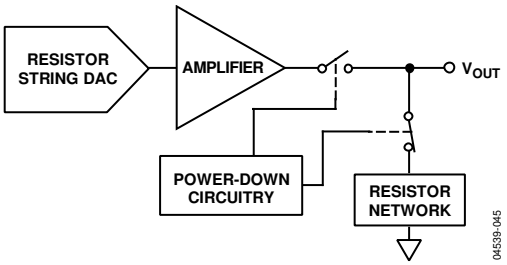


Figure 45. Output Stage During Power-Down

The bias generator, output amplifier, reference, resistor string, and other associated linear circuitry are all shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 5 μs for V_{DD} = 5 V and V_{DD} = 3 V (see Figure 31).

MICROPROCESSOR INTERFACING

AD5660-to-Blackfin® ADSP-BF53x Interface

Figure 46 shows a serial interface between the AD5660 and the Blackfin ADSP-BF53x microprocessor. The ADSP-BF53x processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5660, the setup for the interface is as follows: DT0PRI drives the DIN pin of the AD5660, while TSCLK0 drives the SCLK of the part and $\overline{\text{SYNC}}$ is driven from TFS0.

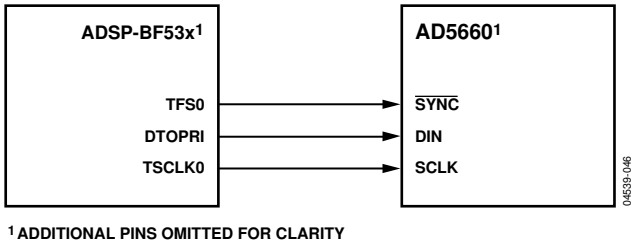


Figure 46. AD5660-to-Blackfin ADSP-BF53x Interface

AD5660-to-68HC11/68L11 Interface

Figure 47 shows a serial interface between the AD5660 and the 68HC11/68L11 microcontroller. SCK of 68HC11/68L11 drives the SCLK of AD5660, and the MOSI output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: The 68HC11/68L11 should be configured so that its CPOL bit is 0, and its CPHA bit is 1. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 is configured in this way, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5660, PC7 is left low after the first eight bits are transferred, a second serial write operation is performed to the DAC, and PC7 is taken high at the end of this procedure.

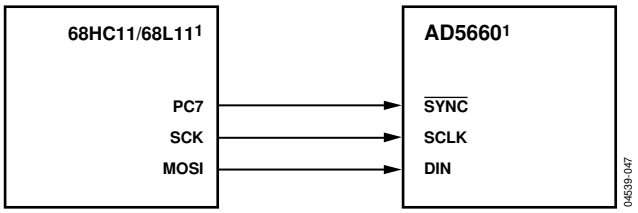


Figure 47. AD5660-to-68HC11/68L11 Interface

AD5660-to-80C51/80L51 Interface

Figure 48 shows a serial interface between the AD5660 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TxD of the 80C51/80L51 drives SCLK of the AD5660, and RxD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit-programmable pin on the port. In this case, Port Line P3.3 is used. When data is to be transmitted to the AD5660, P3.3 is taken low. The 80C51/80L51 transmit data only in 8-bit bytes; therefore, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 output the serial data LSB first; however, the AD5660 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should take this into account.

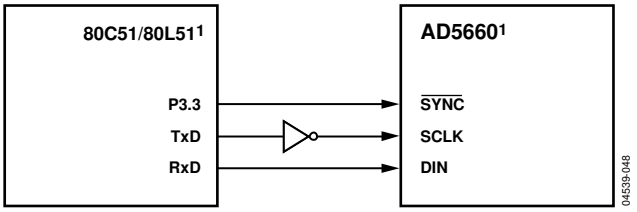


Figure 48. AD5660-to-80C51/80L51 Interface

AD5660-to-MICROWIRE Interface

Figure 49 shows an interface between the AD5660 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5660 on the rising edge of the SK.

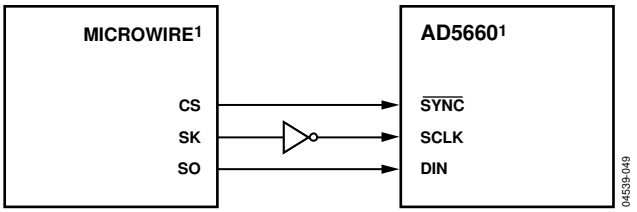


Figure 49. AD5660-to-MICROWIRE Interface

APPLICATIONS INFORMATION

USING A REF19x AS A POWER SUPPLY FOR THE AD5620/AD5640/AD5660

Because the supply current required by the AD5620/AD5640/AD5660 is extremely low, an alternative option is to use a REF19x voltage reference (REF195 for 5 V or REF193 for 3 V) to supply the required voltage to the part (see Figure 50). This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The REF19x outputs a steady supply voltage for the AD5620/AD5640/AD5660. If the low dropout REF195 is used, the current it needs to supply to the AD5660 is 500 µA. This is with no load on the output of the DAC. When the DAC output is loaded, the REF195 also must supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is

500 µA + (5 V/5 kΩ) = 1.5 mA

The load regulation of the REF195 is typically 2 ppm/mA, which results in an error of 3 ppm (15 µV) for the 1.5 mA current drawn from it. This corresponds to a 0.197 LSB error for the AD5660.

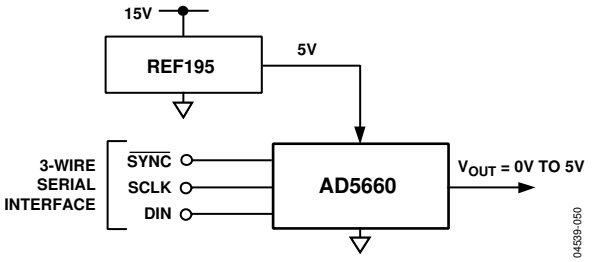


Figure 50. REF195 as the Power Supply to the AD5660

BIPOLAR OPERATION USING THE AD5660

The AD5660 is designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 51. Figure 51 gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as

$$V_O = \left[V_{DD} \times \left(\frac{D}{65536} \right) \times \left(\frac{R1+R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 65535).

When V_{DD} = 5 V, $R1 = R2$ = 10 kΩ,

$$V_O = \left(\frac{10 \times D}{65536} \right) - 5 \text{ V}$$

This results in an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output and 0xFFFF corresponding to a +5 V output.

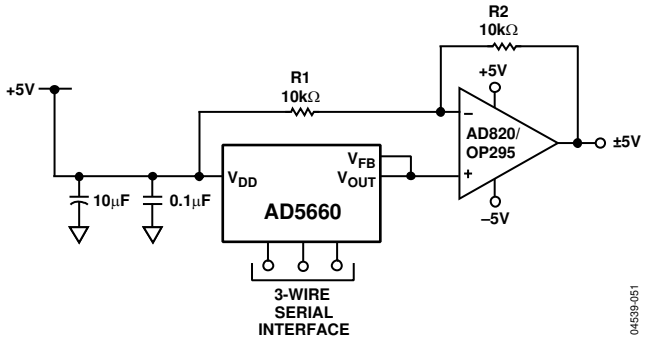


Figure 51. Bipolar Operation with the AD5660

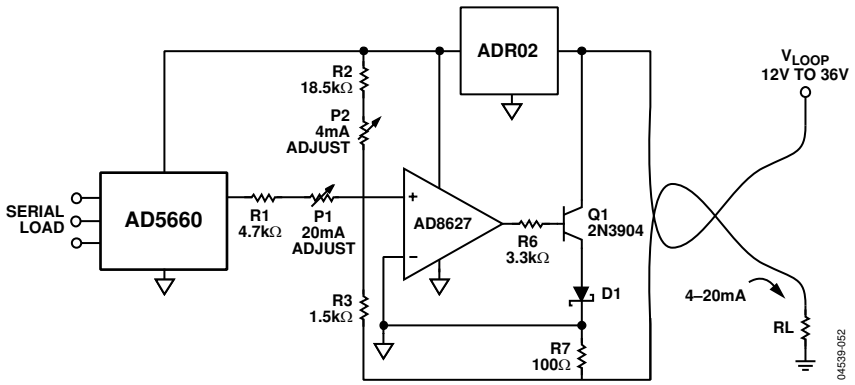


Figure 52. Programmable 4 mA to 20 mA Process Controller

USING THE AD5660 AS AN ISOLATED, PROGRAMMABLE, 4 mA TO 20 mA PROCESS CONTROLLER

In many process-control system applications, 2-wire current transmitters are used to transmit analog signals through noisy environments. These current transmitters use a zero-scale signal current of 4 mA to power the signal conditioning circuitry of the transmitter. The full-scale output signal in these transmitters is 20 mA. The converse approach to process control can also be used, in which a low-power, programmable current source is used to control remotely located sensors or devices in the loop.

A circuit that performs this function is shown in Figure 52. Using the AD5660 as the controller, the circuit provides a programmable output current of 4 to 20 mA, proportional to the digital code of the DAC. Biasing for the controller is provided by the ADR02 and requires no external trim for two reasons: first, the ADR02's tight initial output voltage tolerance, and second, the low supply current consumption of both the AD8627 and the AD5660. The entire circuit, including optocouplers, consumes less than 3 mA from the total budget of 4 mA. The AD8627 regulates the output current to satisfy the current summation at the noninverting node of the AD8627.

$$I_{OUT} = 1/R7\ (V_{DAC} \times R3/R1 + V_{REF} \times R3/R2)$$

For the values shown in Figure 52,

$$I_{OUT} = 0.2435\ \mu A \times D + 4\ mA$$

where $D = 0 \le D \le 65{,}535$, giving a full-scale output current of 20 mA when the AD5660's digital code equals 0xFFFF. Offset trim at 4 mA is provided by P2, and P1 provides the circuit gain trim at 20 mA. These two trims do not interact because the noninverting input of the AD8627 is at virtual ground. The Schottky diode, D1, is required in this circuit to prevent loop supply power-on transients from pulling the noninverting input of the AD8627 more than 300 mV below its inverting input. Without this diode, such transients could cause phase reversal of the AD8627 and possible latch-up of the controller. The loop supply voltage compliance of the circuit is limited by the maximum applied input voltage to the ADR02 and is from 12 V to 40 V.

USING THE AD5620/AD5640/AD5660 WITH A GALVANICALLY ISOLATED INTERFACE

For process-control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from hazardous common-mode voltages that might occur in the area where the DAC is functioning. The *i*Coupler® provides isolation in excess of 2.5 kV. The AD5620/AD5640/AD5660 use a 3-wire serial logic interface; therefore, the ADuM1300 3-channel digital isolator provides the required isolation (see Figure 53). The power supply to the part also must be isolated, which is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5620/AD5640/AD5660.

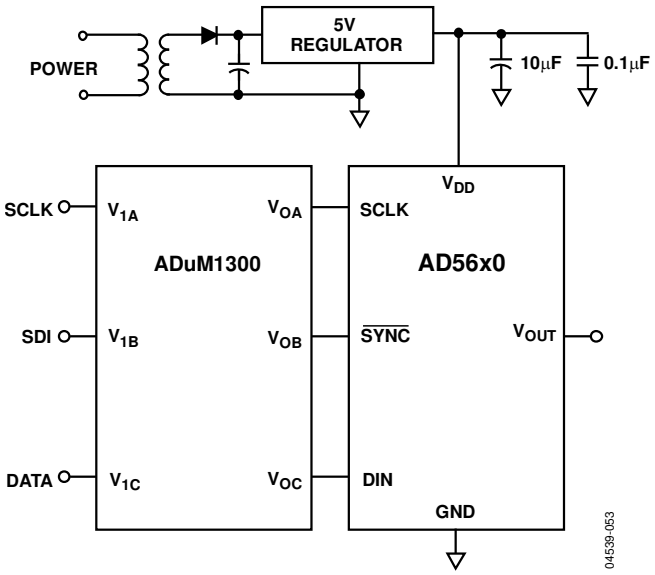


Figure 53. AD5620/AD5640/AD5660 with a Galvanically Isolated Interface

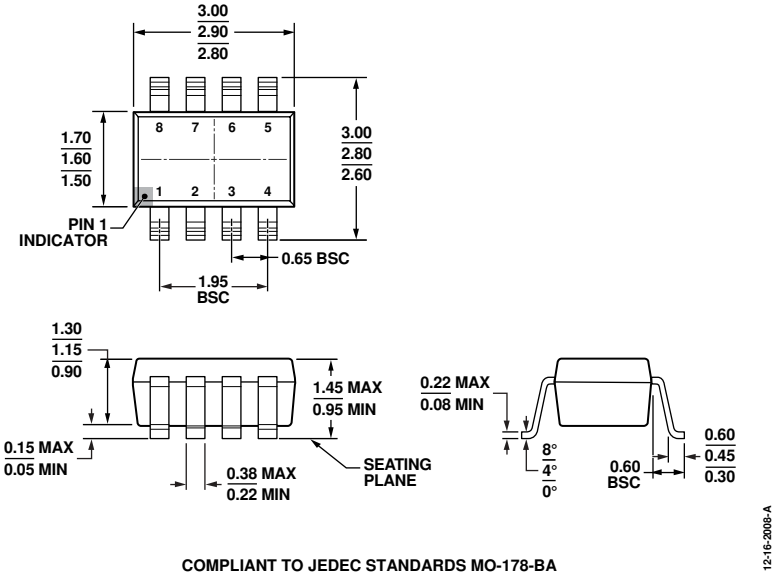
POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5620/AD5640/AD5660 should have separate analog and digital sections, each having its own area of the board. If the AD5620/AD5640/AD5660 are in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5620/AD5640/AD5660.

The power supply to the AD5620/AD5640/AD5660 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be as close as physically possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has a low effective series resistance (ESR) and low effective series inductance (ESI), such as is typical of common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

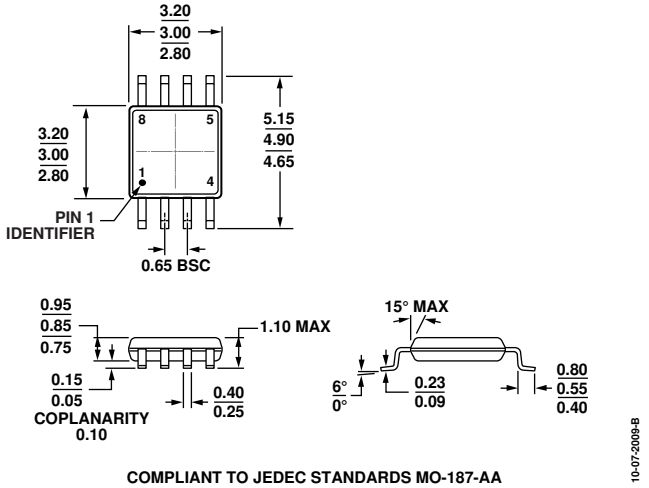
The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other components with fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects on the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS



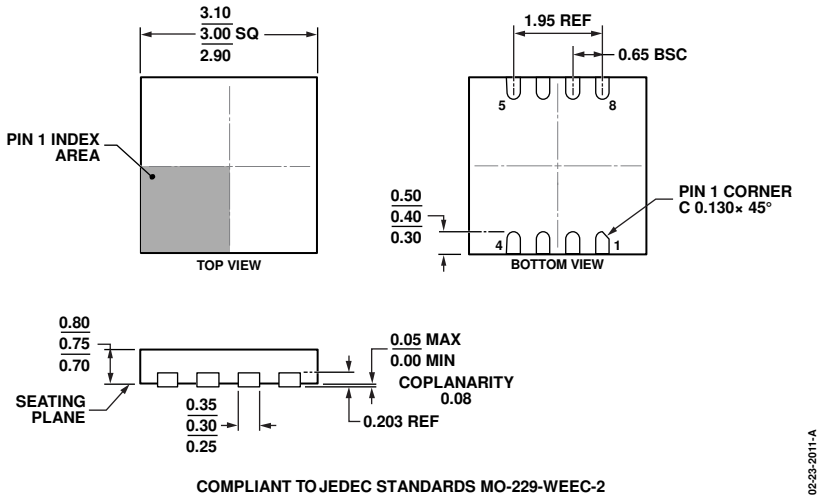
COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 54. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 55. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-229-WEEC-2

Figure 56. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-15)
Dimensions shown in millimeters