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Octal, 12-/14-/16-Bit, SPI Voltage Output *dense*DAC with 5 ppm/°C, On-Chip Reference

Data Sheet

AD5628/AD5648/AD5668

FEATURES

- Low power, small footprint, pin-compatible octal DACs
  - AD5668: 16 bits
  - AD5648: 14 bits
  - AD5628: 12 bits
- 14-lead/16-lead TSSOP, 16-lead LFCSP, and 16-ball WLCSP
- On-chip 1.25 V/2.5 V, 5 ppm/°C reference
- Power down to 400 nA at 5 V, 200 nA at 3 V
- 2.7 V to 5.5 V power supply
- Guaranteed monotonic by design
- Power-on reset to zero scale or midscale
- 3 power-down functions
- Hardware $\overline{\text{LDAC}}$ and $\overline{\text{LDAC}}$ override function
- $\overline{\text{CLR}}$ function to programmable code
- Rail-to-rail operation

APPLICATIONS

- Process control
- Data acquisition systems
- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
- Programmable attenuators

FUNCTIONAL BLOCK DIAGRAM

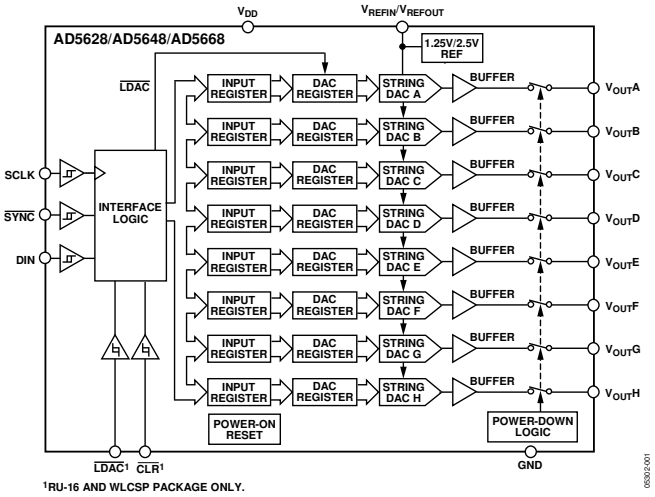

Figure 1.

GENERAL DESCRIPTION

The AD5628/AD5648/AD5668 devices are low power, octal, 12-/14-/16-bit, buffered voltage-output DACs. All devices operate from a single 2.7 V to 5.5 V supply and are guaranteed monotonic by design. The AD5668 and AD5628 are available in both a 4 mm × 4 mm LFCSP and a 16-lead TSSOP, while the AD5648 is available in both a 14-lead and 16-lead TSSOP.

The AD5628/AD5648/AD5668 have an on-chip reference with an internal gain of 2. The AD5628-1/AD5648-1/AD5668-1 have a 1.25 V 5 ppm/°C reference, giving a full-scale output range of 2.5 V; the AD5628-2/AD5648-2/AD5668-2 and AD5668-3 have a 2.5 V 5 ppm/°C reference, giving a full-scale output range of 5 V. The on-board reference is off at power-up, allowing the use of an external reference. The internal reference is enabled via a software write.

The part incorporates a power-on reset circuit that ensures that the DAC output powers up to 0 V (AD5628-1/AD5648-1/AD5668-1, AD5628-2/AD5648-2/AD5668-2) or midscale (AD5668-3) and remains powered up at this level until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 400 nA at 5 V and provides software-selectable output loads while in power-down mode for any or all DAC channels. The outputs of all DACs can be updated simultaneously using the $\overline{\text{LDAC}}$ function, with the added functionality of user-selectable DAC channels to simultaneously update. There is also an asynchronous $\overline{\text{CLR}}$ that updates all DACs to a user-programmable code—zero scale, midscale, or full scale.

The AD5628/AD5648/AD5668 utilize a versatile 3-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards. The on-chip precision output amplifier enables rail-to-rail output swing.

PRODUCT HIGHLIGHTS

1. Octal, 12-/14-/16-bit DAC.
2. On-chip 1.25 V/2.5 V, 5 ppm/°C reference.
3. Available in 14-lead/16-lead TSSOP, 16-lead LFCSP, and 16-ball WLCSP.
4. Power-on reset to 0 V or midscale.
5. Power-down capability. When powered down, the DAC typically consumes 200 nA at 3 V and 400 nA at 5 V.

Rev. J
Document Feedback

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10/2005—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 4.5 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, V_{REFIN} = V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	A Grade[1]			B Grade[1]				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE[2]								
AD5628								
Resolution	12			12			Bits	
Relative Accuracy		±0.5	±4		±0.5	±1	LSB	See Figure 9
Differential Nonlinearity			±0.25			±0.25	LSB	Guaranteed monotonic by design (see Figure 12)
AD5648								
Resolution	14			14			Bits	
Relative Accuracy		±2	±8		±2	±4	LSB	See Figure 8
Differential Nonlinearity			±0.5			±0.5	LSB	Guaranteed monotonic by design (see Figure 11)
AD5668								
Resolution	16			16			Bits	
Relative Accuracy		±8	±32		±8	±16	LSB	See Figure 7
Differential Nonlinearity			±1			±1	LSB	Guaranteed monotonic by design (see Figure 10)
Zero-Code Error		6	19		6	19	mV	All 0s loaded to DAC register (see Figure 26)
Zero-Code Error Drift		±2			±2		µV/°C	
Full-Scale Error		−0.2	−1		−0.2	−1	% FSR	All 1s loaded to DAC register (see Figure 27)
Gain Error			±1			±1	% FSR	
Gain Temperature Coefficient		±2.5			±2.5		ppm	Of FSR/°C
Offset Error		±6	±19		±6	±19	mV	
DC Power Supply Rejection Ratio		−80			−80		dB	V_{DD} ± 10%
DC Crosstalk (External Reference)		10			10		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		5			5		µV/mA	Due to load current change
		10			10		µV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25			25		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10			10		µV/mA	Due to load current change
OUTPUT CHARACTERISTICS[3]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Capacitive Load Stability		2			2		nF	R_L = ∞
		10			10		nF	R_L = 2 kΩ
DC Output Impedance		0.5			0.5		Ω	
Short-Circuit Current		30			30		mA	V_{DD} = 5 V
Power-Up Time		4			4		µs	Coming out of power-down mode, V_{DD} = 5 V
REFERENCE INPUTS								
Reference Current		40	55		40	55	µA	V_{REF} = V_{DD} = 5.5 V (per DAC channel)
Reference Input Range	0		V_{DD}	0		V_{DD}	V	
Reference Input Impedance		14.6			14.6		kΩ	
REFERENCE OUTPUT								
Output Voltage								
AD5628-2/AD5648-2/ AD5668-2, AD5668-3	2.495		2.505	2.495		2.505	V	At ambient
Reference TC[3]		5	10		5	10	ppm/°C	TSSOP
		15			5	10	ppm/°C	LFCSP
Reference Output Impedance		7.5			7.5		kΩ	

Parameter	A Grade[1] Min	A Grade[1] Typ	A Grade[1] Max	B Grade[1] Min	B Grade[1] Typ	B Grade[1] Max	Unit	Test Conditions/Comments
LOGIC INPUTS[3]								
Input Current			±3			±3	μA	All digital inputs
Input Low Voltage, V_{INL}			0.8			0.8	V	V_{DD} = 5 V
Input High Voltage, V_{INH}	2			2			V	V_{DD} = 5 V
Pin Capacitance		3			3		pF	
POWER REQUIREMENTS								
V_{DD}	4.5		5.5	4.5		5.5	V	All digital inputs at 0 or V_{DD}, DAC active, excludes load current
I_{DD} (Normal Mode)[4]								$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		1.0	1.5		1.0	1.5	mA	Internal reference off
V_{DD} = 4.5 V to 5.5 V		1.8	2.25		1.7	2.25	mA	Internal reference on
I_{DD} (All Power-Down Modes)[5]								
V_{DD} = 4.5 V to 5.5 V		0.4	1		0.4	1	μA	$V_{IH} = V_{DD}$ and V_{IL} = GND

[1] Temperature range is −40°C to +105°C, typical at 25°C.
[2] Linearity calculated using a reduced code range of AD5628 (Code 32 to Code 4064), AD5648 (Code 128 to Code 16,256), and AD5668 (Code 512 to 65,024). Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All eight DACs powered down.

V_{DD} = 2.7 V to 3.6 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, V_{REFIN} = V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	A Grade[1] Min	A Grade[1] Typ	A Grade[1] Max	B Grade[1] Min	B Grade[1] Typ	B Grade[1] Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[2]								
AD5628								
Resolution	12			12			Bits	
Relative Accuracy		±0.5	±4		±0.5	±1	LSB	See Figure 9
Differential Nonlinearity			±0.25			±0.25	LSB	Guaranteed monotonic by design (see Figure 12)
AD5648								
Resolution	14			14			Bits	
Relative Accuracy		±2	±8		±2	±4	LSB	See Figure 8
Differential Nonlinearity			±0.5			±0.5	LSB	Guaranteed monotonic by design (see Figure 11)
AD5668								
Resolution	16			16			Bits	
Relative Accuracy		±8	±32		±8	±16	LSB	See Figure 7
Differential Nonlinearity			±1			±1	LSB	Guaranteed monotonic by design (see Figure 10)
Zero-Code Error		6	19		6	19	mV	All 0s loaded to DAC register (see Figure 26)
Zero-Code Error Drift		±2			±2		µV/°C	
Full-Scale Error		−0.2	−1		−0.2	−1	% FSR	All 1s loaded to DAC register (see Figure 27)
Gain Error			±1			±1	% FSR	
Gain Temperature Coefficient		±2.5			±2.5		ppm	Of FSR/°C
Offset Error		±6	±19		±6	±19	mV	
DC Power Supply Rejection Ratio[3]		−80			−80		dB	V_{DD} ± 10%
DC Crosstalk[3] (External Reference)		10			10		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		5			5		µV/mA	Due to load current change
		10			10		µV	Due to powering down (per channel)
DC Crosstalk[3] (Internal Reference)		25			25		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10			10		µV/mA	Due to load current change
OUTPUT CHARACTERISTICS[3]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Capacitive Load Stability		2			2		nF	R_L = ∞
		10			10		nF	R_L = 2 kΩ
DC Output Impedance		0.5			0.5		Ω	
Short-Circuit Current		30			30		mA	V_{DD} = 3 V
Power-Up Time		4			4		µs	Coming out of power-down mode, V_{DD} = 3 V
REFERENCE INPUTS								
Reference Current		40	55		40	55	µA	V_{REF} = V_{DD} = 5.5 V (per DAC channel)
Reference Input Range	0		V_{DD}	0		V_{DD}		
Reference Input Impedance		14.6			14.6		kΩ	
REFERENCE OUTPUT								
Output Voltage								
AD5628/AD5648/AD5668-1	1.247		1.253	1.247		1.253	V	At ambient
Reference TC[3]		5	15		5	15	ppm/°C	TSSOP
		15			5	15	ppm/°C	LFCSP
					15		ppm/°C	WLCSP
Reference Output Impedance		7.5			7.5		kΩ	

Parameter	A Grade[1] Min	Typ	Max	B Grade[1] Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS[3]								
Input Current			±3			±3	μA	All digital inputs
Input Low Voltage, V_{INL}			0.8			0.8	V	V_{DD} = 3 V
Input High Voltage, V_{INH}	2			2			V	V_{DD} = 3 V
Pin Capacitance		3			3		pF	
POWER REQUIREMENTS								
V_{DD}	2.7		3.6	2.7		3.6	V	All digital inputs at 0 or V_{DD}, DAC active, excludes load current
I_{DD} (Normal Mode)[4]								$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		1.0	1.5		1.0	1.5	mA	Internal reference off
V_{DD} = 2.7 V to 3.6 V		1.8	2.25		1.7	2.25	mA	Internal reference on
I_{DD} (All Power-Down Modes)[5]								
V_{DD} = 2.7 V to 3.6 V		0.2	1		0.2	1	μA	$V_{IH} = V_{DD}$ and V_{IL} = GND

[1] Temperature range is −40°C to +105°C, typical at 25°C.
[2] Linearity calculated using a reduced code range of AD5628 (Code 32 to Code 4064), AD5648 (Code 128 to Code 16256), and AD5668 (Code 512 to 65024). Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All eight DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, $V_{REFIN} = V_{DD}$. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments[3]
Output Voltage Settling Time		2.5	7	μs	¼ to ¾ scale settling to ±2 LSB (16-bit resolution)
Slew Rate		1.2		V/μs	
Digital-to-Analog Glitch Impulse		4		nV-s	1 LSB (16-bit resolution) change around major carry (see Figure 42)
		19		nV-s	From code 0xEA00 to code 0xE9FF (16-bit resolution)
Digital Feedthrough		0.1		nV-s	
Digital Crosstalk		0.2		nV-s	
Analog Crosstalk		0.4		nV-s	
DAC-to-DAC Crosstalk		0.8		nV-s	
Multiplying Bandwidth		320		kHz	V_{REF} = 2 V ± 0.2 V p-p
Total Harmonic Distortion		−80		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code = 0x8400(16-bit resolution), 1 kHz
		100		nV/√Hz	DAC code = 0x8400(16-bit resolution), 10 kHz
Output Noise		12		μV p-p	0.1 Hz to 10 Hz, DAC code = 0x0000

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +105°C, typical at 25°C.

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 2. V_{DD} = 2.7 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX} V_{DD} = 2.7 V to 5.5 V	Unit	Test Conditions/Comments
t_1[1]	20	ns min	SCLK cycle time
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ to SCLK falling edge set-up time
t_5	4	ns min	Data set-up time
t_6	4	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	15	ns min	Minimum $\overline{SYNC}$ high time
t_9	13	ns min	$\overline{SYNC}$ rising edge to SCLK fall ignore
t_{10}	0	ns min	SCLK falling edge to $\overline{SYNC}$ fall ignore
t_{11}	10	ns min	$\overline{LDAC}$ pulse width low
t_{12}	15	ns min	SCLK falling edge to $\overline{LDAC}$ rising edge
t_{13}	5	ns min	$\overline{CLR}$ pulse width low
t_{14}	0	ns min	SCLK falling edge to $\overline{LDAC}$ falling edge
t_{15}	300	ns typ	$\overline{CLR}$ pulse activation time

[1] Maximum SCLK frequency is 50 MHz at V_{DD} = 2.7 V to 5.5 V. Guaranteed by design and characterization; not production tested.

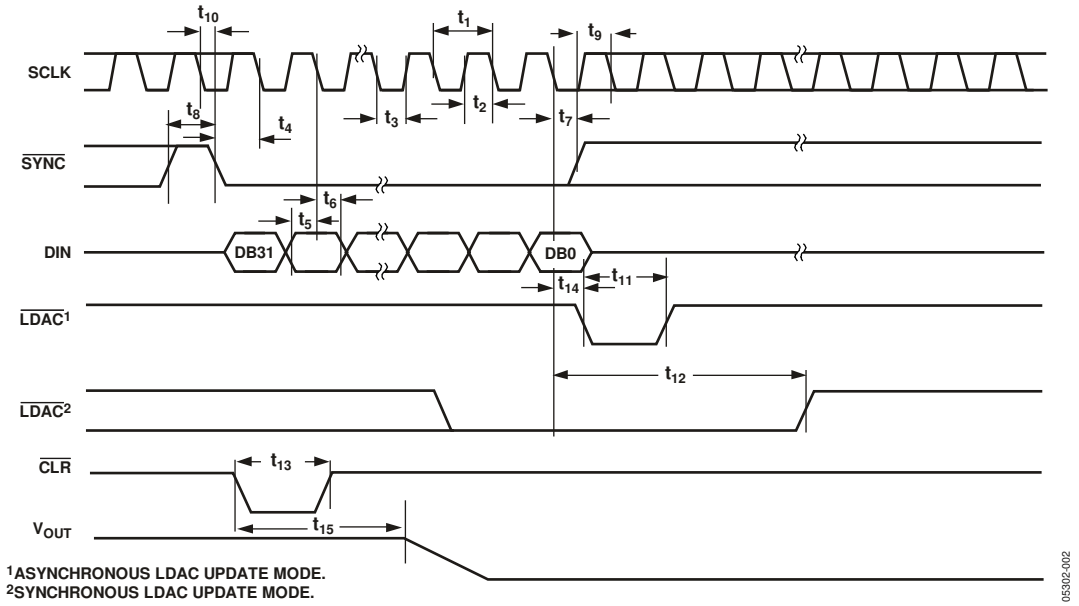

Figure 2. Serial Write Operation

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REFIN}/V_{REFOUT} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\ MAX}$)	150°C
Reflow Soldering Peak Temperature	
Pb Free	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
RU-14[1]	121	35	°C/W
RU-16[1]	113.5	35	°C/W
CP-16-17[2]	50.6	30	°C/W
CB-16-16[1]	45		°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board. See JEDEC JESD51.
[2] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

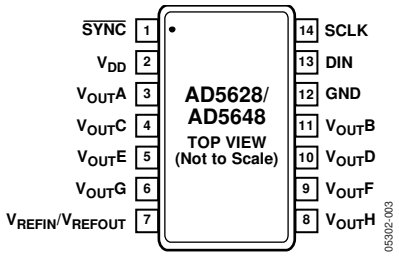

Figure 3. 14-Lead TSSOP (RU-14)

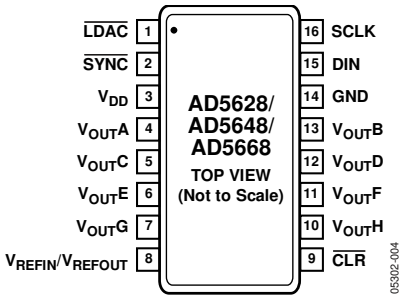

Figure 4. 16-Lead TSSOP (RU-16)

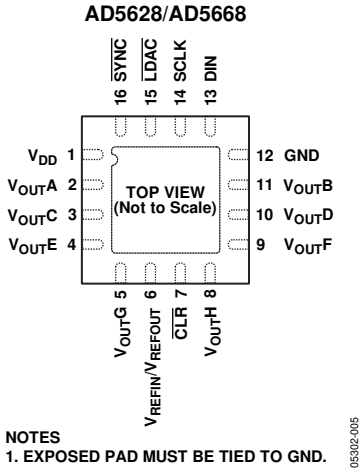

Figure 5. 16-Lead LFCSP (CP-16-17)

Table 7. Pin Function Descriptions

Pin No.				
14-Lead TSSOP	**16-Lead TSSOP**	**16-Lead LFCSP**	**Mnemonic**	**Description**
Not applicable	1	15	$\overline{\text{LDAC}}$	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. Alternatively, this pin can be tied permanently low.
1	2	16	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{SYNC}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
2	3	1	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
3	4	2	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
11	13	11	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
4	5	3	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
10	12	10	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
7	8	6	V_{REFIN}/ V_{REFOUT}	The AD5628/AD5648/AD5668 have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.
Not applicable	9	7	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the $\overline{\text{CLR}}$ code register—zero, midscale, or full scale. Default setting clears the output to 0 V.
5	6	4	$V_{OUT}E$	Analog Output Voltage from DAC E. The output amplifier has rail-to-rail operation.
9	11	9	$V_{OUT}F$	Analog Output Voltage from DAC F. The output amplifier has rail-to-rail operation.
6	7	5	$V_{OUT}G$	Analog Output Voltage from DAC G. The output amplifier has rail-to-rail operation.
8	10	8	$V_{OUT}H$	Analog Output Voltage from DAC H. The output amplifier has rail-to-rail operation.
12	14	12	GND	Ground Reference Point for All Circuitry on the Part.
13	15	13	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
14	16	14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
Not applicable	Not applicable	EPAD	EPAD	It is recommended that the exposed paddle be soldered to the ground plane.

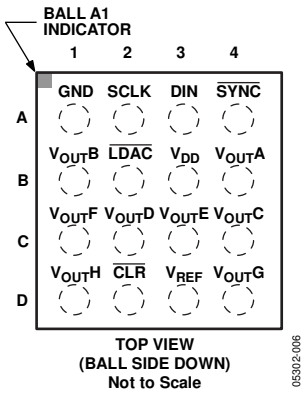

Figure 6. 16-Ball WLCSP (CB-16-16)

Table 8. 16-Ball WLCSP Pin Function Descriptions

Pin. No.	Mnemonic	Description
B2	$\overline{\text{LDAC}}$	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. Alternatively, this pin can be tied permanently low.
A4	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{SYNC}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
B3	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
B4	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
B1	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
C4	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
C2	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
D3	V_{REFIN}/V_{REFOUT}	The AD5628/AD5648/AD5668 have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.
D2	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the $\overline{\text{CLR}}$ code register—zero, midscale, or full scale. Default setting clears the output to 0 V.
C3	$V_{OUT}E$	Analog Output Voltage from DAC E. The output amplifier has rail-to-rail operation.
C1	$V_{OUT}F$	Analog Output Voltage from DAC F. The output amplifier has rail-to-rail operation.
D4	$V_{OUT}G$	Analog Output Voltage from DAC G. The output amplifier has rail-to-rail operation.
D1	$V_{OUT}H$	Analog Output Voltage from DAC H. The output amplifier has rail-to-rail operation.
A1	GND	Ground Reference Point for All Circuitry on the Part.
A3	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
A2	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

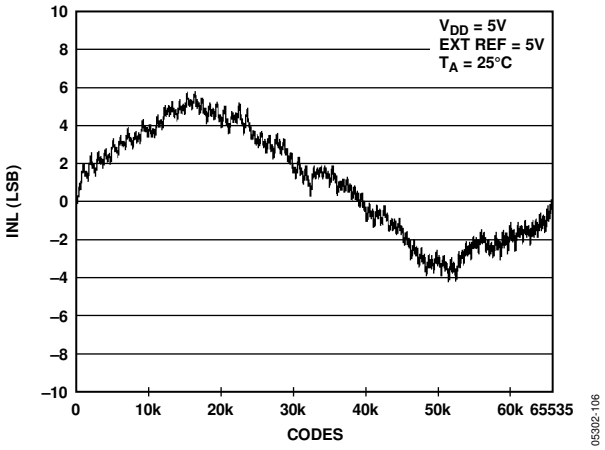

Figure 7. INL AD5668—External Reference

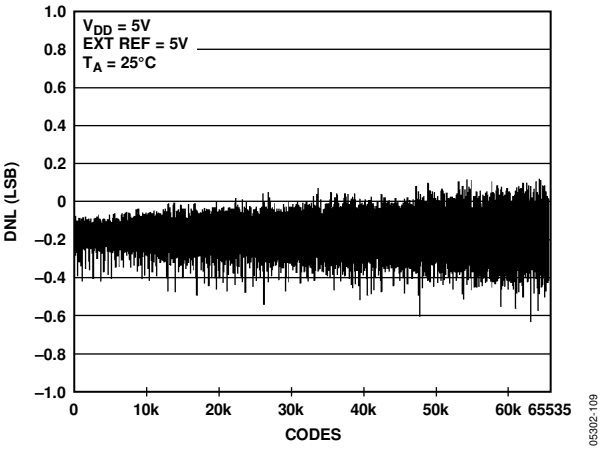

Figure 10. DNL AD5668—External Reference

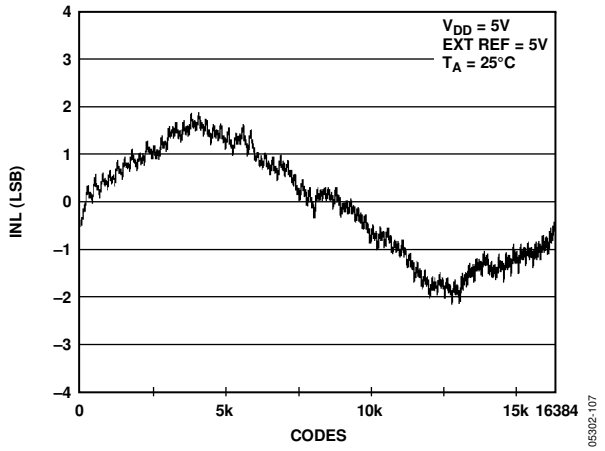

Figure 8. INL AD5648—External Reference

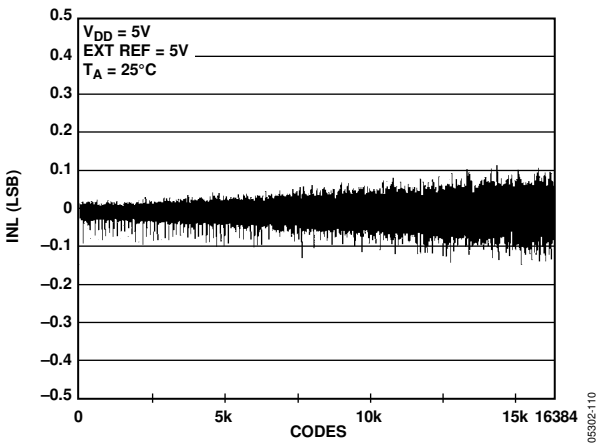

Figure 11. DNL AD5648—External Reference

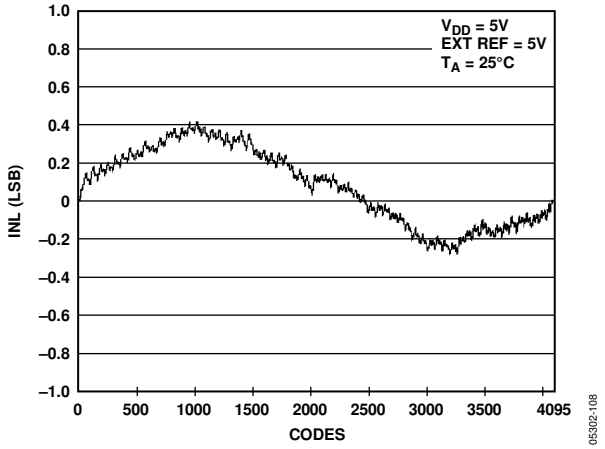

Figure 9. INL AD5628—External Reference

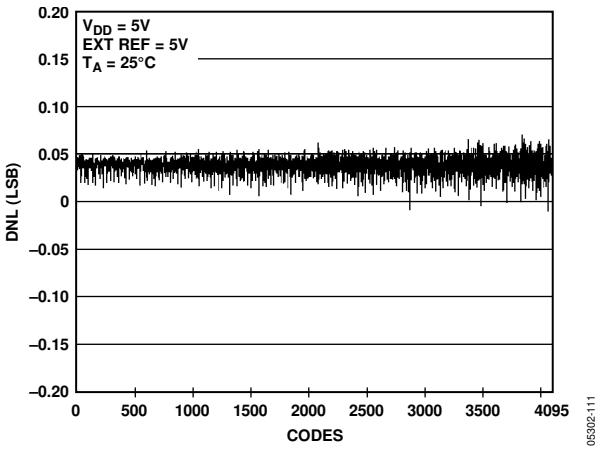

Figure 12. DNL AD5628—External Reference

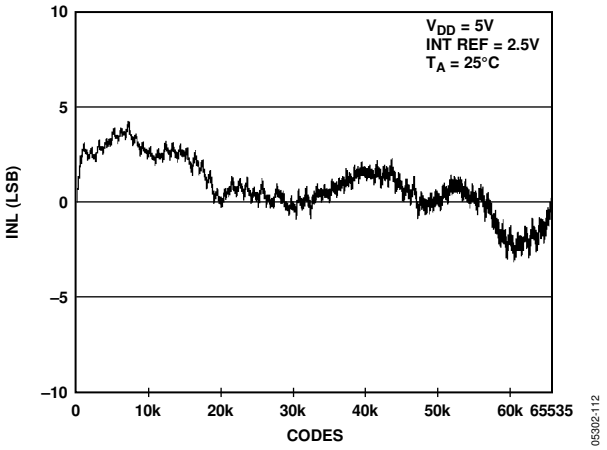

Figure 13. INL AD5668-2/AD5668-3

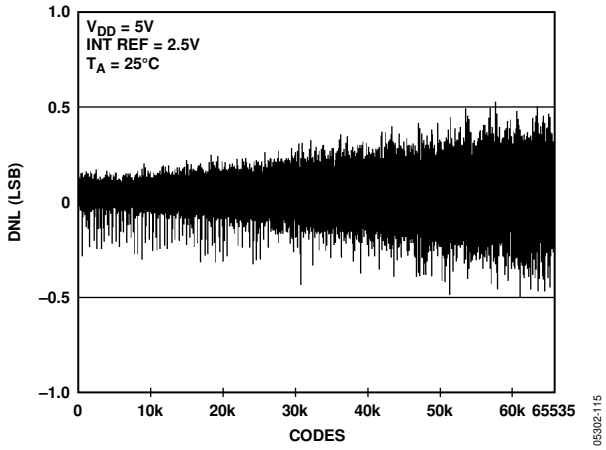

Figure 16. DNL AD5668-2/AD5668-3

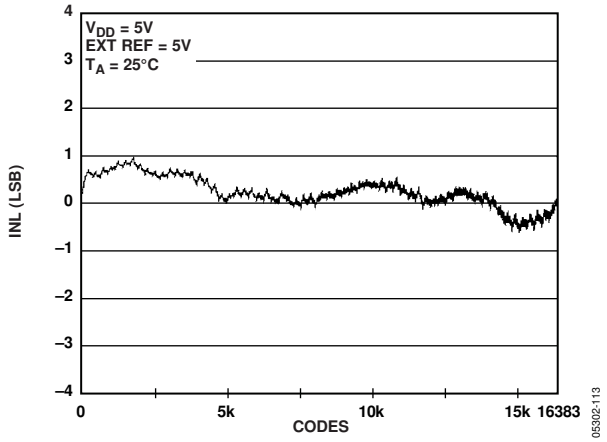

Figure 14. INL AD5648-2

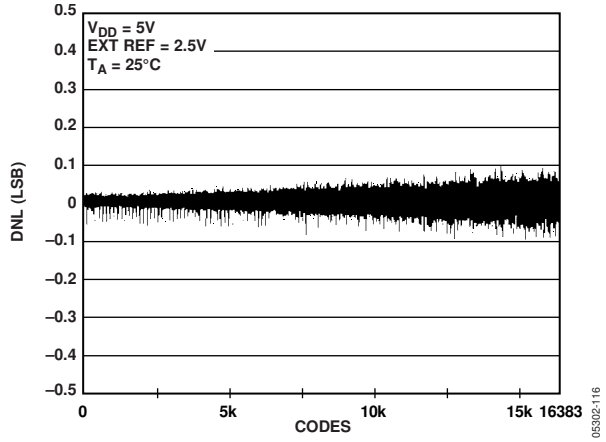

Figure 17. DNL AD5648-2

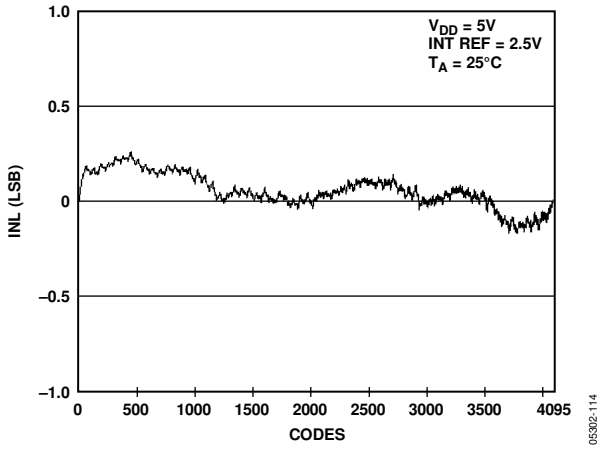

Figure 15. INL AD5628-2

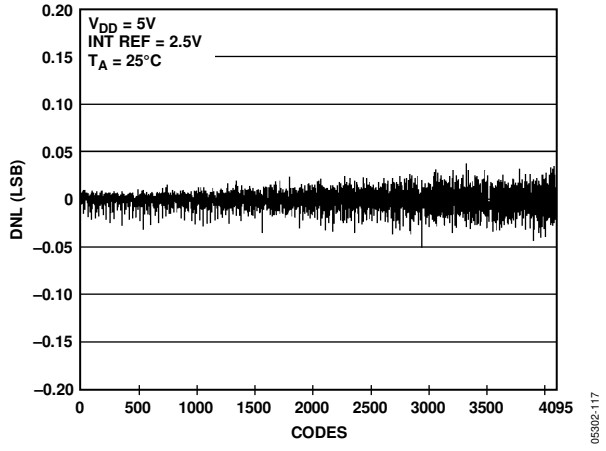

Figure 18. DNL AD5628-2

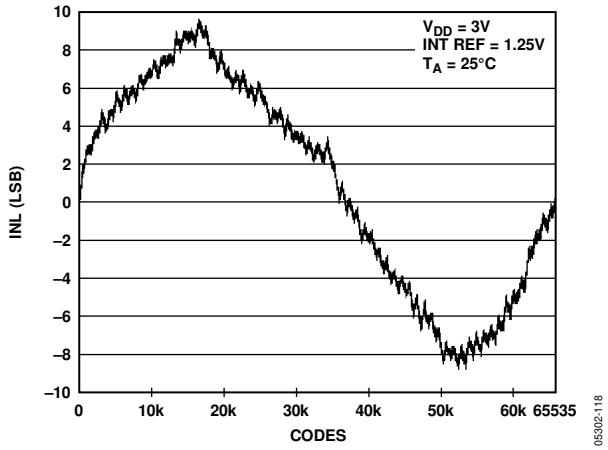

Figure 19. INL AD5668-1

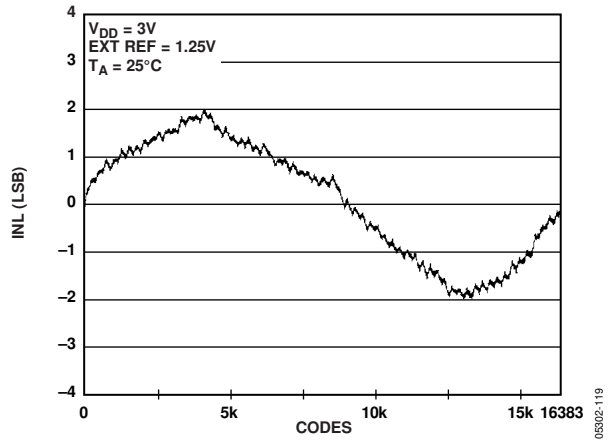

Figure 20. INL AD5648-1

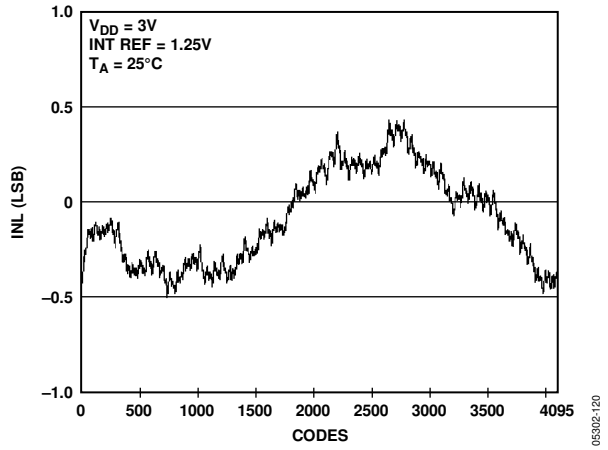

Figure 21. INL AD5628-1

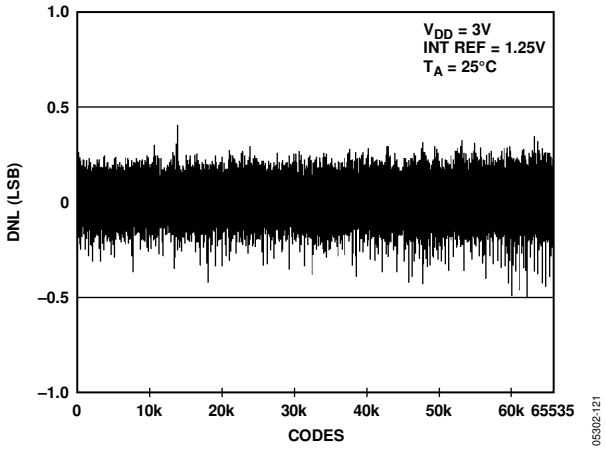

Figure 22. DNL AD5668-1

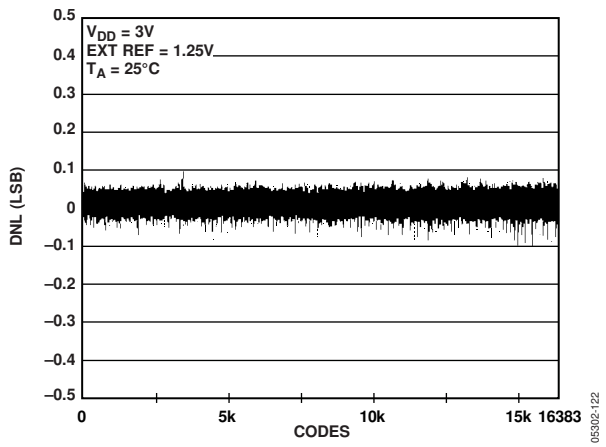

Figure 23. DNL AD5648-1

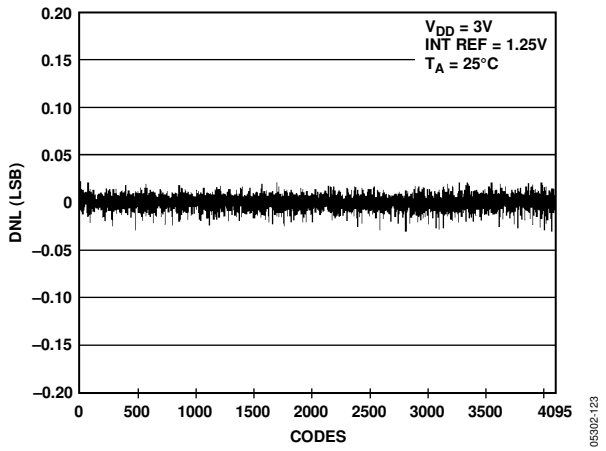

Figure 24. DNL AD5628-1

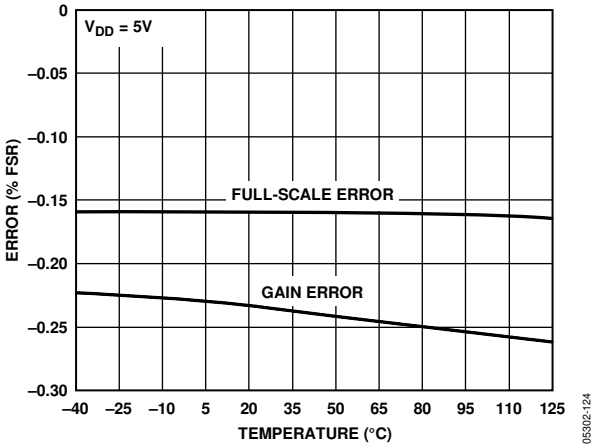

Figure 25. Gain Error and Full-Scale Error vs. Temperature

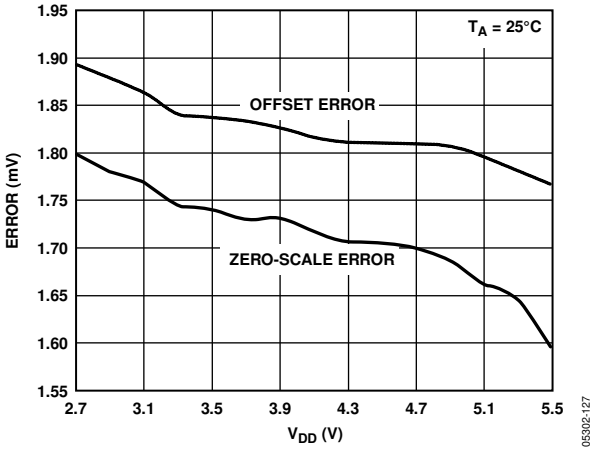

Figure 28. Zero-Scale Error and Offset Error vs. Supply Voltage

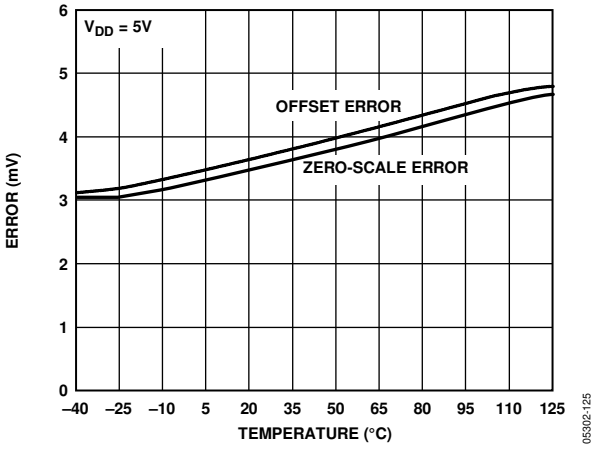

Figure 26. Zero-Scale Error and Offset Error vs. Temperature

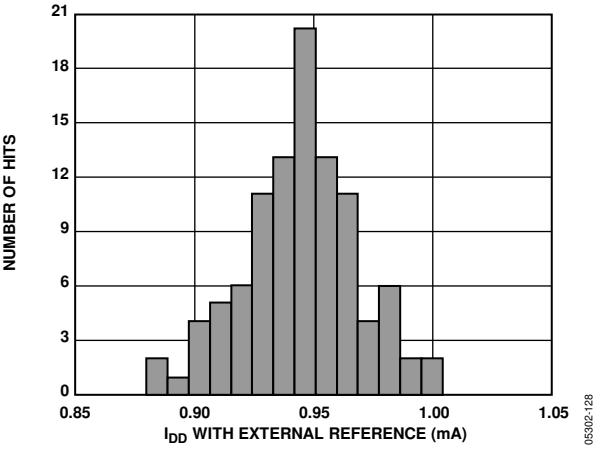

Figure 29. I_{DD} Histogram with External Reference

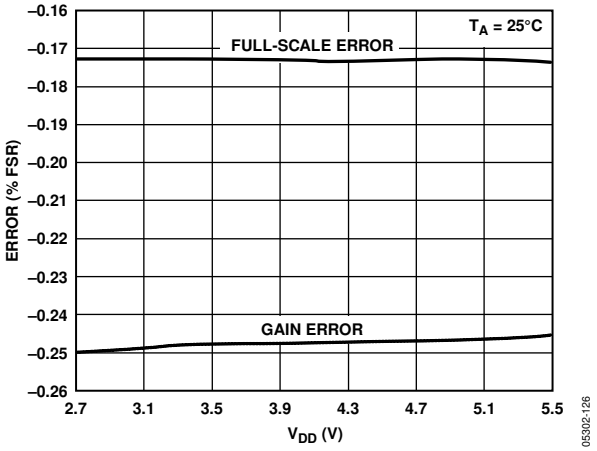

Figure 27. Gain Error and Full-Scale Error vs. Supply Voltage

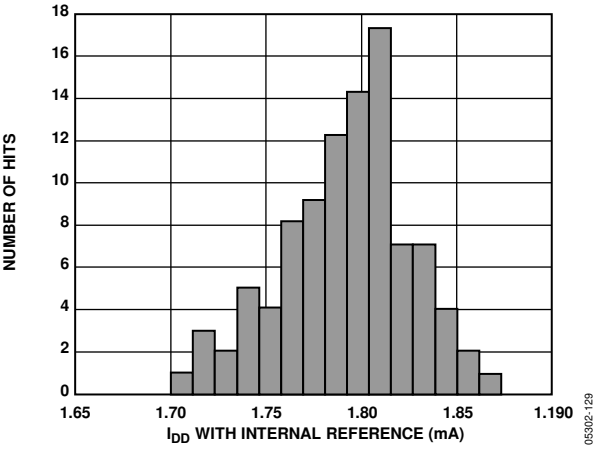

Figure 30. I_{DD} Histogram with Internal Reference

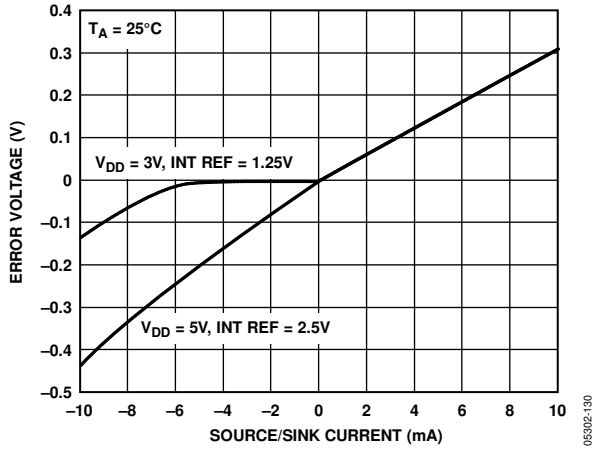

Figure 31. Headroom at Rails vs. Source and Sink

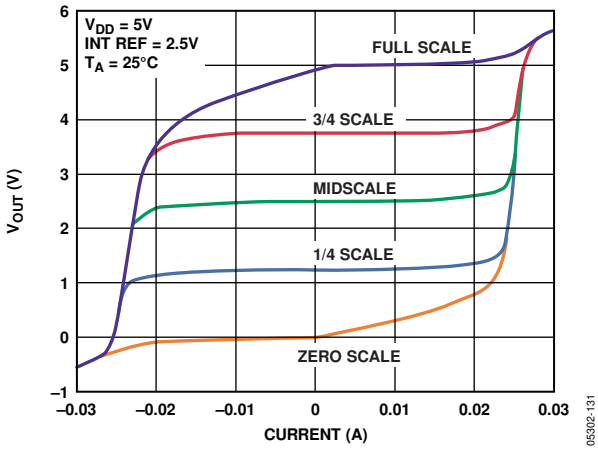

Figure 32. AD5668-2/AD5668-3 Source and Sink Capability

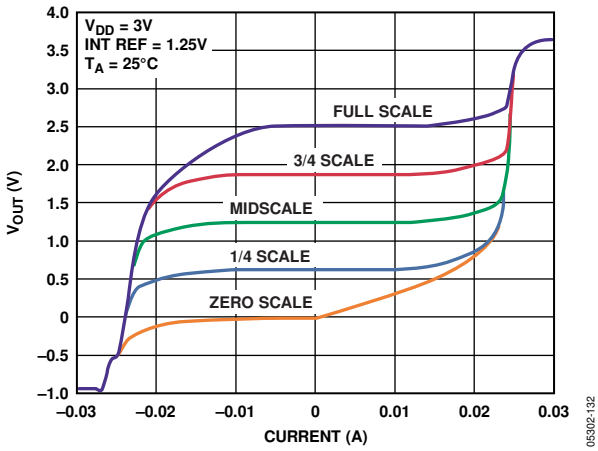

Figure 33. AD5668-1 Source and Sink Capability

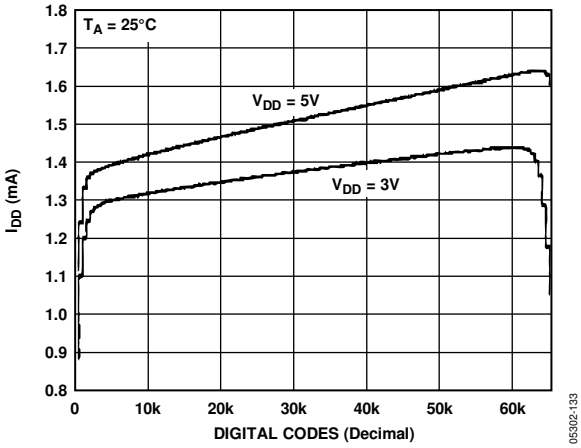

Figure 34. Supply Current vs. Code

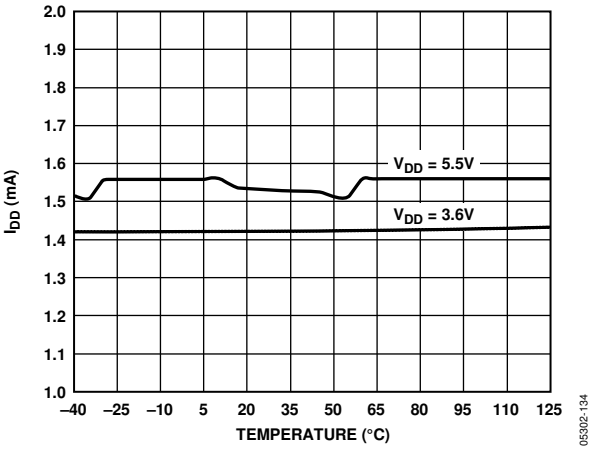

Figure 35. Supply Current vs. Temperature

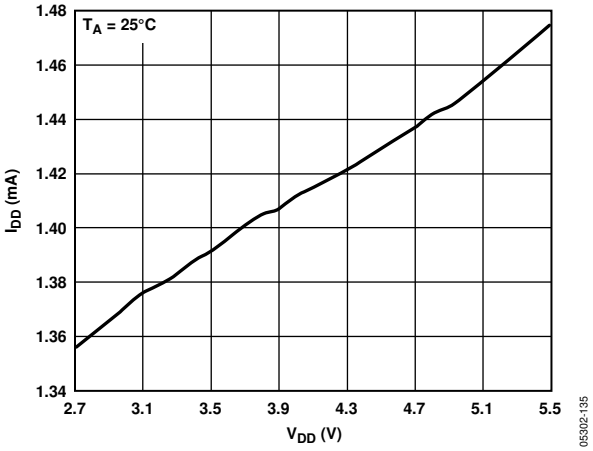

Figure 36. Supply Current vs. Supply Voltage

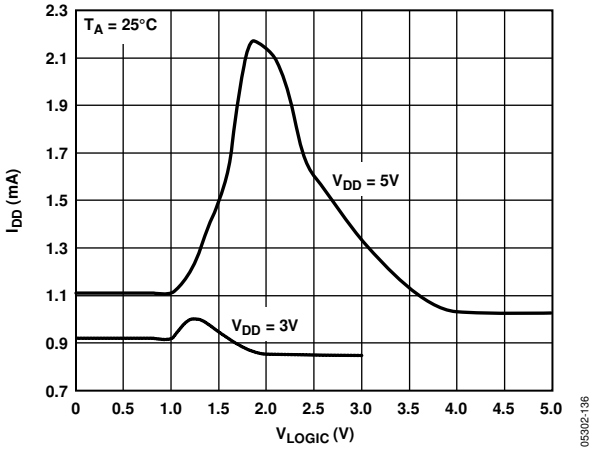

Figure 37. Supply Current vs. Logic Input Voltage

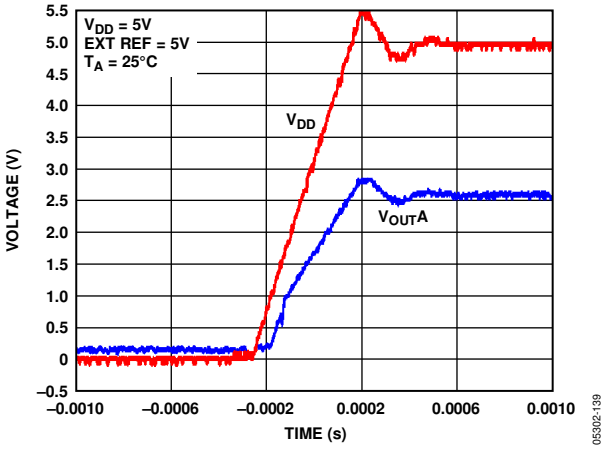

Figure 40. Power-On Reset to Midscale

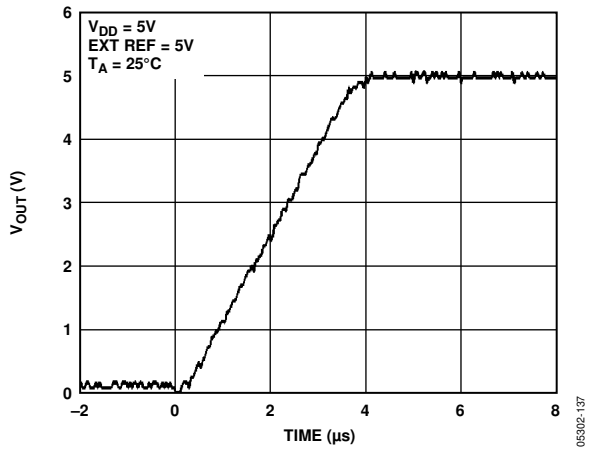

Figure 38. Full-Scale Settling Time, 5 V

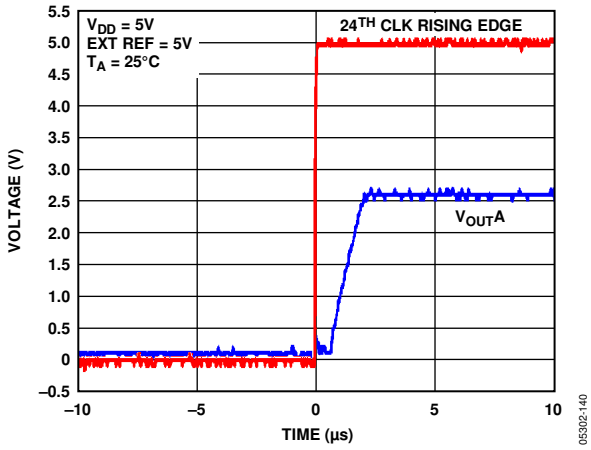

Figure 41. Exiting Power-Down to Midscale

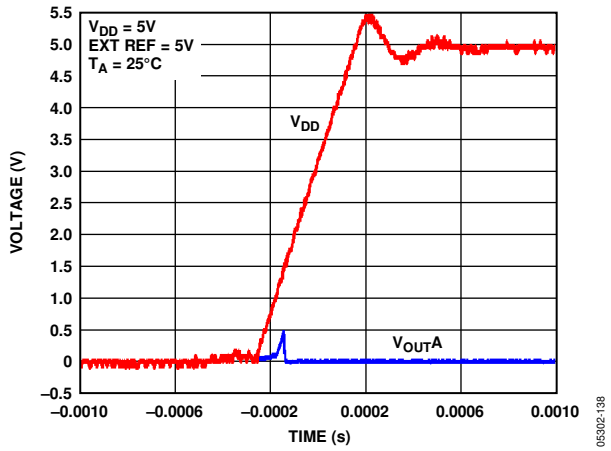

Figure 39. Power-On Reset to 0 V

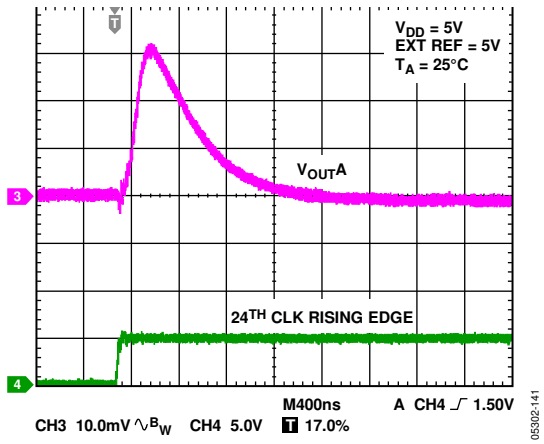

Figure 42. Digital-to-Analog Glitch Impulse (Negative)

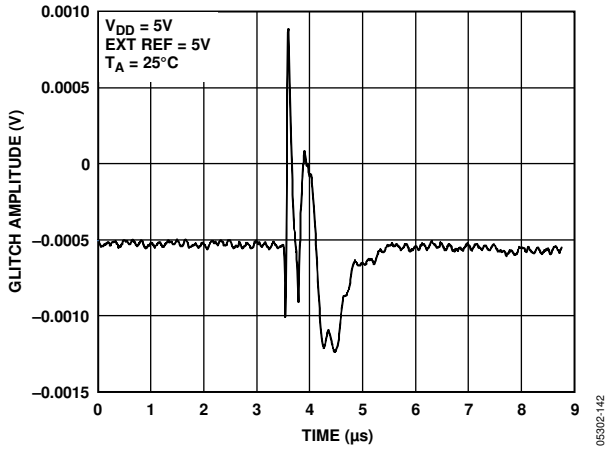

Figure 43. Analog Crosstalk

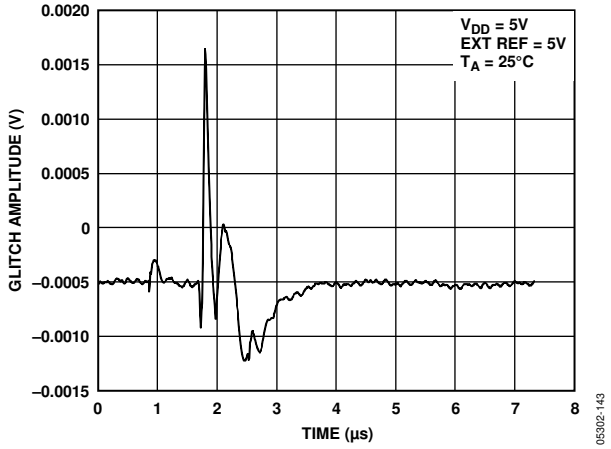

Figure 44. DAC-to-DAC Crosstalk

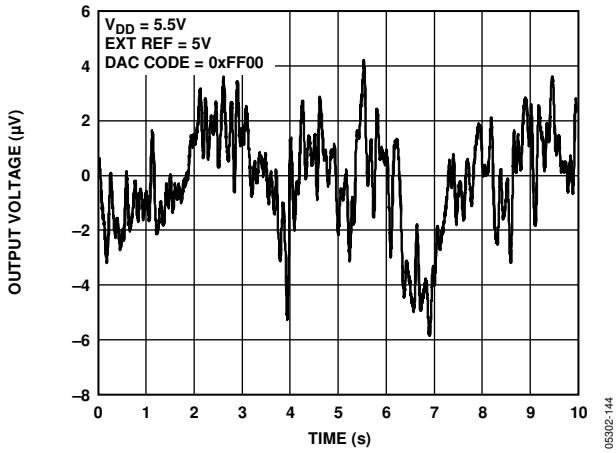

Figure 45. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

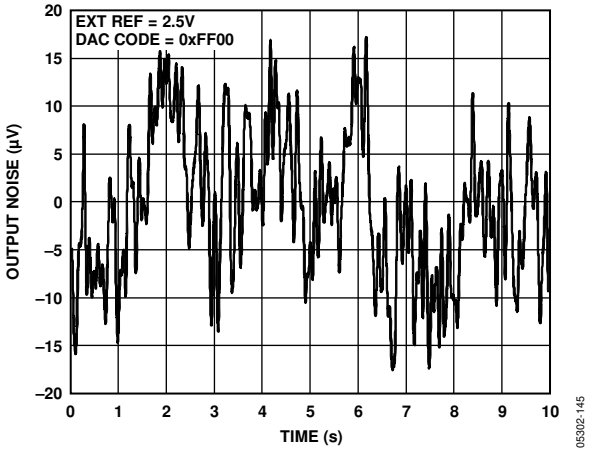

Figure 46. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

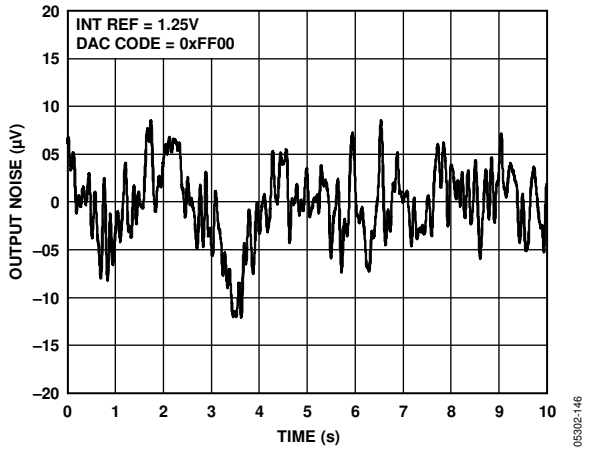

Figure 47. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

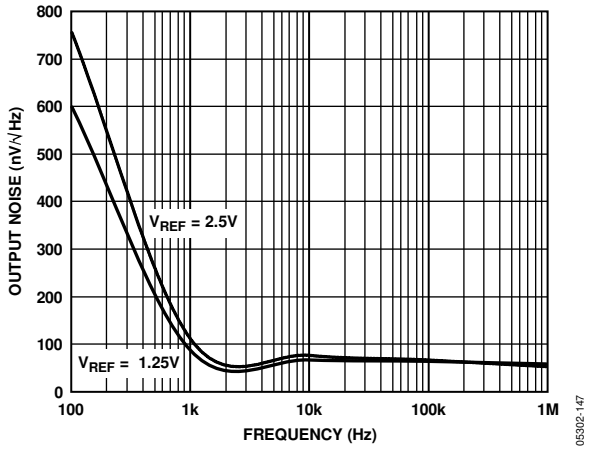

Figure 48. Noise Spectral Density, Internal Reference

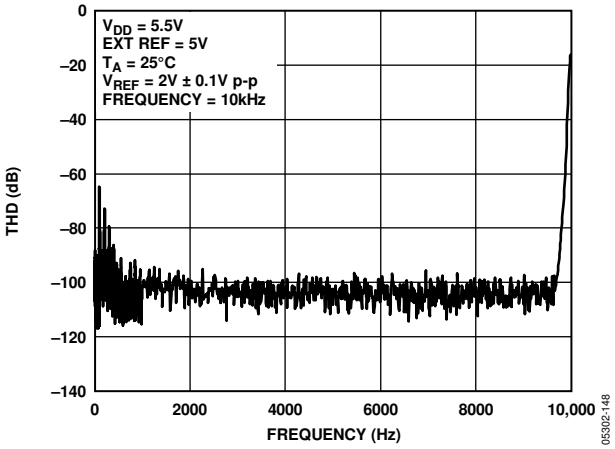

Figure 49. Total Harmonic Distortion

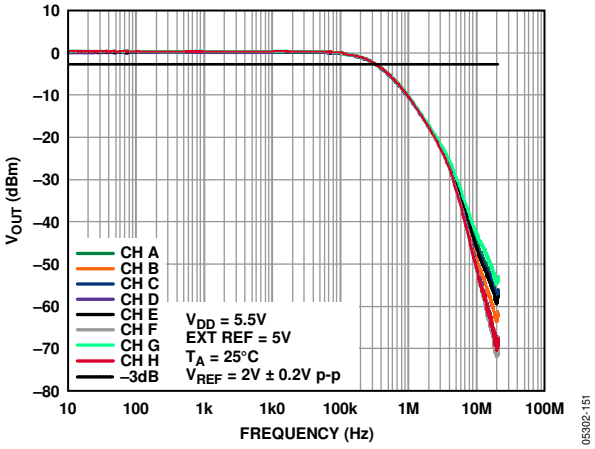

Figure 52. Multiplying Bandwidth

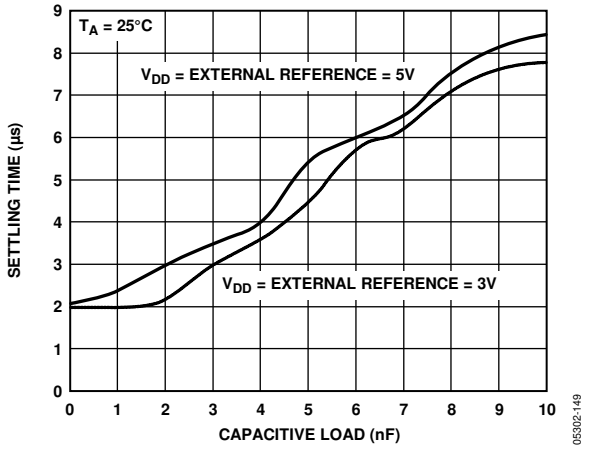

Figure 50. Settling Time vs. Capacitive Load

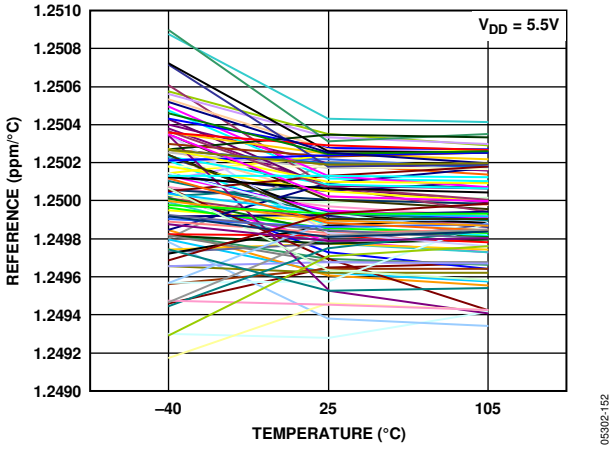

Figure 53. 1.25 V Reference Temperature Coefficient vs. Temperature

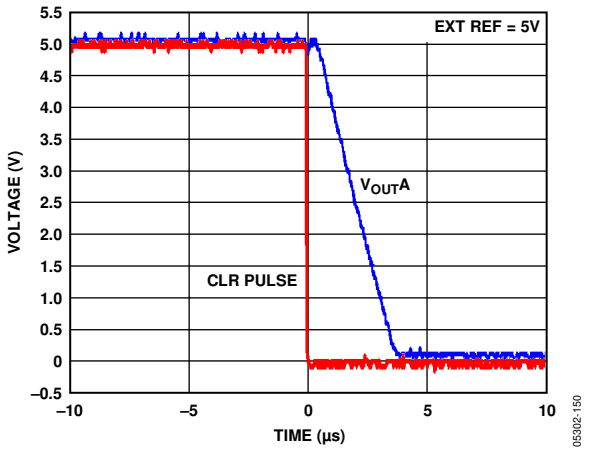

Figure 51. Hardware $\overline{CLR}$

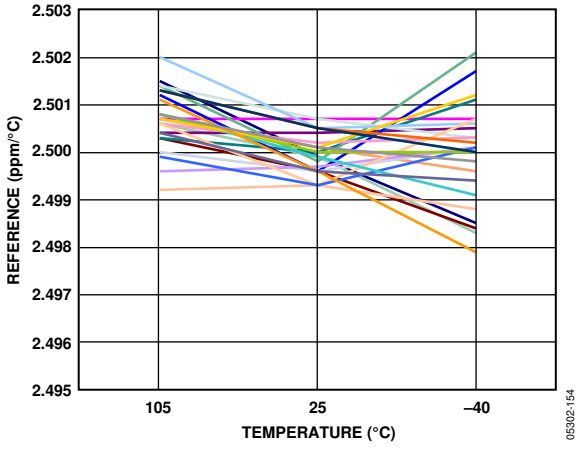

Figure 54. 2.5 V Reference Temperature Coefficient vs. Temperature

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function. Figure 7 to Figure 9, Figure 13 to Figure 15, and Figure 19 to Figure 21 show plots of typical INL vs. code.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Figure 10 to Figure 12, Figure 16 to Figure 18, and Figure 22 to Figure 24 show plots of typical DNL vs. code.

Offset Error
Offset error is a measure of the difference between the actual V_{OUT} and the ideal V_{OUT}, expressed in millivolts in the linear region of the transfer function. Offset error is measured on the AD5668 with Code 512 loaded into the DAC register. It can be negative or positive and is expressed in millivolts.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x0000) is loaded into the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5628/AD5648/AD5668, because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in millivolts. Figure 28 shows a plot of typical zero-code error vs. temperature.

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range.

Zero-Code Error Drift

Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift

Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded into the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range. Figure 25 shows a plot of typical full-scale error vs. temperature.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 42.

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in decibels. V_{REF} is held at 2 V, and V_{DD} is varied ±10%.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in microvolts.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in microvolts per milliamp.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, $\overline{\text{LDAC}}$ is high). It is expressed in decibels.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device, but is measured when the DAC is not being written to ($\overline{\text{SYNC}}$ held high). It is specified in nV-s and measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s or vice versa.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s or vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s or vice versa) while keeping $\overline{\text{LDAC}}$ high, and then pulsing $\overline{\text{LDAC}}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s or vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
Total harmonic distortion is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in decibels.

THEORY OF OPERATION

DAC SECTION

The AD5628/AD5648/AD5668 DACs are fabricated on a CMOS process. The architecture consists of a string of DACs followed by an output buffer amplifier. Each part includes an internal 1.25 V/2.5 V, 5 ppm/°C reference with an internal gain of 2. Figure 55 shows a block diagram of the DAC architecture.

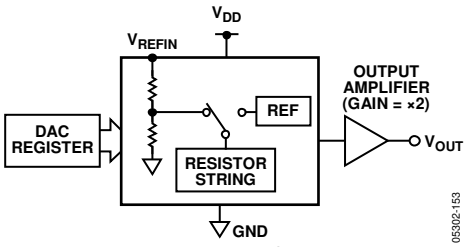

Figure 55. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N} \right)$$

The ideal output voltage when using the internal reference is given by

$$V_{OUT} = 2 \times V_{REFOUT} \times \left(\frac{D}{2^N} \right)$$

where:
D = decimal equivalent of the binary code that is loaded to the DAC register.
  0 to 4095 for AD5628 (12 bits).
  0 to 16,383 for AD5648 (14 bits).
  0 to 65,535 for AD5668 (16 bits).
N = the DAC resolution.

RESISTOR STRING

The resistor string section is shown in Figure 56. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

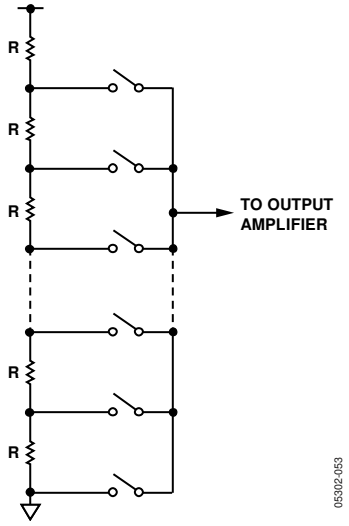

Figure 56. Resistor String

INTERNAL REFERENCE

The AD5628/AD5648/AD5668 have an on-chip reference with an internal gain of 2. The AD5628/AD5648/AD5668-1 have a 1.25 V, 5 ppm/°C reference, giving a full-scale output of 2.5 V; the AD5628/AD5648/AD5668-2, AD5668-3 have a 2.5 V, 5 ppm/°C reference, giving a full-scale output of 5 V. The on-board reference is off at power-up, allowing the use of an external reference. The internal reference is enabled via a write to the control register (see Table 9).

The internal reference associated with each part is available at the V_{REFOUT} pin. A buffer is required if the reference output is used to drive external loads. When using the internal reference, it is recommended that a 100 nF capacitor be placed between the reference output and GND for reference stability.

Individual channel power-down is not supported while using the internal reference.

OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. The amplifier is capable of driving a load of 2 kΩ in parallel with 200 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 32 and Figure 33. The slew rate is 1.5 V/µs with a ¼ to ¾ scale settling time of 7 µs.

SERIAL INTERFACE

The AD5628/AD5648/AD5668 have a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the DIN line is clocked into the 32-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the AD5628/AD5648/AD5668 compatible with high speed DSPs. On the 32nd falling clock edge, the last data bit is clocked in and the programmed function is executed, that is, a change in DAC register contents and/or a change in the mode of operation. At this stage, the $\overline{SYNC}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 15 ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. $\overline{SYNC}$ should be idled low between write sequences for even lower power operation of the part. As is mentioned previously, however, $\overline{SYNC}$ must be brought high again just before the next write sequence.

Table 9. Command Definitions

Command				
C3	C2	C1	C0	Description
0	0	0	0	Write to Input Register n
0	0	0	1	Update DAC Register n
0	0	1	0	Write to Input Register n, update all (software $\overline{LDAC}$)
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Load clear code register
0	1	1	0	Load $\overline{LDAC}$ register
0	1	1	1	Reset (power-on reset)
1	0	0	0	Set up internal REF register
1	0	0	1	Reserved
–	–	–	–	Reserved
1	1	1	1	Reserved

Table 10. Address Commands

Address (n)				
A3	A2	A1	A0	Selected DAC Channel
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	1	1	1	All DACs

INPUT SHIFT REGISTER

The input shift register is 32 bits wide. The first four bits are don't cares. The next four bits are the command bits, C3 to C0 (see Table 9), followed by the 4-bit DAC address, A3 to A0 (see Table 10) and finally the 16-/14-/12-bit data-word. The data-word comprises the 16-/14-/12-bit input code followed by four, six, or eight don't care bits for the AD5668, AD5648, and AD5628, respectively (see Figure 57 through Figure 59). These data bits are transferred to the DAC register on the 32nd falling edge of SCLK.

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for 32 falling edges of SCLK, and the DAC is updated on the 32nd falling edge and rising edge of $\overline{\text{SYNC}}$. However, if $\overline{\text{SYNC}}$ is brought high before the 32nd falling edge, this acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 60).

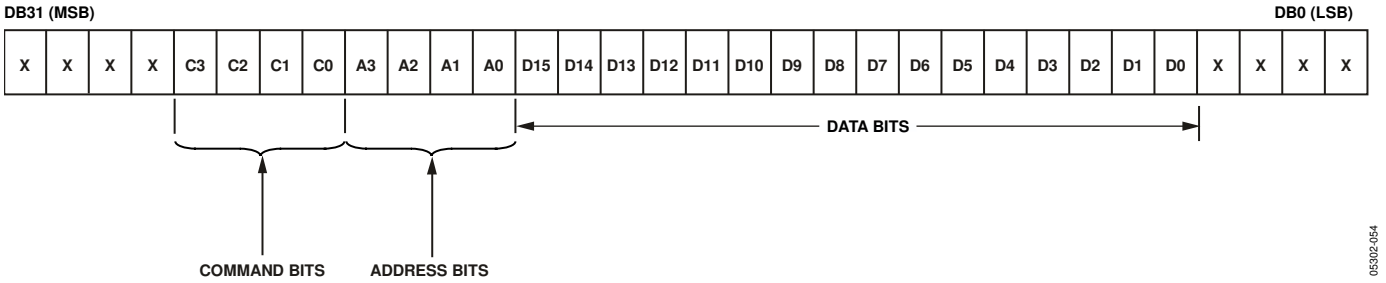

Figure 57. AD5668 Input Register Contents

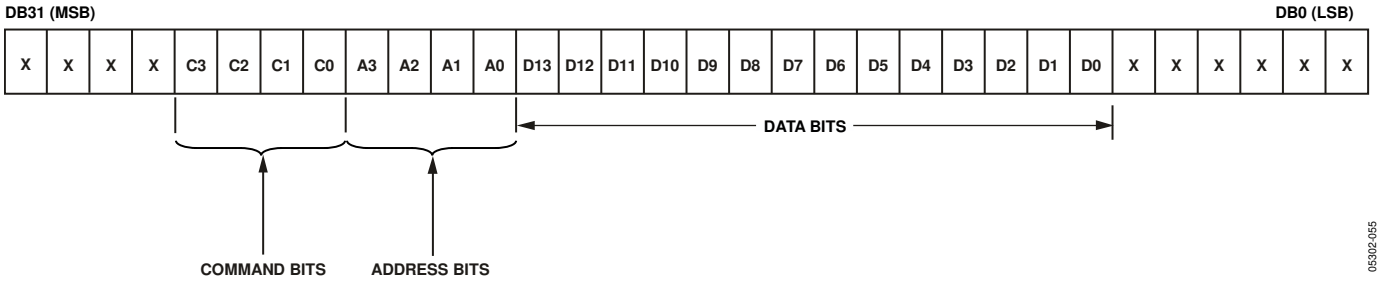

Figure 58. AD5648 Input Register Contents

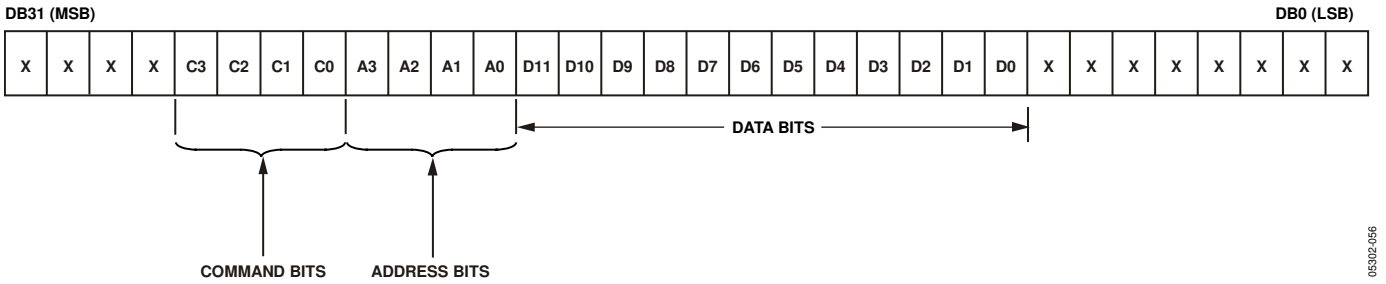

Figure 59. AD5628 Input Register Contents

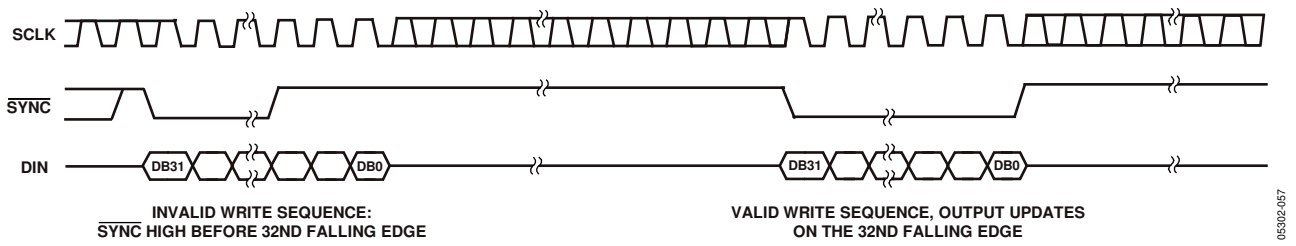

Figure 60. $\overline{\text{SYNC}}$ Interrupt Facility

INTERNAL REFERENCE REGISTER

The on-board reference is off at power-up by default. This allows the use of an external reference if the application requires it. The on-board reference can be turned on or off by a user-programmable internal REF register by setting Bit DB0 high or low (see Table 11). Command 1000 is reserved for setting the internal REF register (see Table 9). Table 13 shows how the state of the bits in the input shift register corresponds to the mode of operation of the device.

POWER-ON RESET

The AD5628/AD5648/AD5668 family contains a power-on reset circuit that controls the output voltage during power-up. The AD5628/AD5648/AD5668-1, -2 DAC output powers up to 0 V, and the AD5668-3 DAC output powers up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0111 is reserved for this reset function (see Table 9). Any events on $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ during power-on reset are ignored.

POWER-DOWN MODES

The AD5628/AD5648/AD5668 contain four separate modes of operation. Command 0100 is reserved for the power-down function (see Table 9). These modes are software-programmable by setting two bits, Bit DB9 and Bit DB8, in the control register.

Table 13 shows how the state of the bits corresponds to the mode of operation of the device. Any or all DACs (DAC H to DAC A) can be powered down to the selected mode by setting the corresponding eight bits (DB7 to DB0) to 1. See Table 14 for the contents of the input shift register during power-down/power-up operation. When using the internal reference, only all channel power-down to the selected modes is supported.

When both bits are set to 0, the part works normally with its normal power consumption of 1.3 mA at 5 V. However, for the three power-down modes, the supply current falls to 0.4 μA at 5 V (0.2 μA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through either a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 61.

The bias generator of the selected DAC(s), output amplifier, resistor string, and other associated linear circuitry are shut down when the power-down mode is activated. The internal reference is powered down only when all channels are powered down. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4 μs for V_{DD} = 5 V and for V_{DD} = 3 V. See Figure 41 for a plot.

Any combination of DACs can be powered up by setting PD1 and PD0 to 0 (normal operation). The output powers up to the value in the input register ($\overline{\text{LDAC}}$ low) or to the value in the DAC register before powering down ($\overline{\text{LDAC}}$ high).

CLEAR CODE REGISTER

The AD5628/AD5648/AD5668 have a hardware $\overline{\text{CLR}}$ pin that is an asynchronous clear input. The $\overline{\text{CLR}}$ input is falling edge sensitive. Bringing the $\overline{\text{CLR}}$ line low clears the contents of the input register and the DAC registers to the data contained in the user-configurable $\overline{\text{CLR}}$ register and sets the analog outputs accordingly. This function can be used in system calibration to load zero scale, midscale, or full scale to all channels together. These clear code values are user-programmable by setting two bits, Bit DB1 and Bit DB0, in the $\overline{\text{CLR}}$ control register (see Table 15). The default setting clears the outputs to 0 V. Command 0101 is reserved for loading the clear code register (see Table 9).

The part exits clear code mode on the 32nd falling edge of the next write to the part. If $\overline{\text{CLR}}$ is activated during a write sequence, the write is aborted.

The $\overline{\text{CLR}}$ pulse activation time—the falling edge of $\overline{\text{CLR}}$ to when the output starts to change—is typically 280 ns. However, if outside the DAC linear region, it typically takes 520 ns after executing $\overline{\text{CLR}}$ for the output to start changing (see Figure 51).

See Table 16 for contents of the input shift register during the loading clear code register operation.