
Chipsmall
深圳市津利帝科技有限公司
Geelead Technology Limited
Chipsmall
采购部

Multiple Range, 16-/12-Bit, Bipolar/Unipolar Voltage Output DACs with 2 ppm/°C Reference

Data Sheet

AD5761R/AD5721R

FEATURES

- **8 software-programmable output ranges: 0 V to 5 V, 0 V to 10 V, 0 V to 16 V, 0 V to 20 V, ±3 V, ±5 V, ±10 V, and −2.5 V to +7.5 V; 5% overrange**
- **Low drift 2.5 V reference: ±2 ppm/°C typical**
- **Total unadjusted error (TUE): 0.1% FSR maximum**
- **16-bit resolution: ±2 LSB maximum INL**
- **Guaranteed monotonicity: ±1 LSB maximum**
- **Single channel, 16-/12-bit DACs**
- **Settling time: 7.5 μs typical**
- **Integrated reference buffers**
- **Low noise: 35 nV/√Hz**
- **Low glitch: 1 nV-sec (0 V to 5 V range)**
- **1.7 V to 5.5 V digital supply range**
- **Asynchronous updating via $\overline{\text{LDAC}}$**
- **Asynchronous $\overline{\text{RESET}}$ to zero scale/midscale**
- **DSP-/microcontroller-compatible serial interface**
- **Robust 4 kV HBM ESD rating**
- **16-lead, 3 mm × 3 mm LFCSP package**
- **16-lead TSSOP package**
- **Operating temperature range: −40°C to +125°C**

APPLICATIONS

- **Industrial automation**
- **Instrumentation, data acquisition**
- **Open-/closed-loop servo control, process control**
- **Programmable logic controllers**

GENERAL DESCRIPTION

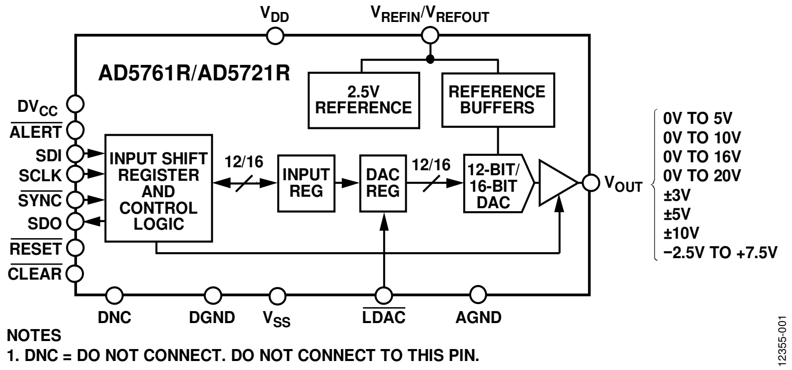
The AD5761R/AD5721R are single channel, 16-/12-bit serial input, voltage output, digital-to-analog converters (DACs). They operate from single supply voltages from 4.75 V to 30 V or dual supply voltages from −16.5 V to 0 V V_{SS} and 4.75 V to 16.5 V V_{DD}. The integrated output amplifier, reference buffer, and reference provide a very easy to use, universal solution.

The devices offer guaranteed monotonicity, integral nonlinearity (INL) of ±2 LSB maximum, 35 nV/√Hz noise, and 7.5 μs settling time on selected ranges.

The AD5761R/AD5721R use a serial interface that operates at clock rates of up to 50 MHz and are compatible with DSP and microcontroller interface standards. Double buffering allows the asynchronous updating of the DAC output. The input coding is user-selectable twos complement or straight binary. The asynchronous reset function resets all registers to their default state. The output range is user selectable, via the RA[2:0] bits in the control register.

The devices available in a 3 mm × 3 mm LFCSP package and a 16-lead TSSOP package offer guaranteed specifications over the −40°C to +125°C industrial temperature range.

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 1.

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5/2015—Rev. 0 to Rev. A

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11/2014—Revision 0: Initial Version

SPECIFICATIONS

V_{DD}[1] = 4.75 V to 30 V, V_{SS}[1] = −16.5 V to 0 V, AGND = DGND = 0 V, V_{REFIN}/V_{REFOUT} = 2.5 V external, DV_{CC} = 1.7 V to 5.5 V, R_{LOAD} = 1 kΩ for all ranges except 0 V to 16 V and 0 V to 20 V for which R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[2]	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					External reference[3] and internal reference, outputs unloaded
Programmable Output Ranges	0		5	V	
	0		10	V	
	0		16	V	
	0		20	V	
	−2.5		+7.5	V	
	−3		+3	V	
	−5		+5	V	
	−10		+10	V	
AD5761R					
Resolution	16			Bits	
Relative Accuracy, INL					
A Grade	−8		+8	LSB	External reference[3] and internal reference
B Grade[4]	−2		+2	LSB	All ranges except 0 V to 16 V and 0 V to 20 V, V_{REFIN}/V_{REFOUT} = 2.5 V external and internal reference
Differential Nonlinearity, DNL	−1		+1	LSB	
AD5721R					
Resolution	12			Bits	
Relative Accuracy, INL					
B Grade	−0.5		+0.5	LSB	External reference[3] and internal reference
Differential Nonlinearity, DNL	−0.5		+0.5	LSB	
Zero-Scale Error	−6		+6	mV	All ranges except ±10 V and 0 V to 20 V, external reference[3]
	−10		+10	mV	0 V to 20 V, ±10 V ranges, external reference[3]
	−6		+6	mV	All ranges except ±5 V, ±10 V and 0 V to 20 V, internal reference
	−8		+8	mV	±5 V range, internal reference
	−9		+9	mV	0 V to 20 V range, internal reference
	−13		+13	mV	±10 V range, internal reference
Zero-Scale Temperature Coefficient (TC)[5]		±5		µV/°C	Unipolar ranges, external reference[3] and internal reference
		±15		µV/°C	Bipolar ranges, external reference[3] and internal reference
Bipolar Zero Error	−5		+5	mV	All bipolar ranges except ±10 V
	−7		+7	mV	±10 V output range
Bipolar Zero TC[5]		±2		µV/°C	±3 V range, external reference[3] and internal reference
		±5		µV/°C	All bipolar ranges except ±3 V range, external reference[3] and internal reference
Offset Error	−6		+6	mV	All ranges except ±10 V and 0 V to 20 V, external reference[3]
	−10		+10	mV	0 V to 20 V, ±10 V ranges, external reference[3]
	−6		+6	mV	All ranges except ±5 V, ±10 V, and 0 V to 20 V; internal reference
	−8		+8	mV	±5 V range, internal reference
	−9		+9	mV	0 V to 20 V range, internal reference
	−13		+13	mV	±10 V range, internal reference

Parameter[2]	Min	Typ	Max	Unit	Test Conditions/Comments
Offset Error TC[5]		±5		µV/°C	Unipolar ranges, external reference[3] and internal reference
		±15		µV/°C	Bipolar ranges, external reference[3] and internal reference
Gain Error	−0.1		+0.1	% FSR	External reference[3]
	−0.15		+0.15	% FSR	Internal reference
Gain Error TC[5]		±1.5		ppm FSR/°C	External reference[3] and internal reference
TUE	−0.1		+0.1	% FSR	External reference[3]
	−0.15		+0.15	% FSR	Internal reference
REFERENCE INPUT (EXTERNAL)[5]					
Reference Input Voltage (V_{REF})		2.5		V	±1% for specified performance
Input Current	−2	±0.5	+2	µA	
Reference Range	2		3	V	
REFERENCE OUTPUT (INTERNAL)[5]					
Output Voltage		2.5		V	±3 mV, at ambient temperature
Voltage Reference TC		2	5	ppm/°C	
Output Impedance		25		kΩ	
Output Voltage Noise		6		µV p-p	0.1 Hz to 10 Hz
Noise Spectral Density		10		nV/√Hz	At ambient; f = 10 kHz
Line Regulation		6		µV/V	At ambient
Thermal Hysteresis		80		ppm	First temperature cycle
Start-Up Time		3.5		ms	Coming out of power-down mode with a 10 nF capacitor on the V_{REFIN}/V_{REFOUT} pin to improve noise performance; outputs unloaded
OUTPUT CHARACTERISTICS[5]					
Output Voltage Range	$-V_{OUT}$		$+V_{OUT}$		See Table 7 for the different output voltage ranges available
	−10		+10	V	V_{DD}/V_{SS} = ±11 V, ±10 V output range
	−10.5		+10.5	V	V_{DD}/V_{SS} = ±11 V, ±10 V output range with 5% overrange
Capacitive Load Stability			1	nF	
Headroom		0.5	1	V	R_{LOAD} = 1 kΩ for all ranges except 0 V to16 V and 0 V to 20 V ranges (R_{LOAD} = 2 kΩ)
Output Voltage TC		±3		ppm FSR/°C	±10 V range, external reference
Short-Circuit Current		25		mA	Short on the V_{OUT} pin
Resistive Load			1	kΩ	All ranges except 0 V to16 V and 0 V to 20 V
			2	kΩ	0 V to 16 V, 0 V to 20 V ranges
Load Regulation		0.3		mV/mA	Outputs unloaded
DC Output Impedance		0.5		Ω	Outputs unloaded
LOGIC INPUTS[5]					DV_{CC} = 1.7 V to 5.5 V, JEDEC compliant
Input Voltage					
High, V_{IH}	0.7 × DV_{CC}			V	
Low, V_{IL}			0.3 × DV_{CC}	V	
Input Current					
Leakage Current	−1		+1	µA	SDI, SCLK, $\overline{\text{SYNC}}$
	−1		+1	µA	$\overline{\text{LDAC}}$, $\overline{\text{CLEAR}}$, $\overline{\text{RESET}}$ pins held high
	−55			µA	$\overline{\text{LDAC}}$, $\overline{\text{CLEAR}}$, $\overline{\text{RESET}}$ pins held low
Pin Capacitance		5		pF	Per pin, outputs unloaded

Parameter[2]	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (SDO, $\overline{\text{ALERT}}$)[5]					
Output Voltage					
Low, V_{OL}			0.4	V	DV_{CC} = 1.7 V to 5.5 V, sinking 200 μA
High, V_{OH}	DV_{CC} − 0.5			V	DV_{CC} = 1.7 V to 5.5 V, sourcing 200 μA
High Impedance, SDO Pin					
Leakage Current	−1		+1	μA	
Pin Capacitance		5		pF	
POWER REQUIREMENTS					
V_{DD}	4.75		30	V	
V_{SS}	−16.5		0	V	
DV_{CC}	1.7		5.5	V	
I_{DD}		5.1	6.5	mA	Outputs unloaded, external reference
I_{SS}		1	3	mA	Outputs unloaded
DI_{CC}		0.005	1	μA	$V_{IH} = DV_{CC}$, V_{IL} = DGND
Power Dissipation		67.1		mW	±11 V operation, outputs unloaded, TSSOP package
DC Power Supply Rejection Ratio (PSRR)[5]		0.1		mV/V	V_{DD} ± 10%, V_{SS} = −15 V
		0.1		mV/V	V_{SS} ±10%, V_{DD} = +15 V
AC PSRR[5]		65		dB	V_{DD} ±200 mV, 50 Hz/60 Hz, V_{SS} = −15 V, internal reference, C_{LOAD} = 100 nF
		65		dB	V_{SS} ±200 mV, 50 Hz/60 Hz, V_{DD} = +15 V, internal reference, C_{LOAD} = 100 nF
		80		dB	V_{DD} ±200 mV, 50 Hz/60 Hz, V_{SS} = −15 V, external reference, C_{LOAD} = unloaded
		80		dB	V_{SS} ±200 mV, 50 Hz/60 Hz, V_{DD} = +15 V, external reference, C_{LOAD} = unloaded

[1] For specified performance, headroom requirement is 1 V.
[2] Temperature range: −40°C to +125°C, typical at +25°C.
[3] External reference means 2 V to 2.85 V with overrange and 2 V to 3 V without overrange.
[4] Integral nonlinearity error is specified at ±4 LSB (min/max) for 16 V and 20 V ranges with V_{REFIN}/V_{REFOUT} = 2.5 V external and internal, and for all ranges with V_{REFIN}/V_{REFOUT} = 2 V to 2.85 V with overrange and 2 V to 3 V without overrange.
[5] Guaranteed by design and characterization, not production tested.

AC PERFORMANCE CHARACTERISTICS

V_{DD}[1] = 4.75 V to 30 V, V_{SS}[1] = −16.5 V to 0 V, AGND = DGND = 0 V, V_{REFIN}/V_{REFOUT} = 2.5 V external, DV_{CC} = 1.7 V to 5.5 V, R_{LOAD} = 1 kΩ for all ranges except 0 V to 16 V and 0 V to 20 V for which R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[2]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[3]					
Output Voltage Settling Time		9	12.5	µs	20 V step to 1 LSB at 16-bit resolution
		7.5	8.5	µs	10 V step to 1 LSB at 16-bit resolution
			5	µs	512 LSB step to 1 LSB at 16-bit resolution
Digital-to-Analog Glitch Impulse		8		nV-sec	±10 V range
		1		nV-sec	0 V to 5 V range
Glitch Impulse Peak Amplitude		15		mV	±10 V range
		10		mV	0 V to 5 V range
Power-On Glitch		100		mV p-p	
Digital Feedthrough		0.6		nV-sec	
Output Noise					
0.1 Hz to 10 Hz Bandwidth		15		µV p-p	
100 kHz Bandwidth		45		µV rms	0 V to 20 V and 0 V to 16 V ranges, 2.5 V external reference
		35		µV rms	0 V to 10 V, ±10 V, and −2.5 V to +7.5 V ranges, 2.5 V external reference
		25		µV rms	±5 V range, 2.5 V external reference
		15		µV rms	0 V to 5 V and ±3 V ranges, 2.5 V external reference
Output Noise Spectral Density, at 10 kHz		80		nV/√Hz	±10 V range, 2.5 V external reference
		35		nV/√Hz	±3 V range, 2.5 V external reference
		70		nV/√Hz	±5 V, 0 V to 10 V, and −2.5 V to +7.5 V ranges, 2.5 V external reference
		110		nV/√Hz	0 V to 20 V range, 2.5 V external reference
		90		nV/√Hz	0 V to 16 V range, 2.5 V external reference
		45		nV/√Hz	0 V to 5 V range, 2.5 V external reference
Total Harmonic Distortion (THD)[4]		−87		dB	2.5 V external reference, 1 kHz tone
Signal-to-Noise Ratio (SNR)		92		dB	At ambient, 2.5 V external reference, BW = 20 kHz, f_{OUT} = 1 kHz
Peak Harmonic or Spurious Noise (SFDR)		92		dB	At ambient, 2.5 V external reference, BW = 20 kHz, f_{OUT} = 1 kHz
Signal-to-Noise-and-Distortion (SINAD) Ratio		85		dB	At ambient, 2.5 V external reference, BW = 20 kHz, f_{OUT} = 1 kHz

[1] For specified performance, headroom requirement is 1 V.
[2] Temperature range: −40°C to +125°C, typical at +25°C.
[3] Guaranteed by design and characterization, not production tested.
[4] Digitally generated sine wave at 1 kHz.

TIMING CHARACTERISTICS

DV_{CC} = 1.7 V to 5.5 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1[1]	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	15	ns min	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time
t_5	10	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge time
t_6	20	ns min	Minimum $\overline{\text{SYNC}}$ high time (write mode)
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	10	ns min	$\overline{\text{LDAC}}$ falling edge to $\overline{\text{SYNC}}$ falling edge
t_{10}	20	ns min	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge
t_{11}	20	ns min	$\overline{\text{LDAC}}$ pulse width low
t_{12}	9	µs typ	DAC output settling time, 20 V step to 1 LSB at 16-bit resolution (see Table 2)
	7.5	µs typ	DAC output settling time, 10 V step to 1 LSB at 16-bit resolution
t_{13}	20	ns min	$\overline{\text{CLEAR}}$ pulse width low
t_{14}	200	ns typ	$\overline{\text{CLEAR}}$ pulse activation time
t_{15}	10	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK falling edge
t_{16}	40	ns max	SCLK rising edge to SDO valid (C_{L_SDO}[2] = 15 pF)
t_{17}	50	ns min	Minimum $\overline{\text{SYNC}}$ high time (readback/daisy-chain mode)

[1] Maximum SCLK frequency is 50 MHz for write mode and 33 MHz for readback mode.

[2] C_{L_SDO} is the capacitive load on the SDO output.

TIMING DIAGRAMS

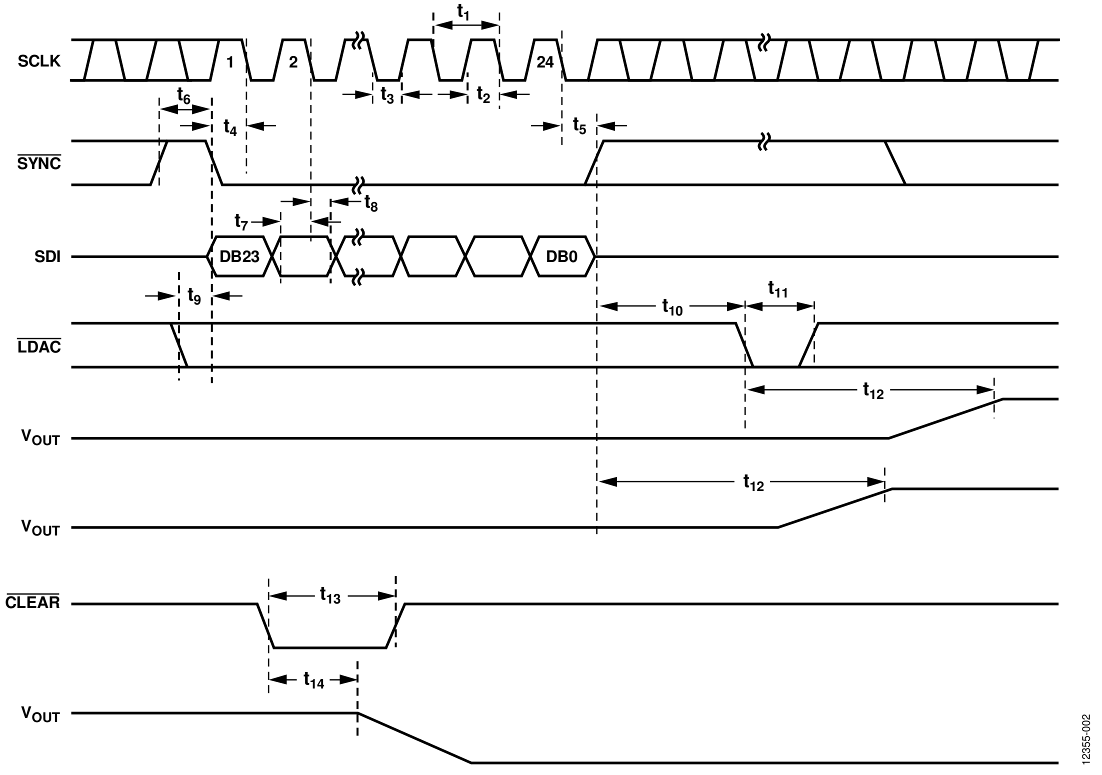


Figure 2. Serial Interface Timing Diagram

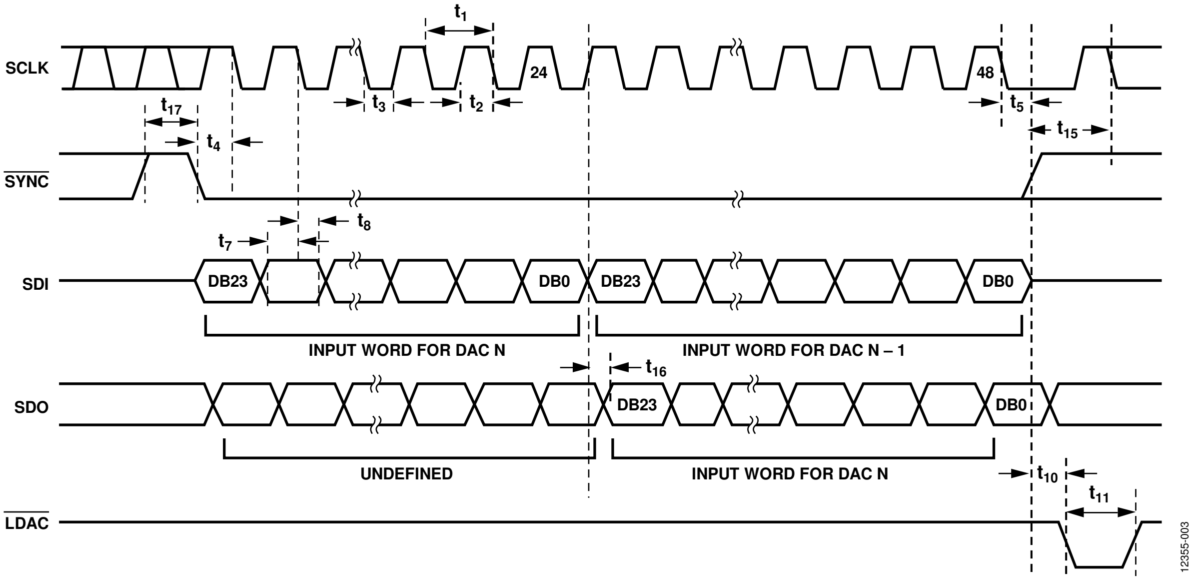


Figure 3. Daisy-Chain Timing Diagram

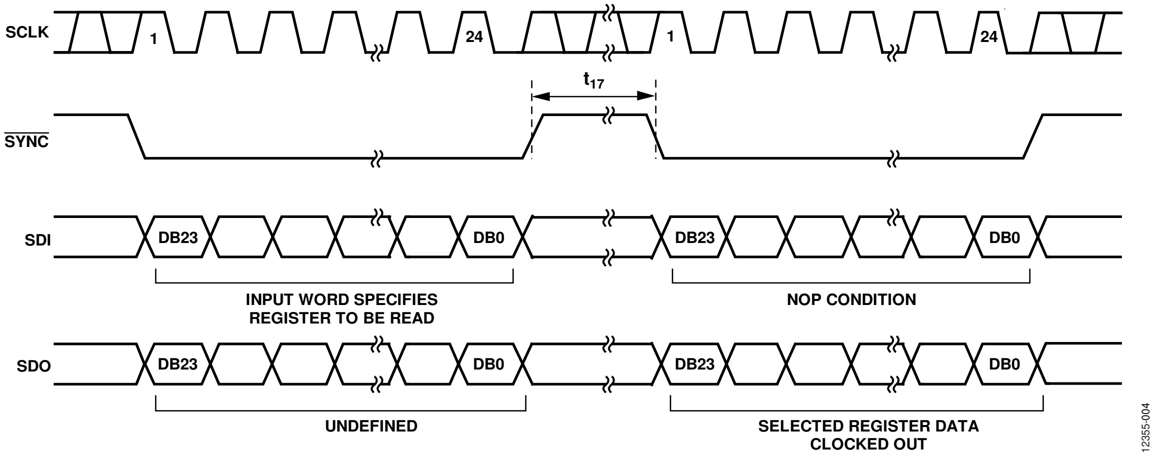


Figure 4. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 200 mA do not cause silicon controlled rectifier (SCR) latch-up.

Table 4.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +34 V
V_{SS} to AGND	+0.3 V to −17 V
V_{DD} to V_{SS}	−0.3 V to +34 V
DV_{CC} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital Outputs to DGND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
V_{REFIN}/V_{REFOUT} to DGND	−0.3 V to +7 V
V_{OUT} to AGND	V_{SS} to V_{DD}
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range, T_A Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature, $T_{J\,MAX}$	150°C
16-Lead TSSOP Package	
θ_{JA} Thermal Impedance	113°C/W[1]
θ_{JC} Thermal Impedance	28°C/W
16-Lead LFCSP Package	
θ_{JA} Thermal Impedance	75°C/W[1]
θ_{JC} Thermal Impedance	4.5°C/W[2]
Power Dissipation	$(T_{J\,MAX} - T_A)/\theta_{JA}$
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD (Human Body Model)	4 kV

[1] JEDEC 2S2P test board, still air (0 m/sec airflow).

[2] Measured to exposed paddle, with infinite heat sink on package top surface.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

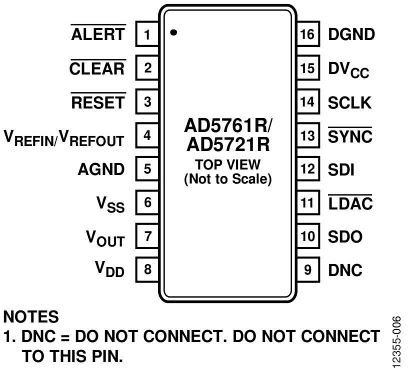
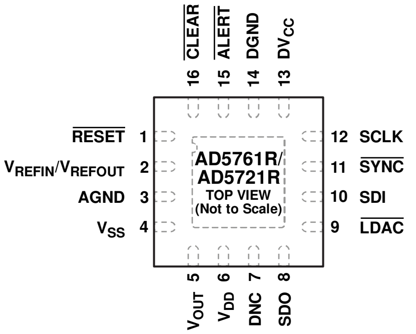


Figure 5. 16-Lead TSSOP Pin Configuration

Table 5. 16-Lead TSSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{ALERT}}$	Active Low Alert. This pin is asserted low when the die temperature exceeds approximately 150°C, or when an output short circuit or a brownout occurs. This pin is also asserted low during power-up, a full software reset, or a hardware reset, for which a write to the control register asserts the pin high.
2	$\overline{\text{CLEAR}}$	Falling Edge Clear Input. Asserting this pin sets the DAC register to zero scale, midscale, or full-scale code (user selectable) and updates the DAC output. This pin can be left floating because there is an internal pull-up resistor.
3	$\overline{\text{RESET}}$	Active Low Reset Input. Asserting this pin returns the AD5761R/AD5721R to their default power-on status where the output is clamped to ground and the output buffer is powered down. This pin can be left floating because there is an internal pull-up resistor.
4	V_{REFIN}/V_{REFOUT}	Internal Reference Voltage Output and External Reference Voltage Input. For specified performance, V_{REFIN}/V_{REFOUT} = 2.5 V. Connect a 10 nF capacitor with the internal reference to minimize the noise.
5	AGND	Ground Reference Pin for Analog Circuitry.
6	V_{SS}	Negative Analog Supply Connection. A voltage in the range of −16.5 V to 0 V can be connected to this pin. For unipolar output ranges, connect this pin to 0 V. V_{SS} must be decoupled to AGND.
7	V_{OUT}	Analog Output Voltage of the DAC. The output amplifier is capable of directly driving a 2 kΩ, 1 nF load.
8	V_{DD}	Positive Analog Supply Connection. A voltage in the range of 4.75 V to 30 V can be connected to this pin for unipolar output ranges. Bipolar output ranges accept a voltage in the range of 4.75 V to 16.5 V. V_{DD} must be decoupled to AGND.
9	DNC	Do Not Connect. Do not connect to this pin.
10	SDO	Serial Data Output. This pin clocks data from the serial register in daisy-chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
11	$\overline{\text{LDAC}}$	Load DAC. This logic input updates the DAC register and, consequently, the analog output. When tied permanently low, the DAC register is updated when the input register is updated. If $\overline{\text{LDAC}}$ is held high during the write to the input register, the DAC output register is not updated, and the DAC output update is held off until the falling edge of $\overline{\text{LDAC}}$. This pin can be left floating because there is an internal pull-up resistor.
12	SDI	Serial Data Input. Data must be valid on the falling edge of SCLK.
13	$\overline{\text{SYNC}}$	Active Low Synchronization Input. This pin is the frame synchronization signal for the serial interface. While $\overline{\text{SYNC}}$ is low, data is transferred in on the falling edge of SCLK. Data is latched on the rising edge of $\overline{\text{SYNC}}$.
14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This pin operates at clock speeds of up to 50 MHz.
15	DV_{CC}	Digital Supply. The voltage range is from 1.7 V to 5.5 V. The applied voltage sets the voltage at which the digital interface operates.
16	DGND	Digital Ground.



NOTES
1. DNC = DO NOT CONNECT.
2. THE EXPOSED PAD MUST BE MECHANICALLY CONNECTED TO THE PCB COPPER PLANE FOR OPTIMAL THERMAL PERFORMANCE. THE EXPOSED PAD CAN BE LEFT ELECTRICALLY FLOATING.

12335-106

Figure 6. 16-Lead LFCSP Pin Configuration

Table 6. 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Active Low Reset Input. Asserting this pin returns the AD5761R/AD5721R to their default power-on status where the output is clamped to ground and the output buffer is powered down. This pin can be left floating because there is an internal pull-up resistor.
2	V_{REFIN}/V_{REFOUT}	Internal Reference Voltage Output and External Reference Voltage Input. For specified performance, V_{REFIN}/V_{REFOUT} = 2.5 V. Connect a 10 nF capacitor with the internal reference to minimize the noise.
3	AGND	Ground Reference Pin for Analog Circuitry.
4	V_{SS}	Negative Analog Supply Connection. A voltage in the range of −16.5 V to 0 V can be connected to this pin. For unipolar output ranges, connect this pin to 0 V. V_{SS} must be decoupled to AGND.
5	V_{OUT}	Analog Output Voltage of the DAC. The output amplifier is capable of directly driving a 2 kΩ, 1 nF load.
6	V_{DD}	Positive Analog Supply Connection. A voltage in the range of 4.75 V to 30 V can be connected to this pin for unipolar output ranges. Bipolar output ranges accept a voltage in the range of 4.75 V to 16.5 V. V_{DD} must be decoupled to AGND.
7	DNC	Do Not Connect. Do not connect to this pin.
8	SDO	Serial Data Output. This pin clocks data from the serial register in daisy-chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
9	$\overline{\text{LDAC}}$	Load DAC. This logic input updates the DAC register and, consequently, the analog output. When tied permanently low, the DAC register is updated when the input register is updated. If $\overline{\text{LDAC}}$ is held high during the write to the input register, the DAC output register is not updated, and the DAC output update is held off until the falling edge of $\overline{\text{LDAC}}$. This pin can be left floating because there is an internal pull-up resistor.
10	SDI	Serial Data Input. Data must be valid on the falling edge of SCLK.
11	$\overline{\text{SYNC}}$	Active Low Synchronization Input. This pin is the frame synchronization signal for the serial interface. While $\overline{\text{SYNC}}$ is low, data is transferred in on the falling edge of SCLK. Data is latched on the rising edge of $\overline{\text{SYNC}}$.
12	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This pin operates at clock speeds of up to 50 MHz.
13	DV_{CC}	Digital Supply. The voltage range is from 1.7 V to 5.5 V. The applied voltage sets the voltage at which the digital interface operates.
14	DGND	Digital Ground.
15	$\overline{\text{ALERT}}$	Active Low Alert. This pin is asserted low when the die temperature exceeds approximately 150°C, or when an output short circuit or a brownout occurs. This pin is also asserted low during power-up, a full software reset, or a hardware reset, for which a write to the control register asserts the pin high.
16	$\overline{\text{CLEAR}}$	Falling Edge Clear Input. Asserting this pin sets the DAC register to zero scale, midscale, or full-scale code (user selectable) and updates the DAC output. This pin can be left floating because there is an internal pull-up resistor.
	EPAD	Exposed Pad. The exposed pad must be mechanically connected to the PCB copper plane for optimal thermal performance. The exposed pad can be left electrically floating.

TYPICAL PERFORMANCE CHARACTERSTICS

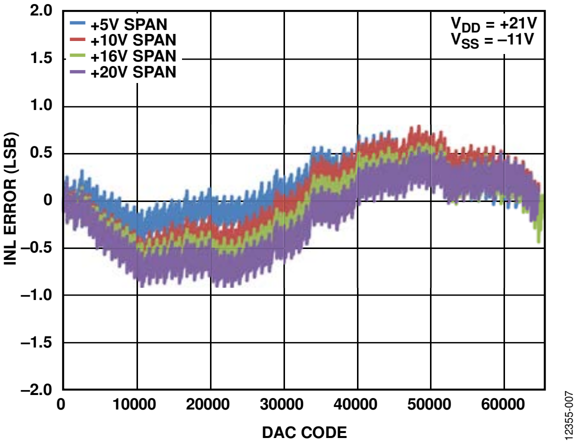


Figure 7. AD5761R INL Error vs. DAC Code, Unipolar Output

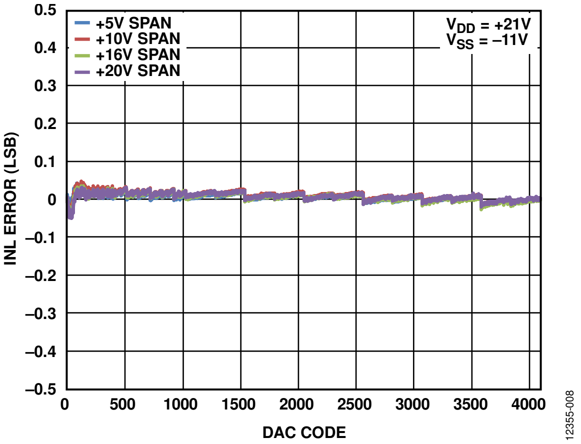


Figure 8. AD5721R INL Error vs. DAC Code, Unipolar Output

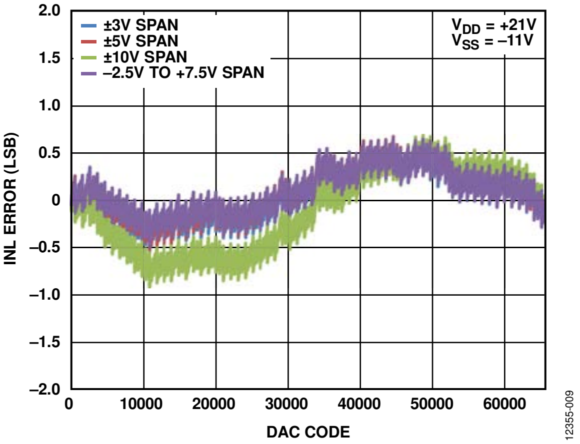


Figure 9. AD5761R INL Error vs. DAC Code, Bipolar Output

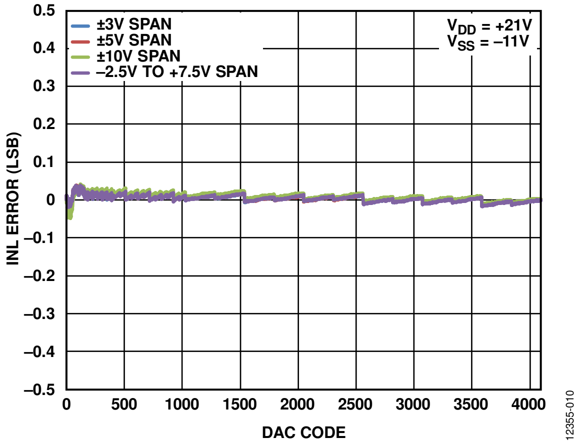


Figure 10. AD5721R INL Error vs. DAC Code, Bipolar Output

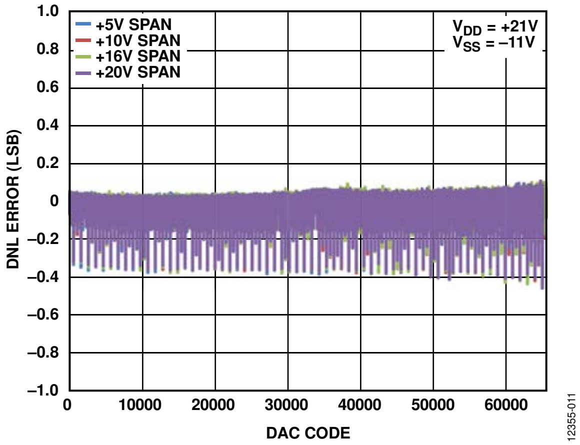


Figure 11. AD5761R DNL Error vs. DAC Code, Unipolar Output

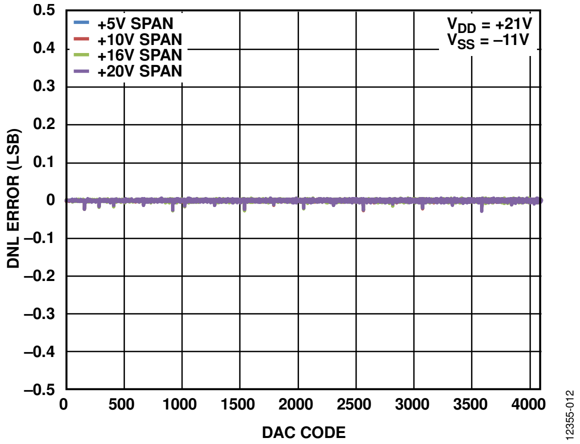


Figure 12. AD5721R DNL Error vs. DAC Code, Unipolar Output

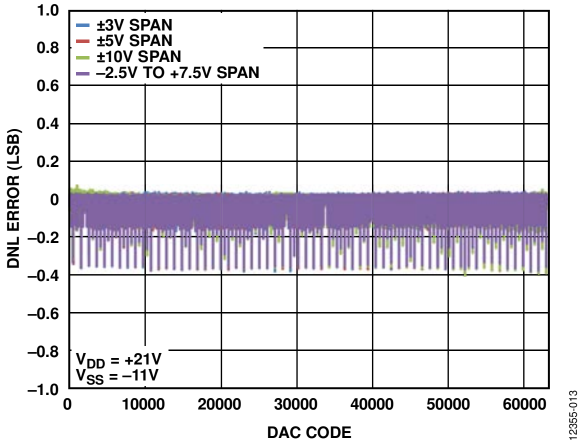


Figure 13. AD5761R DNL Error vs. DAC Code, Bipolar Output

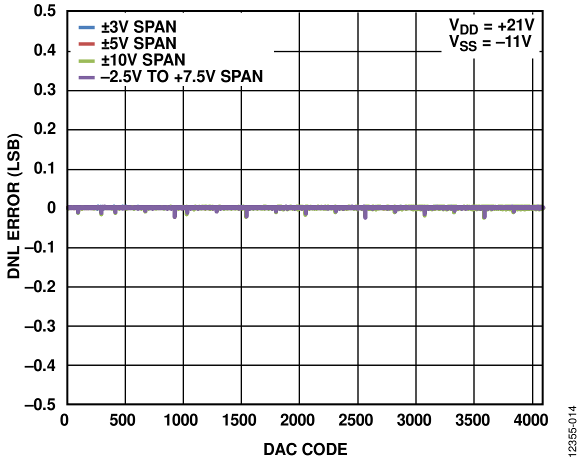


Figure 14. AD5721R DNL Error vs. DAC Code, Bipolar Output

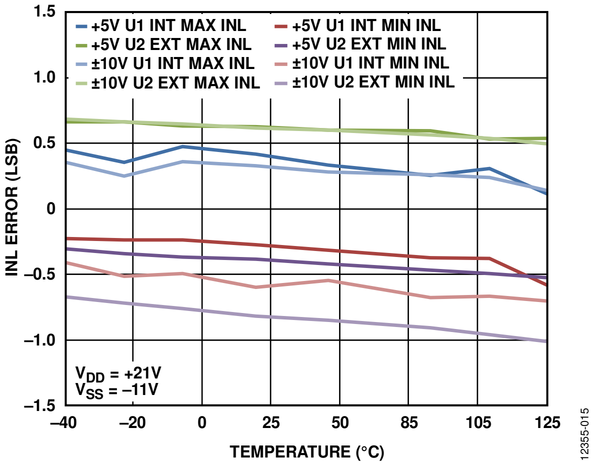


Figure 15. INL Error vs. Temperature

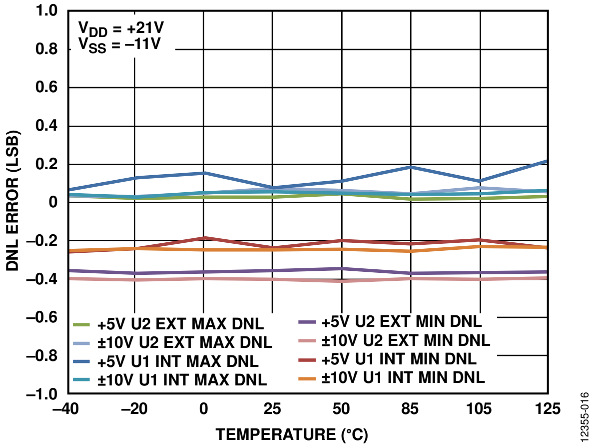


Figure 16. DNL Error vs. Temperature

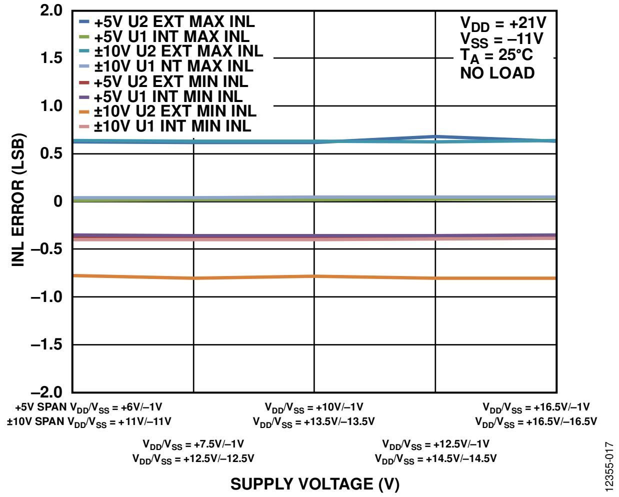


Figure 17. INL Error vs. Supply Voltage

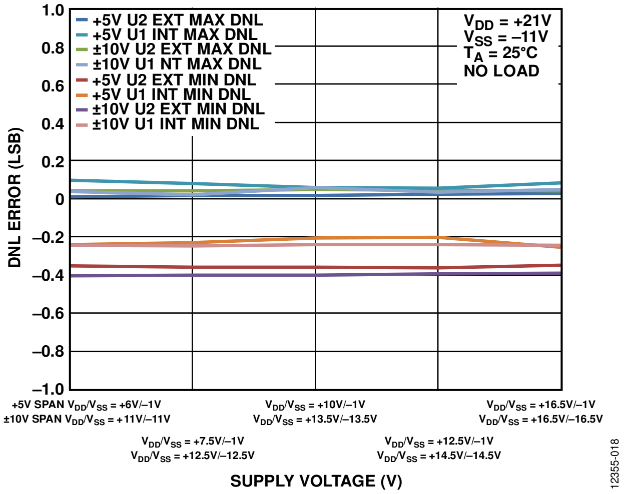


Figure 18. DNL Error vs. Supply Voltage

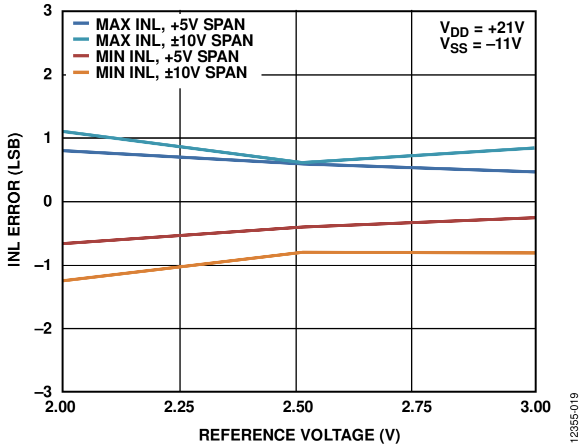


Figure 19. INL Error vs. Reference Voltage

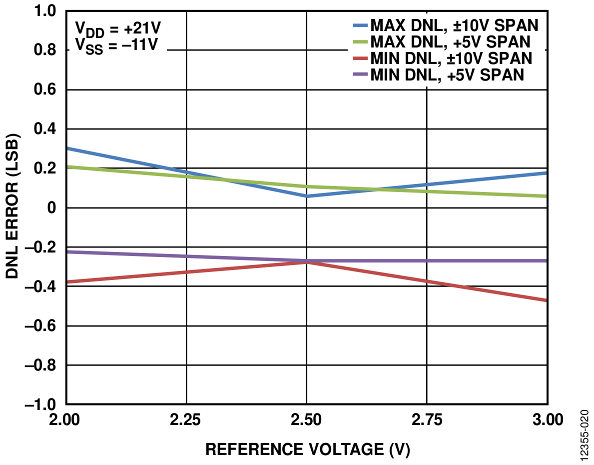


Figure 20. DNL Error vs. Reference Voltage

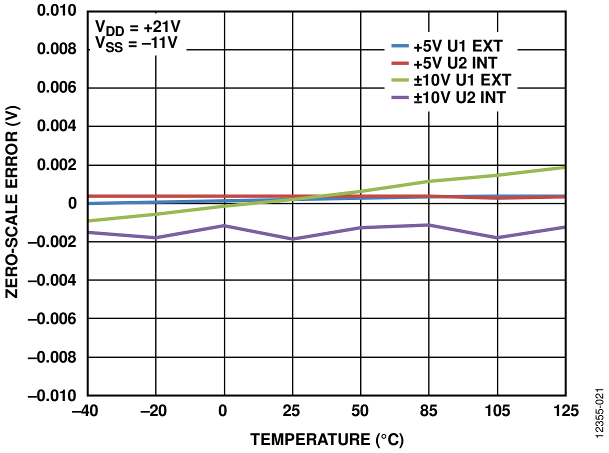


Figure 21. Zero-Scale Error vs. Temperature

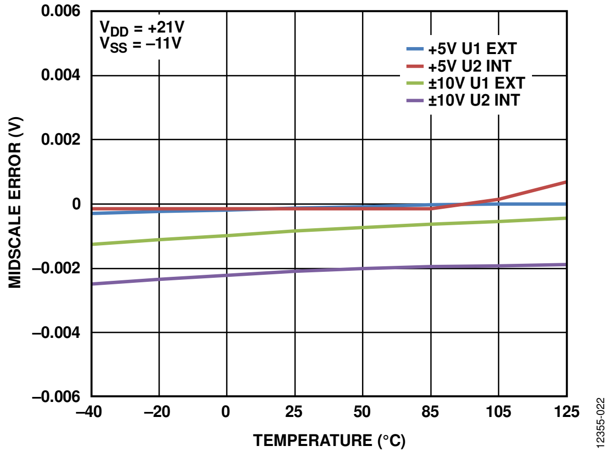


Figure 22. Midscale Error vs. Temperature

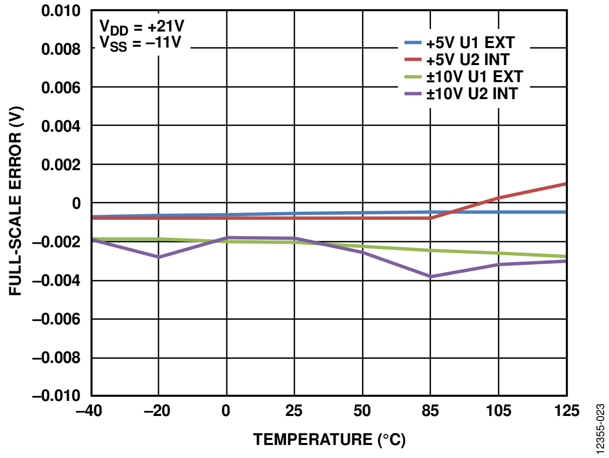


Figure 23. Full-Scale Error vs. Temperature

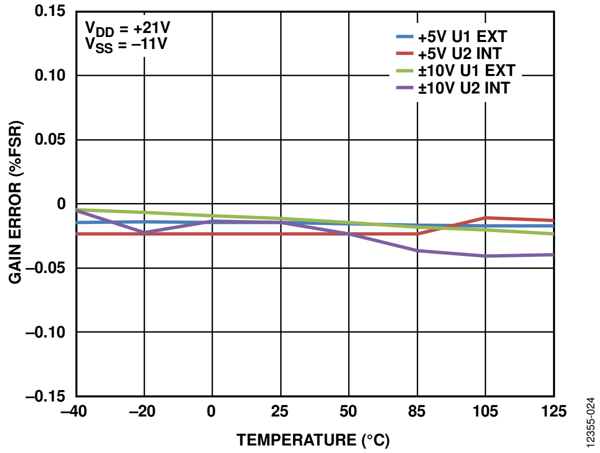


Figure 24. Gain Error vs. Temperature

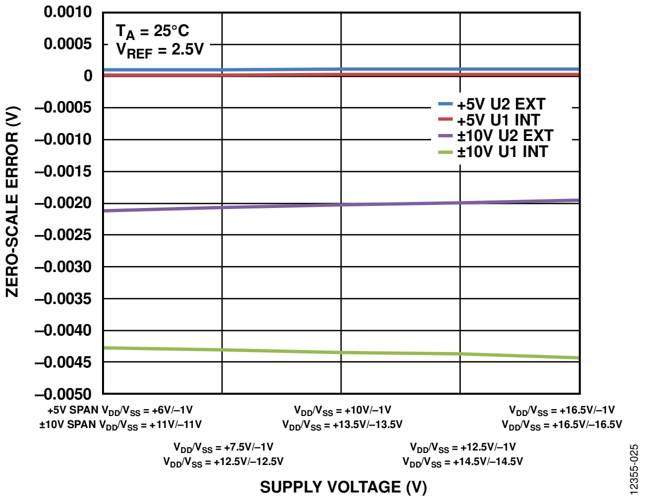


Figure 25. Zero-Scale Error vs. Supply Voltage

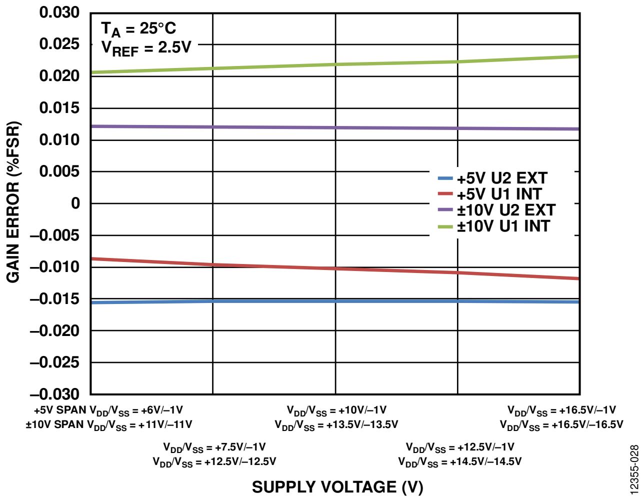


Figure 28. Gain Error vs. Supply Voltage

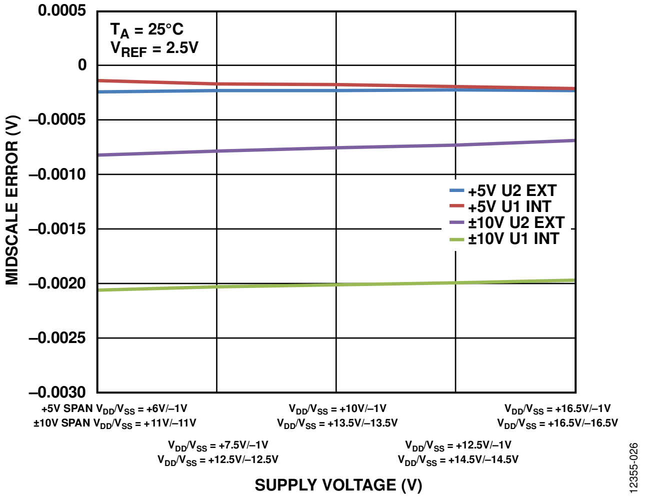


Figure 26. Midscale Error vs. Supply Voltage

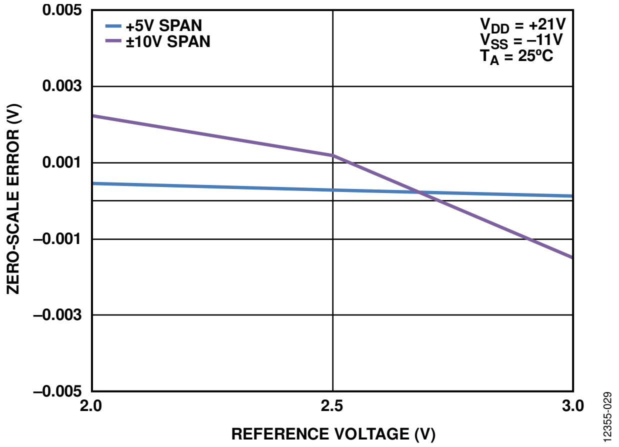


Figure 29. Zero-Scale Error vs. Reference Voltage

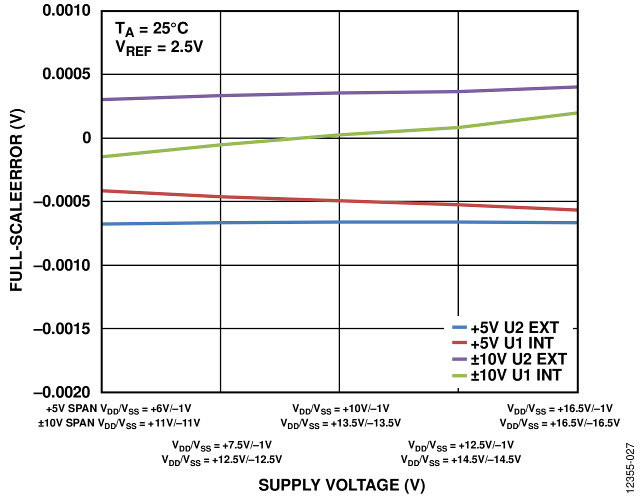


Figure 27. Full-Scale Error vs. Supply Voltage

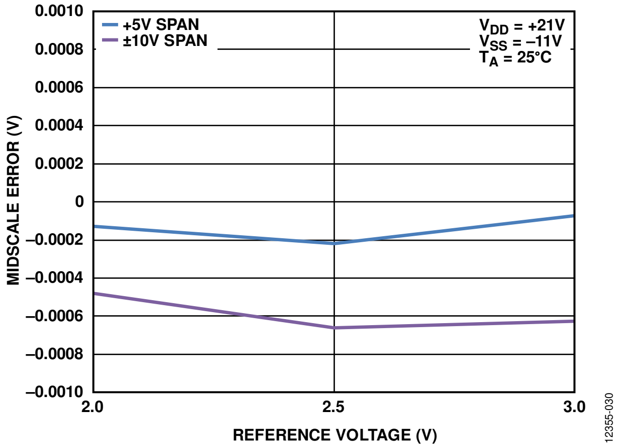


Figure 30. Midscale Error vs. Reference Voltage

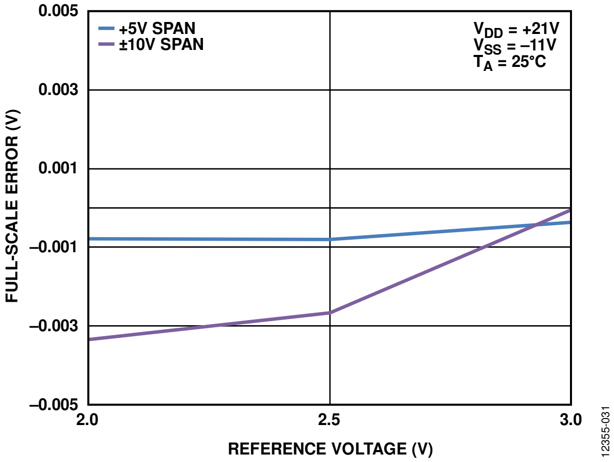


Figure 31. Full-Scale Error vs. Reference Voltage

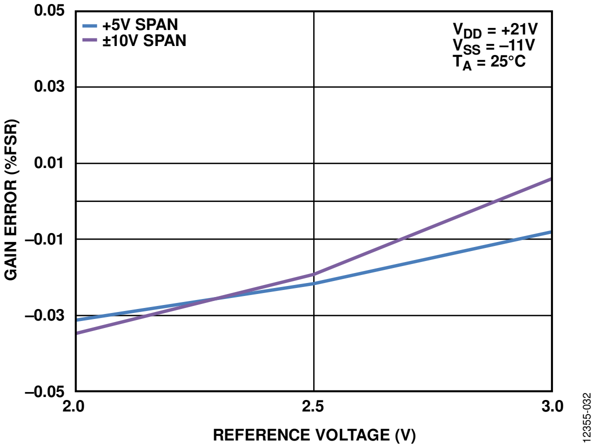


Figure 32. Gain Error vs. Reference Voltage

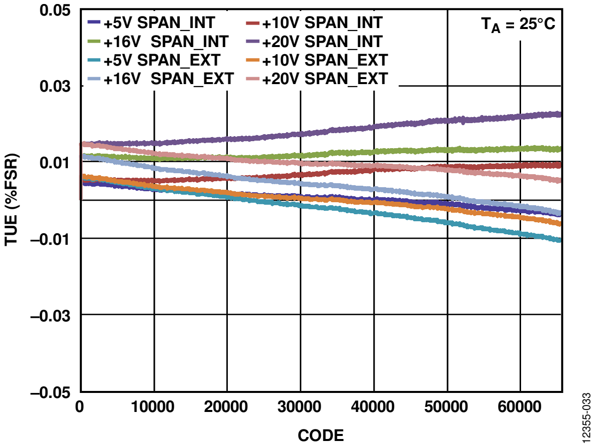


Figure 33. TUE vs. Code, Unipolar Output

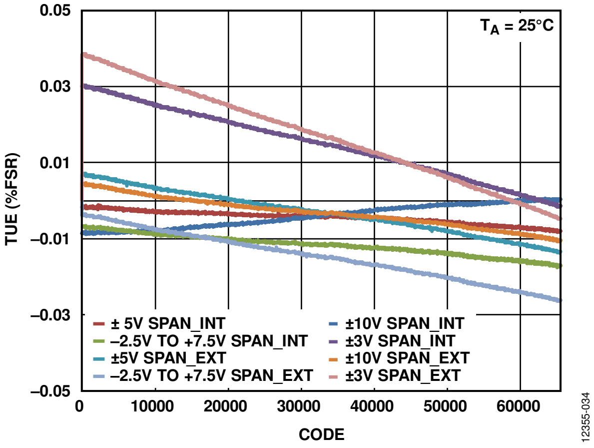


Figure 34. TUE vs. Code, Bipolar Output

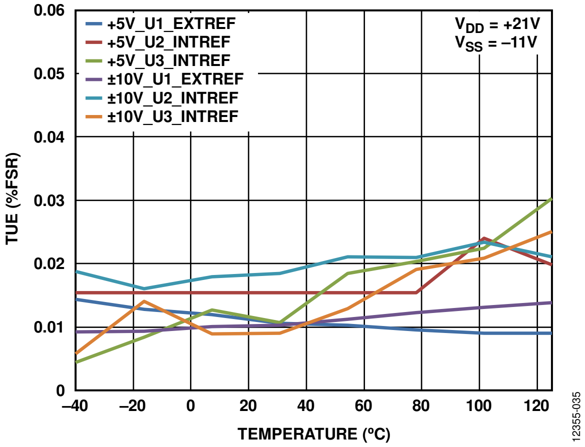


Figure 35. TUE vs. Temperature

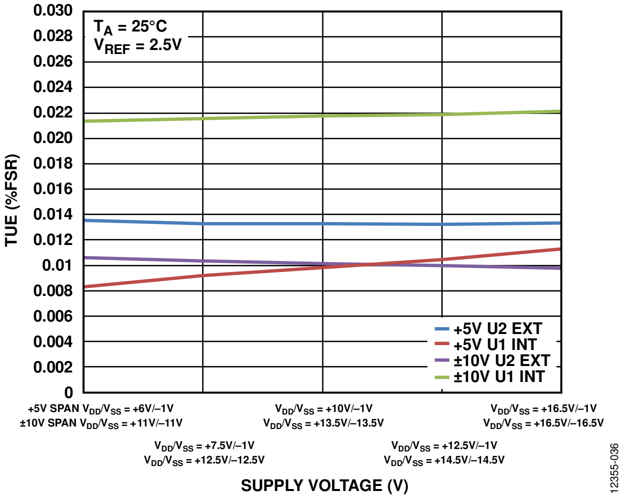


Figure 36. TUE vs. Supply Voltage

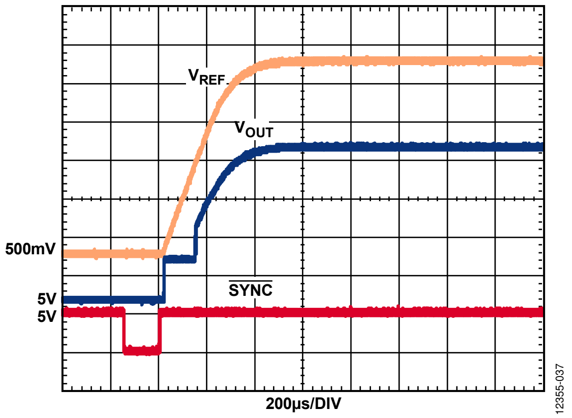


Figure 37. Reference Output Voltage Turn On Transient

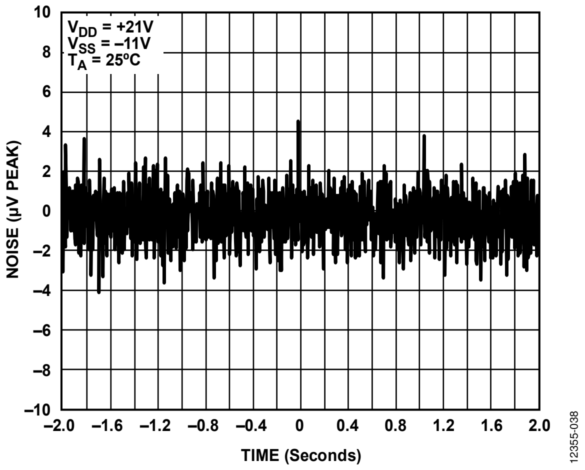


Figure 38. Internal Reference Noise (100 kHz Bandwidth)

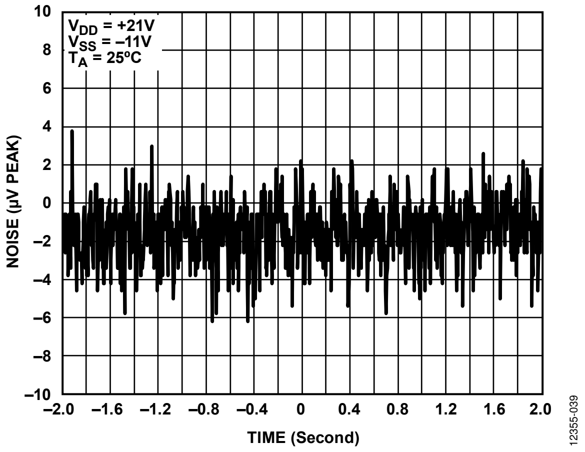


Figure 39. Internal Reference Noise (0.1 Hz to 10 Hz Bandwidth)

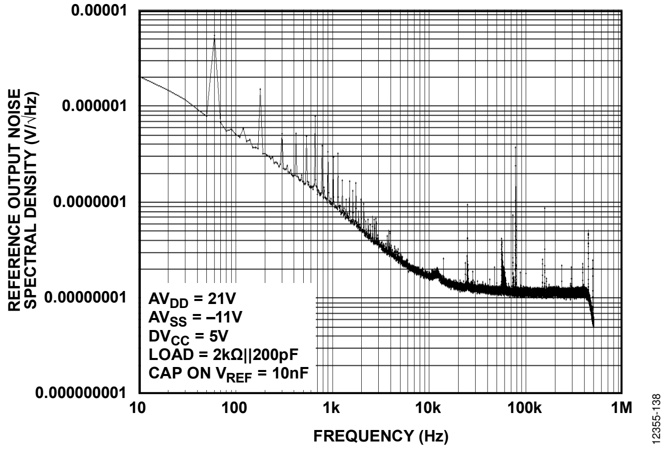


Figure 40. Reference Output Noise Spectral Density vs. Frequency

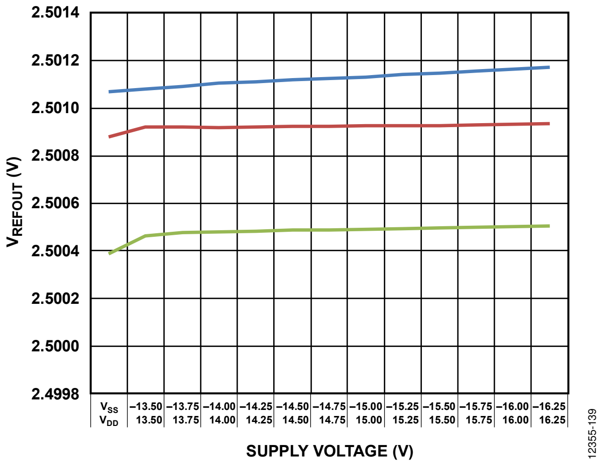


Figure 41. Reference Output Voltage (V_{REFOUT}) vs. Supply Voltage

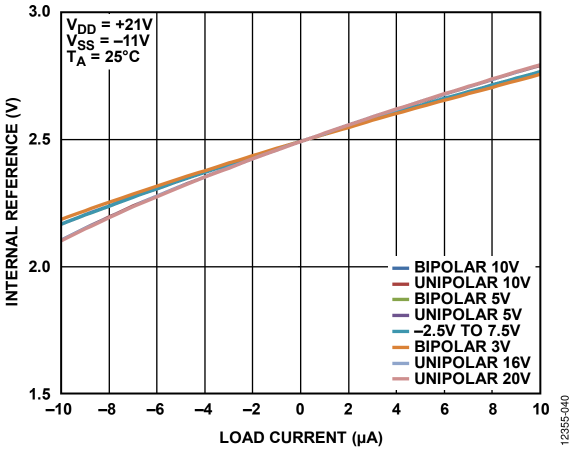


Figure 42. Internal Reference vs. Load Current

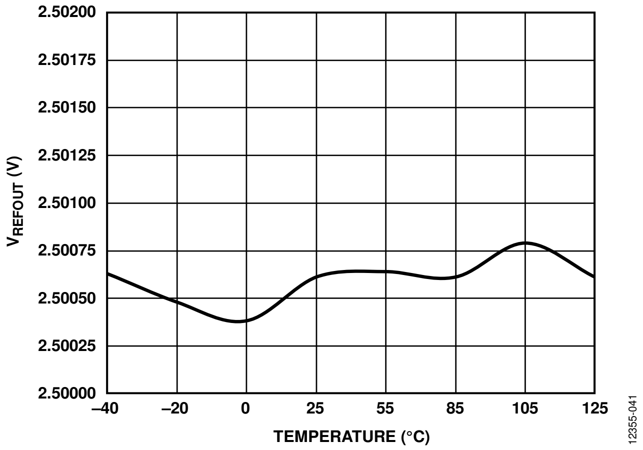


Figure 43. Reference Output Voltage vs. Temperature

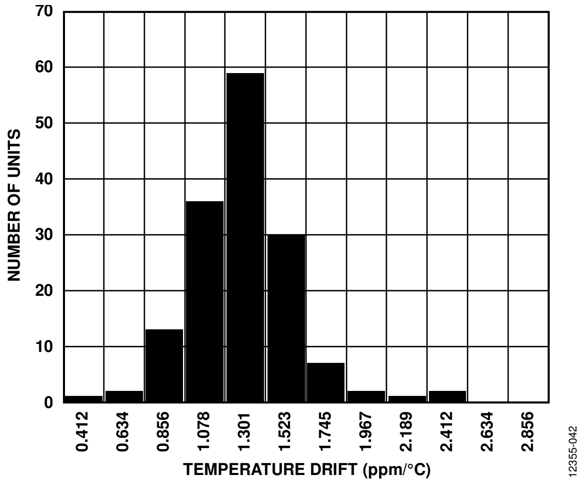


Figure 44. Reference Output TC

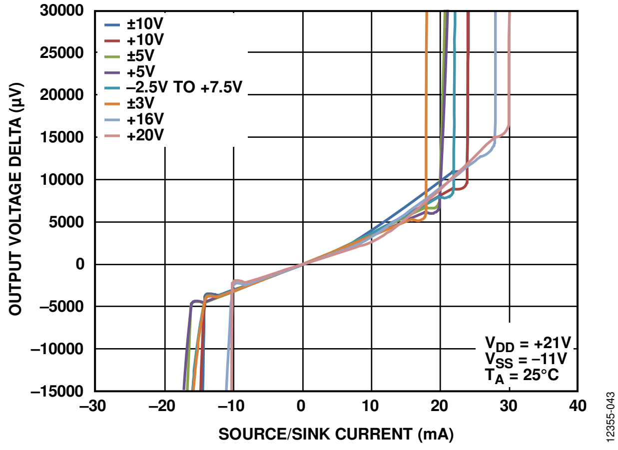


Figure 45. Source and Sink Capability of Output Amplifier with Positive Full Scale Loaded

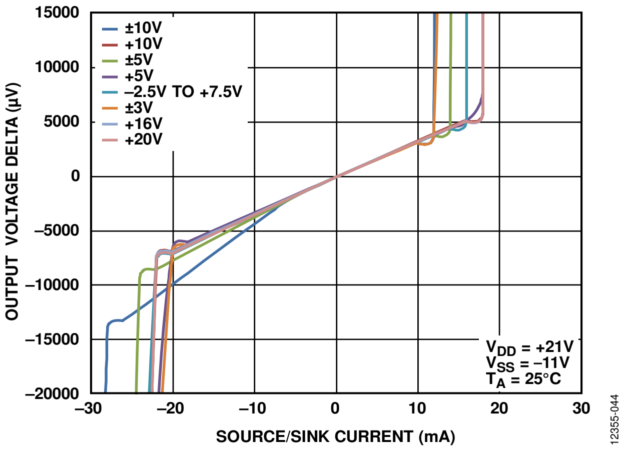


Figure 46. Source and Sink Capability of Output Amplifier with Negative Full Scale Loaded

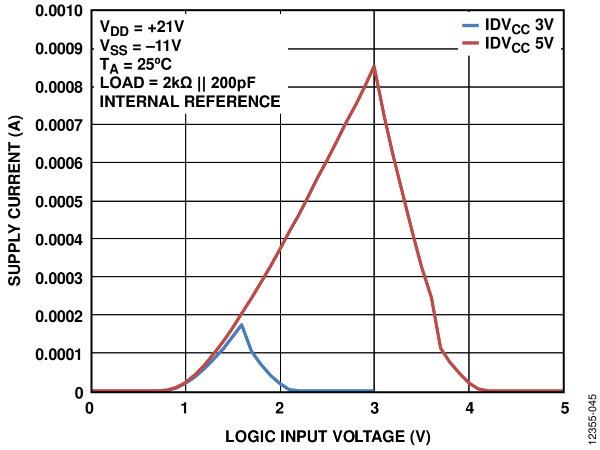


Figure 47. Supply Current vs. Logic Input Voltage

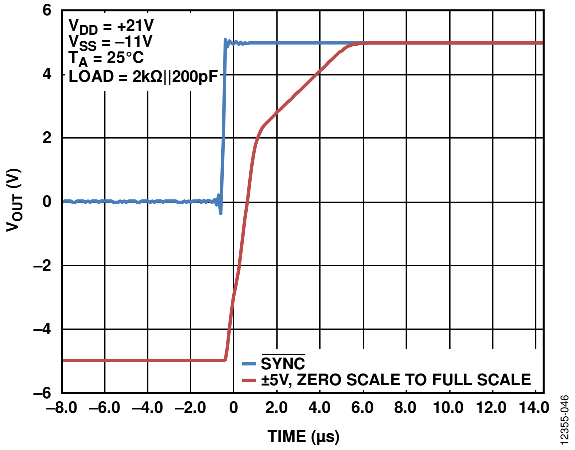


Figure 48. Full-Scale Settling Time (Rising Voltage Step), ±5 V Range

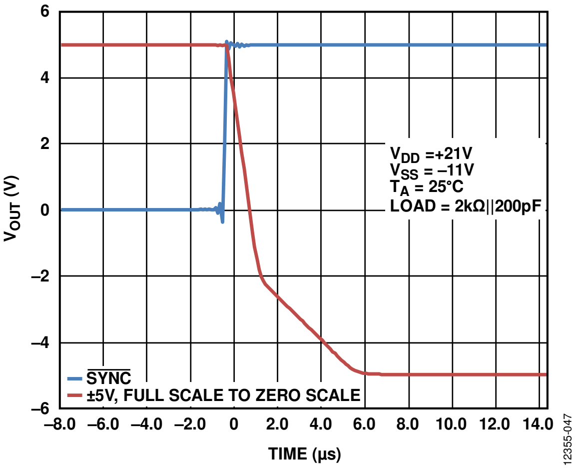


Figure 49. Full-Scale Settling Time (Falling Voltage Step), ±5 V Range

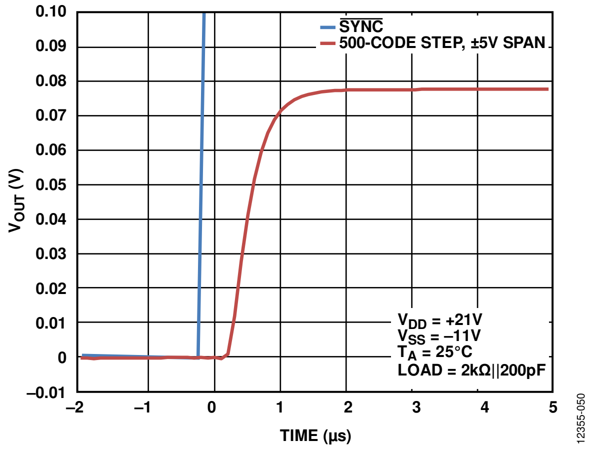


Figure 52. 500-Code Step Settling Time, ±5 V Range

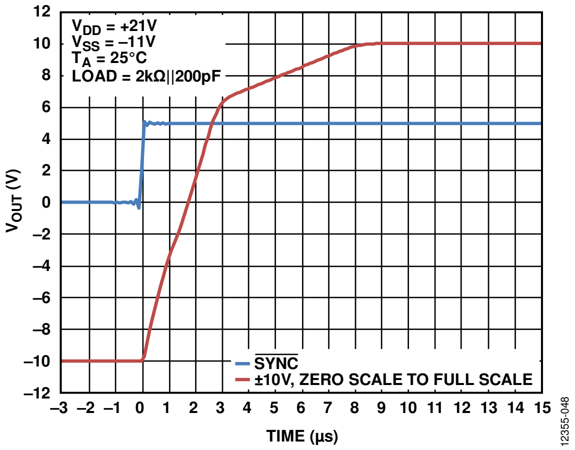


Figure 50. Full-Scale Settling Time (Rising Voltage Step), ±10 V Range

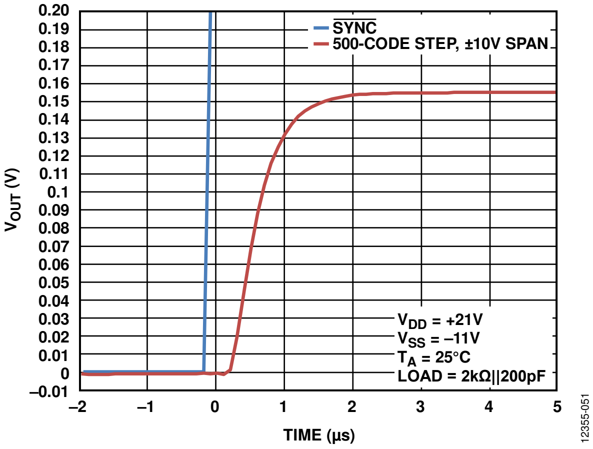


Figure 53. 500-Code Step Settling Time, ±10 V Range

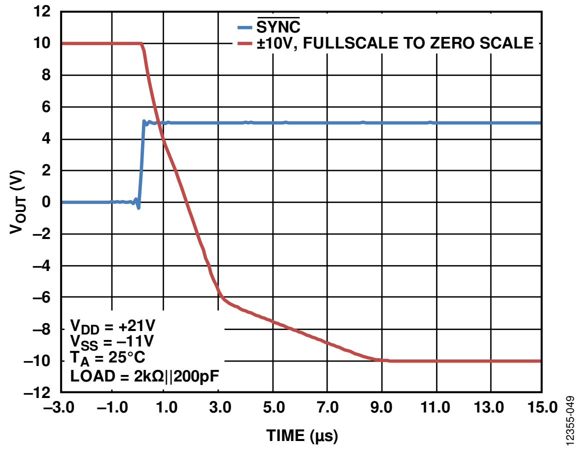


Figure 51. Full-Scale Settling Time (Falling Voltage Step), ±10 V Range

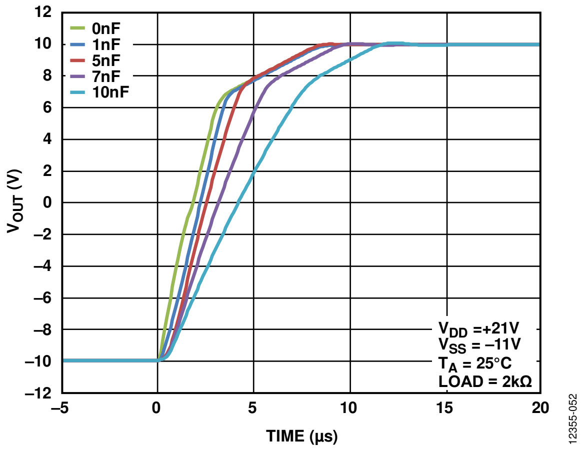


Figure 54. Full-Scale Settling Time at Various Capacitive Loads, ±10 V Range

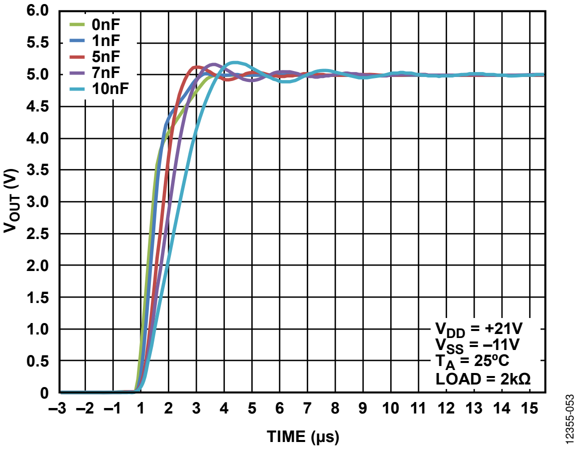


Figure 55. Full-Scale Settling Time at Various Capacitive Loads, 0 V to 5 V Range

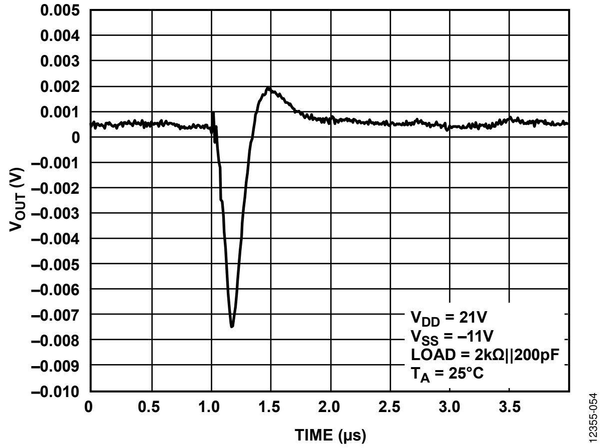


Figure 56. Digital-to-Analog Glitch Energy, 5 V Range

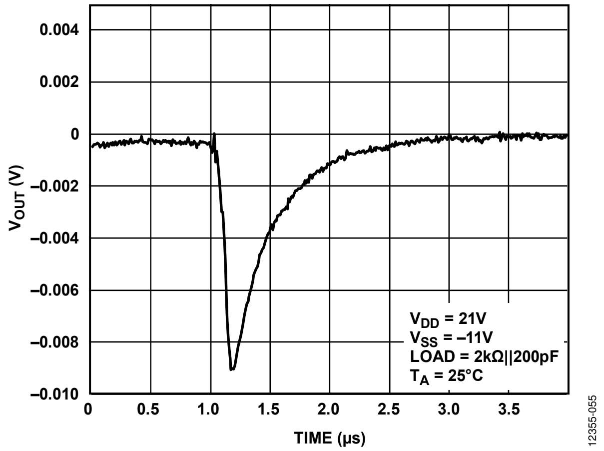


Figure 57. Digital-to-Analog Glitch Energy, ±10 V Range

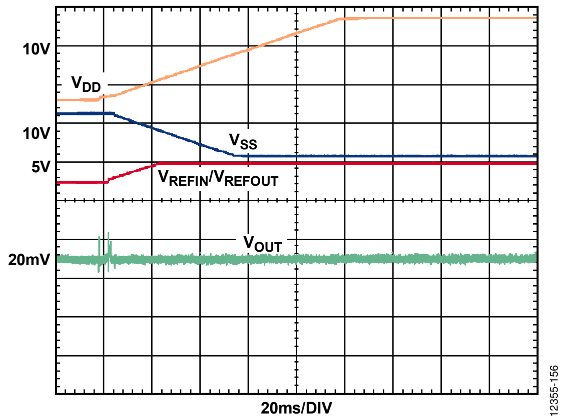


Figure 58. Power-Up Glitch

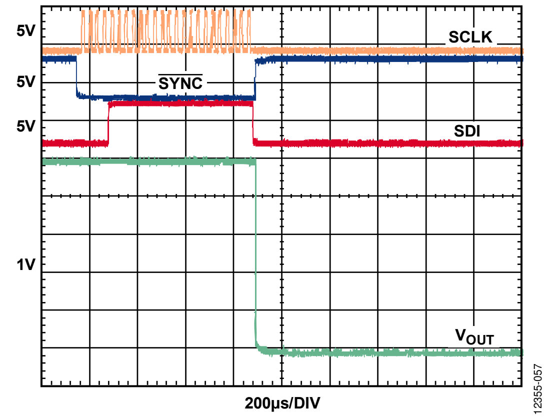


Figure 59. Software Full Reset Glitch from Full Scale with Output Loaded, 0 V to 5 V Range

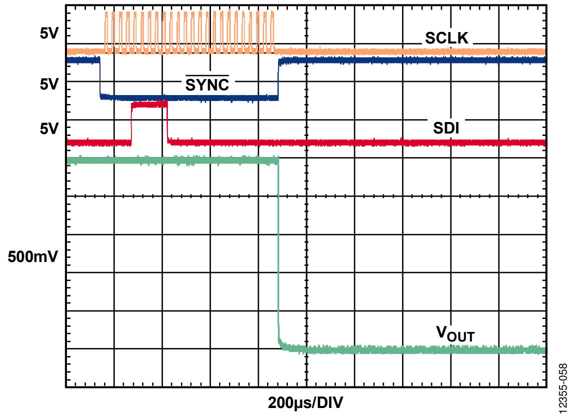


Figure 60. Software Full Reset Glitch from Midscale with Output Loaded, 5 V Range

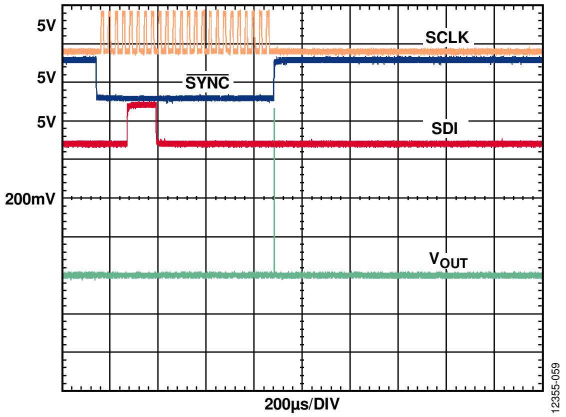


Figure 61. Software Full Reset Glitch from Zero Scale with Output Loaded, 0 V to 5 V Range

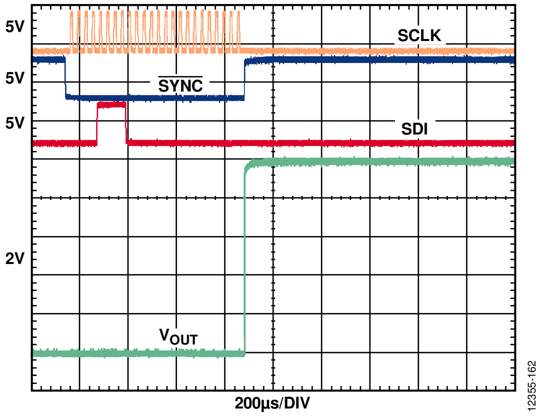


Figure 64. Software Full Reset Glitch from Zero Scale with Output Loaded, ±10 V Range

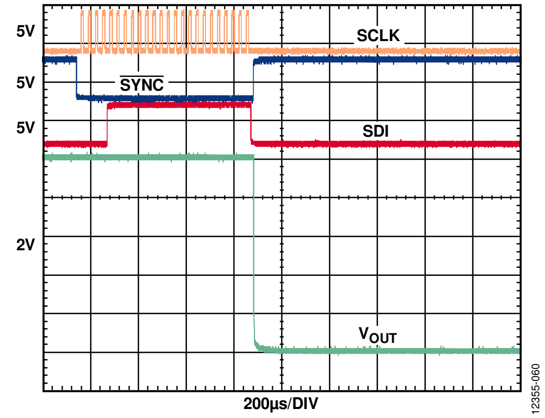


Figure 62. Software Full Reset Glitch from Full Scale with Output Loaded, ±10 V Range

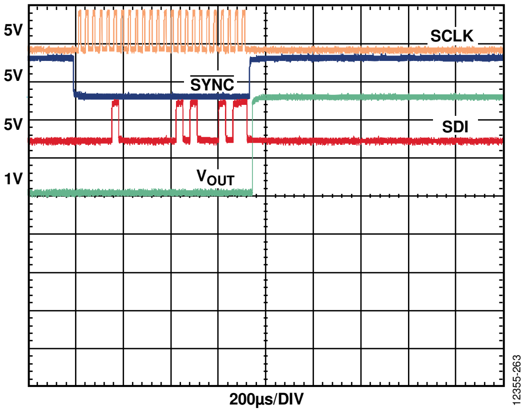


Figure 65. Output Range Change Glitch, 0 V to 5 V Range

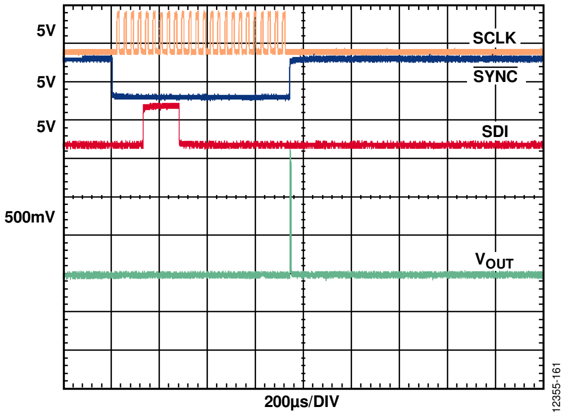


Figure 63. Software Full Reset Glitch from Midscale with Output Loaded, ±10 V Range

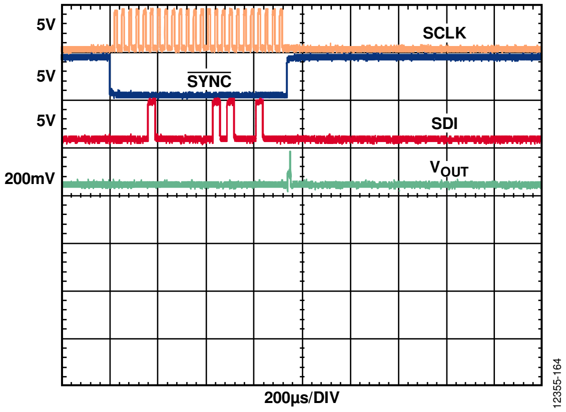


Figure 66. Output Range Change Glitch, ±10 V Range

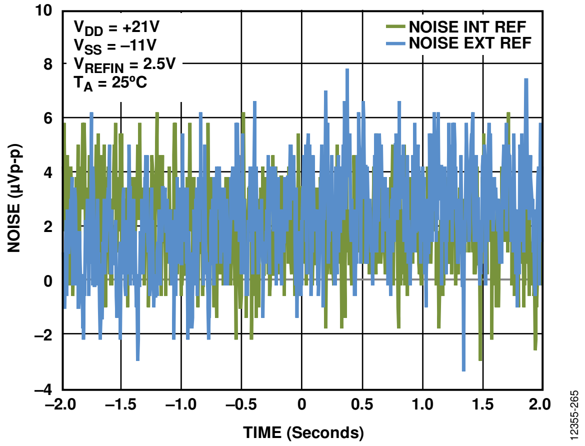


Figure 67. Peak-to-Peak Noise (Voltage Output Noise), 0.1 Hz to 10 Hz Bandwidth

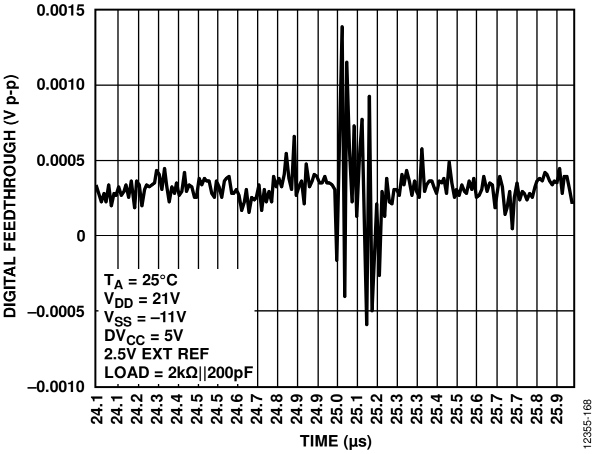


Figure 70. Digital Feedthrough

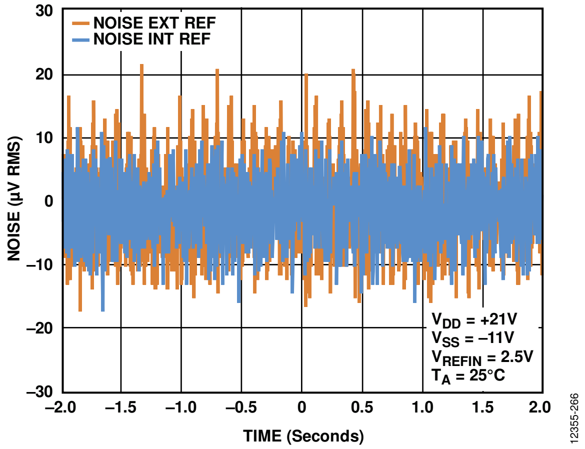


Figure 68. Peak-to-Peak Noise (Voltage Output Noise), 100 kHz Bandwidth

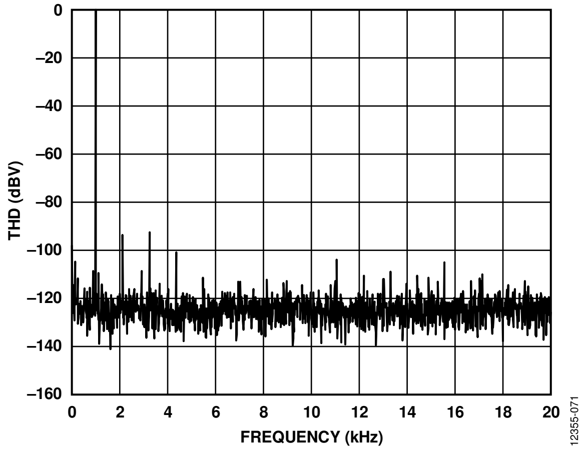


Figure 71. Total Harmonic Distortion

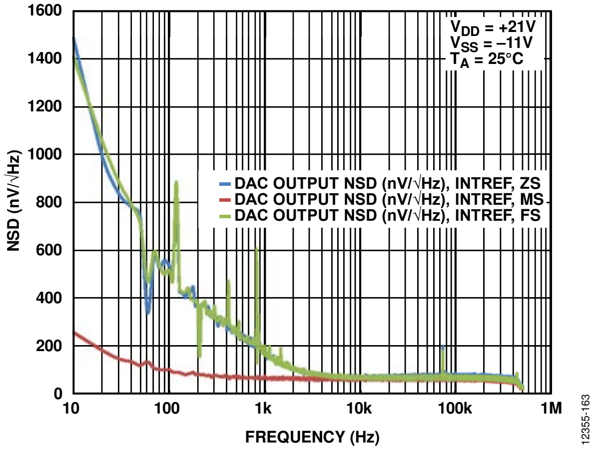


Figure 69. DAC Output Noise Spectral Density (NSD) vs. Frequency, ±10 V Range

TERMINOLOGY

Total Unadjusted Error (TUE)

Total unadjusted error is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy, or integral nonlinearity, is a measure of the maximum deviation, in LSB, from a straight line passing through the endpoints of the DAC transfer function. A typical INL error vs. DAC code plot is shown in Figure 7.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. The AD5761R/AD5721R are guaranteed monotonic. A typical DNL error vs. code plot is shown in Figure 11.

Monotonicity

A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5761R/AD5721R are monotonic over their full operating temperature range.

Bipolar Zero Error

Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (straight binary coding) or 0x0000 (twos complement coding) for the AD5761R/AD5721R.

Bipolar Zero Temperature Coefficient (TC)

Bipolar zero TC is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in µV/°C.

Zero-Scale Error

Zero-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) or 0x8000 (twos complement coding) is loaded to the DAC register. Ideally, the output voltage is negative full scale. A plot of zero-scale error vs. temperature is shown in Figure 21.

Zero-Scale Error Temperature Coefficient (TC)

Zero-scale error TC is a measure of the change in zero-scale error with a change in temperature. It is expressed in µV/°C.

Offset Error

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function.

Offset Error Temperature Coefficient (TC)

Offset error TC is a measurement of the change in offset error with a change in temperature. It is expressed in µV/°C.

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed in % FSR. A plot of gain error vs. temperature is shown in Figure 24.

Gain Error Temperature Coefficient (TC)

Gain error TC is a measure of the change in gain error with changes in temperature. It is expressed in ppm FSR/°C.

DC Power Supply Rejection Ratio (DC PSRR)

DC power supply rejection ratio is a measure of the rejection of the output voltage to dc changes in the power supplies applied to the DAC. It is measured for a given dc change in power supply voltage and is expressed in mV/V.

AC Power Supply Rejection Ratio (AC PSRR)

AC power supply rejection ratio is a measure of the rejection of the output voltage to ac changes in the power supplies applied to the DAC. It is measured for a given amplitude and frequency change in power supply voltage and is expressed in decibels.

Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change. Full-scale settling time is shown in Figure 48 to Figure 51.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (see Figure 56 and Figure 57).

Glitch Impulse Peak Amplitude

Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the amplitude of the glitch in mV and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

Noise Spectral Density (NSD)

Noise spectral density is a measurement of the internally generated random noise characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to full scale and measuring noise at the output. It is measured in nV/√Hz. A plot of noise spectral density is shown in Figure 69.

Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C as follows:

$$TC = \left[\frac{V_{REF\_MAX} - V_{REF\_MIN}}{V_{REF\_NOM} \times Temp\ Range} \right] \times 10^6$$

where:
V_{REF_MAX} is the maximum reference output measured over the total temperature range.
V_{REF_MIN} is the minimum reference output measured over the total temperature range.
V_{REF_NOM} is the nominal reference output voltage, 2.5 V.
Temp Range is the specified temperature range, −40°C to +125°C.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the fundamental.

For the AD5761R/AD5721R, it is defined as

$$THD\ (dB) = 20 \times \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5761R/AD5721R are single channel, 16-/12-bit voltage output DACs. The AD5761R/AD5721R output ranges are software selectable and can be configured as follows:

- Unipolar output voltage: 0 V to 5 V, 0 V to 10 V, 0 V to 16 V, 0 V to 20 V
- Bipolar output voltage: −2.5 V to +7.5 V, ±3 V, ±5 V, ±10 V

Data is written to the AD5761R/AD5721R in a 24-bit word format via a 4-wire, serial peripheral interface (SPI) compatible, digital interface. The devices also offer an SDO pin to facilitate daisy-chaining and readback.

TRANSFER FUNCTION

The internal reference is on by default. The input coding to the DAC can be straight binary or twos complement (bipolar ranges case only). Therefore, the transfer function is given by

$$V_{OUT} = V_{REF} \times \left[\left(m \times \frac{D}{65{,}536}\right) - c\right]$$

where:
V_{REF} is 2.5 V.
D is the decimal equivalent of the code loaded to the DAC register as follows:
0 to 4095 for the 12-bit device.
0 to 65,535 for the 16-bit device.
The values for m and c are as shown in Table 7.

Table 7. m and c Values for Various Output Ranges

Range	m	c
±10 V	8	4
±5 V	4	2
±3 V	2.4	1.2
−2.5 V to +7.5 V	4	1
0 V to 20 V	8	0
0 V to 16 V	6.4	0
0 V to 10 V	4	0
0 V to 5 V	2	0

DAC ARCHITECTURE

The DAC architecture consists of an R-2R DAC followed by an output buffer amplifier. Figure 72 shows a block diagram of the DAC architecture. Note that the reference input is buffered prior to being applied to the DAC. The AD5761R/AD5721R offer a 2.5 V, 5 ppm/°C maximum internal reference on chip.

The output voltage range obtained from the configurable output amplifier is selected by writing to the 3 LSBs (RA[2:0]) in the control register.

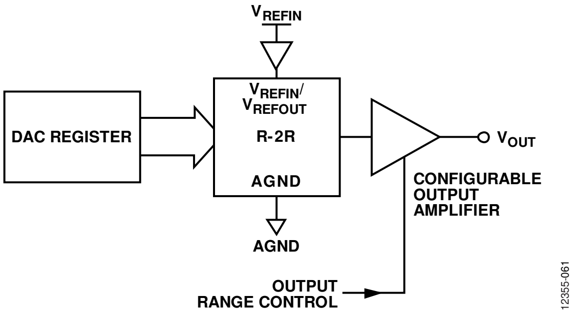


Figure 72. DAC Architecture

R-2R DAC

The architecture of the AD5761R consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 73. The 6 MSBs of the 16-bit data-word are decoded to drive 63 switches, E0 to E62, while the remaining 10 bits of the data-word drive the S0 to S9 switches of a 10-bit voltage mode R-2R ladder network.

The code loaded into the DAC register determines which arms of the ladder are switched between V_{REF} and ground (AGND). The output voltage is taken from the end of the ladder and amplified afterwards to provide the selected output voltage.

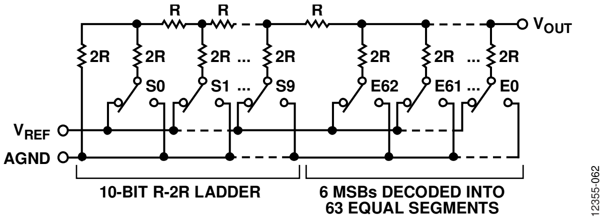


Figure 73. DAC Ladder Structure

Internal Reference

The AD5761R/AD5721R feature an on-chip reference. The on-chip reference is on at power-up, and this reference can be turned off by setting the software-programmable bit, DB5, in the control register. Table 12 shows how the state of the bit corresponds to the mode of operation.

The internal reference is available at the V_{RFEFIN}/V_{REFOUT} pin. A buffer is required if the reference output is used to drive external loads. Place a capacitor in the range of 1 nF to 100 nF between the reference output and DGND to improve the noise performance.

Reference Buffer

The AD5761R/AD5721R can operate with either an external or internal reference. The reference input has an input range of 2 V to 3 V with 2.5 V for specified performance. This input voltage is then buffered before it is applied to the DAC core.