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# Quad-Channel, 12-Bit, Serial Input, 4 mA to 20 mA Output DAC with Dynamic Power Control and HART Connectivity

Data Sheet **AD5737**

## FEATURES

**12-bit resolution and monotonicity**
**Dynamic power control for thermal management or external PMOS mode**
**Current output ranges: 0 mA to 20 mA, 4 mA to 20 mA, and 0 mA to 24 mA**
**±0.1% total unadjusted error (TUE) maximum**
**User-programmable offset and gain**
**On-chip diagnostics**
**On-chip reference: ±10 ppm/°C maximum**
**–40°C to +105°C temperature range**

## APPLICATIONS

**Process control**
**Actuator control**
**PLCs**
**HART network connectivity**

## GENERAL DESCRIPTION

The AD5737 is a quad-channel current output DAC that operates with a power supply range from 10.8 V to 33 V. On-chip dynamic power control minimizes package power dissipation by regulating the voltage on the output driver from 7.4 V to 29.5 V using a dc-to-dc boost converter optimized for minimum on-chip power dissipation.

Each channel has a corresponding CHART pin so that HART signals can be coupled onto the current output of the AD5737.

The AD5737 uses a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with standard SPI, QSPI™, MICROWIRE®, DSP, and microcontroller interface standards. The serial interface also features optional CRC-8 packet error checking, as well as a watchdog timer that monitors activity on the interface.

## PRODUCT HIGHLIGHTS

1. Dynamic power control for thermal management.
2. 12-bit performance.
3. Quad channel.
4. HART compliant.

## COMPANION PRODUCTS

**Product Family: AD5755, AD5755-1, AD5757, AD5735**
**HART Modem: AD5700, AD5700-1**
**External References: ADR445, ADR02**
**Digital Isolators: ADuM1410, ADuM1411**
**Power: ADP2302, ADP2303**
***Additional companion products on the AD5737 product page***

## FUNCTIONAL BLOCK DIAGRAM

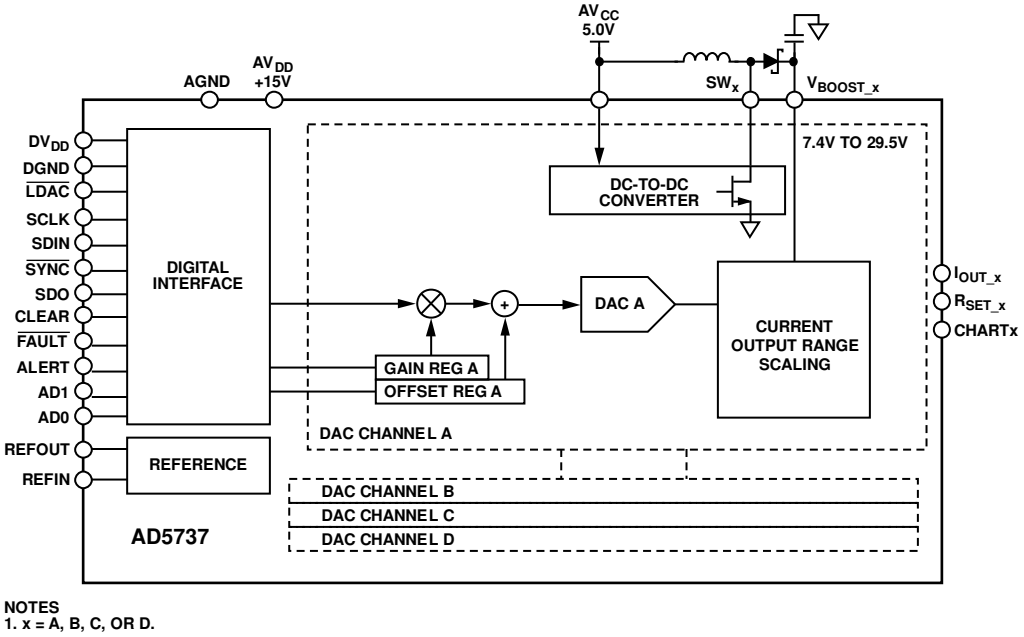


*Figure 1.*

**Rev. E** **Document Feedback**


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# AD5737* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD5757 Evaluation Board

## DOCUMENTATION

**Application Notes**

- AN-1289: Using the AD5755 and Similar Dynamic Power Control DACs in Applications Without Dynamic Power Control

**Data Sheet**

- AD5737: Quad-Channel, 12-Bit, Serial Input, 4 mA to 20 mA Output DAC with Dynamic Power Control and HART Connectivity Datasheet

## SOFTWARE AND SYSTEMS REQUIREMENTS

- AD5755 IIO Multi-Channel DAC Linux Driver

## REFERENCE MATERIALS

**Solutions Bulletins & Brochures**

- Digital to Analog Converters ICs Solutions Bulletin

## DESIGN RESOURCES

- AD5737 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD5737 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

# TABLE OF CONTENTS

## REVISION HISTORY

**9/14—Rev. D to Rev. E**

Changes to Table 3 ..... 7
Changes to Software Register and Status Register Descriptions ..... 24
Changes to Software Register Section, Table 24, and Table 25 ... 30
Changes to Status Register Section and Table 34 ..... 33
Changes to Packet Error Checking Section ..... 35

**6/14—Rev. C to Rev. D**

Change to Thermal Hysteresis Parameter, Table 1 ..... 6
Changes to Table 3 ..... 7
Changes to Figure 5 and Added Figure 6; Renumbered Sequentially ..... 9
Changes to Table 5 ..... 10
Changes to Figure 33, Figure 34, Figure 35, and Figure 36 ..... 18
Changes to Terminology Section ..... 21
Changes to Table 8 and Table 9 ..... 24
Changes to Software Register Section, Table 24, and Table 25 ..... 30
Changes to Readback Operation Section and Table 34, Added Table 30 and Table 31; Renumbered Sequentially ..... 31
Changes to Status Readback During a Write Section ..... 34
Changes to Packet Error Checking Section ..... 35
Changes to Table 36 ..... 37
Changes to Figure 62 ..... 40

**11/12—Rev. B to Rev. C**

Changed Thermal Impedance from 20°C/W to 28°C/W ..... 10
Changes to Pin 6 Description ..... 11
Changes to DUT_AD1, DUT_AD0 Description, Table 11 ..... 26
Changes to Changes to Packet Error Checking Section and Internal Reference Section ..... 34
Changes to Figure 56 ..... 36
Changes to Figure 62 ..... 41
Changes to Figure 65 ..... 43
Updated Outline Dimensions ..... 44

**5/12—Rev. A to Rev. B**

Changes to Companion Products Section ..... 1
Change to Table 5 ..... 12
Added Industrial HART Capable Analog Output Application Section and Figure 65, Renumbered Sequentially ..... 42
Updated Outline Dimensions ..... 43

**11/11—Rev. 0 to Rev. A**

Change to Accuracy, External $R_{SET}$ Parameter in Table 1 ..... 4
Changes to Power-On State of the AD5737 Section ..... 21
Changes to Readback Operation Section and Readback Example Section ..... 30

**7/11—Revision 0: Initial Version**

# DETAILED FUNCTIONAL BLOCK DIAGRAM

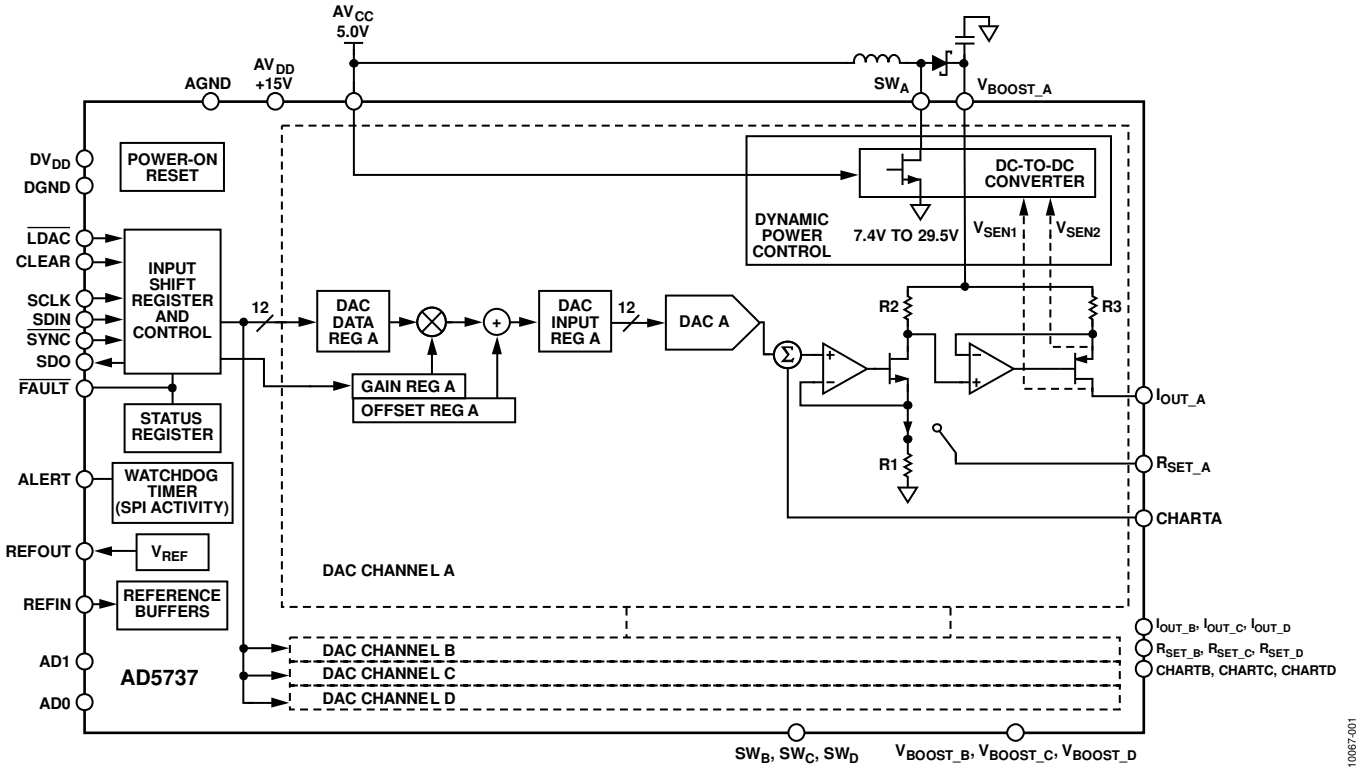



*Figure 2.*

# SPECIFICATIONS

$AV_{DD}$ = $V_{BOOST\_x}$ = 15 V; $DV_{DD}$ = 2.7 V to 5.5 V; $AV_{CC}$ = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; $R_L$ = 300 Ω; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 1.**

| Parameter[1] | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| CURRENT OUTPUT | | | | | |
| Output Current Ranges | 0 | | 24 | mA | |
| | 0 | | 20 | mA | |
| | 4 | | 20 | mA | |
| Resolution | 12 | | | Bits | |
| ACCURACY, EXTERNAL $R_{SET}$ | | | | | Assumes ideal resistor (see the External Current Setting Resistor section for more information) |
| Total Unadjusted Error (TUE) | −0.1 | ±0.019 | +0.1 | % FSR | |
| TUE Long-Term Stability | | 100 | | ppm FSR | Drift after 1000 hours, $T_J$ = 150°C |
| Relative Accuracy (INL) | −0.032 | ±0.006 | +0.032 | % FSR | |
| Differential Nonlinearity (DNL) | −1 | | +1 | LSB | Guaranteed monotonic |
| Offset Error | −0.1 | ±0.012 | +0.1 | % FSR | |
| Offset Error Drift[2] | | ±4 | | ppm FSR/°C | |
| Gain Error | −0.1 | ±0.004 | +0.1 | % FSR | |
| Gain TC[2] | | ±3 | | ppm FSR/°C | |
| Full-Scale Error | −0.1 | ±0.014 | +0.1 | % FSR | |
| Full-Scale TC[2] | | ±5 | | ppm FSR/°C | |
| DC Crosstalk | | 0.0005 | | % FSR | External $R_{SET}$ |
| ACCURACY, INTERNAL $R_{SET}$ | | | | | |
| Total Unadjusted Error (TUE)[3, 4] | −0.14 | ±0.022 | +0.14 | % FSR | |
| TUE Long-Term Stability | | 180 | | ppm FSR | Drift after 1000 hours, $T_J$ = 150°C |
| Relative Accuracy (INL) | −0.032 | ±0.006 | +0.032 | % FSR | |
| Differential Nonlinearity (DNL) | −1 | | +1 | LSB | Guaranteed monotonic |
| Offset Error[3, 4] | −0.1 | ±0.017 | +0.1 | % FSR | |
| Offset Error Drift[2] | | ±6 | | ppm FSR/°C | |
| Gain Error | −0.12 | ±0.004 | +0.12 | % FSR | |
| Gain TC[2] | | ±9 | | ppm FSR/°C | |
| Full-Scale Error[3, 4] | −0.14 | ±0.02 | +0.14 | % FSR | |
| Full-Scale TC[2] | | ±14 | | ppm FSR/°C | |
| DC Crosstalk[4] | | −0.011 | | % FSR | Internal $R_{SET}$ |
| OUTPUT CHARACTERISTICS[2] | | | | | |
| Current Loop Compliance Voltage | | $V_{BOOST\_x}$ − 2.4 | $V_{BOOST\_x}$ − 2.7 | V | |
| Output Current Drift vs. Time | | | | | Drift after 1000 hours, ¾ scale output, $T_J$ = 150°C |
| | | 90 | | ppm FSR | External $R_{SET}$ |
| | | 140 | | ppm FSR | Internal $R_{SET}$ |
| Resistive Load | | | 1000 | Ω | The dc-to-dc converter has been characterized with a maximum load of 1 kΩ, chosen such that compliance is not exceeded; see Figure 31 and the DC-DC MaxV bits in Table 27 |
| DC Output Impedance | | 100 | | MΩ | |
| DC PSRR | | 0.02 | 1 | µA/V | |
| REFERENCE INPUT/OUTPUT | | | | | |
| Reference Input[2] | | | | | |
| Reference Input Voltage | 4.95 | 5 | 5.05 | V | For specified performance |
| DC Input Impedance | 45 | 150 | | MΩ | |
| Reference Output | | | | | |
| Output Voltage | 4.995 | 5 | 5.005 | V | $T_A$ = 25°C |
| Reference TC[2] | −10 | ±5 | +10 | ppm/°C | |

| Parameter[1] | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| Output Noise (0.1 Hz to 10 Hz)[2] | | 7 | | μV p-p | |
| Noise Spectral Density[2] | | 100 | | nV/√Hz | At 10 kHz |
| Output Voltage Drift vs. Time[2] | | 180 | | ppm | Drift after 1000 hours, $T_J$ = 150°C |
| Capacitive Load[2] | | 1000 | | nF | |
| Load Current | | 9 | | mA | See Figure 42 |
| Short-Circuit Current | | 10 | | mA | |
| Line Regulation[2] | | 3 | | ppm/V | See Figure 43 |
| Load Regulation[2] | | 95 | | ppm/mA | See Figure 42 |
| Thermal Hysteresis[2] | | 200 | | ppm | |
| DC-TO-DC CONVERTER | | | | | |
| Switch | | | | | |
| Switch On Resistance | | 0.425 | | Ω | |
| Switch Leakage Current | | 10 | | nA | |
| Peak Current Limit | | 0.8 | | A | |
| Oscillator | | | | | |
| Oscillator Frequency | 11.5 | 13 | 14.5 | MHz | This oscillator is divided down to provide the dc-to-dc converter switching frequency |
| Maximum Duty Cycle | | 89.6 | | % | At 410 kHz dc-to-dc switching frequency |
| DIGITAL INPUTS[2] | | | | | JEDEC compliant |
| Input High Voltage, $V_{IH}$ | 2 | | | V | |
| Input Low Voltage, $V_{IL}$ | | | 0.8 | V | |
| Input Current | −1 | | +1 | μA | Per pin |
| Pin Capacitance | | 2.6 | | pF | Per pin |
| DIGITAL OUTPUTS[2] | | | | | |
| SDO, ALERT Pins | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | Sinking 200 μA |
| Output High Voltage, $V_{OH}$ | $DV_{DD}$ − 0.5 | | | V | Sourcing 200 μA |
| High Impedance Leakage Current | −1 | | +1 | μA | |
| High Impedance Output Capacitance | | 2.5 | | pF | |
| $\overline{\text{FAULT}}$ Pin | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | 10 kΩ pull-up resistor to $DV_{DD}$ |
| | | 0.6 | | V | At 2.5 mA |
| Output High Voltage, $V_{OH}$ | 3.6 | | | V | 10 kΩ pull-up resistor to $DV_{DD}$ |
| POWER REQUIREMENTS | | | | | |
| $AV_{DD}$ | 9 | | 33 | V | |
| $DV_{DD}$ | 2.7 | | 5.5 | V | |
| $AV_{CC}$ | 4.5 | | 5.5 | V | |
| $AI_{DD}$ | | 7 | 7.5 | mA | |
| $DI_{CC}$ | | 9.2 | 11 | mA | $V_{IH}$ = $DV_{DD}$, $V_{IL}$ = DGND, internal oscillator running, over supplies |
| $AI_{CC}$ | | | 1 | mA | Outputs unloaded, over supplies |
| $I_{BOOST}$[5] | | | 1 | mA | Per channel, 0 mA output |
| Power Dissipation | | 155 | | mW | $AV_{DD}$ = 15 V, $DV_{DD}$ = 5 V, dc-to-dc converter enabled, outputs disabled |

[1] Temperature range: −40°C to +105°C; typical at +25°C.
[2] Guaranteed by design and characterization; not production tested.
[3] For current outputs with internal $R_{SET}$, the offset, full-scale, and TUE measurements exclude dc crosstalk. The measurements are made with all four channels enabled and loaded with the same code.
[4] See the Current Output Mode with Internal $R_{SET}$ section for more information about dc crosstalk.
[5] Efficiency plots in Figure 33 through Figure 36 include the $I_{BOOST}$ quiescent current.

## AC PERFORMANCE CHARACTERISTICS

$AV_{DD}$ = $V_{BOOST\_x}$ = 15 V; $DV_{DD}$ = 2.7 V to 5.5 V; $AV_{CC}$ = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; $R_L$ = 300 Ω; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| Parameter[1] | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE, CURRENT OUTPUT | | | | | |
| Output Current Settling Time | | 15 | | µs | To 0.1% FSR, 0 mA to 24 mA range |
| | | See Test Conditions/Comments | | ms | For settling times when using the dc-to-dc converter, see Figure 26, Figure 27, and Figure 28 |
| Output Noise (0.1 Hz to 10 Hz Bandwidth) | | 0.15 | | LSB p-p | 12-bit LSB, 0 mA to 24 mA range |
| Output Noise Spectral Density | | 0.5 | | nA/√Hz | Measured at 10 kHz, midscale output, 0 mA to 24 mA range |

[1] Guaranteed by design and characterization; not production tested.

## TIMING CHARACTERISTICS

$AV_{DD}$ = $V_{BOOST\_x}$ = 15 V; $DV_{DD}$ = 2.7 V to 5.5 V; $AV_{CC}$ = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; $R_L$ = 300 Ω; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 3.**

| Parameter[1, 2, 3] | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Description |
|---|---|---|---|
| $t_1$ | 33 | ns min | SCLK cycle time |
| $t_2$ | 13 | ns min | SCLK high time |
| $t_3$ | 13 | ns min | SCLK low time |
| $t_4$ | 13 | ns min | $\overline{SYNC}$ falling edge to SCLK falling edge setup time |
| $t_5$ | 13 | ns min | 24th/32nd SCLK falling edge to $\overline{SYNC}$ rising edge (see Figure 54) |
| $t_6$ | 198 | ns min | $\overline{SYNC}$ high time following a configuration write |
| | 5 | µs min | $\overline{SYNC}$ high time following a DAC update write |
| $t_7$ | 5 | ns min | Data setup time |
| $t_8$ | 5 | ns min | Data hold time |
| $t_9$ | 20 | µs min | $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (applies to any channel with digital slew rate control enabled; single DAC updated) |
| | 5 | µs min | $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (single DAC updated) |
| $t_{10}$ | 10 | ns min | $\overline{LDAC}$ pulse width low |
| $t_{11}$ | 500 | ns max | $\overline{LDAC}$ falling edge to DAC output response time |
| $t_{12}$ | See Table 2 | µs max | DAC output settling time |
| $t_{13}$ | 10 | ns min | CLEAR high time |
| $t_{14}$ | 5 | µs max | CLEAR activation time |
| $t_{15}$ | 40 | ns max | SCLK rising edge to SDO valid |
| $t_{16}$ | 5 | µs min | $\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC}$ = 0) (single DAC updated) |
| $t_{17}$ | 500 | ns min | $\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge |
| $t_{18}$ | 800 | ns min | $\overline{RESET}$ pulse width |
| $t_{19}$ | 20 | µs min | $\overline{SYNC}$ rising edge to next $\overline{SYNC}$ low (falling edge (digital slew rate control enabled; single DAC updated) |
| | 5 | µs min | $\overline{SYNC}$ rising edge to next $\overline{SYNC}$ low (falling edge (digital slew rate control disabled; single DAC updated) |

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_{RISE}$ = $t_{FALL}$ = 5 ns (10% to 90% of $DV_{DD}$) and timed from a voltage level of 1.2 V.
[3] See Figure 3, Figure 4, Figure 5, and Figure 7.

### *Timing Diagrams*

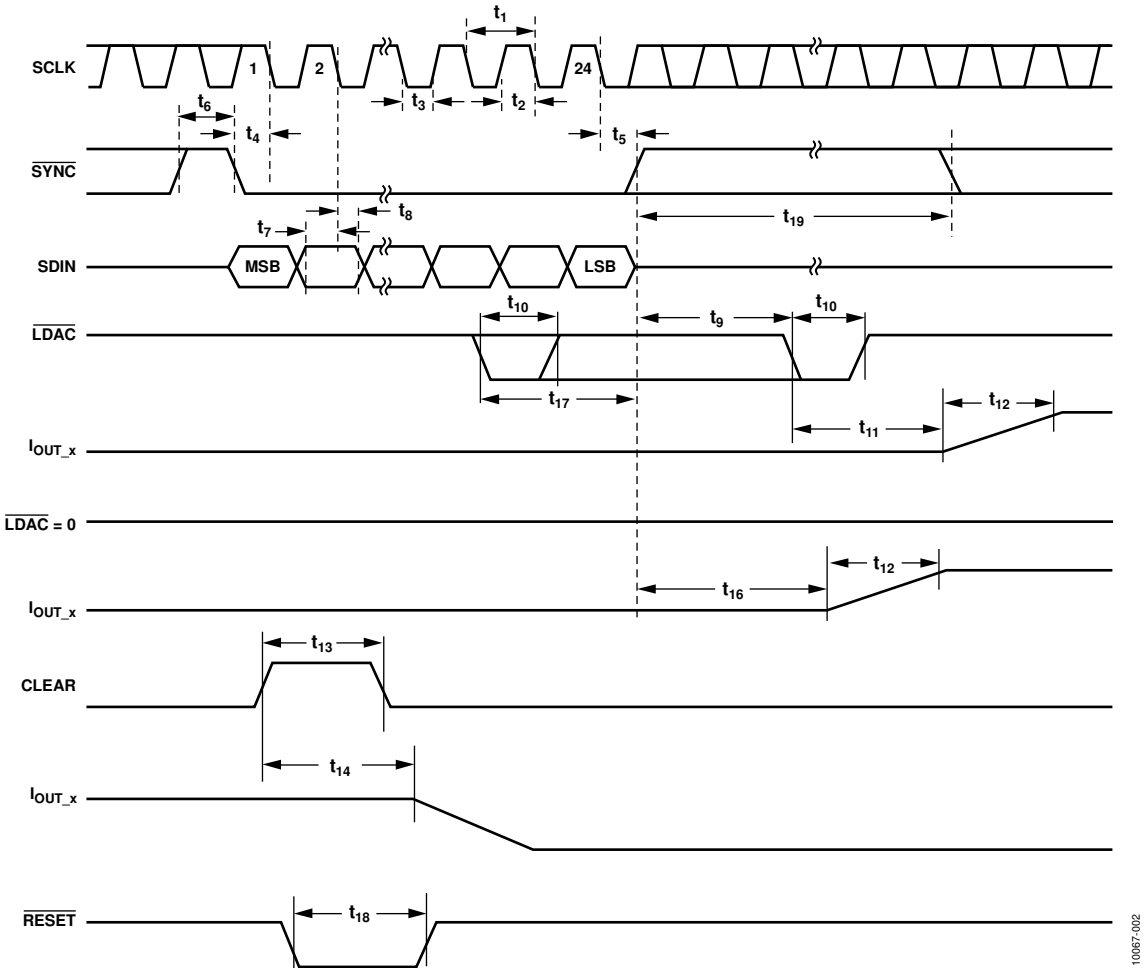
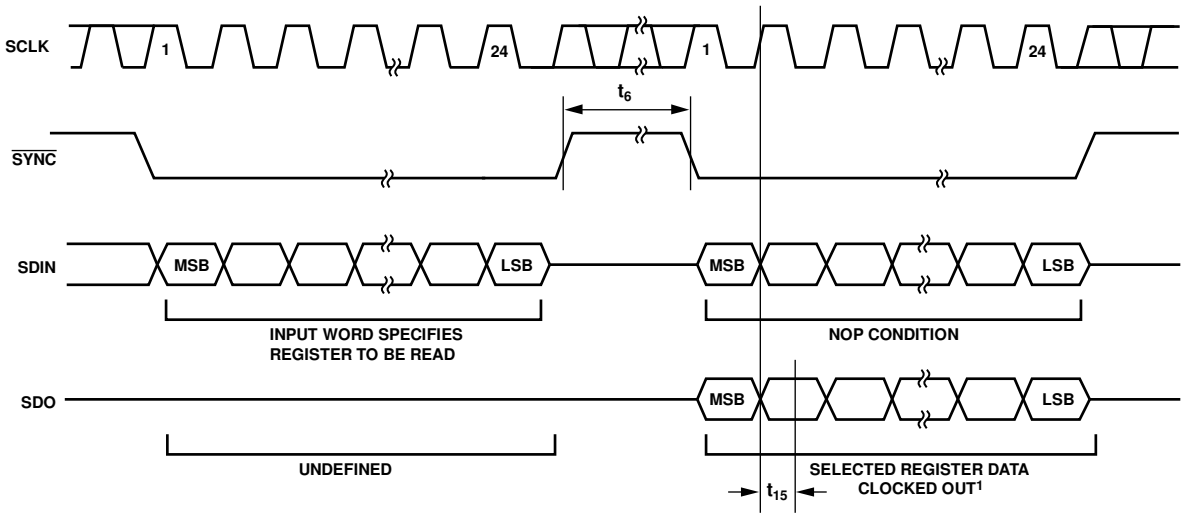
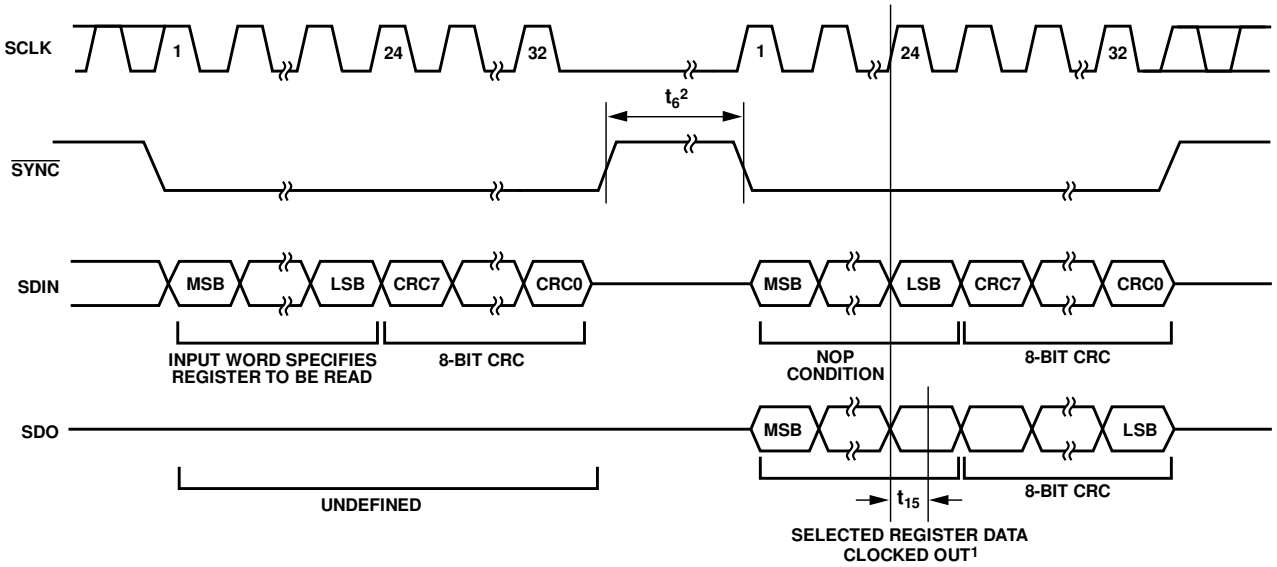



*Figure 3. Serial Interface Timing Diagram*




**[1]IF FIRST SCLK IS NEGATIVE EDGE WITHIN SYNC FRAME OF NOP CONDITION, 7 DONT CARE BITS + 16 DATA BITS CLOCKED OUT (TOTAL 23 BITS). IF FIRST SCLK IS POSITIVE EDGE WITHIN SYNC FRAME OF NOP CONDITION, 8 DONT CARE BITS + 16 DATA BITS CLOCKED OUT (TOTAL 24 BITS). SEE THE READBACK OPERATION SECTION FOR FURTHER INFORMATION.**

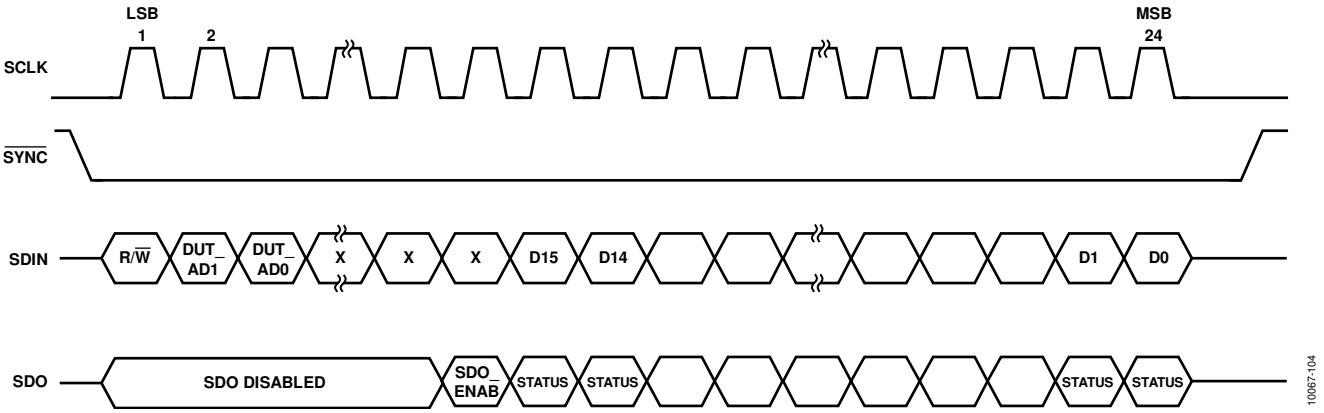
*Figure 4. Readback Timing Diagram (Packet Error Checking Disabled)*




[1]IF FIRST SCLK IS NEGATIVE EDGE WITHIN SYNC FRAME OF NOP CONDITION, 7 DONT CARE BITS + 16 DATA BITS CLOCKED OUT + 8 CRC BITS (TOTAL 31 BITS). IF FIRST SCLK IS POSITIVE EDGE WITHIN SYNC FRAME OF NOP CONDITION, 8 DONT CARE BITS + 16 DATA BITS CLOCKED OUT + 8 CRC BITS (TOTAL 32 BITS).
[2]AVOID SCLK ACTIVITY DURING $t_6$ AS IT MAY RESULT IN A PEC ERROR ON READBACK.
SEE THE READBACK OPERATION AND PACKET ERROR CHECKING SECTIONS FOR FURTHER INFORMATION.

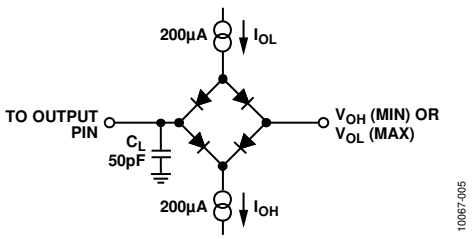
10067-004

*Figure 5. Readback Timing Diagram (Packet Error Checking Enabled)*




10067-104

*Figure 6. Status Readback During a Write*




10067-005

*Figure 7. Load Circuit for SDO Timing Diagrams*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

**Table 4.**

| Parameter | Rating |
|---|---|
| $AV_{DD}$, $V_{BOOST\_x}$ to AGND, DGND | −0.3 V to +33 V |
| $AV_{CC}$ to AGND | −0.3 V to +7 V |
| $DV_{DD}$ to DGND | −0.3 V to +7 V |
| Digital Inputs to DGND | −0.3 V to $DV_{DD}$ + 0.3 V or +7 V (whichever is less) |
| Digital Outputs to DGND | −0.3 V to $DV_{DD}$ + 0.3 V or +7 V (whichever is less) |
| REFIN, REFOUT to AGND | −0.3 V to $AV_{DD}$ + 0.3 V or +7 V (whichever is less) |
| $I_{OUT\_x}$ to AGND | AGND to $V_{BOOST\_x}$ or 33 V if using the dc-to-dc converter |
| $SW_x$ to AGND | −0.3 V to +33 V |
| AGND, $GNDSW_x$ to DGND | −0.3 V to +0.3 V |
| Operating Temperature Range ($T_A$) | |
| Industrial[1] | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature ($T_J$ max) | 125°C |
| Power Dissipation | ($T_J$ max − $T_A$)/$\theta_{JA}$ |
| Lead Temperature | JEDEC industry standard |
| Soldering | J-STD-020 |

[1] Power dissipated on chip must be derated to keep the junction temperature below 125°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

Junction-to-air thermal resistance ($\theta_{JA}$) is specified for a JEDEC 4-layer test board.

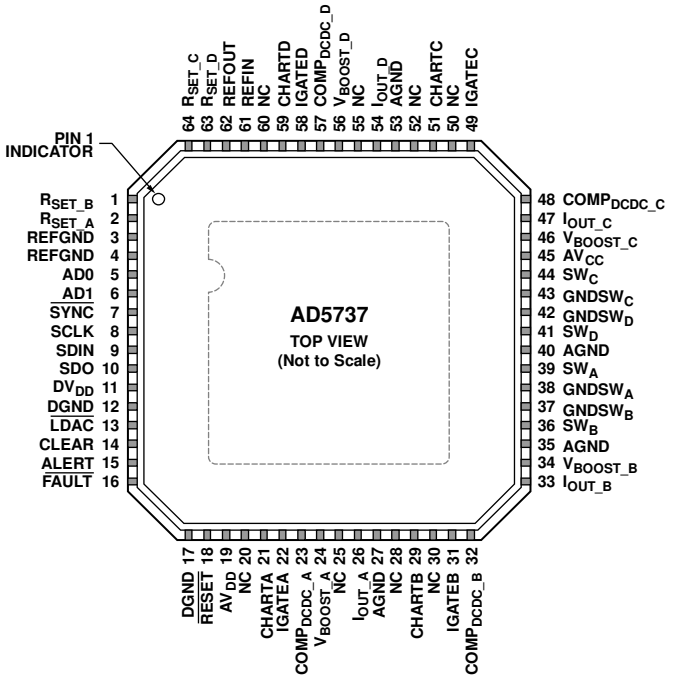
**Table 5. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 64-Lead LFCSP (CP-64-3) | 28 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS




NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PADDLE SHOULD BE CONNECTED TO AGND, OR, ALTERNATIVELY, IT CAN BE LEFT ELECTRICALLY UNCONNECTED. IT IS RECOMMENDED THAT THE PADDLE BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE.

10067-006

*Figure 8. Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $R_{SET\_B}$ | An external, precision, low drift, 15 kΩ current setting resistor can be connected to this pin to improve the $I_{OUT\_B}$ temperature drift performance. For more information, see the External Current Setting Resistor section. |
| 2 | $R_{SET\_A}$ | An external, precision, low drift, 15 kΩ current setting resistor can be connected to this pin to improve the $I_{OUT\_A}$ temperature drift performance. For more information, see the External Current Setting Resistor section. |
| 3 | REFGND | Ground Reference Point for Internal Reference. |
| 4 | REFGND | Ground Reference Point for Internal Reference. |
| 5 | AD0 | Address Decode for the Device Under Test (DUT) on the Board. |
| 6 | AD1 | Address Decode for the DUT on the Board. It is not recommended to tie both AD1 and AD0 low when using PEC (see the Packet Error Checking section). |
| 7 | $\overline{SYNC}$ | Frame Synchronization Signal for the Serial Interface. Active low input. When $\overline{SYNC}$ is low, data is clocked into the input shift register on the falling edge of SCLK. |
| 8 | SCLK | Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. The serial interface operates at clock speeds of up to 30 MHz. |
| 9 | SDIN | Serial Data Input. Data must be valid on the falling edge of SCLK. |
| 10 | SDO | Serial Data Output. Used to clock data from the serial register in readback mode (see Figure 4 and Figure 5). |
| 11 | $DV_{DD}$ | Digital Supply Pin. The voltage range is from 2.7 V to 5.5 V. |
| 12 | DGND | Digital Ground. |
| 13 | $\overline{LDAC}$ | Load DAC. This active low input is used to update the DAC register and, consequently, the DAC outputs. When $\overline{LDAC}$ is tied permanently low, the addressed DAC data register is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle, the DAC input register is updated, but the DAC output is updated only on the falling edge of $\overline{LDAC}$ (see Figure 3). Using this mode, all analog outputs can be updated simultaneously. Do not leave the $\overline{LDAC}$ pin unconnected. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 14 | CLEAR | Active High, Edge Sensitive Input. When this pin is asserted, the output current is set to the programmed clear code bit setting. Only channels enabled to be cleared are cleared. For more information, see the Asynchronous Clear section. When CLEAR is active, the DAC output register cannot be written to. |
| 15 | ALERT | Active High Output. This pin is asserted when there is no SPI activity on the interface pins for a preset time. For more information, see the Alert Output section. |
| 16 | $\overline{\text{FAULT}}$ | Active Low, Open-Drain Output. This pin is asserted low when any of the following conditions is detected: open circuit, PEC error, or an overtemperature condition (see the Fault Output section). |
| 17 | DGND | Digital Ground. |
| 18 | $\overline{\text{RESET}}$ | Hardware Reset, Active Low Input. |
| 19 | $AV_{DD}$ | Positive Analog Supply Pin. The voltage range is from 9 V to 33 V. |
| 20 | NC | No Connect. Do not connect to this pin. |
| 21 | CHARTA | HART Input Connection for DAC Channel A. For more information, see the HART Connectivity section. |
| 22 | IGATEA | Optional Connection for External Pass Transistor. Leave this pin unconnected when using the dc-to-dc converter. For more information, see the External PMOS Mode section. |
| 23 | $COMP_{DCDC\_A}$ | DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel A dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin. For more information, see the DC-to-DC Converter Compensation Capacitors section and the $AI_{CC}$ Supply Requirements—Slewing section. |
| 24 | $V_{BOOST\_A}$ | Supply for Channel A Current Output Stage (see Figure 49). To use the dc-to-dc converter, connect this pin as shown in Figure 56. |
| 25 | NC | No Connect. Do not connect to this pin. |
| 26 | $I_{OUT\_A}$ | Current Output Pin for DAC Channel A. |
| 27 | AGND | Ground Reference Point for Analog Circuitry. This pin must be connected to 0 V. |
| 28 | NC | No Connect. Do not connect to this pin. |
| 29 | CHARTB | HART Input Connection for DAC Channel B. For more information, see the HART Connectivity section. |
| 30 | NC | No Connect. Do not connect to this pin. |
| 31 | IGATEB | Optional Connection for External Pass Transistor. Leave this pin unconnected when using the dc-to-dc converter. For more information, see the External PMOS Mode section. |
| 32 | $COMP_{DCDC\_B}$ | DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel B dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin. For more information, see the DC-to-DC Converter Compensation Capacitors section and the $AI_{CC}$ Supply Requirements—Slewing section. |
| 33 | $I_{OUT\_B}$ | Current Output Pin for DAC Channel B. |
| 34 | $V_{BOOST\_B}$ | Supply for Channel B Current Output Stage (see Figure 49). To use the dc-to-dc converter, connect this pin as shown in Figure 56. |
| 35 | AGND | Ground Reference Point for Analog Circuitry. This pin must be connected to 0 V. |
| 36 | $SW_B$ | Switching Output for Channel B DC-to-DC Circuitry. To use the dc-to-dc converter, connect this pin as shown in Figure 56. |
| 37 | $GNDSW_B$ | Ground Connection for DC-to-DC Switching Circuit. This pin must always be connected to ground. |
| 38 | $GNDSW_A$ | Ground Connection for DC-to-DC Switching Circuit. This pin must always be connected to ground. |
| 39 | $SW_A$ | Switching Output for Channel A DC-to-DC Circuitry. To use the dc-to-dc converter, connect this pin as shown in Figure 56. |
| 40 | AGND | Ground Reference Point for Analog Circuitry. This pin must be connected to 0 V. |
| 41 | $SW_D$ | Switching Output for Channel D DC-to-DC Circuitry. To use the dc-to-dc converter, connect this pin as shown in Figure 56. |
| 42 | $GNDSW_D$ | Ground Connection for DC-to-DC Switching Circuit. This pin must always be connected to ground. |
| 43 | $GNDSW_C$ | Ground Connection for DC-to-DC Switching Circuit. This pin must always be connected to ground. |
| 44 | $SW_C$ | Switching Output for Channel C DC-to-DC Circuitry. To use the dc-to-dc converter, connect this pin as shown in Figure 56. |
| 45 | $AV_{CC}$ | Supply for DC-to-DC Circuitry. The voltage range is from 4.5 V to 5.5 V. |
| 46 | $V_{BOOST\_C}$ | Supply for Channel C Current Output Stage (see Figure 49). To use the dc-to-dc converter, connect this pin as shown in Figure 56. |
| 47 | $I_{OUT\_C}$ | Current Output Pin for DAC Channel C. |
| 48 | $COMP_{DCDC\_C}$ | DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel C dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin. For more information, see the DC-to-DC Converter Compensation Capacitors section and the $AI_{CC}$ Supply Requirements—Slewing section. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 49 | IGATEC | Optional Connection for External Pass Transistor. Leave this pin unconnected when using the dc-to-dc converter. For more information, see the External PMOS Mode section. |
| 50 | NC | No Connect. Do not connect to this pin. |
| 51 | CHARTC | HART Input Connection for DAC Channel C. For more information, see the HART Connectivity section. |
| 52 | NC | No Connect. Do not connect to this pin. |
| 53 | AGND | Ground Reference Point for Analog Circuitry. This pin must be connected to 0 V. |
| 54 | $I_{OUT\_D}$ | Current Output Pin for DAC Channel D. |
| 55 | NC | No Connect. Do not connect to this pin. |
| 56 | $V_{BOOST\_D}$ | Supply for Channel D Current Output Stage (see Figure 49). To use the dc-to-dc converter, connect this pin as shown in Figure 56. |
| 57 | $COMP_{DCDC\_D}$ | DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel D dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin. For more information, see the DC-to-DC Converter Compensation Capacitors section and the $AI_{CC}$ Supply Requirements—Slewing section. |
| 58 | IGATED | Optional Connection for External Pass Transistor. Leave this pin unconnected when using the dc-to-dc converter. For more information, see the External PMOS Mode section. |
| 59 | CHARTD | HART Input Connection for DAC Channel D. For more information, see the HART Connectivity section. |
| 60 | NC | No Connect. Do not connect to this pin. |
| 61 | REFIN | External Reference Voltage Input. |
| 62 | REFOUT | Internal Reference Voltage Output. It is recommended that a 0.1 µF capacitor be placed between REFOUT and REFGND. REFOUT must be connected to REFIN to use the internal reference. |
| 63 | $R_{SET\_D}$ | An external, precision, low drift, 15 kΩ current setting resistor can be connected to this pin to improve the $I_{OUT\_D}$ temperature drift performance. For more information, see the External Current Setting Resistor section. |
| 64 | $R_{SET\_C}$ | An external, precision, low drift, 15 kΩ current setting resistor can be connected to this pin to improve the $I_{OUT\_C}$ temperature drift performance. For more information, see the External Current Setting Resistor section. |
| | EPAD | Exposed Pad. The exposed paddle must be connected to AGND, or, alternatively, it can be left electrically unconnected. It is recommended that the paddle be thermally connected to a copper plane for enhanced thermal performance. |

# TYPICAL PERFORMANCE CHARACTERISTICS

## CURRENT OUTPUTS

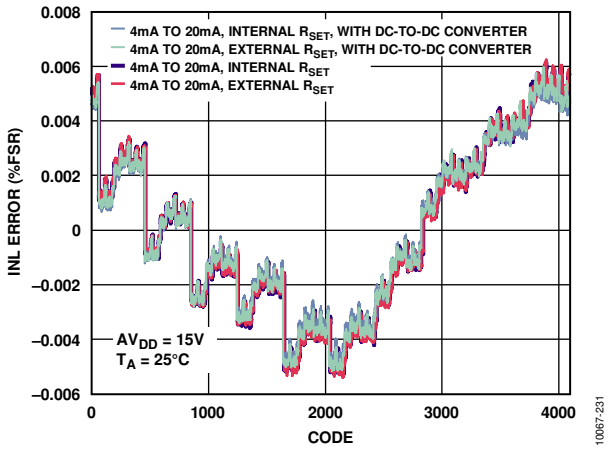



Figure 9. Integral Nonlinearity Error vs. DAC Code

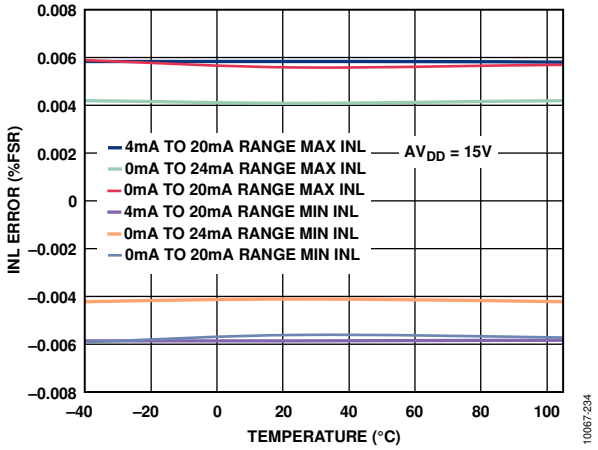



Figure 12. Integral Nonlinearity Error vs. Temperature, Internal $R_{SET}$

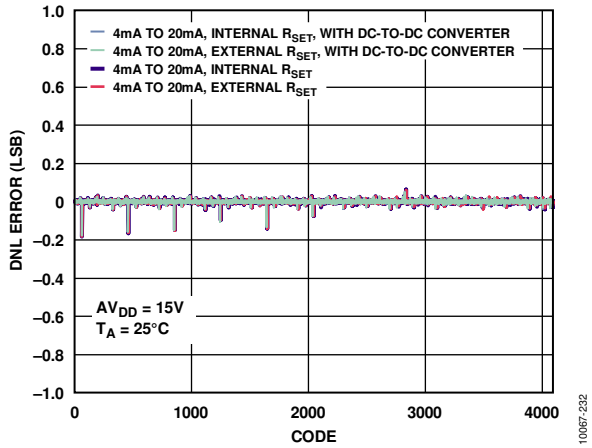



Figure 10. Differential Nonlinearity Error vs. DAC Code

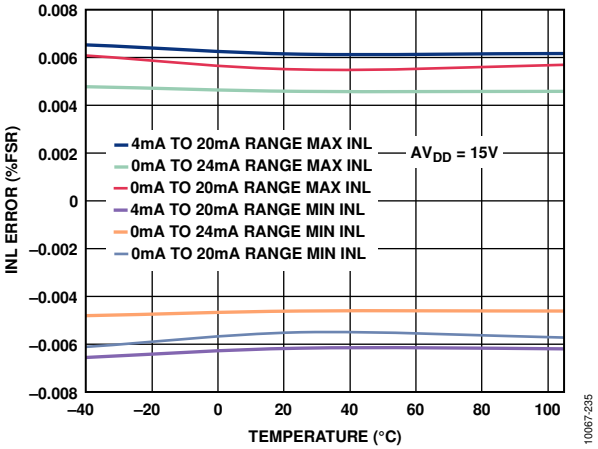



Figure 13. Integral Nonlinearity Error vs. Temperature, External $R_{SET}$

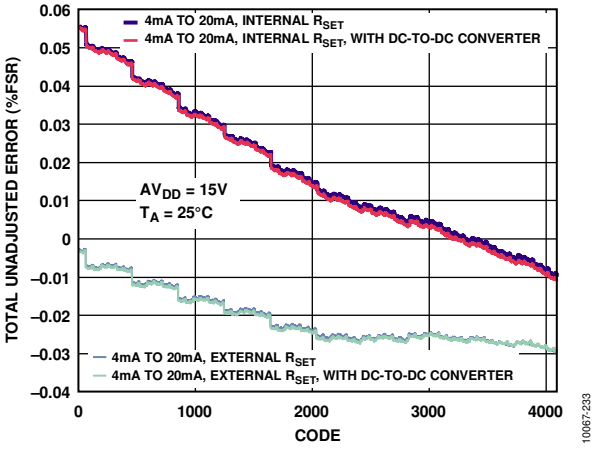



Figure 11. Total Unadjusted Error vs. DAC Code

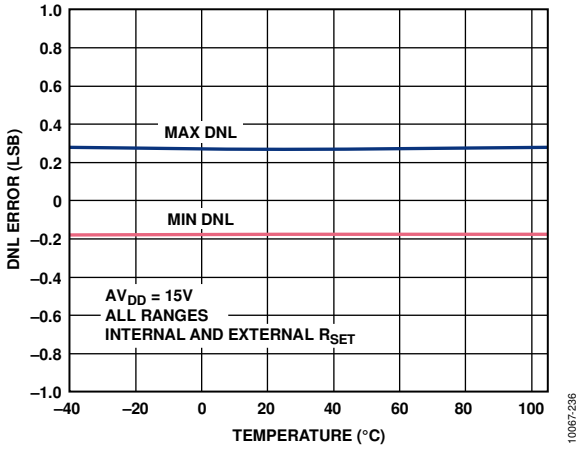



Figure 14. Differential Nonlinearity Error vs. Temperature

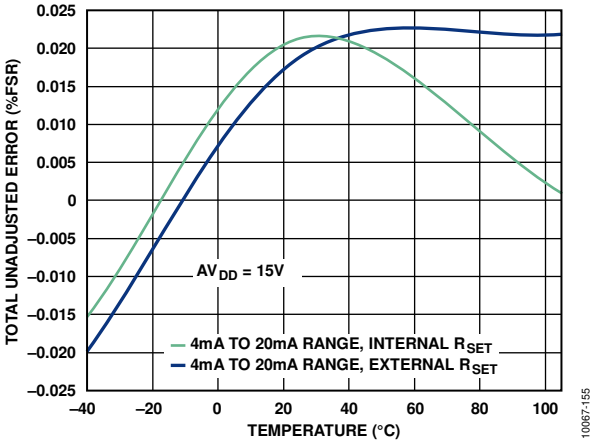



Figure 15. Total Unadjusted Error vs. Temperature

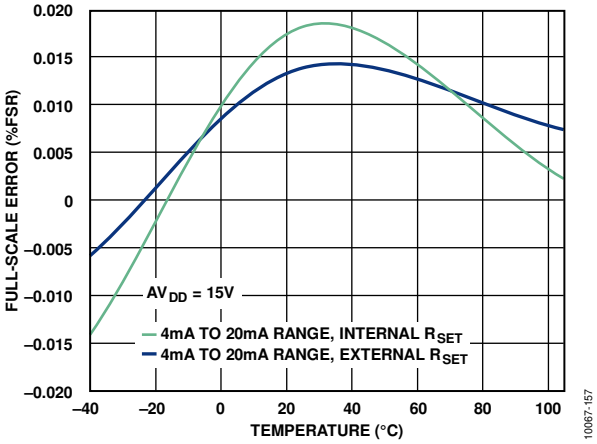



Figure 16. Full-Scale Error vs. Temperature

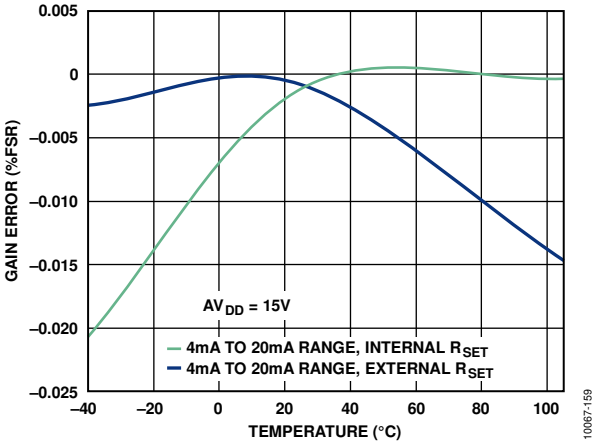



Figure 17. Gain Error vs. Temperature

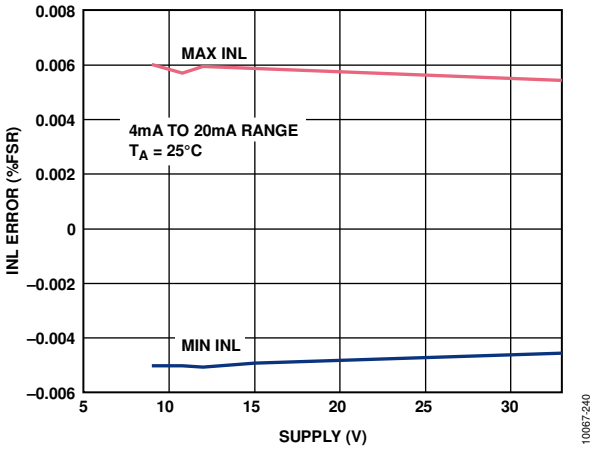



Figure 18. Integral Nonlinearity Error vs. Supply, External $R_{SET}$

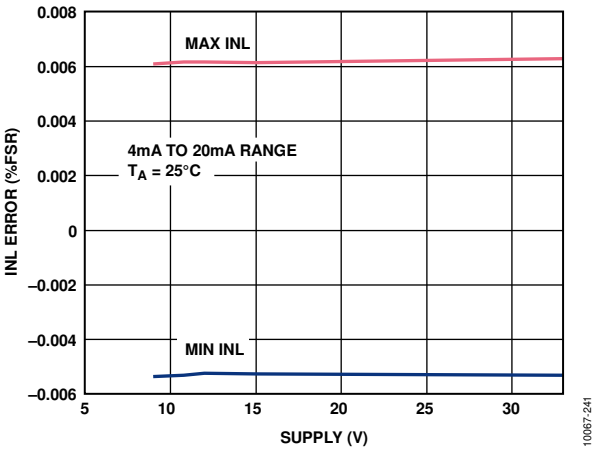



Figure 19. Integral Nonlinearity Error vs. Supply, Internal $R_{SET}$

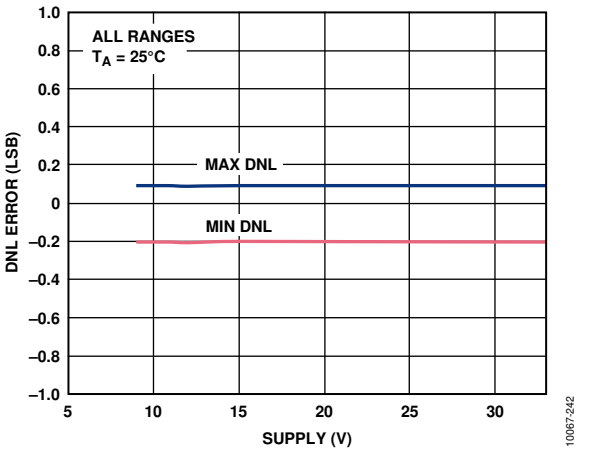



Figure 20. Differential Nonlinearity Error vs. Supply

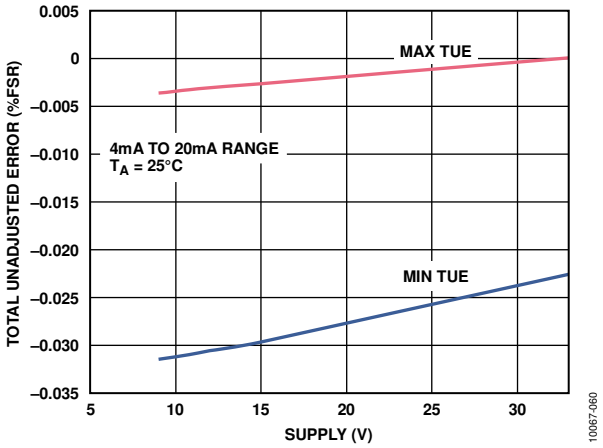



Figure 21. Total Unadjusted Error vs. Supply, External $R_{SET}$

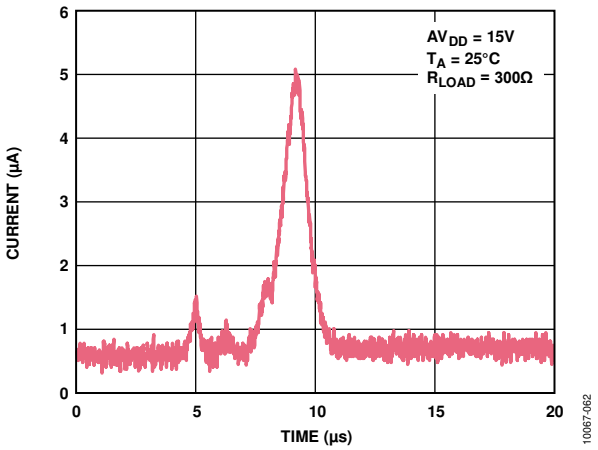



Figure 24. Current vs. Time on Power-Up

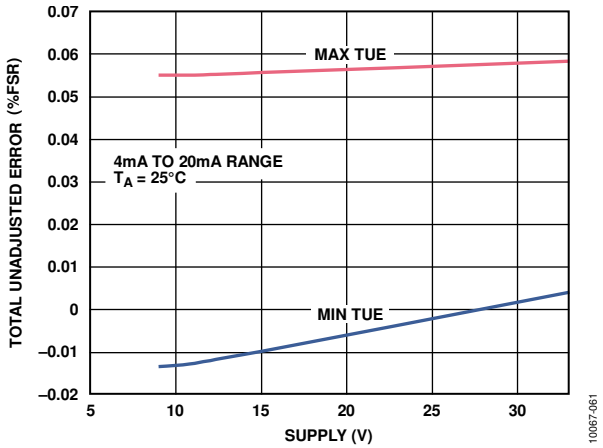



Figure 22. Total Unadjusted Error vs. Supply, Internal $R_{SET}$

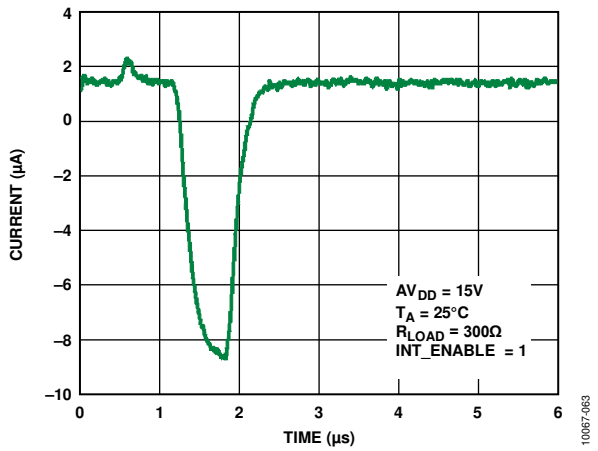



Figure 25. Current vs. Time on Output Enable

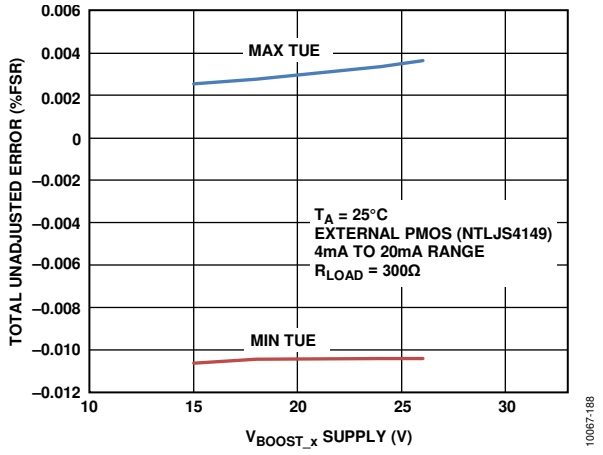



Figure 23. Total Unadjusted Error vs. $V_{BOOST\_x}$ Supply Using External PMOS Mode

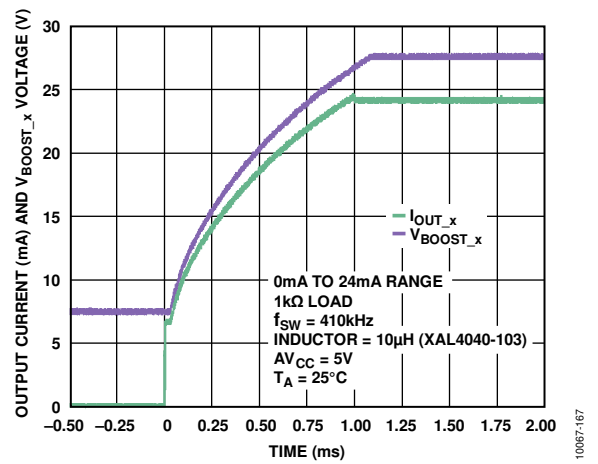



Figure 26. Output Current and $V_{BOOST\_x}$ Settling Time with DC-to-DC Converter (See Figure 56)

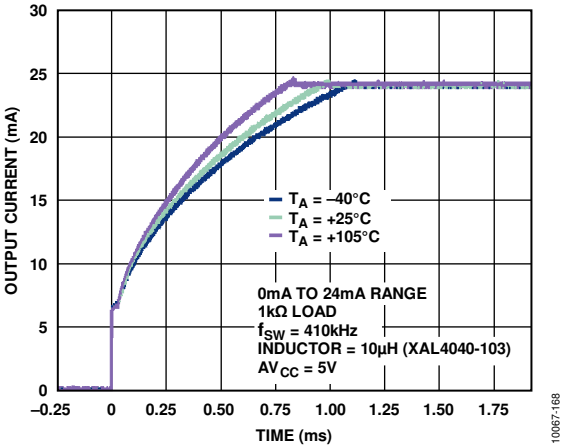



Figure 27. Output Current Settling Time with DC-to-DC Converter over Temperature (See Figure 56)

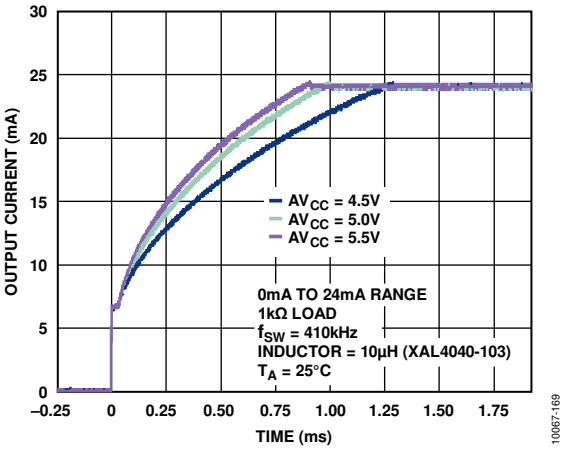



Figure 28. Output Current Settling Time with DC-to-DC Converter over $AV_{CC}$ (See Figure 56)

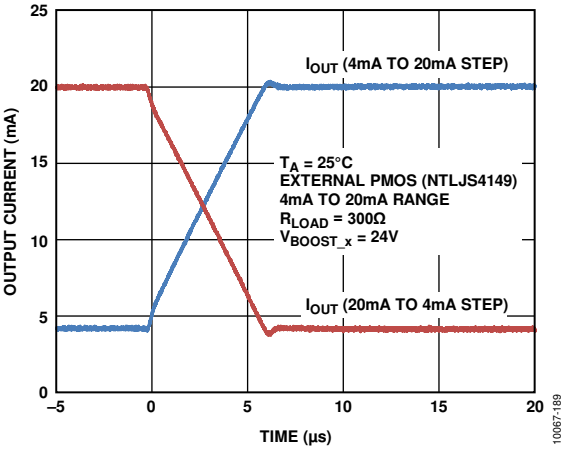



Figure 29. Output Current Settling Time with External PMOS Transistor

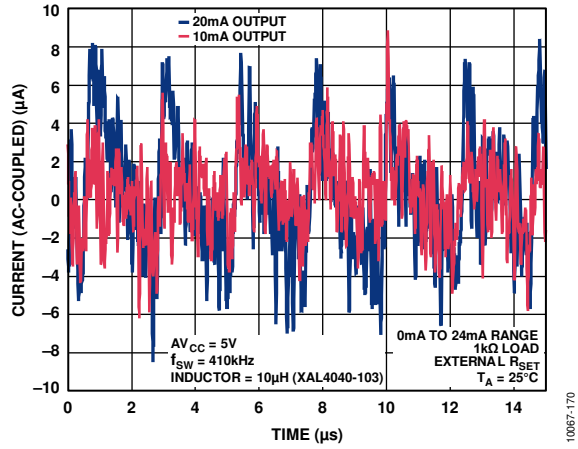



Figure 30. Output Current, AC-Coupled vs. Time with DC-to-DC Converter (See Figure 56)

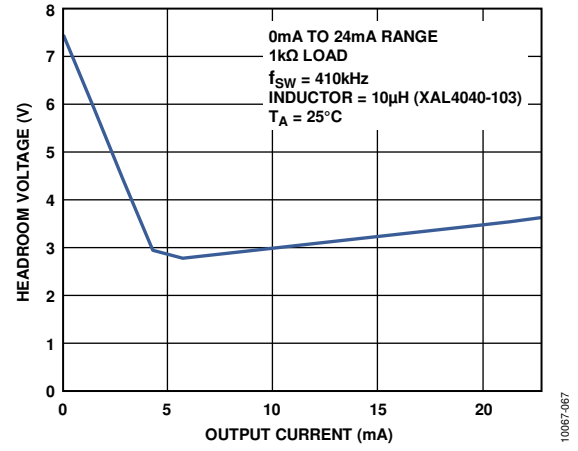



Figure 31. DC-to-DC Converter Headroom vs. Output Current (See Figure 56)

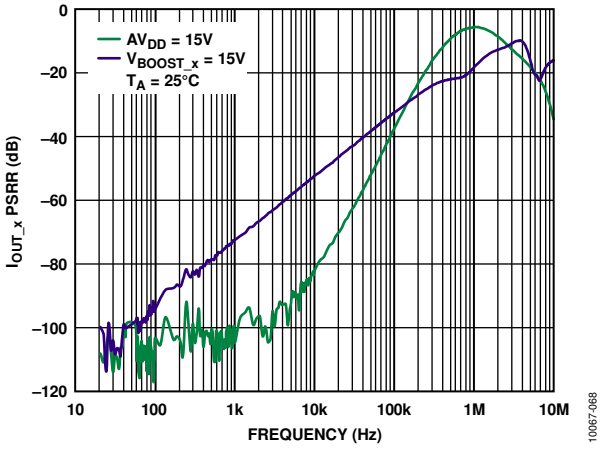



Figure 32. $I_{OUT\_x}$ PSRR vs. Frequency

## DC-TO-DC CONVERTER

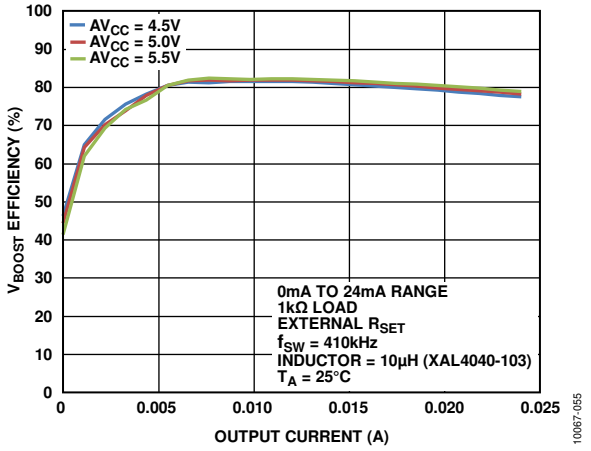



Figure 33. Efficiency at $V_{BOOST\_x}$ vs. Output Current (See Figure 56)

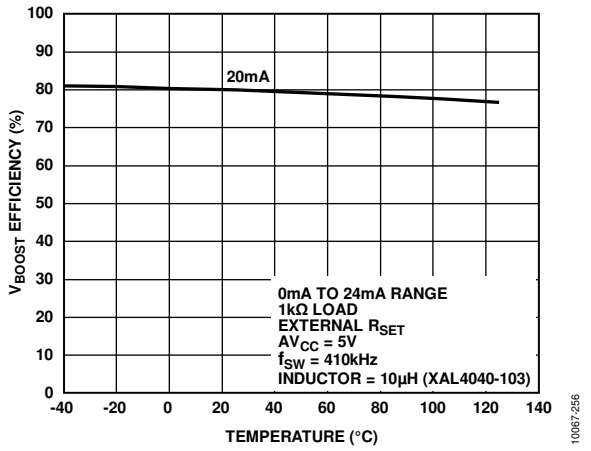



Figure 34. Efficiency at $V_{BOOST\_x}$ vs. Temperature (See Figure 56)

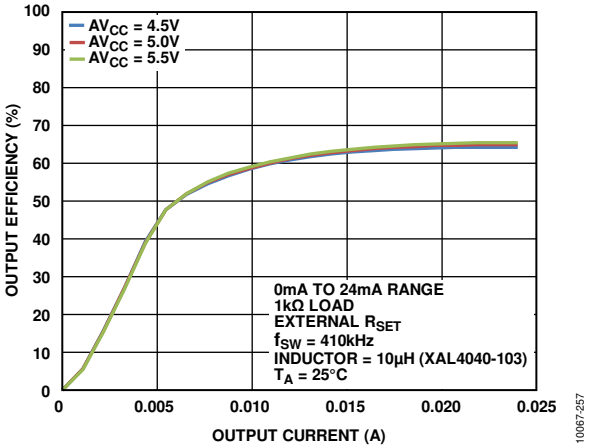



Figure 35. Output Efficiency vs. Output Current (See Figure 56)

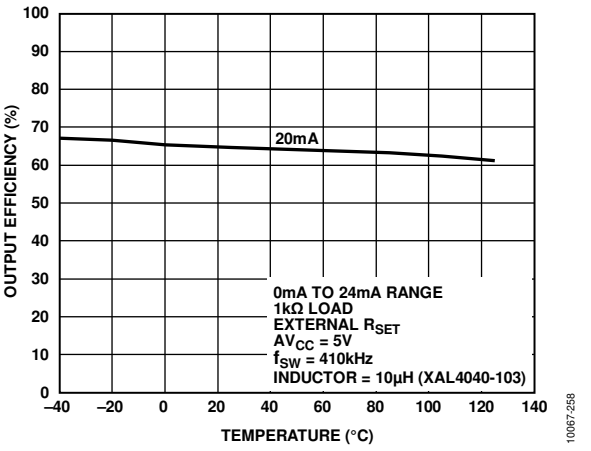



Figure 36. Output Efficiency vs. Temperature (See Figure 56)

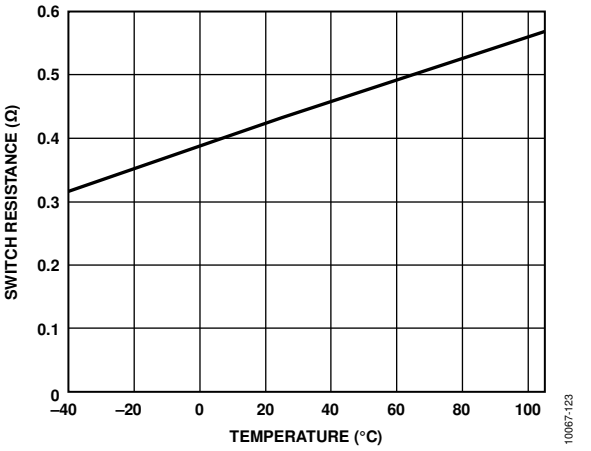



Figure 37. Switch Resistance vs. Temperature

## REFERENCE

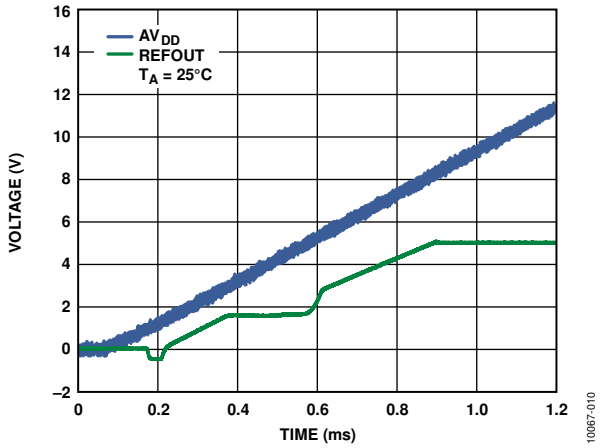



Figure 38. REFOUT Voltage Turn-On Transient

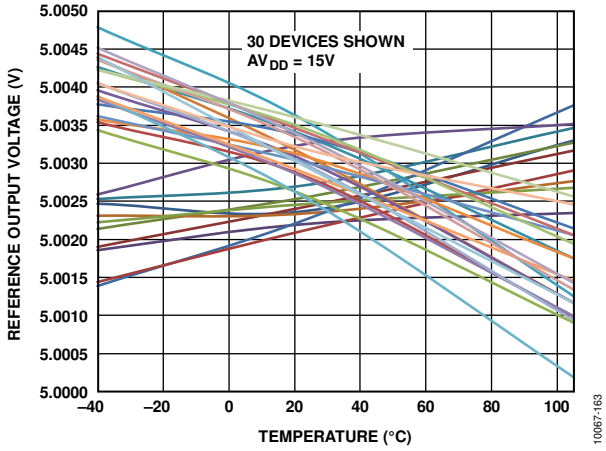



Figure 41. REFOUT Voltage vs. Temperature (When the AD5737 is soldered onto a PCB, the reference shifts due to thermal shock on the package. The average output voltage shift is −4 mV. Measurement of these parts after seven days shows that the outputs typically shift back 2 mV toward their initial values. This second shift is due to the relaxation of stress incurred during soldering.)

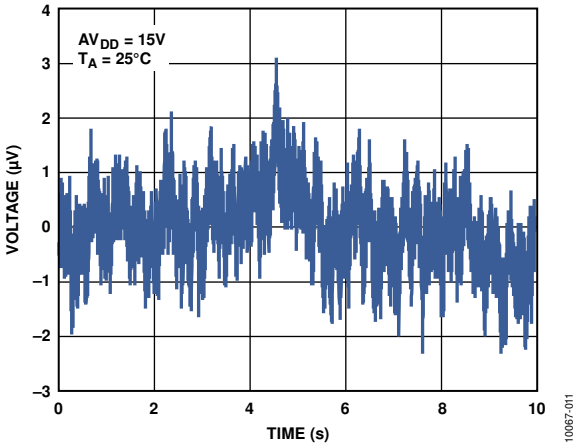



Figure 39. REFOUT Output Noise (0.1 Hz to 10 Hz Bandwidth)

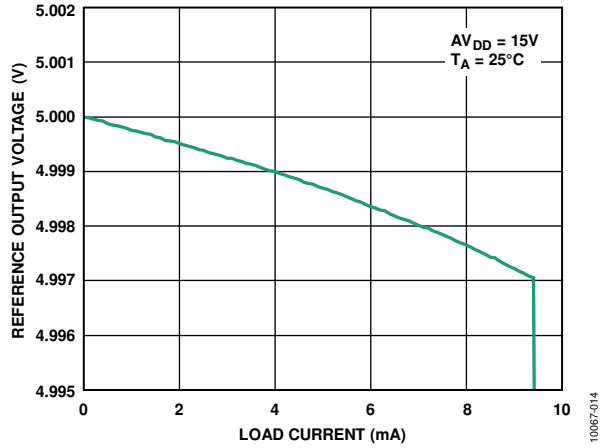



Figure 42. REFOUT Voltage vs. Load Current

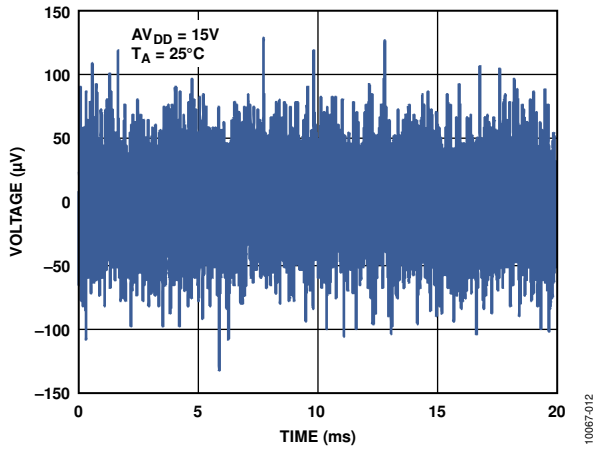



Figure 40. REFOUT Output Noise (100 kHz Bandwidth)

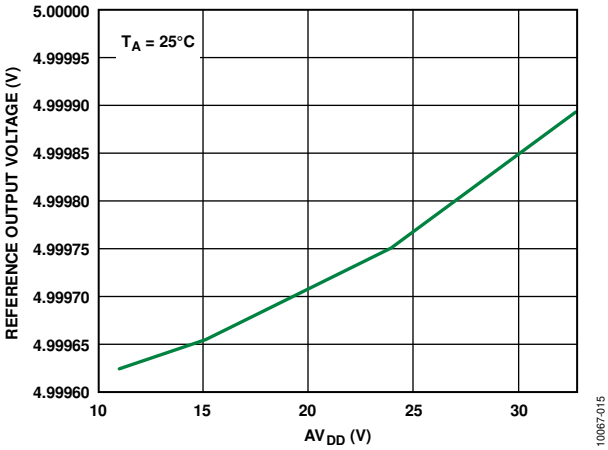



Figure 43. REFOUT Voltage vs. $AV_{DD}$

## GENERAL

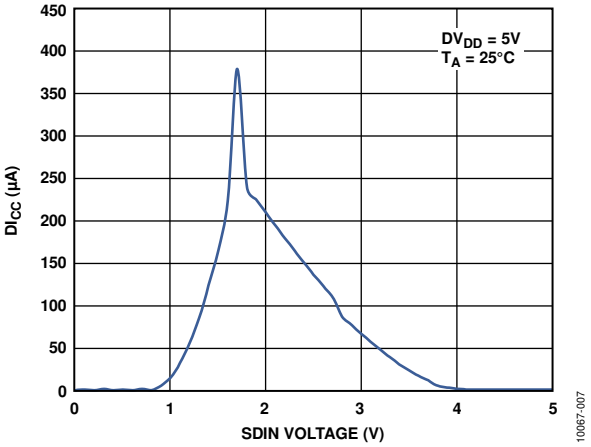



Figure 44. $DI_{CC}$ vs. Logic Input Voltage

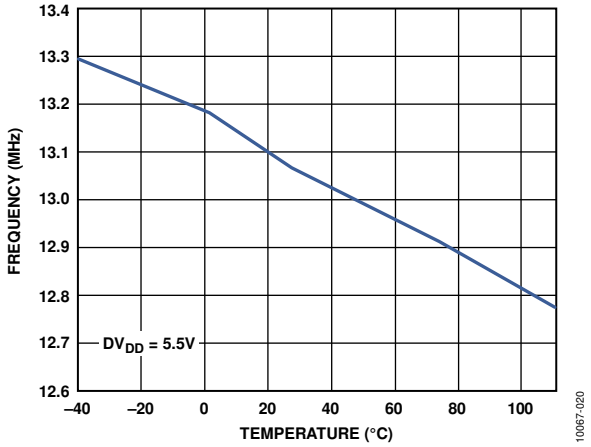



Figure 46. Internal Oscillator Frequency vs. Temperature

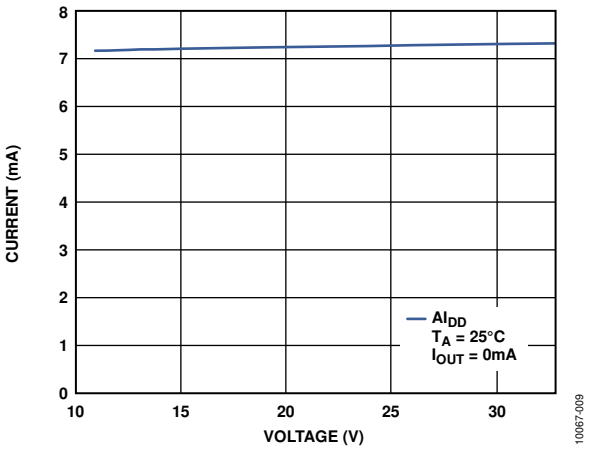



Figure 45. Supply Current ($AI_{DD}$) vs. Supply Voltage ($AV_{DD}$)

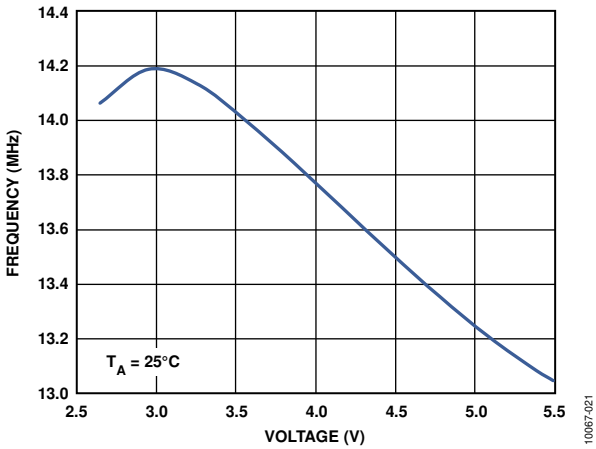



Figure 47. Internal Oscillator Frequency vs. $DV_{DD}$ Supply Voltage

# TERMINOLOGY

**Relative Accuracy or Integral Nonlinearity (INL)**
Relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation from the best fit line through the DAC transfer function. INL is expressed in percent of full-scale range (% FSR). A typical INL vs. code plot is shown in Figure 9.

**Differential Nonlinearity (DNL)**
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity. The AD5737 is guaranteed monotonic by design. A typical DNL vs. code plot is shown in Figure 10.

**Monotonicity**
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5737 is monotonic over its full operating temperature range.

**Offset Error**
Offset error is the deviation of the analog output from the ideal zero-scale output when all DAC registers are loaded with 0x0000. It is expressed in % FSR.

**Offset Error Drift or Offset TC**
Offset error drift, or offset TC, is a measure of the change in offset error with changes in temperature and is expressed in ppm FSR/°C.

**Gain Error**
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer function from the ideal, expressed in % FSR.

**Gain Temperature Coefficient (TC)**
Gain TC is a measure of the change in gain error with changes in temperature and is expressed in ppm FSR/°C.

**Full-Scale Error**
Full-scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output is full-scale − 1 LSB. Full-scale error is expressed in % FSR.

**Full-Scale Temperature Coefficient (TC)**
Full-scale TC is a measure of the change in full-scale error with changes in temperature and is expressed in ppm FSR/°C.

**Total Unadjusted Error (TUE)**
Total unadjusted error (TUE) is a measure of the output error that includes all the error measurements: INL error, offset error, gain error, temperature, and time. TUE is expressed in % FSR.

**DC Crosstalk**
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC, which is at midscale.

**Current Loop Compliance Voltage**
The current loop compliance voltage is the maximum voltage at the $I_{OUT\_x}$ pin for which the output current is equal to the programmed value.

**Voltage Reference Thermal Hysteresis**
Voltage reference thermal hysteresis is the difference in output voltage measured at +25°C compared to the output voltage measured at +25°C after cycling the temperature from +25°C to −40°C to +105°C and back to +25°C. The hysteresis is expressed in ppm.

**Power-On Glitch Energy**
Power-on glitch energy is the impulse injected into the analog output when the AD5737 is powered on. It is specified as the area of the glitch in nV-sec (see Figure 24).

**Power Supply Rejection Ratio (PSRR)**
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

**Reference Temperature Coefficient (TC)**
Reference TC is a measure of the change in the reference output voltage with changes in temperature. It is expressed in ppm/°C.

**Line Regulation**
Line regulation is the change in the reference output voltage due to a specified change in supply voltage. It is expressed in ppm/V.

**Load Regulation**
Load regulation is the change in the reference output voltage due to a specified change in load current. It is expressed in ppm/mA.

**DC-to-DC Converter Headroom**
DC-to-DC converter headroom is the difference between the voltage required at the current output and the voltage supplied by the dc-to-dc converter (see Figure 31).

**Output Efficiency**
Output efficiency is defined as the ratio of the power delivered to a channel's load and the power delivered to the channel's dc-to-dc input. The $V_{BOOST\_x}$ quiescent current is considered part of the dc-to-dc converter's losses.

$$\frac{I_{OUT}{}^2 \times R_{LOAD}}{AV_{CC} \times AI_{CC}}$$

**Efficiency at $V_{BOOST\_x}$**
The efficiency at $V_{BOOST\_x}$ is defined as the ratio of the power delivered to a channel's $V_{BOOST\_x}$ supply and the power delivered to the channel's dc-to-dc input. The $V_{BOOST\_x}$ quiescent current is considered part of the dc-to-dc converter's losses.

$$\frac{I_{OUT} \times V_{BOOST\_x}}{AV_{CC} \times AI_{CC}}$$

# THEORY OF OPERATION

The AD5737 is a quad, precision digital-to-current loop converter designed to meet the requirements of industrial process control applications. It provides a high precision, fully integrated, low cost, single-chip solution for generating current loop outputs. The current ranges available are 0 mA to 20 mA, 4 mA to 20 mA, and 0 mA to 24 mA. The output configuration is user-selectable via the DAC control register.

On-chip dynamic power control minimizes package power dissipation (see the Dynamic Power Control section).

## DAC ARCHITECTURE

The DAC core architecture of the AD5737 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 48. The four MSBs of the 12-bit data-word are decoded to drive 15 switches, E1 to E15. Each switch connects one of 15 matched resistors either to ground or to the reference buffer output. The remaining eight bits of the data-word drive Switch S0 to Switch S7 of an 8-bit voltage mode R-2R ladder network.

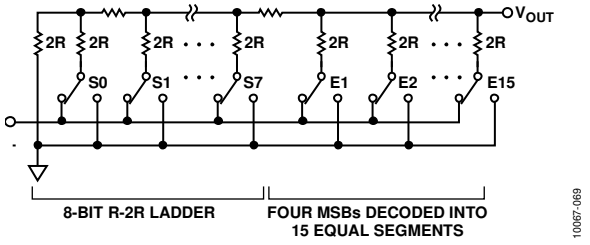



*Figure 48. DAC Ladder Structure*

The voltage output from the DAC core is converted to a current, which is then mirrored to the supply rail so that the application sees only a current source output (see Figure 49). The current outputs are supplied by $V_{BOOST\_x}$.

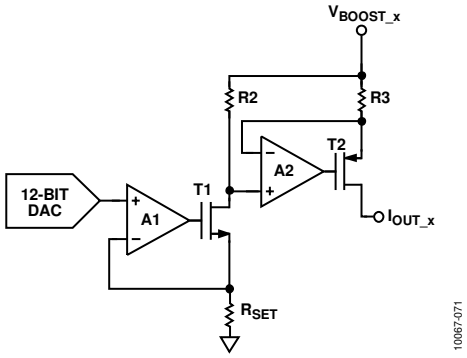



*Figure 49. Voltage-to-Current Conversion Circuitry*

### *Reference Buffers*

The AD5737 can operate with either an external or internal reference. The reference input requires a 5 V reference for specified performance. This input voltage is then buffered before it is applied to the DAC.

## POWER-ON STATE OF THE AD5737

When the AD5737 is first powered on, the $I_{OUT\_x}$ pins are in tristate mode. After a device power-on or a device reset, it is recommended that the user wait at least 100 µs before writing to the device to allow time for internal calibrations to take place.

## SERIAL INTERFACE

The AD5737 is controlled by a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP standards. Data coding is always straight binary.

### *Input Shift Register*

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of the serial clock input, SCLK. Data is clocked in on the falling edge of SCLK.

If packet error checking (PEC) is enabled, an additional eight bits must be written to the AD5737, creating a 32-bit serial interface (see the Packet Error Checking section).

The DAC outputs can be updated in one of two ways: individual DAC updating or simultaneous updating of all DACs.

#### Individual DAC Updating

To update an individual DAC, $\overline{\text{LDAC}}$ is held low while data is clocked into the DAC data register. The addressed DAC output is updated on the rising edge of $\overline{\text{SYNC}}$. See Table 3 and Figure 3 for timing information.

#### Simultaneous Updating of All DACs

To update all DACs simultaneously, $\overline{\text{LDAC}}$ is held high while data is clocked into the DAC data register. After $\overline{\text{LDAC}}$ is taken high, only the first write to the DAC data register of each channel is valid; subsequent writes to the DAC data register are ignored, although these subsequent writes are returned if a readback is initiated. All DAC outputs are updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ is taken high.

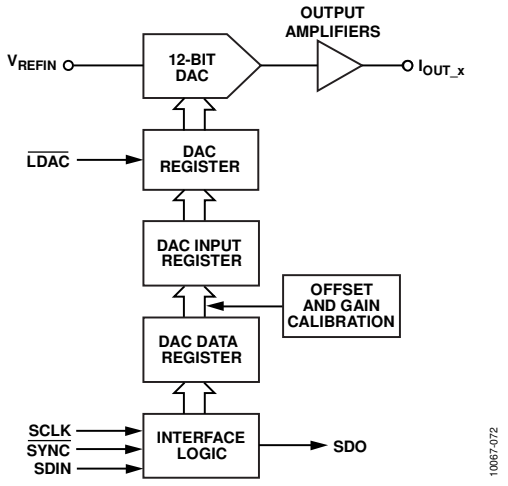



*Figure 50. Simplified Serial Interface of the Input Loading Circuitry for One DAC Channel*

## TRANSFER FUNCTION

For the 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA current output ranges, the output current is expressed by the following equations:

For the 0 mA to 20 mA range,

$$I_{OUT} = \left( \frac{20\,\text{mA}}{2^N} \right) \times D$$

For the 0 mA to 24 mA range,

$$I_{OUT} = \left( \frac{24\,\text{mA}}{2^N} \right) \times D$$

For the 4 mA to 20 mA range,

$$I_{OUT} = \left( \frac{16\,\text{mA}}{2^N} \right) \times D + 4\,\text{mA}$$

where:
$D$ is the decimal equivalent of the code loaded to the DAC.
$N$ is the bit resolution of the DAC.

# REGISTERS

Table 7, Table 8, and Table 9 provide an overview of the registers for the AD5737.

**Table 7. Data Registers for the AD5737**

| Register | Description |
|---|---|
| DAC Data Registers | The four DAC data registers (one register per DAC channel) are used to write a DAC code to each DAC channel. The DAC data bits are D15 to D4. |
| Gain Registers | The four gain registers (one register per DAC channel) are used to program the gain trim on a per-channel basis. The gain data bits are D15 to D4. |
| Offset Registers | The four offset registers (one register per DAC channel) are used to program the offset trim on a per-channel basis. The offset data bits are D15 to D4. |
| Clear Code Registers | The four clear code registers (one register per DAC channel) are used to program the clear code on a per-channel basis. The clear code data bits are D15 to D4. |

**Table 8. Control Registers for the AD5737**

| Register | Description |
|---|---|
| Main Control Register | The main control register is used to configure functions for the entire part. These functions include the following: enabling status readback during a write; enabling the output on all four DAC channels simultaneously; power-on of the dc-to-dc converter on all four DAC channels simultaneously; and enabling and configuring the watchdog timer. For more information, see the Main Control Register section. |
| DAC Control Registers | The four DAC control registers (one register per DAC channel) are used to configure the following functions on a per-channel basis: output range (for example, 4 mA to 20 mA); selection of the internal current sense resistor or an external current sense resistor; enabling/disabling the use of a clear code; enabling/disabling the internal circuitry (dc-to-dc converter, DAC, and internal amplifiers); power-on/power-off of the dc-to-dc converter; and enabling/disabling the output channel. |
| Software Register | The software register is used to perform a reset, to toggle the user bit in the status register, and, as part of the watchdog timer feature, to verify correct data communication operation. |
| DC-to-DC Control Register | The dc-to-dc control register is used to set the control parameters for the dc-to-dc converter: maximum output voltage, phase, and switching frequency. This register is also used to select the internal compensation resistor or an external compensation resistor for the dc-to-dc converter. |
| Slew Rate Control Registers | The four slew rate control registers (one register per DAC channel) are used to program the slew rate of the DAC output. |

**Table 9. Readback Register for the AD5737**

| Register | Description |
|---|---|
| Status Register | The status register contains any fault information, as well as a user toggle bit. |