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Quad Channel, 16-Bit, Serial Input, 4 mA to 20 mA and Voltage Output DAC, Dynamic Power Control

Data Sheet

AD5755

FEATURES

- **16-bit resolution and monotonicity**
- **Dynamic power control for thermal management**
- **Current and voltage output pins connectable to a single terminal**
- **Current output ranges: 0 mA to 20 mA, 4 mA to 20 mA, or 0 mA to 24 mA**
  - **±0.05% total unadjusted error (TUE) maximum**
- **Voltage output ranges (with 20% overrange): 0 V to 5 V, 0 V to 10 V, ±5 V, and ±10 V**
  - **±0.04% total unadjusted error (TUE) maximum**
- **User programmable offset and gain**
- **On-chip diagnostics**
- **On-chip reference (±10 ppm/°C maximum)**
- **−40°C to +105°C temperature range**

APPLICATIONS

- **Process control**
- **Actuator control**
- **PLCs**

GENERAL DESCRIPTION

The AD5755 is a quad, voltage and current output DAC that operates with a power supply range from −26.4 V to +33 V.

On-chip dynamic power control minimizes package power dissipation in current mode. This is achieved by regulating the voltage on the output driver from 7.4 V to 29.5 V using a dc-to-dc boost converter optimized for minimum on chip power dissipation.

The part uses a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with standard SPI, QSPI™, MICROWIRE™, DSP, and microcontroller interface standards. The interface also features optional CRC-8 packet error checking, as well as a watchdog timer that monitors activity on the interface.

PRODUCT HIGHLIGHTS

1. Dynamic power control for thermal management.
2. 16-bit performance.
3. Multichannel.

COMPANION PRODUCTS

Product Family: AD5755-1, AD5757
External References: ADR445, ADR02
Digital Isolators: ADuM1410, ADuM1411
Power: ADP2302, ADP2303
Additional companion products on the AD5755 product page

FUNCTIONAL BLOCK DIAGRAM

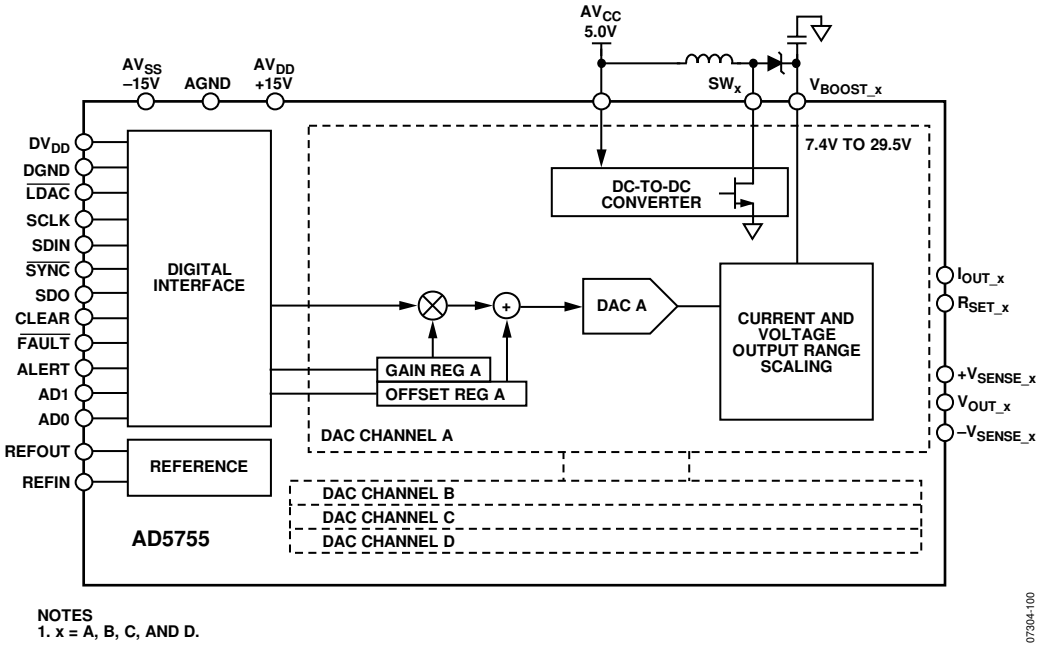

Figure 1.

Rev. D **Document Feedback**

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AD5755* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD5755 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1289: Using the AD5755 and Similar Dynamic Power Control DACs in Applications Without Dynamic Power Control

Data Sheet

- AD5755: Quad Channel, 16-Bit, Serial Input, 4 mA to 20 mA and Voltage Output DAC, Dynamic Power Control Data Sheet

User Guides

- UG-244: Evaluation Board for a Quad Channel, 16-Bit, Serial Input, 4 mA to 20 mA, Voltage Output DAC with Dynamic Power Control and HART Connectivity

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD5755 - Microcontroller No-OS Driver
- AD5755 IIO Multi-Channel DAC Linux Driver
- AD5755 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design
- BeMicro FPGA Project for AD5755 with Nios driver

TOOLS AND SIMULATIONS

- AD5755/AD5755-1 IBIS Model

REFERENCE DESIGNS

- CN0198

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

Technical Articles

- MS-2646: Dynamic Power Control DPC Minimizes Power Loss, Maximizes Temperature Range

DESIGN RESOURCES

- AD5755 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD5755 EngineerZone Discussions.

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TABLE OF CONTENTS

REVISION HISTORY

5/14—Rev. C to Rev. D

Changes to Thermal Hysteresis Parameter, Table 1 7
Changes to t_6 Parameter, t_9 Parameter, and t_{19} Parameter, Table 3 9
Changes to Figure 4 10
Added Figure 5; Renumbered Sequentially, Change to Figure 6 11
Changes to Figure 54, Figure 55, Figure 56, and Figure 57 24
Change to Figure 65, Figure 68, and Figure 69 26
Changes to Voltage Reference Thermal Hysteresis Section 27
Changes to Table 12 and Table 14 34
Changes to Readback Operation Section, Added Table 27, Table 28, and Table 29; Renumbered Sequentially 38
Changes to Status Readback During a Write Section 41
Changes to Packet Error Checking Section 42
Changes to Table 35 44
Changes to Ordering Guide 50

1/13—Rev. B to Rev. C

Changes to Figure 2 4
Changed Thermal Impedance from 20°C/W to 28°C/W 12
Changes to Pin 6 Description, Table 5 13
Changes to Figure 25 18
Changes to Bit DUT_AD1, DUT_AD0 Description, Table 9 33
Changes to Packet Error Checking Section 41
Changes to Figure 79 43
Changes to Figure 84 47
Updated Outline Dimensions 49
Changes to Ordering Guide 49

5/12—Rev. A to Rev. B

Changes to Figure 2 4
Changes to Figure 21 18
Changes to Figure 43 22
Changes to Internal Reference Section 41

11/11—Rev. 0 to Rev. A

Changes to Figure 2 4
Changes to Table 1 5
Added Timing Diagram heading and changes to Figure 5 10
Changes to Figure 6 11
Changes to Table 5 13
Changes to Figure 13 16
Changes to Figure 21 18
Changes to Figure 37 20
Changes to Figure 44 22
Changes to Figure 56 and Figure 58 24
Changes to Figure 71 29
Changes to Power-On State of AD5575 Section 29
Changes to Table 17 35
Changes to Readback Operation Section and changes to Table 26 38
Changes to Voltage Output Short-Circuit Protection Section 40
Changes to Figure 78 41
Changes to Figure 81 through Figure 84 Captions 44
Changes to Transient Voltage Protection Section and changes to Figure 85 47
Changes to Galvanically Isolated Interface Section 48

5/11—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

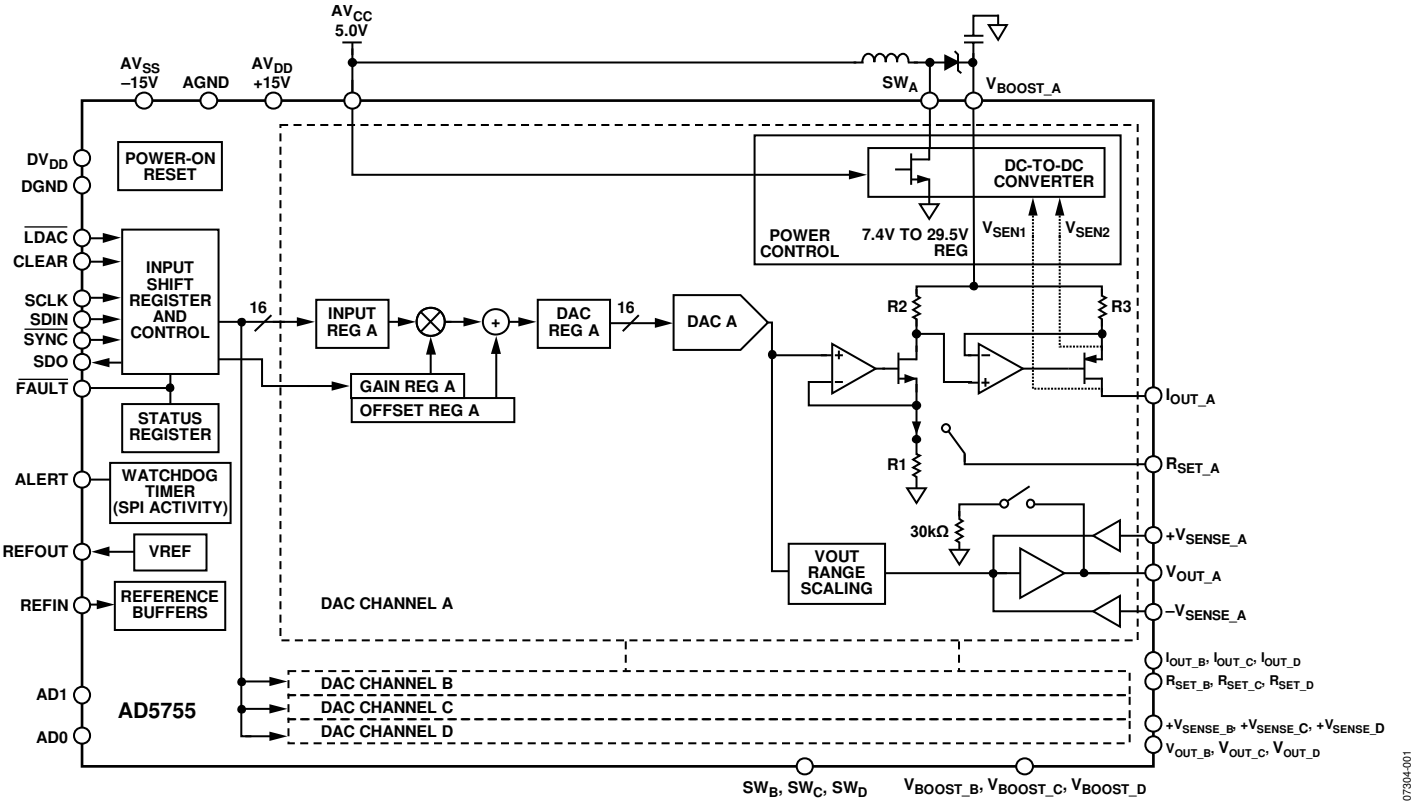


Figure 2.

SPECIFICATIONS

AV_{DD} = V_{BOOST_x} = 15 V; AV_{SS} = −15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; voltage outputs: R_L = 1 kΩ, C_L = 220 pF; current outputs: R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE OUTPUT					
Output Voltage Ranges	0		5	V	
	0		10	V	
	−5		+5	V	
	−10		+10	V	
	0		6	V	
	0		12	V	
	−6		+6	V	
	−12		+12	V	
Resolution	16			Bits	
ACCURACY					AV_{SS} = −15 V, loaded and unloaded
Total Unadjusted Error (TUE)					
B Version	−0.04		+0.04	% FSR	
	−0.03	±0.0032	+0.03	% FSR	T_A = 25°C
A Version	−0.25		+0.25	% FSR	
	−0.075	±0.02	+0.075	% FSR	T_A = 25°C
TUE Long-Term Stability		35		ppm FSR	Drift after 1000 hours, T_J = 150°C
Relative Accuracy (INL)	−0.006	±0.0012	+0.006	% FSR	0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V ranges
	−0.008	±0.0012	+0.008	% FSR	On overranges
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.03	±0.002	+0.03	% FSR	
Zero-Scale TC[2]		±2		ppm FSR/°C	
Bipolar Zero Error	−0.03	±0.002	+0.03	% FSR	
Bipolar Zero TC[2]		±1		ppm FSR/°C	
Offset Error	−0.03	±0.002	+0.03	% FSR	
Offset TC[2]		±2		ppm FSR/°C	
Gain Error	−0.03	±0.004	+0.03	% FSR	
Gain TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.03	±0.002	+0.03	% FSR	
Full-Scale TC[2]		±2		ppm FSR/°C	
OUTPUT CHARACTERISTICS[2]					
Headroom		1	2.2	V	With respect to V_{BOOST} supply
Footroom		1	1.4	V	With respect to the AV_{SS} supply
Output Voltage Drift vs. Time		20		ppm FSR	Drift after 1000 hours, ¾ scale output, T_J = 150°C, AV_{SS} = −15 V
Short-Circuit Current	12/6	16/8		mA	Programmable by user, defaults to 16 mA typical level
Load	1			kΩ	For specified performance
Capacitive Load Stability			10	nF	
			2	µF	External compensation capacitor of 220 pF connected
DC Output Impedance		0.06		Ω	
DC PSRR		50		µV/V	
DC Crosstalk		24		µV	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT OUTPUT					
Output Current Ranges	0		24	mA	
	0		20	mA	
	4		20	mA	
Resolution	16			Bits	
ACCURACY (EXTERNAL R_{SET})					Assumes ideal resistor; see the External Current Setting Resistor section for more information.
Total Unadjusted Error (TUE)					
B Version	−0.05	±0.009	+0.05	% FSR	
A Version	−0.2	±0.04	+0.2	% FSR	
TUE Long-Term Stability		100		ppm FSR	Drift after 1000 hours, T_J = 150°C
Relative Accuracy (INL)	−0.006		+0.006	% FSR	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.05	±0.005	+0.05	% FSR	
Offset Error Drift[2]		±4		ppm FSR/°C	
Gain Error	−0.05	±0.004	+0.05	% FSR	
Gain TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.05	±0.008	+0.05	% FSR	
Full-Scale TC[2]		±5		ppm FSR/°C	
DC Crosstalk		0.0005		% FSR	External R_{SET}
ACCURACY (INTERNAL R_{SET})					
Total Unadjusted Error (TUE)[3, 4]					
B Version	−0.14		+0.14	% FSR	
	−0.11	±0.009	+0.11	% FSR	T_A = 25°C
A Version	−0.35		+0.35	% FSR	
	−0.2	+0.04	+0.2	% FSR	T_A = 25°C
TUE Long-Term Stability		180		ppm FSR	Drift after 1000 hours, T_J = 150°C
Relative Accuracy (INL)	−0.006		+0.006	% FSR	
Relative Accuracy (INL)	−0.004		+0.004	% FSR	T_A = 25°C
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error[3, 4]	−0.05		+0.05	% FSR	
	−0.04	±0.007	+0.04	% FSR	T_A = 25°C
Offset Error Drift[2]		±6		ppm FSR/°C	
Gain Error	−0.12		+0.12	% FSR	
	−0.06	±0.002	+0.06	% FSR	T_A = 25°C
Gain TC[2]		±9		ppm FSR/°C	
Full-Scale Error[3, 4]	−0.14		+0.14	% FSR	
	−0.1	±0.007	+0.1	% FSR	T_A = 25°C
Full-Scale TC[2]		±14		ppm FSR/°C	
DC Crosstalk[4]		−0.011		% FSR	Internal R_{SET}
OUTPUT CHARACTERISTICS[2]					
Current Loop Compliance Voltage		V_{BOOST_x} − 2.4	V_{BOOST_x} − 2.7	V	
Output Current Drift vs. Time					Drift after 1000 hours, ¾ scale output, T_J = 150°C
		90		ppm FSR	External R_{SET}
		140		ppm FSR	Internal R_{SET}

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Resistive Load			1000	Ω	The dc-to-dc converter has been characterized with a maximum load of 1 kΩ, chosen such that compliance is not exceeded; see Figure 53 and DC-DC MaxV bits in Table 25
Output Impedance		100		MΩ	
DC PSRR		0.02	1	µA/V	
REFERENCE INPUT/OUTPUT					
Reference Input[2]					
Reference Input Voltage	4.95	5	5.05	V	For specified performance
DC Input Impedance	45	150		MΩ	
Reference Output					
Output Voltage	4.995	5	5.005	V	T_A = 25°C
Reference TC[2]	−10	±5	+10	ppm/°C	
Output Noise (0.1 Hz to 10 Hz)[2]		7		µV p-p	
Noise Spectral Density[2]		100		nV/√Hz	At 10 kHz
Output Voltage Drift vs. Time[2]		180		ppm	Drift after 1000 hours, T_J = 150°C
Capacitive Load[2]		1000		nF	
Load Current		9		mA	See Figure 64
Short-Circuit Current		10		mA	
Line Regulation[2]		3		ppm/V	See Figure 65
Load Regulation[2]		95		ppm/mA	See Figure 64
Thermal Hysteresis[2]		200		ppm	
DC-TO-DC					
Switch					
Switch On Resistance		0.425		Ω	
Switch Leakage Current		10		nA	
Peak Current Limit		0.8		A	
Oscillator					
Oscillator Frequency	11.5	13	14.5	MHz	This oscillator is divided down to give the dc-to-dc converter switching frequency
Maximum Duty Cycle		89.6		%	At 410 kHz dc-to-dc switching frequency
DIGITAL INPUTS[2]					JEDEC compliant
V_{IH}, Input High Voltage	2			V	
V_{IL}, Input Low Voltage			0.8	V	
Input Current	−1		+1	µA	Per pin
Pin Capacitance		2.6		pF	Per pin
DIGITAL OUTPUTS[2]					
SDO, ALERT					
V_{OL}, Output Low Voltage			0.4	V	Sinking 200 µA
V_{OH}, Output High Voltage	DVDD − 0.5			V	Sourcing 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance		2.5		pF	
$\overline{FAULT}$					
V_{OL}, Output Low Voltage			0.4	V	10 kΩ pull-up resistor to DV_{DD}
V_{OL}, Output Low Voltage		0.6		V	At 2.5 mA
V_{OH}, Output High Voltage	3.6			V	10 kΩ pull-up resistor to DV_{DD}
POWER REQUIREMENTS					
AV_{DD}	9		33	V	
AV_{SS}	−26.4		−10.8	V	
DV_{DD}	2.7		5.5	V	
AV_{CC}	4.5		5.5	V	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
AI_{DD}		8.6	10.5	mA	Voltage output mode on all channels, output unloaded, over supplies
		7	7.5	mA	Current output mode on all channels,
AI_{SS}	−11	−8.8		mA	Voltage output mode on all channels, output unloaded, over supplies
	−1.7			mA	Current output mode on all channels
DI_{CC}		9.2	11	mA	$V_{IH} = DV_{DD}$, V_{IL} = DGND, internal oscillator running, over supplies
AI_{CC}			1	mA	Output unloaded, over supplies
I_{BOOST}[5]			2.7	mA	Per channel, voltage output mode, output unloaded, over supplies
			1	mA	Per channel, current output mode
Power Dissipation		173		mW	AV_{DD} = 15 V, AV_{SS} = −15 V, dc-to-dc converter enable, current output mode, outputs disabled

[1] Temperature range: −40°C to +105°C; typical at +25°C.
[2] Guaranteed by design and characterization; not production tested.
[3] For current outputs with internal R_{SET}, the offset, full-scale, and TUE measurements exclude dc crosstalk. The measurements are made with all four channels enabled loaded with the same code.
[4] See the Current Output Mode with Internal R_{SET} section for more explanation of the dc crosstalk.
[5] Efficiency plots in Figure 55, Figure 56, Figure 57, and Figure 58 include the I_{BOOST} quiescent current.

AC PERFORMANCE CHARACTERISTICS

$AV_{DD} = V_{BOOST\_x}$ = 15 V; AV_{SS} = −15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; voltage outputs: R_L = 2 kΩ, C_L = 220 pF; current outputs: R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Voltage Output					
Output Voltage Settling Time		11		µs	5 V step to ±0.03% FSR, 0 V to 5 V range
			18	µs	10 V step to ±0.03% FSR, 0 V to 10 V range
			13	µs	100 mV step to 1 LSB (16-bit LSB), 0 V to 10 V range
Slew Rate		1.9		V/µs	0 V to 10 V range
Power-On Glitch Energy		150		nV-sec	
Digital-to-Analog Glitch Energy		6		nV-sec	
Glitch Impulse Peak Amplitude		25		mV	
Digital Feedthrough		1		nV-sec	
DAC to DAC Crosstalk		2		nV-sec	0 V to 10 V range
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.15		LSB p-p	16-bit LSB, 0 V to 10 V range
Output Noise Spectral Density		150		nV/√Hz	Measured at 10 kHz, midscale output, 0 V to 10 V range
AC PSRR		83		dB	200 mV 50 Hz/60 Hz sine wave superimposed on power supply voltage
Current Output					
Output Current Settling Time		15		µs	To 0.1% FSR (0 mA to 24 mA)
		See test conditions/ comments		ms	See Figure 49, Figure 50, and Figure 51
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.15		LSB p-p	16-bit LSB, 0 mA to 24 mA range
Output Noise Spectral Density		0.5		nA/√Hz	Measured at 10 kHz, midscale output, 0 mA to 24 mA range

[1] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

AV_{DD} = V_{BOOST_x} = 15 V; AV_{SS} = −15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; voltage outputs: R_L = 1 kΩ, C_L = 220 pF; current outputs: R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	13	ns min	24th/32nd SCLK falling edge to $\overline{SYNC}$ rising edge (see Figure 78)
t_6	198	ns min	$\overline{SYNC}$ high time after a configuration write
	5	µs min	$\overline{SYNC}$ high time after a DAC update write
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	20	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (applies to any channel with digital slew rate control enabled; single DAC updated)
	5	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (single DAC updated)
t_{10}	10	ns min	$\overline{LDAC}$ pulse width low
t_{11}	500	ns max	$\overline{LDAC}$ falling edge to DAC output response time
t_{12}	See the AC Performance Characteristics section	µs max	DAC output settling time
t_{13}	10	ns min	CLEAR high time
t_{14}	5	µs max	CLEAR activation time
t_{15}	40	ns max	SCLK rising edge to SDO valid
t_{16}	5	µs min	$\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC}$ = 0) (single DAC updated)
t_{17}	500	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge
t_{18}	800	ns min	$\overline{RESET}$ pulse width
t_{19}	20	µs min	$\overline{SYNC}$ high to next $\overline{SYNC}$ low (digital slew rate control enabled) (single DAC updated)
	5	µs min	$\overline{SYNC}$ high to next $\overline{SYNC}$ low (digital slew rate control disabled) (single DAC updated)

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with t_{RISE} = t_{FALL} = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.2 V.
[3] See Figure 3, Figure 4, Figure 6, and Figure 7.

Timing Diagrams

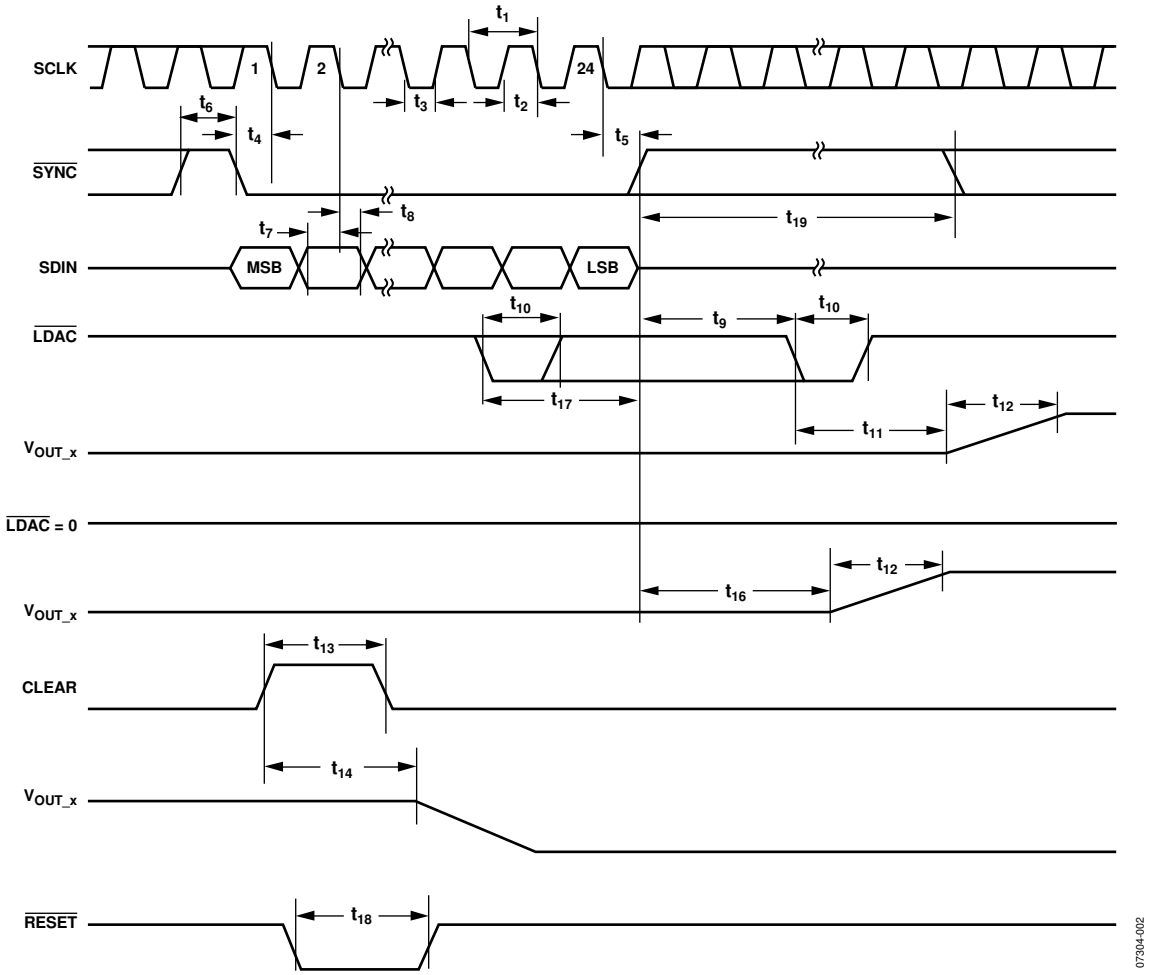
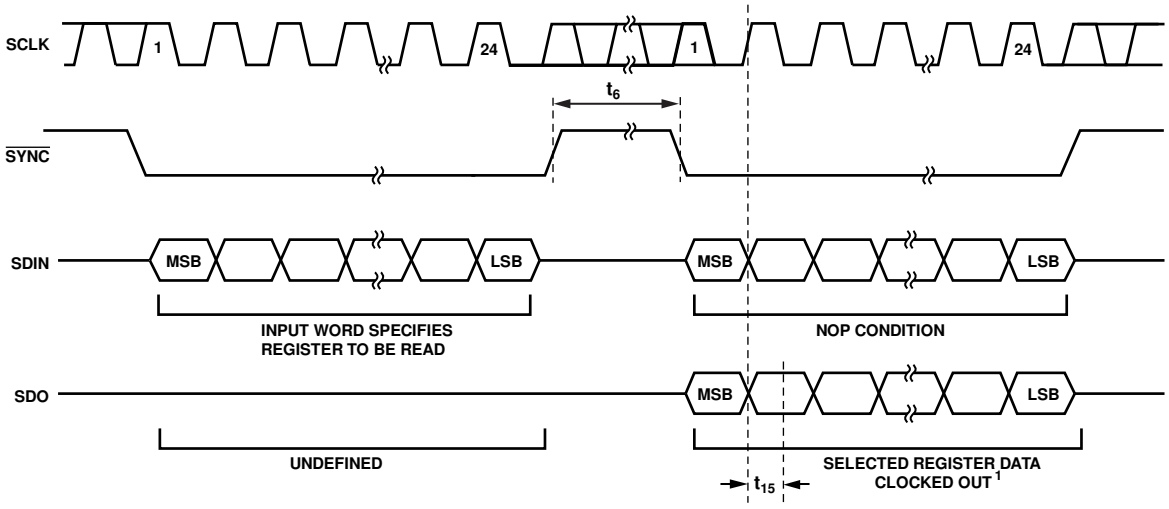
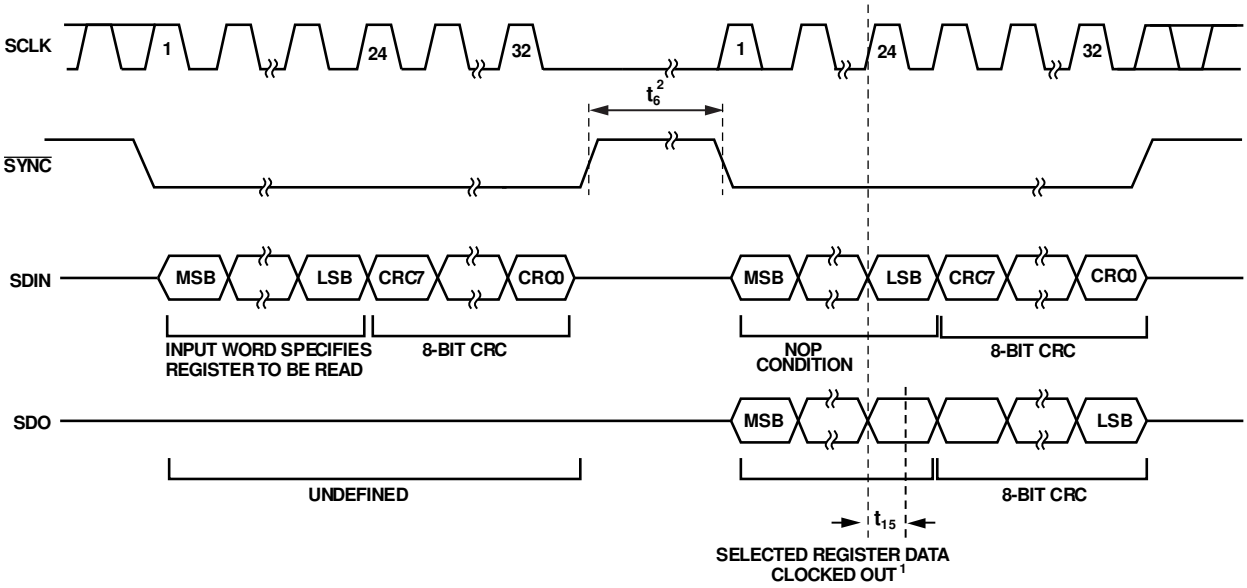


Figure 3. Serial Interface Timing Diagram



[1] IF FIRST SCLK IS NEGATIVE EDGE WITHIN $\overline{\text{SYNC}}$ FRAME OF NOP CONDITION, 7 DONT CARE BITS + 16 DATA BITS CLOCKED OUT (TOTAL 23 BITS)
IF FIRST SCLK IS POSITIVE EDGE WITHIN $\overline{\text{SYNC}}$ FRAME OF NOP CONDITION, 8 DONT CARE BITS + 16 DATA BITS CLOCKED OUT (TOTAL 24 BITS)
SEE THE READBACK OPERATION SECTION FOR FURTHER INFORMATION

Figure 4. Readback Timing Diagram (Packet Error Checking Disabled)

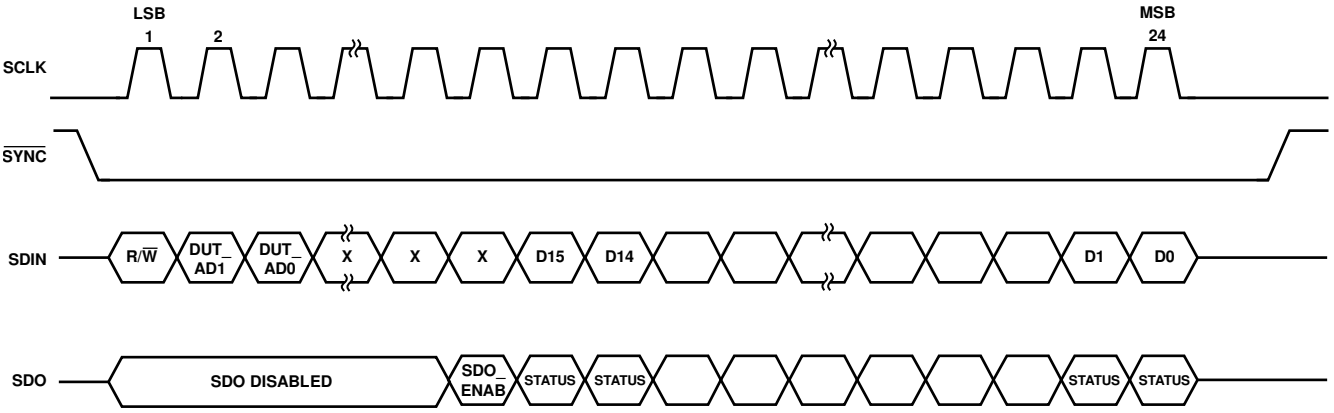


1 IF FIRST SCLK IS NEGATIVE EDGE WITHIN $\overline{SYNC}$ FRAME OF NOP CONDITION, 7 DONT CARE BITS + 16 DATA BITS CLOCKED OUT + 8 CRC BITS (TOTAL 31 BITS)
IF FIRST SCLK IS POSITIVE EDGE WITHIN $\overline{SYNC}$ FRAME OF NOP CONDITION, 8 DONT CARE BITS + 16 DATA BITS CLOCKED OUT + 8 CRC BITS (TOTAL 32 BITS)
2 AVOID SCLK ACTIVITY DURING t_6 AS IT MAY RESULT IN A PEC ERROR ON READBACK

SEE THE READBACK OPERATION AND PACKET ERROR CHECKING SECTIONS FOR FURTHER INFORMATION

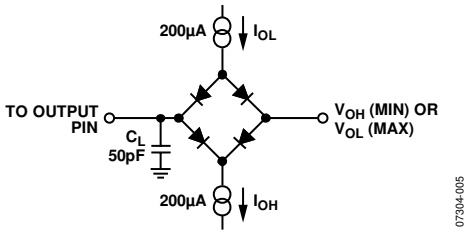
07304-305

Figure 5. Readback Timing Diagram (Packet Error Checking Enabled)



07304-104

Figure 6. Status Readback During Write



07304-005

Figure 7. Load Circuit for SDO Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4.

Parameter	Rating
AV_{DD}, V_{BOOST_x} to AGND, DGND	−0.3 V to +33 V
AV_{SS} to AGND, DGND	+0.3 V to −28 V
AV_{DD} to AV_{SS}	−0.3 V to +60 V
AV_{CC} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{DD} + 0.3 V or +7 V (whichever is less)
Digital Outputs to DGND	−0.3 V to DV_{DD} + 0.3 V or +7 V (whichever is less)
REFIN, REFOUT to AGND	−0.3 V to AV_{DD} + 0.3 V or +7 V (whichever is less)
V_{OUT_x} to AGND	AV_{SS} to V_{BOOST_x} or 33 V if using the dc-to-dc circuitry
$+V_{SENSE\_x}$, $-V_{SENSE\_x}$ to AGND	AV_{SS} to V_{BOOST_x} or 33 V if using the dc-to-dc circuitry
I_{OUT_x} to AGND	AV_{SS} to V_{BOOST_x} or 33 V if using the dc-to-dc circuitry
SW_x to AGND	−0.3 to +33 V
AGND, $GNDSW_x$ to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A)	
Industrial[1]	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
64-Lead LFCSP	
θ_{JA} Thermal Impedance[2]	28°C/W
Power Dissipation	(T_J max − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

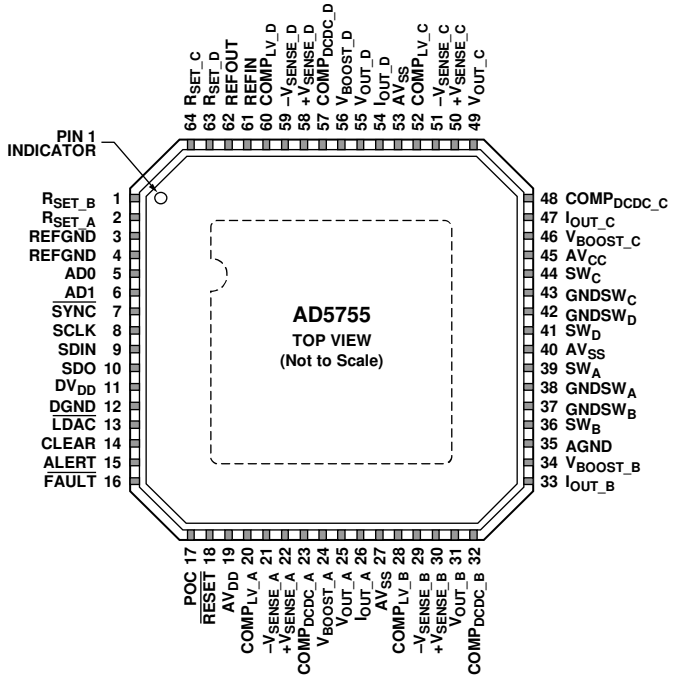
[1] Power dissipated on chip must be derated to keep the junction temperature below 125°C.
[2] Based on a JEDEC 4-layer test board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THIS EXPOSED PADDLE SHOULD BE CONNECTED TO THE POTENTIALOF THE AV_{SS} PIN, OR, ALTERNATIVELY, IT CAN BE LEFT ELECTRICALLY UNCONNECTED. IT IS RECOMMENDED THAT THE PADDLE BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE.

07304-006

Figure 8. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{SET_B}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_B} temperature drift performance. See the Device Features section.
2	R_{SET_A}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_A} temperature drift performance. See the Device Features section.
3	REFGND	Ground Reference Point for Internal Reference.
4	REFGND	Ground Reference Point for Internal Reference.
5	AD0	Address Decode for the Device Under Test (DUT) on the Board.
6	AD1	Address Decode for the DUT on the Board. It is not recommended to tie both AD1 and AD0 low when using PEC, see the Packet Error Checking section.
7	$\overline{SYNC}$	Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{SYNC}$ is low, data is transferred in on the falling edge of SCLK.
8	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This operates at clock speeds of up to 30 MHz.
9	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
10	SDO	Serial Data Output. Used to clock data from the serial register in readback mode. See Figure 4 and Figure 6.
11	DV_{DD}	Digital Supply. The voltage range is from 2.7 V to 5.5 V.
12	DGND	Digital Ground.
13	$\overline{LDAC}$	Load DAC, Active Low Input. This is used to update the DAC register and consequently the DAC outputs. When tied permanently low, the addressed DAC data register is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle, the DAC input register is updated, but the DAC output update only takes place at the falling edge of $\overline{LDAC}$ (see Figure 3). Using this mode, all analog outputs can be updated simultaneously. The $\overline{LDAC}$ pin must not be left unconnected.
14	CLEAR	Active High, Edge Sensitive Input. Asserting this pin sets the output current and voltage to the preprogrammed clear code bit setting. Only channels enabled to be cleared are cleared. See the Device Features section for more information. When CLEAR is active, the DAC output register cannot be written to.

Pin No.	Mnemonic	Description
15	ALERT	Active High Output. This pin is asserted when there has been no SPI activity on the interface pins for a predetermined time. See the Device Features section for more information.
16	$\overline{\text{FAULT}}$	Active Low Output. This pin is asserted low when an open circuit in current mode is detected, a short circuit in voltage mode is detected, a PEC error is detected, or an overtemperature is detected (see the Device Features section). Open-drain output.
17	POC	Power-On Condition. This pin determines the power-on condition and is read during power-on or, alternatively, after a device reset. If POC = 0, the device is powered up with the voltage and current channels in tristate mode. If POC = 1, the device is powered up with a 30 kΩ pull-down resistor to ground on the voltage output channel, and the current channel is in tristate mode.
18	$\overline{\text{RESET}}$	Hardware Reset, Active Low Input.
19	AV_{DD}	Positive Analog Supply. The voltage range is from 9 V to 33 V.
20	$COMP_{LV\_A}$	Optional Compensation Capacitor Connection for V_{OUT_A} Output Buffer. Connecting a 220 pF capacitor between this pin and the V_{OUT_A} pin allows the voltage output to drive up to 2 µF. Note that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
21	$-V_{SENSE\_A}$	Sense Connection for the Negative Voltage Output Load Connection for V_{OUT_A}. This pin must stay within ±3.0 V of AGND for specified operation.
22	$+V_{SENSE\_A}$	Sense Connection for the Positive Voltage Output Load Connection for V_{OUT_A}.
23	$COMP_{DCDC\_A}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel A dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin (see the DC-to-DC Converter Compensation Capacitors and the AI_{CC} Supply Requirements—Slewing sections in the Device Features section for more information).
24	V_{BOOST_A}	Supply for Channel A Current Output Stage (see Figure 73). This is also the supply for the V_{OUT_x} stage, which is regulated to 15 V by the dc-to-dc converter. To use the dc-to-dc feature of the device, connect as shown in Figure 79.
25	V_{OUT_A}	Buffered Analog Output Voltage for DAC Channel A.
26	I_{OUT_A}	Current Output Pin for DAC Channel A.
27	AV_{SS}	Negative Analog Supply Pin. Voltage range is from −10.8 V to −26.4 V.
28	$COMP_{LV\_B}$	Optional Compensation Capacitor Connection for V_{OUT_B} Output Buffer. Connecting a 220 pF capacitor between this pin and the V_{OUT_B} pin allows the voltage output to drive up to 2 µF. Note that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
29	$-V_{SENSE\_B}$	Sense Connection for the Negative Voltage Output Load Connection for V_{OUT_B}. This pin must stay within ±3.0 V of AGND for specified operation.
30	$+V_{SENSE\_B}$	Sense Connection for the Positive Voltage Output Load Connection for V_{OUT_B}.
31	V_{OUT_B}	Buffered Analog Output Voltage for DAC Channel B.
32	$COMP_{DCDC\_B}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel B dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin (see the DC-to-DC Converter Compensation Capacitors and the AI_{CC} Supply Requirements—Slewing sections in the Device Features section for more information).
33	I_{OUT_B}	Current Output Pin for DAC Channel B.
34	V_{BOOST_B}	Supply for Channel B Current Output Stage (see Figure 73). This is also the supply for the V_{OUT_x} stage, which is regulated to 15 V by the dc-to-dc converter. To use the dc-to-dc feature of the device, connect as shown in Figure 79.
35	AGND	Ground Reference Point for Analog Circuitry. This must be connected to 0 V.
36	SW_B	Switching Output for Channel B DC-to-DC Circuitry. To use the dc-to-dc feature of the device, connect as shown in Figure 79.
37	$GNDSW_B$	Ground Connection for DC-to-DC Switching Circuit. This pin should always be connected to ground.
38	$GNDSW_A$	Ground Connection for DC-to-DC Switching Circuit. This pin should always be connected to ground.
39	SW_A	Switching Output for Channel A DC-to-DC Circuitry. To use the dc-to-dc feature of the device, connect as shown in Figure 79.
40	AV_{SS}	Negative Analog Supply Pin. The voltage range is from −10.8 V to −26.4 V.
41	SW_D	Switching Output for Channel D DC-to-DC Circuitry. To use the dc-to-dc feature of the device, connect as shown in Figure 79.
42	$GNDSW_D$	Ground Connections for DC-to-DC Switching Circuit. This pin should always be connected to ground.
43	$GNDSW_C$	Ground Connections for DC-to-DC Switching Circuit. This pin should always be connected to ground.

Pin No.	Mnemonic	Description
44	SW_C	Switching Output for Channel C DC-to-DC Circuitry. To use the dc-to-dc feature of the device, connect as shown in Figure 79.
45	AV_{CC}	Supply for DC-to-DC Circuitry.
46	V_{BOOST_C}	Supply for Channel C Current Output Stage (see Figure 73). This is also the supply for the V_{OUT_x} stage, which is regulated to 15 V by the dc-to-dc converter. To use the dc-to-dc feature of the device, connect as shown in Figure 79.
47	I_{OUT_C}	Current Output Pin for DAC Channel C.
48	$COMP_{DCDC\_C}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel C dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin (see the DC-to-DC Converter Compensation Capacitors and AI_{CC} Supply Requirements—Slewing sections in the Device Features section for more information).
49	V_{OUT_C}	Buffered Analog Output Voltage for DAC Channel C.
50	$+V_{SENSE\_C}$	Sense Connection for the Positive Voltage Output Load Connection for V_{OUT_C}.
51	$-V_{SENSE\_C}$	Sense Connection for the Negative Voltage Output Load Connection for V_{OUT_C}. This pin must stay within ±3.0 V of AGND for specified operation.
52	$COMP_{LV\_C}$	Optional Compensation Capacitor Connection for V_{OUT_C} Output Buffer. Connecting a 220 pF capacitor between this pin and the V_{OUT_C} pin allows the voltage output to drive up to 2 µF. Note that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
53	AV_{SS}	Negative Analog Supply Pin.
54	I_{OUT_D}	Current Output Pin for DAC Channel D.
55	V_{OUT_D}	Buffered Analog Output Voltage for DAC Channel D.
56	V_{BOOST_D}	Supply for Channel D Current Output Stage (see Figure 73). This is also the supply for the V_{OUT_x} stage, which is regulated to 15 V by the dc-to-dc converter. To use the dc-to-dc feature of the device, connect as shown in Figure 79.
57	$COMP_{DCDC\_D}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of Channel D dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin (see the DC-to-DC Converter Compensation Capacitors and AI_{CC} Supply Requirements—Slewing sections in the Device Features section for more information).
58	$+V_{SENSE\_D}$	Sense Connection for the Positive Voltage Output Load Connection for V_{OUT_D}.
59	$-V_{SENSE\_D}$	Sense Connection for the Negative Voltage Output Load Connection for V_{OUT_D}. This pin must stay within ±3.0 V of AGND for specified operation.
60	$COMP_{LV\_D}$	Optional Compensation Capacitor Connection for V_{OUT_D} Output Buffer. Connecting a 220 pF capacitor between this pin and the V_{OUT_D} pin allows the voltage output to drive up to 2 µF. Note that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
61	REFIN	External Reference Voltage Input.
62	REFOUT	Internal Reference Voltage Output. It is recommended to place a 0.1 µF capacitor between REFOUT and REFGND.
63	R_{SET_D}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_D} temperature drift performance. See the Device Features section.
64	R_{SET_C}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_C} temperature drift performance. See the Device Features section.
	EPAD	Exposed Pad. This exposed pad should be connected to the potential of the AV_{SS} pin, or, alternatively, it can be left electrically unconnected. It is recommended that the pad be thermally connected to a copper plane for enhanced thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE OUTPUTS

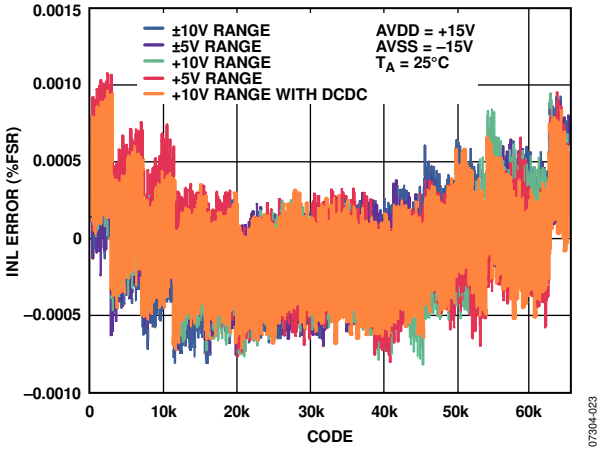


Figure 9. Integral Nonlinearity Error vs. DAC Code

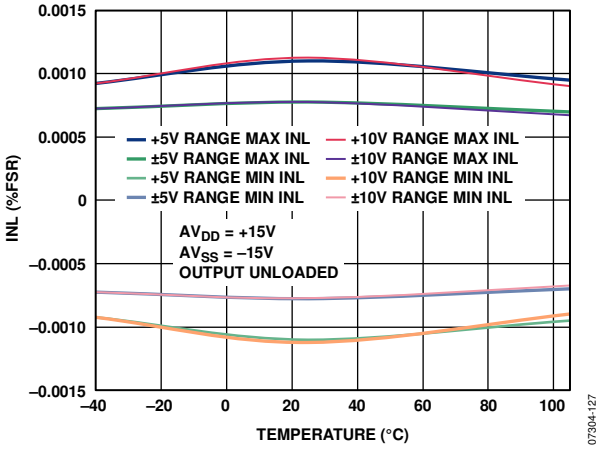


Figure 12. Integral Nonlinearity Error vs. Temperature

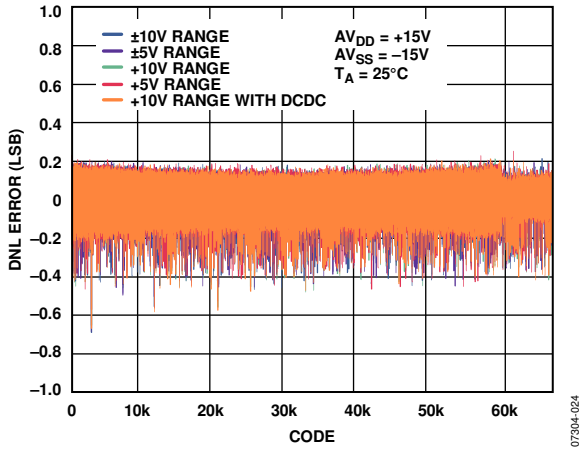


Figure 10. Differential Nonlinearity Error vs. DAC Code

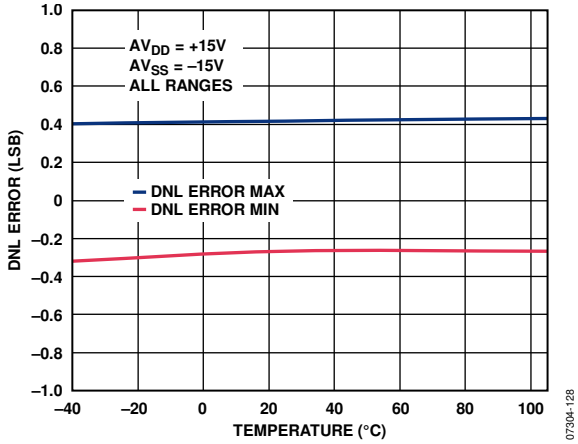


Figure 13. Differential Nonlinearity Error vs. Temperature

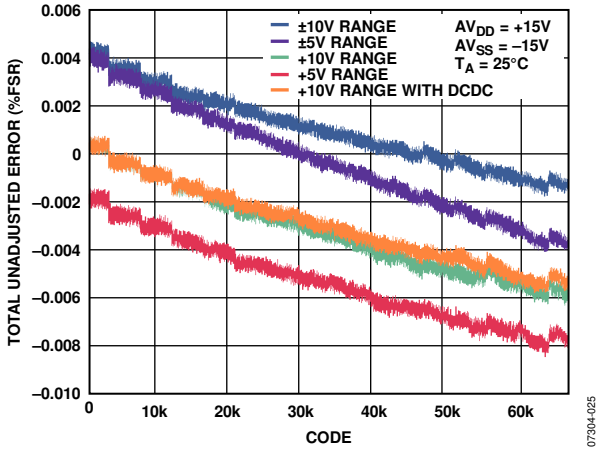


Figure 11. Total Unadjusted Error vs. DAC Code

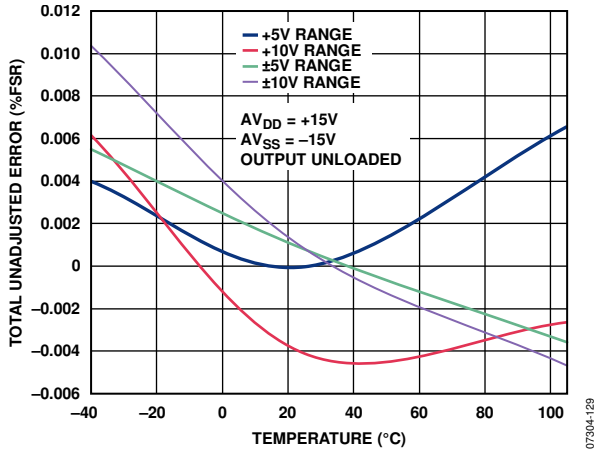


Figure 14. Total Unadjusted Error vs. Temperature

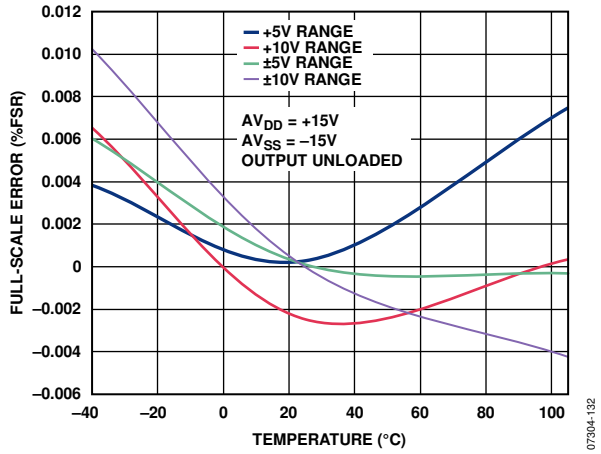


Figure 15. Full-Scale Error vs. Temperature

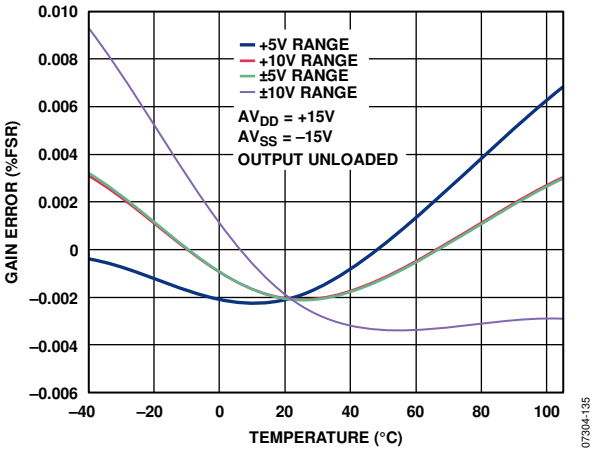


Figure 18. Gain Error vs. Temperature

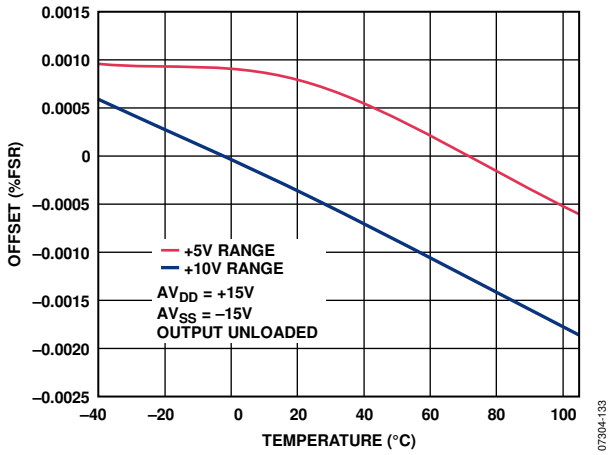


Figure 16. Offset Error vs. Temperature

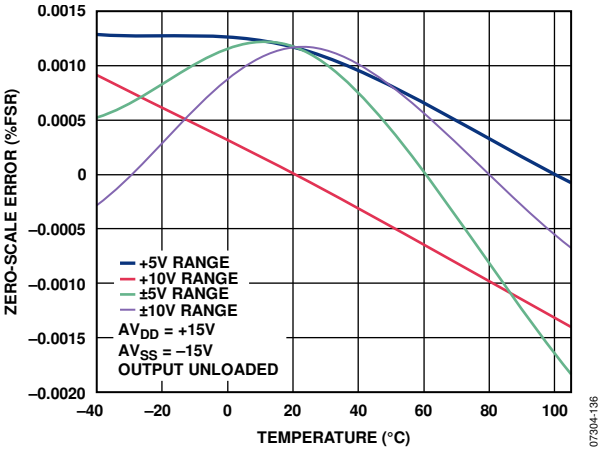


Figure 19. Zero-Scale Error vs. Temperature

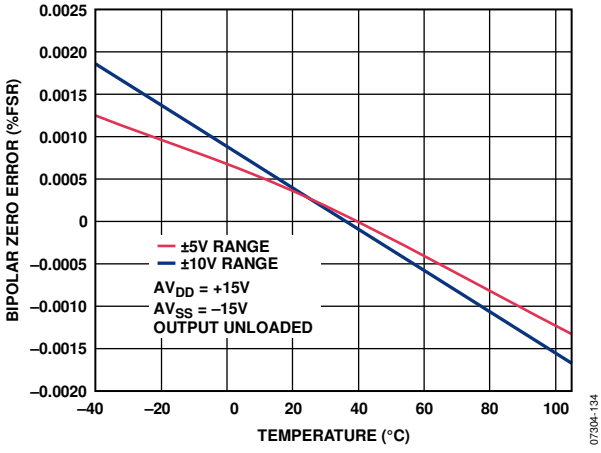


Figure 17. Bipolar Zero Error vs. Temperature

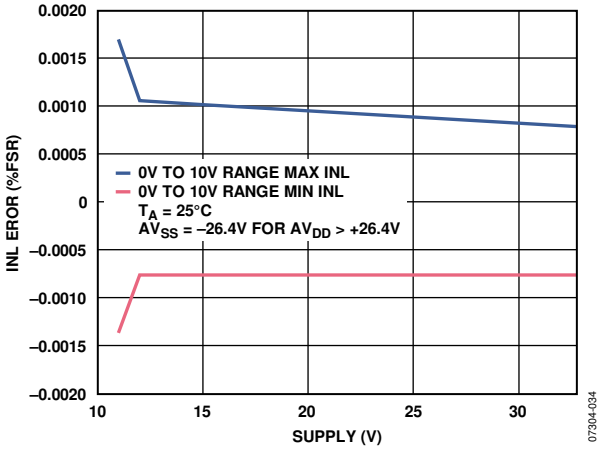


Figure 20. Integral Nonlinearity Error vs. $AV_{DD}/|AV_{SS}|$

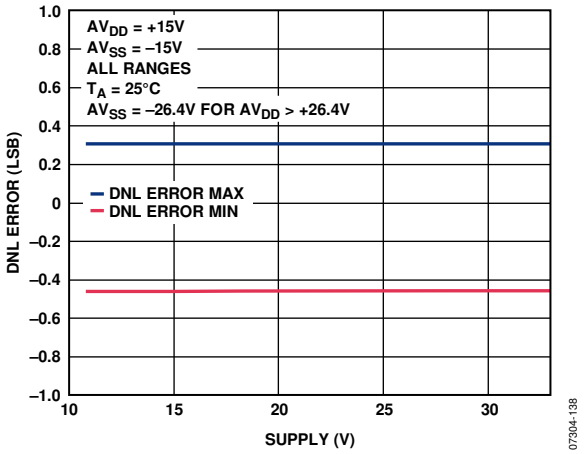


Figure 21. Differential Nonlinearity Error vs. $AV_{DD}/|AV_{SS}|$

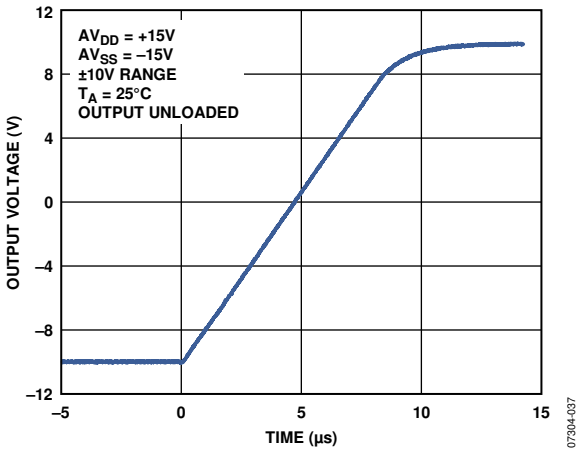


Figure 24. Full-Scale Positive Step

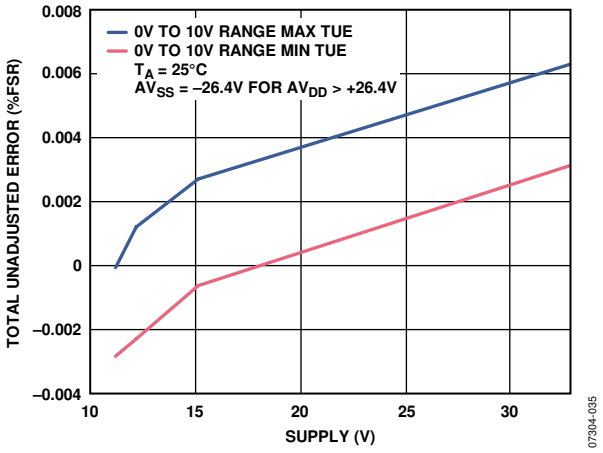


Figure 22. Total Unadjusted Error vs. $AV_{DD}/|AV_{SS}|$

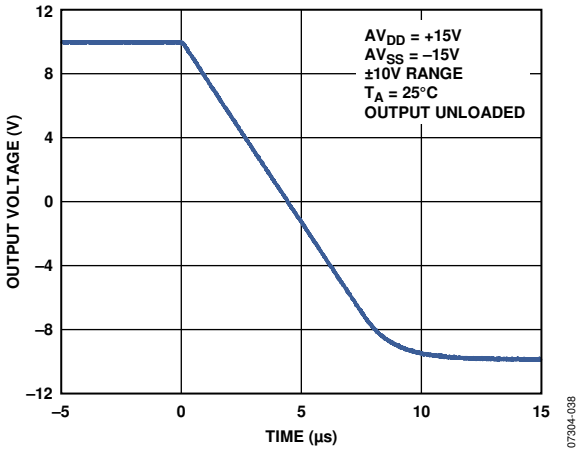


Figure 25. Full-Scale Negative Step

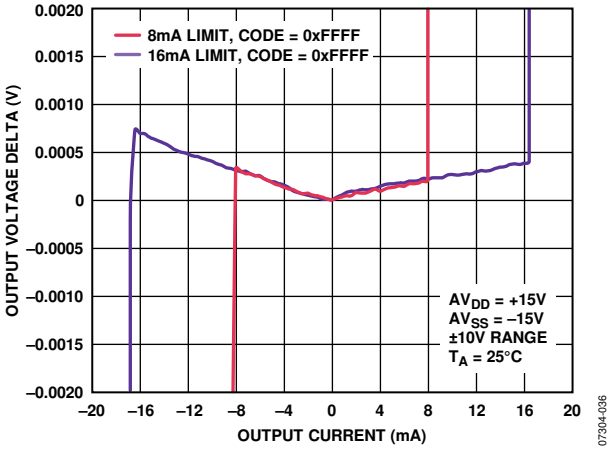


Figure 23. Source and Sink Capability of Output Amplifier

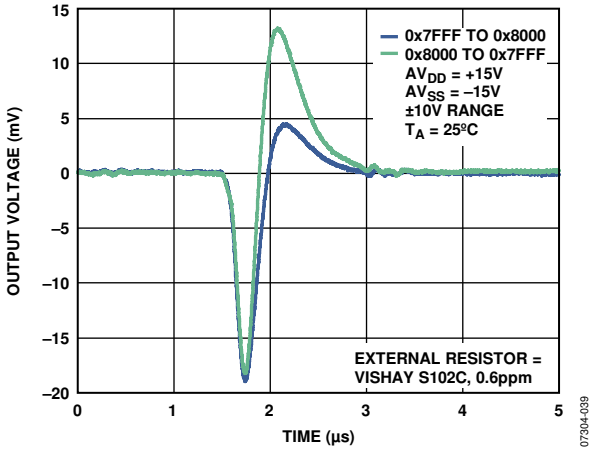


Figure 26. Digital-to-Analog Glitch

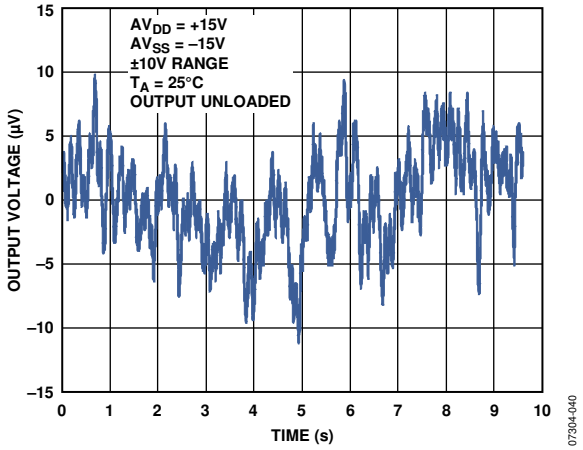


Figure 27. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

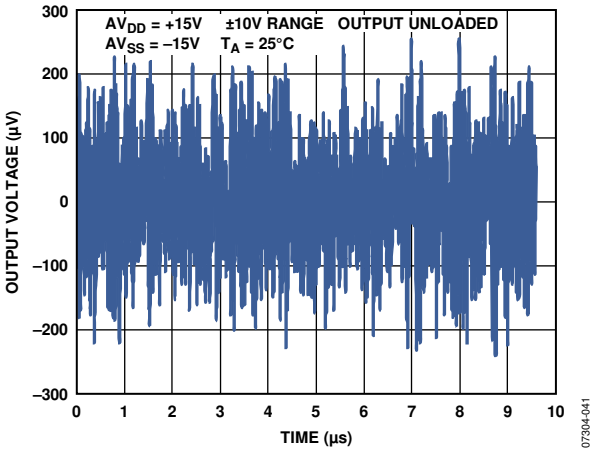


Figure 28. Peak-to-Peak Noise (100 kHz Bandwidth)

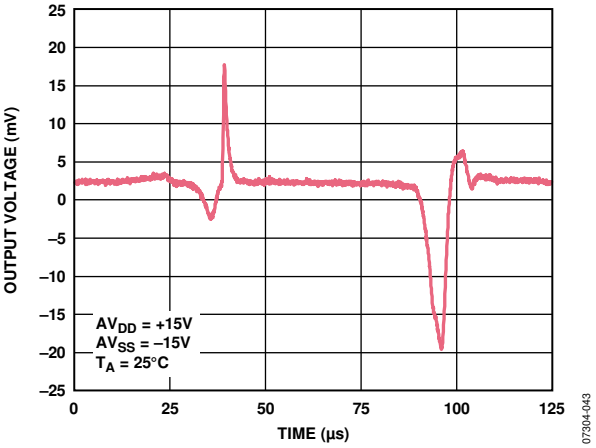


Figure 29. V_{OUT_x} vs. Time on Power-Up

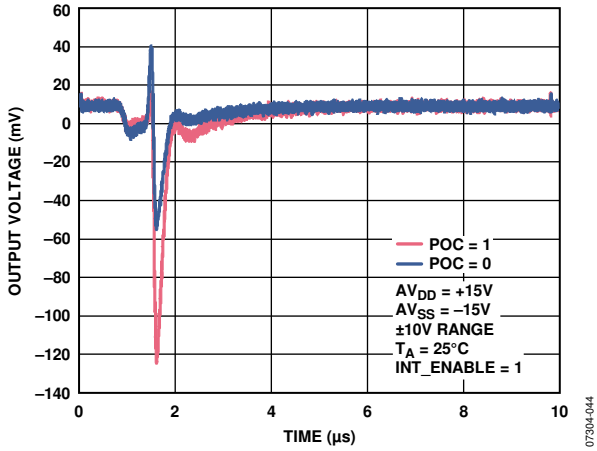


Figure 30. V_{OUT_x} vs. Time on Output Enable

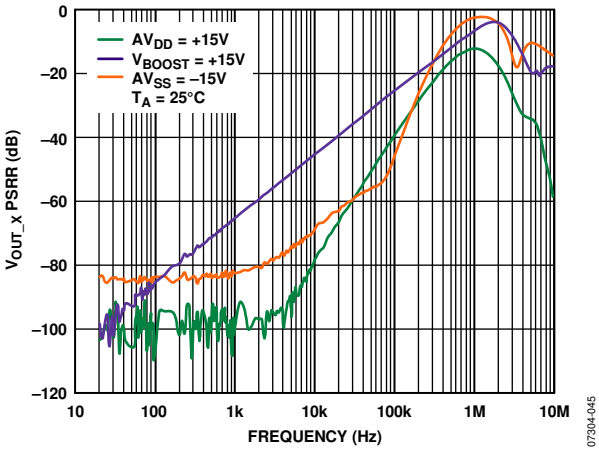


Figure 31. V_{OUT_x} PSRR vs. Frequency

CURRENT OUTPUTS

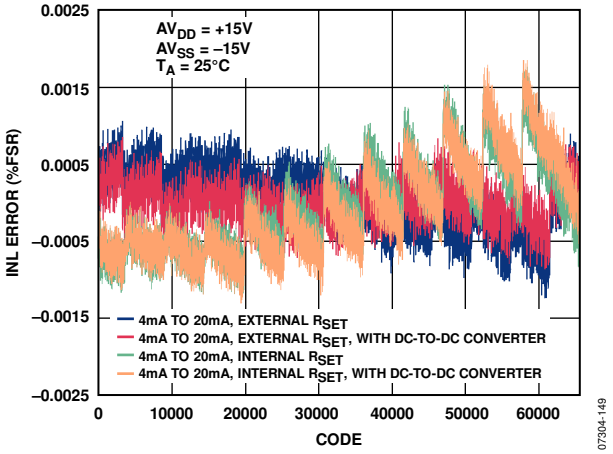


Figure 32. Integral Nonlinearity vs. Code

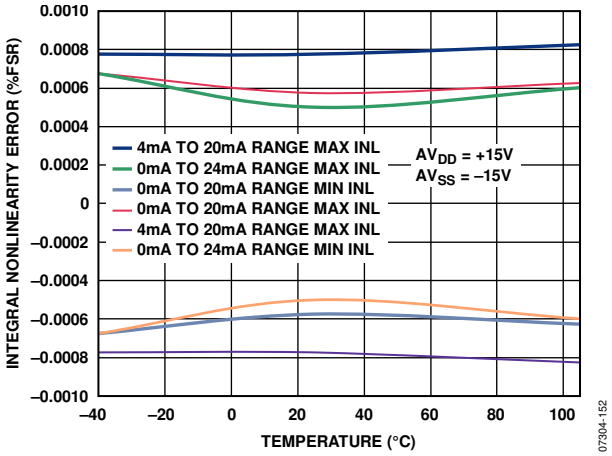


Figure 35. Integral Nonlinearity vs. Temperature, Internal R_{SET}

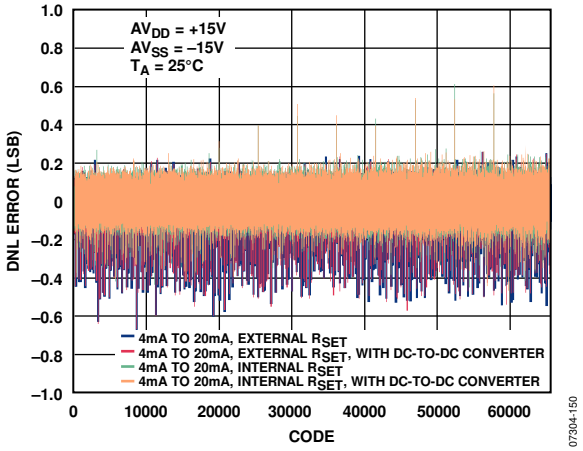


Figure 33. Differential Nonlinearity vs. Code

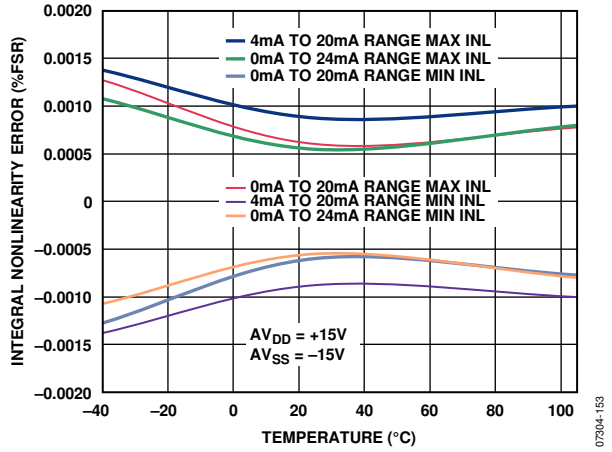


Figure 36. Integral Nonlinearity vs. Temperature, External R_{SET}

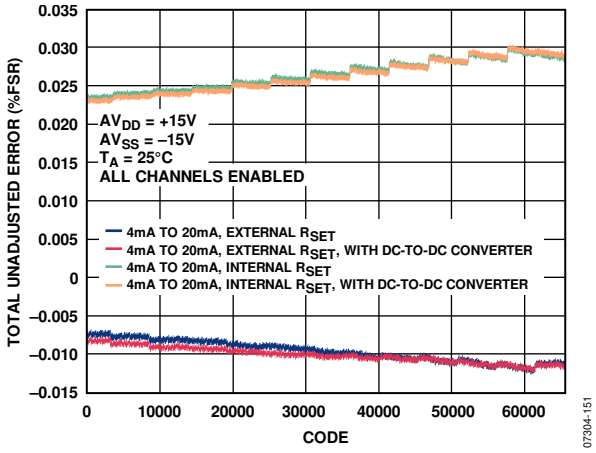


Figure 34. Total Unadjusted Error vs. Code

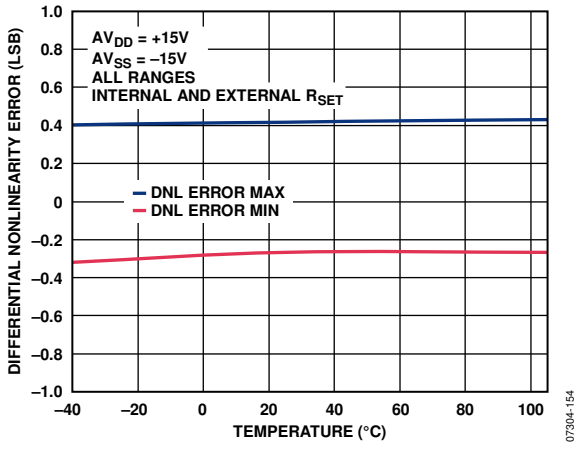


Figure 37. Differential Nonlinearity vs. Temperature

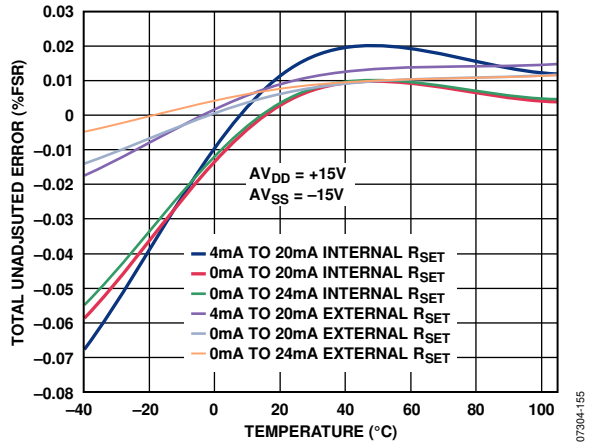


Figure 38. Total Unadjusted Error vs. Temperature

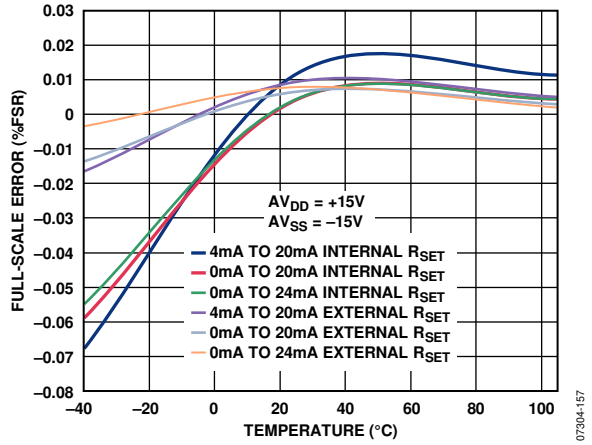


Figure 39. Full-Scale Error vs. Temperature

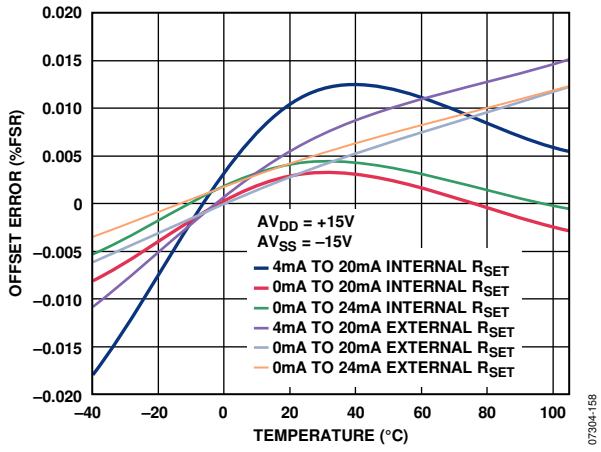


Figure 40. Offset Error vs. Temperature

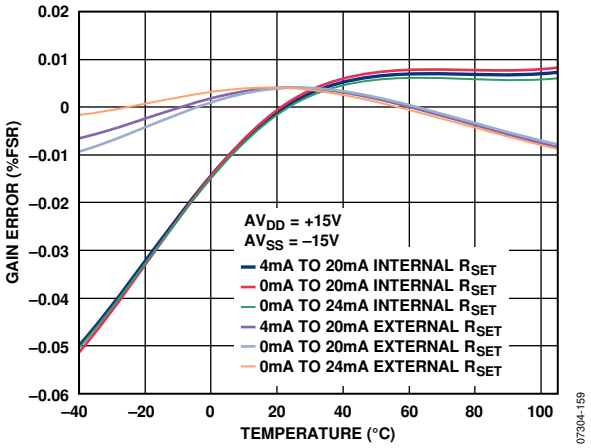


Figure 41. Gain Error vs. Temperature

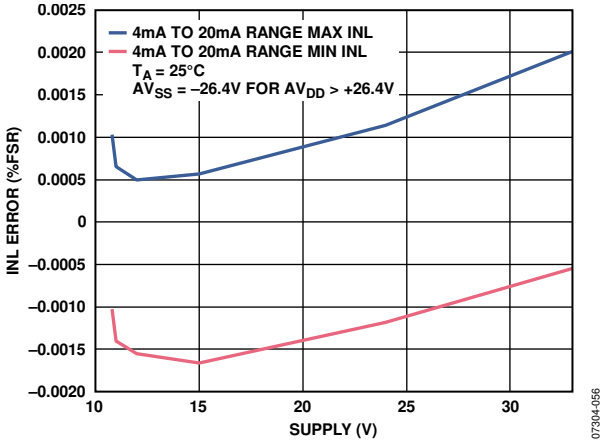


Figure 42. Integral Nonlinearity Error vs. $AV_{DD}/|AV_{SS}|$, Over Supply, External R_{SET}

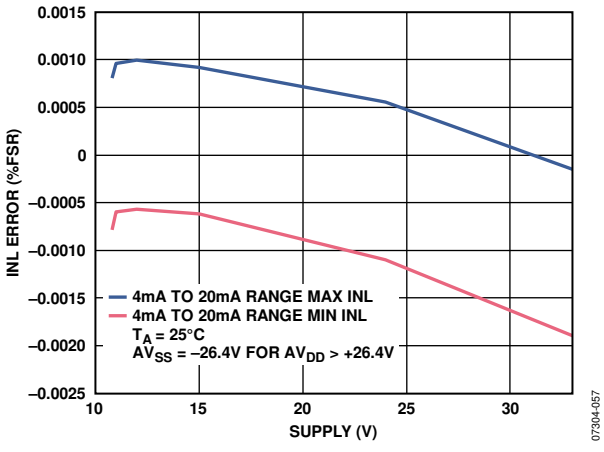


Figure 43. Integral Nonlinearity Error vs. $AV_{DD}/|AV_{SS}|$, Over Supply, Internal R_{SET}

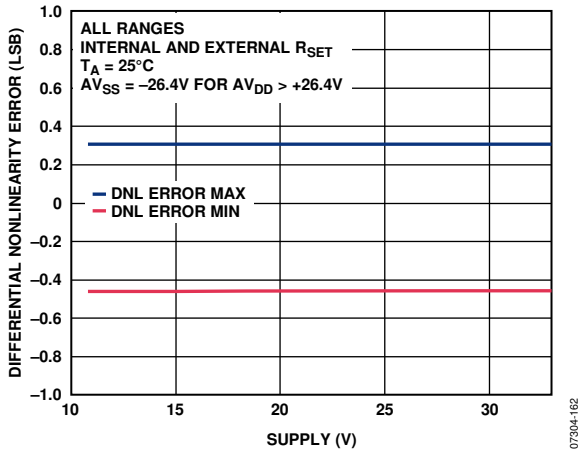


Figure 44. Differential Nonlinearity Error vs. AV_{DD}

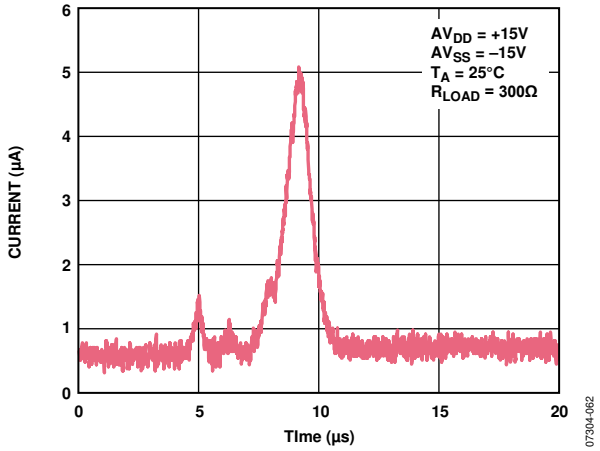


Figure 47. Output Current vs. Time on Power-Up

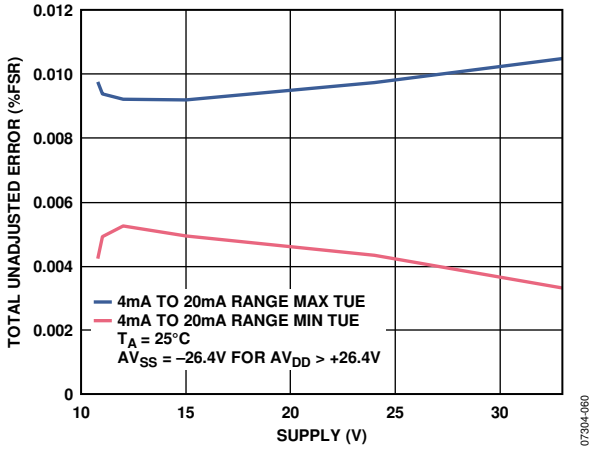


Figure 45. Total Unadjusted Error vs. AV_{DD}, External R_{SET}

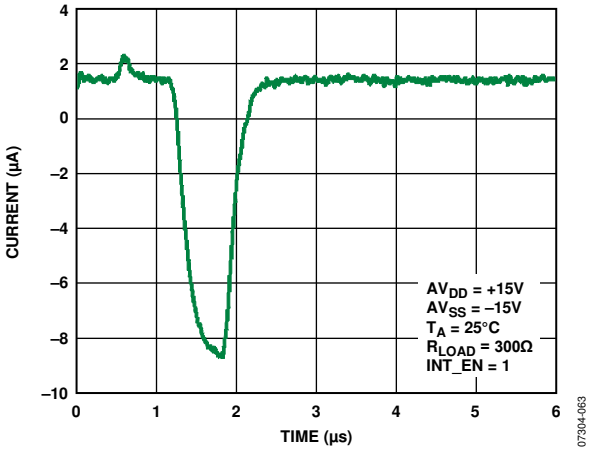


Figure 48. Output Current vs. Time on Output Enable

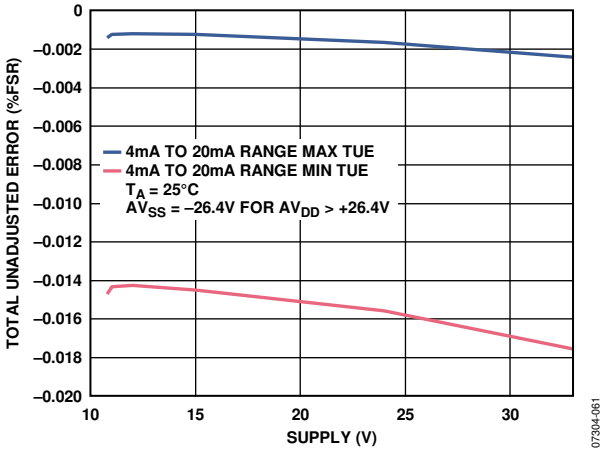


Figure 46. Total Unadjusted Error vs. AV_{DD}, Internal R_{SET}

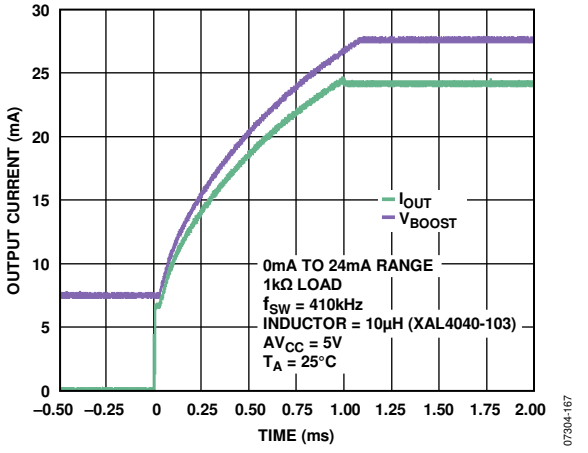


Figure 49. Output Current and V_{BOOST_x} Settling with DC-to-DC Converter (See Figure 79)

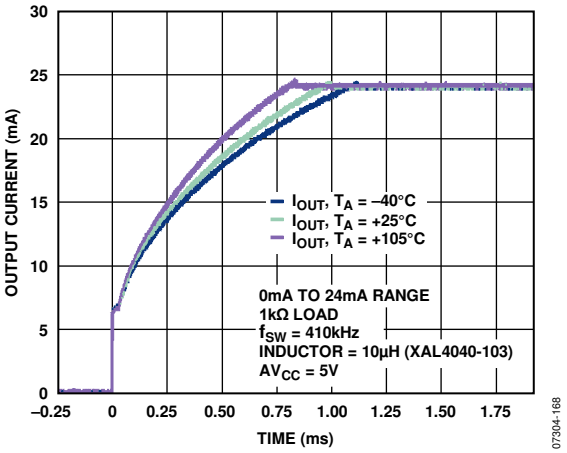


Figure 50. Output Current Settling with DC-to-DC Converter vs. Time and Temperature (See Figure 79)

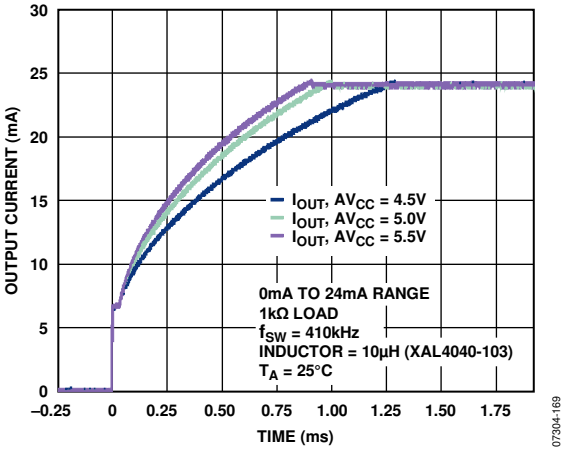


Figure 51. Output Current Settling with DC-to-DC Converter vs. Time and AV_{CC} (See Figure 79)

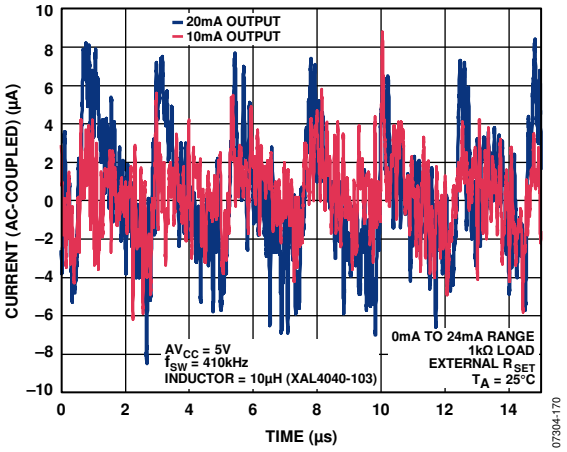


Figure 52. Output Current vs. Time with DC-to-DC Converter (See Figure 79)

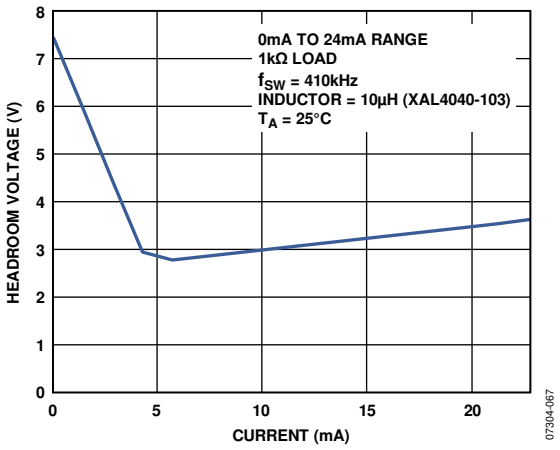


Figure 53. DC-to-DC Converter Headroom vs. Output Current (See Figure 79)

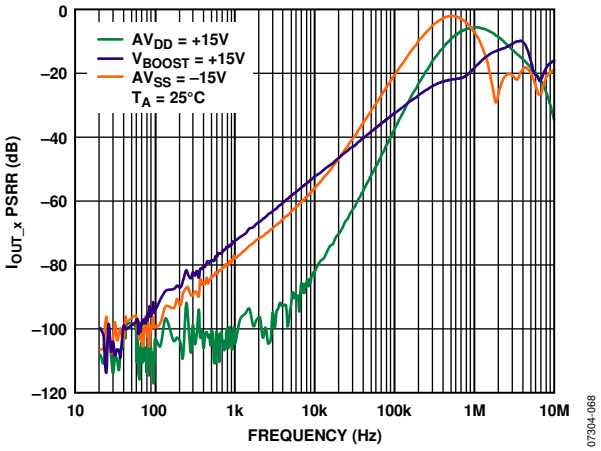


Figure 54. I_{OUT_x} PSRR vs. Frequency

DC-TO-DC BLOCK

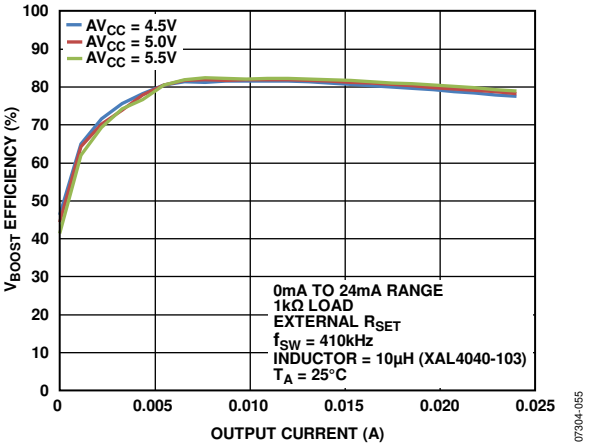


Figure 55. Efficiency at V_{BOOST_x} vs. Output Current (See Figure 79)

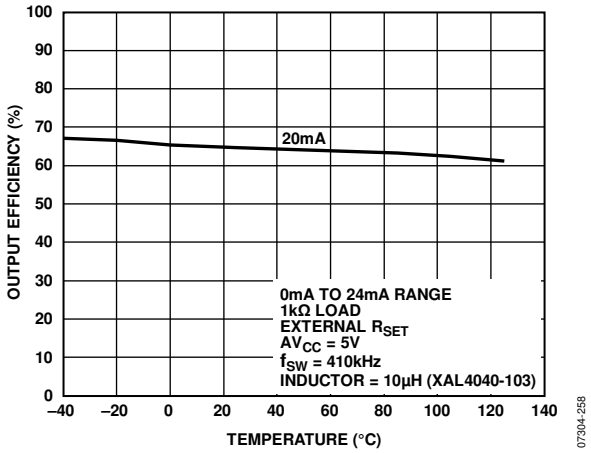


Figure 58. Output Efficiency vs. Temperature (See Figure 79)

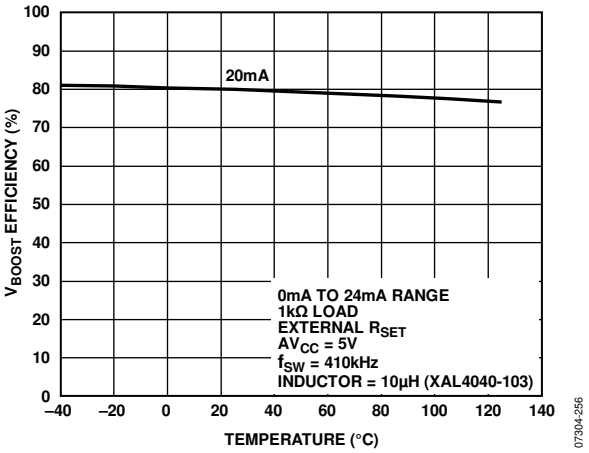


Figure 56. Efficiency at V_{BOOST_x} vs. Temperature (See Figure 79)

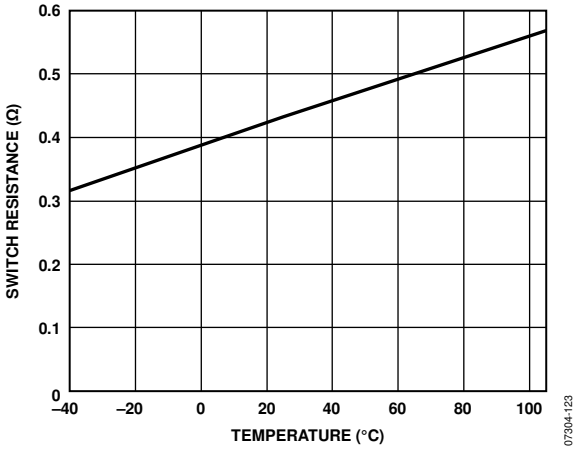


Figure 59. Switch Resistance vs. Temperature

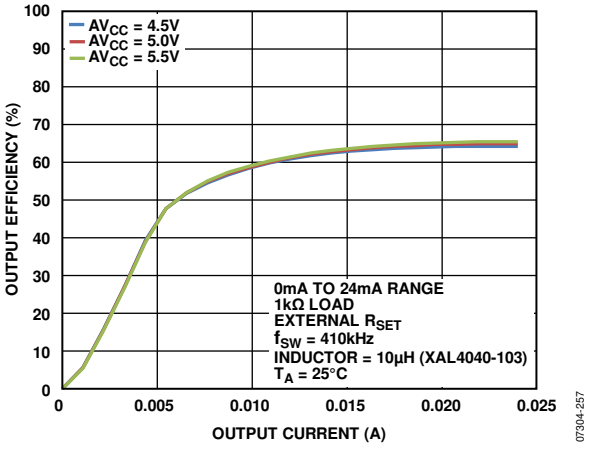


Figure 57. Output Efficiency vs. Output Current (See Figure 79)