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Single-Channel, 16-Bit Current and Voltage Output DAC with Dynamic Power Control and HART Connectivity

Data Sheet **AD5758**

FEATURES

- 16-bit resolution and monotonicity
- DPC for thermal management
- Current/voltage output available on a single terminal
- Current output ranges: 0 mA to 20 mA, 4 mA to 20 mA, 0 mA to 24 mA, ±20 mA, ±24 mA, −1 mA to +22 mA
- Voltage output ranges (with 20% overrange): 0 V to 5 V, 0 V to 10 V, ±5 V, and ±10 V
- User-programmable offset and gain
- Advanced on-chip diagnostics, including a 12-bit ADC
- On-chip reference
- Robust architecture, including output fault protection
- −40°C to +115°C temperature range
- 32-lead, 5 mm × 5 mm LFCSP package

APPLICATIONS

- Process control
- Actuator control
- Channel isolated analog outputs
- Programmable logic controller (PLC) and distributed control systems (DCS) applications
- HART network connectivity

GENERAL DESCRIPTION

The AD5758 is a single-channel, voltage and current output digital-to-analog converter (DAC) that operates with a power supply range from −33 V (minimum) on AV_{SS} to +33 V (maximum) on AV_{DD1} with a maximum operating voltage between the two rails of 60 V. On-chip dynamic power control (DPC) minimizes package power dissipation, which is achieved by regulating the supply voltage (V_{DPC+}) to the VI_{OUT} output driver circuitry from 5 V to 27 V using a buck dc-to-dc converter, optimized for minimum on-chip power dissipation. The C_{HART} pin enables a HART® signal to be coupled onto the current output.

The device uses a versatile 4-wire serial peripheral interface (SPI) that operates at clock rates of up to 50 MHz and is compatible with standard SPI, QSPI™, MICROWIRE™, DSP, and microcontroller interface standards. The interface also features an optional SPI cyclic redundancy check (CRC) and a watchdog timer (WDT). The AD5758 offers improved diagnostic features from its predecessors, such as output current monitoring and an integrated 12-bit diagnostic analog-to-digital converter (ADC). Additional robustness is provided by the inclusion of a fault protection switch on the VI_{OUT}, $+V_{SENSE}$, and $-V_{SENSE}$ pins.

PRODUCT HIGHLIGHTS

1. Range of diagnostic features, including integrated ADC.
2. DPC, using an integrated buck dc-to-dc converter for thermal management, enabling higher channel count in smaller size module housing.
3. Programmable power control (PPC) mode to enable faster settling time (15 µs typical).
4. 16-bit performance.
5. HART compliant.

COMPANION PRODUCTS

Product Family: AD5755-1, AD5422
HART Modem: AD5700, AD5700-1
External References: ADR431, ADR3425, ADR4525
Digital Isolators: ADuM142D, ADuM141D
Power: LT8300, ADP2360, ADM6339

Rev. 0 Document Feedback

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REVISION HISTORY

5/2018—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

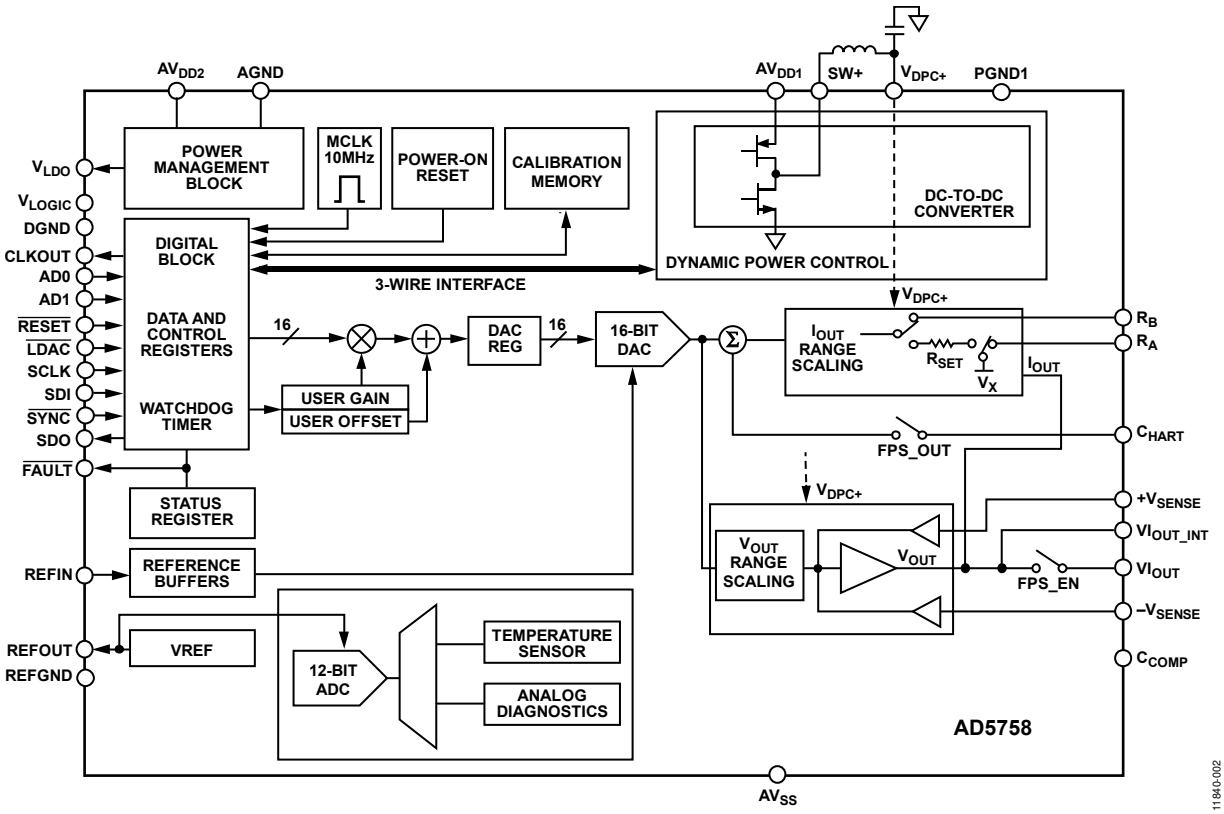


Figure 1.

SPECIFICATIONS

AV_{DD1} = V_{DPC+} = 15 V; dc-to-dc converter disabled; AV_{DD2} = 5 V; AV_{SS} = −15 V; V_{LOGIC} = 1.71 V to 5.5 V; AGND = DGND = REFGND = PGND1 = 0 V; REFIN = 2.5 V external; voltage output: R_L = 1 kΩ, C_L = 220 pF; current output: R_L = 300 Ω; all specifications at T_A = −40°C to +115°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE OUTPUT					Statement of available ranges rather than absolute minimum and maximum values
Output Voltage Ranges (V_{OUT})	0		5	V	Trimmed V_{OUT} ranges
	0		10	V	
	−5		+5	V	
	−10		+10	V	
Output Voltage Overranges	0		6	V	Untrimmed overranges
	0		12	V	
	−6		+6	V	
	−12		+12	V	
Output Voltage Offset Ranges	−0.3		+5.7	V	Untrimmed negatively offset ranges
	−0.4		+11.6	V	
Resolution	16			Bits	
VOLTAGE OUTPUT ACCURACY					Loaded and unloaded, accuracy specifications refer to trimmed V_{OUT} ranges only, unless otherwise noted
Total Unadjusted Error (TUE)	−0.05		+0.05	% FSR	
	−0.01		+0.01	% FSR	T_A = 25°C
TUE Long-Term Stability[1]		15		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		0.35	1.5	ppm FSR/°C	Output drift
Relative Accuracy (INL)	−0.006		+0.006	% FSR	All ranges
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic, all ranges
Zero-Scale Error	−0.02	±0.002	+0.02	% FSR	
Zero-Scale Error Temperature Coefficient (TC) [2]		±0.3		ppm FSR/°C	
Bipolar Zero Error	−0.015	+0.001	+0.015	% FSR	±5 V, ±10 V
Bipolar Zero Error TC[2]		±0.3		ppm FSR/°C	±5 V, ±10 V
Offset Error	−0.02	±0.002	+0.02	% FSR	
Offset Error TC[2]		±0.3		ppm FSR/°C	
Gain Error	−0.02	±0.001	+0.02	% FSR	
Gain Error TC[2]		±0.3		ppm FSR/°C	
Full-Scale Error	−0.02	±0.001	+0.02	% FSR	
Full-Scale Error TC[2]		±0.3		ppm FSR/°C	
VOLTAGE OUTPUT CHARACTERISTICS					
Headroom		1.5	2.5	V	With respect to V_{DPC+} supply
Footroom		1.5	2.5	V	With respect to the AV_{SS} supply
Short-Circuit Current		16		mA	
Load[2]	1			kΩ	For specified performance
Capacitive Load Stability[2]			10	nF	
			2	µF	External compensation capacitor of 220 pF connected
DC Output Impedance		5		mΩ	
DC Power Supply Rejection Ratio (PSRR)		10		µV/V	
V_{OUT}/−V_{SENSE} Common-Mode Rejection Ration (CMRR)		10		µV/V	Error in V_{OUT} voltage due to changes in −V_{SENSE} voltage

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT OUTPUT					
Output Current Ranges (I_{OUT})	0		24	mA	
	0		20	mA	
	4		20	mA	
	−20		+20	mA	
	−24		+24	mA	
	−1		+22	mA	
Resolution	16			Bits	
CURRENT OUTPUT ACCURACY (EXTERNAL R_{SET})[3]					Assumes ideal 13.7 kΩ resistor
Unipolar Ranges					4 mA to 20 mA, 0 mA to 20 mA, and 0 mA to 24 mA ranges
TUE	−0.06		+0.06	% FSR	
	−0.012		+0.012	% FSR	T_A = 25°C
TUE Long-Term Stability		125		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		3	7	ppm FSR/°C	
INL	−0.006		+0.006	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.03	±0.002	+0.03	% FSR	
Zero-Scale TC[2]		±0.5		ppm FSR/°C	
Offset Error	−0.035	±0.001	+0.035	% FSR	
Offset Error TC[2]		±0.7		ppm FSR/°C	
Gain Error	−0.05	±0.001	+0.05	% FSR	
Gain Error TC[2]		±4		ppm FSR/°C	
Full-Scale Error	−0.06	±0.001	+0.06	% FSR	
Full-Scale Error TC[2]		±3.5		ppm FSR/°C	
Bipolar Ranges					±20 mA, ±24 mA, and −1 mA to +22 mA ranges
Total Unadjusted Error (TUE)	−0.13		+0.13	% FSR	
	−0.014		+0.014	% FSR	T_A = 25°C
TUE Long-Term Stability[1]		125		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		12	15.5	ppm FSR/°C	
INL	−0.01		+0.01	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.04	±0.002	+0.04	% FSR	
Zero-Scale TC[2]		±0.5		ppm FSR/°C	
Bipolar Zero Error	−0.02	±0.002	+0.02	% FSR	
Bipolar Zero Error TC[2]		±0.4		ppm FSR/°C	
Offset Error	−0.15	±0.002	+0.15	% FSR	
Offset Error TC[2]		±12		ppm FSR/°C	
Gain Error	−0.25	±0.003	+0.25	% FSR	
Gain Error TC[2]		±22		ppm FSR/°C	
Full-Scale Error	−0.12	±0.002	+0.12	% FSR	
Full-Scale Error TC[2]		±11		ppm FSR/°C	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT OUTPUT ACCURACY (INTERNAL R_{SET})					
Unipolar Ranges					4 mA to 20 mA, 0 mA to 20 mA, and 0 mA to 24 mA ranges
TUE	−0.12		+0.23	% FSR	
TUE Long-Term Stability[1]		380		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		6	21	ppm FSR/°C	Output drift
INL	−0.01		+0.01	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.06	±0.002	+0.06	% FSR	
Zero-Scale TC[2]		±0.5		ppm FSR/°C	
Offset Error	−0.06	±0.001	+0.06	% FSR	
Offset Error TC[2]		±1		ppm FSR/°C	
Gain Error	−0.12	±0.005	+0.18	% FSR	
Gain Error TC[2]		±4.5		ppm FSR/°C	
Full-Scale Error	−0.15	±0.005	0.23	% FSR	
Full-Scale Error TC[2]		±3.5		ppm FSR/°C	
Bipolar Ranges					±20 mA, ±24 mA, and −1 mA to +22 mA ranges
TUE	−0.15		+0.23	% FSR	
TUE Long-Term Stability[1]		380		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		12	22	ppm FSR/°C	Output drift
INL	−0.01		+0.01	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.06	±0.002	+0.06	% FSR	
Zero-Scale TC[2]		±0.5		ppm FSR/°C	
Bipolar Zero Error	−0.02	±0.002	+0.02	% FSR	
Bipolar Zero Error TC[2]		±0.3		ppm FSR/°C	
Offset Error	−0.15	±0.004	+0.15	% FSR	
Offset Error TC[2]		±10		ppm FSR/°C	
Gain Error	−0.3	±0.007	+0.3	% FSR	
Gain Error TC[2]		±23		ppm FSR/°C	
Full-Scale Error	−0.14	±0.005	0.16	% FSR	
Full-Scale Error TC[2]		±10		ppm FSR/°C	
CURRENT OUTPUT CHARACTERISTICS					
Headroom		1.6	2.5	V	With respect to V_{DPC+} supply; the current output compliance voltage associated with this headroom margin is V_{DPC+} − 2.5 V
Footroom		1.7	2.5	V	With respect to AV_{SS} supply
Resistive Load[2]			1000	Ω	The dc-to-dc converter is characterized with a maximum load of 1 kΩ, chosen such that headroom/footroom compliance is not exceeded
Output Impedance		100		MΩ	Midscale output
DC PSRR		0.1		µA/V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUT/OUTPUT					
Reference Input					
Reference Input Voltage[2]	2.497	2.5	2.503	V	For specified performance
DC Input Impedance	55	120		MΩ	
Reference Output					
Output Voltage	2.497	2.5	2.503	V	T_A = 25°C
Reference TC[2]	−10		+10	ppm/°C	
Output Noise (0.1 Hz to 10 Hz)[2]		7		µV p-p	
Noise Spectral Density[2]		80		nV/√Hz	At 10 kHz
Output Voltage Drift vs. Time[1]		650		ppm	Drift after 1000 hours, T_J = 150°C
Capacitive Load[2]			1000	nF	
Load Current		3		mA	
Short-Circuit Current		5		mA	
Line Regulation		1		ppm/V	
Load Regulation		80		ppm/mA	
Thermal Hysteresis[2]		150		ppm	
V_{LDO} OUTPUT					
Output Voltage		3.3		V	
Output Voltage TC[2]		25		ppm/°C	
Output Voltage Accuracy	−2		+2	%	
Externally Available Current			30	mA	
Short-Circuit Current		55		mA	
Load Regulation		0.8		mV/mA	
Capacitive Load		0.1		µF	Recommended operation
DC-TO-DC					
Start-Up Time		1.25		ms	
Switch					
Peak Current Limit[2]	150		400	mA	User-programmable in 50 mA steps via the DCDC_CONFIG2 register
Oscillator					
Oscillator Frequency (f_{SW})		500		kHz	
Minimum Duty Cycle		5		%	
Current Output DPC Mode					Current output dynamic power control mode
V_{DPC+} Voltage Range	4.95		27	V	Assuming sufficient supply margin between AV_{DD1} and V_{DPC+}; see the Power Dissipation Control section for further details; maximum operating range of $\lvert V_{DPC+}$ to $AV_{SS}\rvert$ = 50 V
V_{DPC+} Headroom		2.1		V	Typical voltage required between VI_{OUT} and V_{DPC+}; only applicable when dc-to-dc converter is in regulation (that is, load is sufficiently high)
Current Output PPC Mode					PPC mode
V_{DPC+} Voltage Range	5.43		28.48	V	Assuming sufficient supply margin between AV_{DD1} and V_{DPC+}; see the Power Dissipation Control section and Table 18 for further details; maximum operating range of $\lvert V_{DPC+}$ to $AV_{SS}\rvert$ = 50 V
V_{DPC+} Voltage Accuracy	−500		+500	mV	Only applicable when dc-to-dc is operating in regulation (that is, load is sufficiently high)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Voltage Output DPC Mode					Voltage output dynamic power control mode
V_{DPC+} Voltage Range	5	15	25	V	5 V = $-V_{SENSE (MIN)}$ + 15 V; 25 V = $-V_{SENSE (MAX)}$ + 15 V; assuming sufficient supply margin between AV_{DD1} and V_{DPC+}; see the Power Dissipation Control section for further details; maximum operating range of $\lvert V_{DPC+}$ to $AV_{SS}\rvert$ = 50 V
V_{DPC+} Voltage Accuracy	−500		+500	mV	Only applicable when dc-to-dc is operating in regulation (that is, load sufficiently high)
FAULT PROTECTION SWITCH					
On Resistance, R_{ON}		6.5		Ω	T_A = 25°C
On Time, t_{ON}		10		µs	
Off Time, t_{OFF}		200		ns	
Overvoltage Response Time, $t_{RESPONSE}$		250		ns	
Overvoltage Recovery Time, $t_{RECOVERY}$		3.2		µs	
Overvoltage Leakage Current		±30		µA	Fault protection switch sinks current for a positive fault and sources current for a negative fault
ADC					
Resolution		12		Bits	
Total Error		±0.3		% FSR	Table 18 lists all ADC input nodes
Conversion Time[2]		100		µs	
DIGITAL INPUTS					
Input Voltage					
3 V ≤ V_{LOGIC} ≤ 5.5 V					
High, V_{IH}	0.7 × V_{LOGIC}			V	
Low, V_{IL}			0.3 × V_{LOGIC}	V	
1.71 V ≤ V_{LOGIC} < 3 V					
High, V_{IH}	0.8 × V_{LOGIC}			V	
Low, V_{IL}			0.2 × V_{LOGIC}	V	
Input Current	−1.5		+1.5	µA	Per pin, internal pull-down on SCLK, SDI, $\overline{\text{RESET}}$, and $\overline{\text{LDAC}}$; internal pull-up on $\overline{\text{SYNC}}$
Pin Capacitance[2]		2.4		pF	Per pin
DIGITAL OUTPUTS					
SDO					
Output Voltage					
Low, V_{OL}			0.4	V	Sinking 200 µA
High, V_{OH}	V_{LOGIC} − 0.2			V	Sourcing 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance[2]		2.2		pF	
$\overline{\text{FAULT}}$					
Output Voltage					
Low, V_{OL}			0.4	V	10 kΩ pull-up resistor to V_{LOGIC}
		0.6		V	At 2.5 mA
High, V_{OH}	V_{LOGIC} − 0.05			V	10 kΩ pull-up resistor to V_{LOGIC}

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
Supply Voltages					
AV_{DD1}[4]	7		33	V	Maximum operating range of $\lvert AV_{DD1}$ to $AV_{SS}\rvert$ = 60 V
AV_{DD2}	5		33	V	Maximum operating range of $\lvert AV_{DD2}$ to $AV_{SS}\rvert$ = 50 V
AV_{SS}[4]	−33		0	V	Maximum operating range of $\lvert AV_{DD1}$ to $AV_{SS}\rvert$ = 60 V; for bipolar output ranges, V_{OUT}/I_{OUT} headroom must be obeyed when calculating AV_{SS} maximum; for unipolar current output ranges, AV_{SS} maximum = 0 V; for unipolar voltage output ranges, AV_{SS} maximum = −2.5 V
V_{LOGIC}	1.71		5.5	V	
Supply Quiescent Currents[4]					Quiescent current, assuming no load current
AI_{DD1}		0.05	0.1	mA	Voltage output mode, dc-to-dc converter enabled but not active
		0.05	0.1	mA	Current output mode, dc-to-dc converter enabled but not active
AI_{DD2}		3.3	3.6	mA	Voltage output mode, dc-to-dc converter enabled but not active
		2.9	3.1	mA	Current output mode, dc-to-dc converter enabled but not active
AI_{SS}	−1.4	−1.1		mA	Voltage output mode
	−3.0	−2.3		mA	Bipolar current output mode
	−0.26	−0.23		mA	Unipolar current output mode
I_{LOGIC}			0.01	mA	$V_{IH} = V_{LOGIC}$, V_{IL} = DGND
I_{DPC+}		1.0	1.3	mA	Voltage output mode
		0.8	1	mA	Bipolar current output mode
		2.3	3	mA	Unipolar current output mode
Power Dissipation					Power dissipation assuming an ideal power supply and excluding external load power dissipation, current output DPC mode, 0 mA to 20 mA range; see the Example Module Power Calculation section for calculation methodology
		100		mW	AV_{DD1} = 24 V, AV_{DD2} = 5 V, AV_{SS} = −15 V, R_{LOAD} = 1 kΩ, I_{OUT} = 20 mA
		145		mW	AV_{DD1} = 24 V, AV_{DD2} = 5 V, AV_{SS} = −15 V, R_{LOAD} = 0 Ω, I_{OUT} = 20 mA
		155		mW	$AV_{DD1} = AV_{DD2}$ = 24 V, AV_{SS} = −15 V, R_{LOAD} = 1 kΩ, I_{OUT} = 20 mA
		200		mW	$AV_{DD1} = AV_{DD2}$ = 24 V, AV_{SS} = −15 V, R_{LOAD} = 0 Ω, I_{OUT} = 20 mA

[1] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.
[2] Guaranteed by design and characterization; not production tested.
[3] See the Current Output section for more information about the internal and external R_{SET} resistors.
[4] Production tested to AV_{DD1} maximum = 30 V and AV_{SS} minimum = −30 V.

AC PERFORMANCE CHARACTERISTICS

AV_{DD1} = V_{DPC+} = 15 V; dc-to-dc converter disabled; AV_{DD2} = 5 V; AV_{SS} = −15 V; V_{LOGIC} = 1.71 V to 5.5 V; AGND = DGND = REFGND = PGND1 = 0 V; REFIN = 2.5 V external; voltage output: R_L = 1 kΩ, C_L = 220 pF; current output: R_L = 300 Ω; all specifications at T_A = −40°C to +115°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]					
Voltage Output					
Output Voltage Settling Time					Output voltage settling time specifications also apply for dc-to-dc converter enabled
		6	20	µs	5 V step to ±0.03% FSR, 0 V to 5 V range
		12	20	µs	10 V step to ±0.03% FSR, 0 V to 10 V range
			15	µs	100 mV step to 1 LSB (16-bit LSB), 0 V to 10 V range
Slew Rate		3		V/µs	0 V to 10 V range, digital slew rate control disabled
Power-On Glitch Energy		25		nV-sec	
Digital-to-Analog Glitch Energy		3		nV-sec	
Glitch Impulse Peak Amplitude		25		mV	
Digital Feedthrough		2		nV-sec	
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.2		LSB p-p	16-bit LSB, 0 V to 10 V range
Output Noise Spectral Density		185		nV/√Hz	Measured at 10 kHz, midscale output, 0 V to 10 V range
AC PSRR		70		dB	200 mV, 50 Hz/60 Hz sine wave superimposed on power supply voltage
Current Output					
Output Current Settling Time					
		15		µs	To 0.1% FSR (0 mA to 24 mA), dc-to-dc converter disabled
		15		µs	PPC mode, dc-to-dc converter enabled, dc-to-dc current limit = 150 mA
		200		µs	DPC mode, dc-to-dc converter enabled; external inductor and capacitor components as described in Table 10, dc-to-dc current limit = 150 mA.
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.2		LSB p-p	16-bit LSB, 0 mA to 24 mA range
Output Noise Spectral Density		0.8		nA/√Hz	Measured at 10 kHz, midscale output, 0 mA to 24 mA range
AC PSRR		80		dB	200 mV, 50 Hz/60 Hz sine wave superimposed on power supply voltage

[1] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

AV_{DD1} = V_{DPC+} = 15 V; dc-to-dc converter disabled; AV_{DD2} = 5 V; AV_{SS} = −15 V; V_{LOGIC} = 1.71 V to 5.5 V; AGND = DGND = REGND = PGND1 = 0 V; REFIN = 2.5 V external; voltage output: R_L = 1 kΩ, C_L = 220 pF; current output: R_L = 300 Ω; all specifications at T_A = −40°C to +115°C, unless otherwise noted.

Table 3.

Parameter[1, 2, 3]	1.71 V ≤ V_{LOGIC} < 3 V	3 V ≤ V_{LOGIC} ≤ 5.5 V	Unit	Description
t_1	33	20	ns min	SCLK cycle time, write operation
	120	66	ns min	SCLK cycle time, read operation
t_2	16	10	ns min	SCLK high time, write operation
	60	33	ns min	SCLK high time, read operation
t_3	16	10	ns min	SCLK low time, write operation
	60	33	ns min	SCLK low time, read operation
t_4	10	10	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time, write operation
	33	33	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time, read operation
t_5	10	10	ns min	24th/32nd SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	500	500	ns min	$\overline{SYNC}$ high time (all register writes outside of those listed in this table)
	1.5	1.5	µs min	$\overline{SYNC}$ high time (DAC_INPUT register write)
	500	500	µs min	$\overline{SYNC}$ high time (DAC_CONFIG register write, where the Range[3:0] bits change; see the Calibration Memory CRC section)
t_7	5	5	ns min	Data setup time
t_8	6	6	ns min	Data hold time
t_9	750	750	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge
t_{10}	1.5	1.5	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{11}	250	250	ns min	$\overline{LDAC}$ pulse width low
t_{12}	600	600	ns max	$\overline{LDAC}$ falling edge to DAC output response time, digital slew rate control disabled.
	2	2	µs max	$\overline{LDAC}$ falling edge to DAC output response time, digital slew rate control enabled.
t_{13}	See the AC Performance Characteristics section		µs max	DAC output settling time
t_{14}	1.5	1.5	µs max	$\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC}$ = 0)
t_{15}	5	5	µs min	$\overline{RESET}$ pulse width
t_{16}	40	28	ns max	SCLK rising edge to SDO valid
t_{17}	100	100	µs min	$\overline{RESET}$ rising edge to 1st SCLK falling edge after $\overline{SYNC}$ falling edge (t_{17} does not appear in the timing diagrams)

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{LOGIC}) and timed from a voltage level of 1.2 V. t_R is rise time. t_F is fall time.
[3] See Figure 2, Figure 3, Figure 4, and Figure 5.

Timing Diagrams

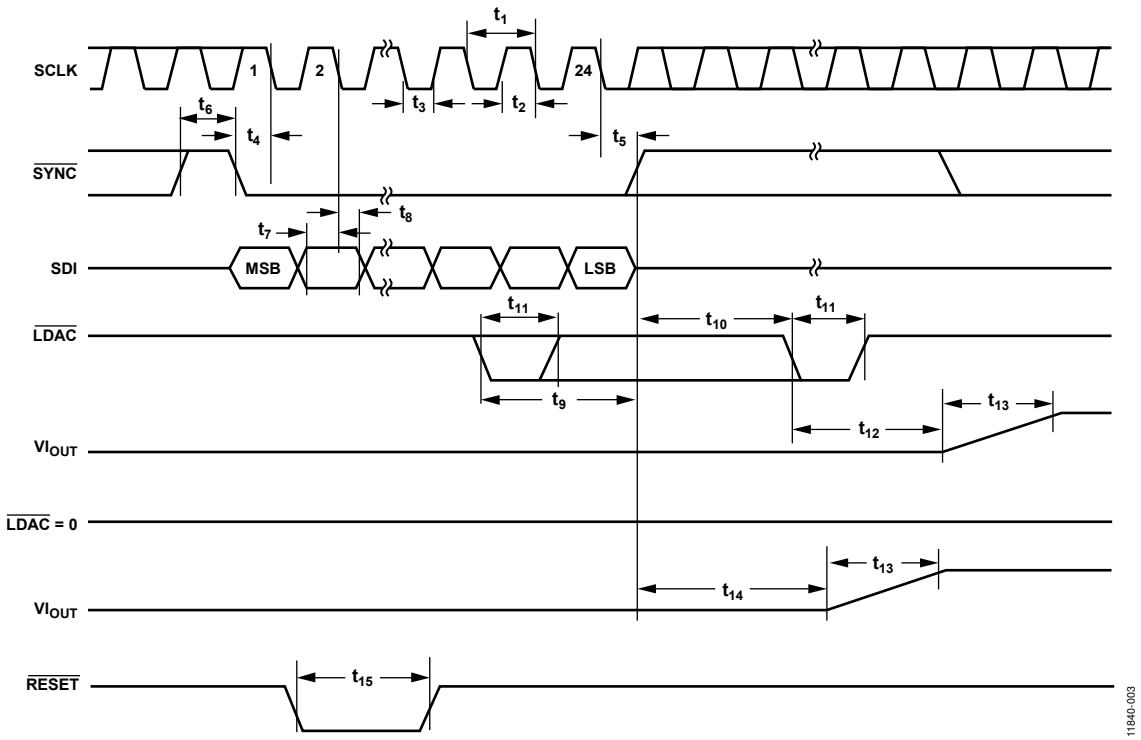


Figure 2. Serial Interface Timing Diagram

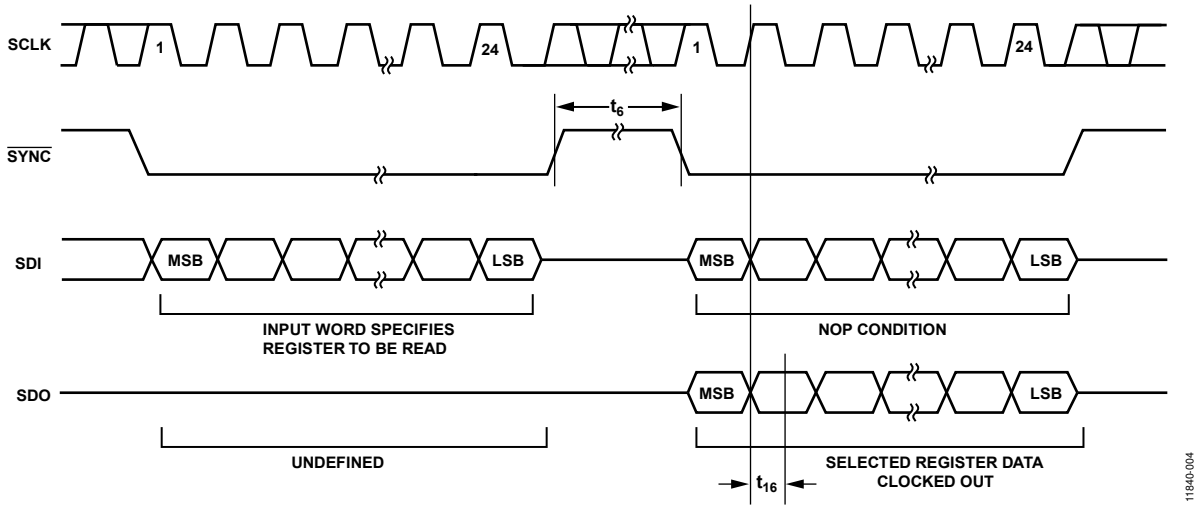
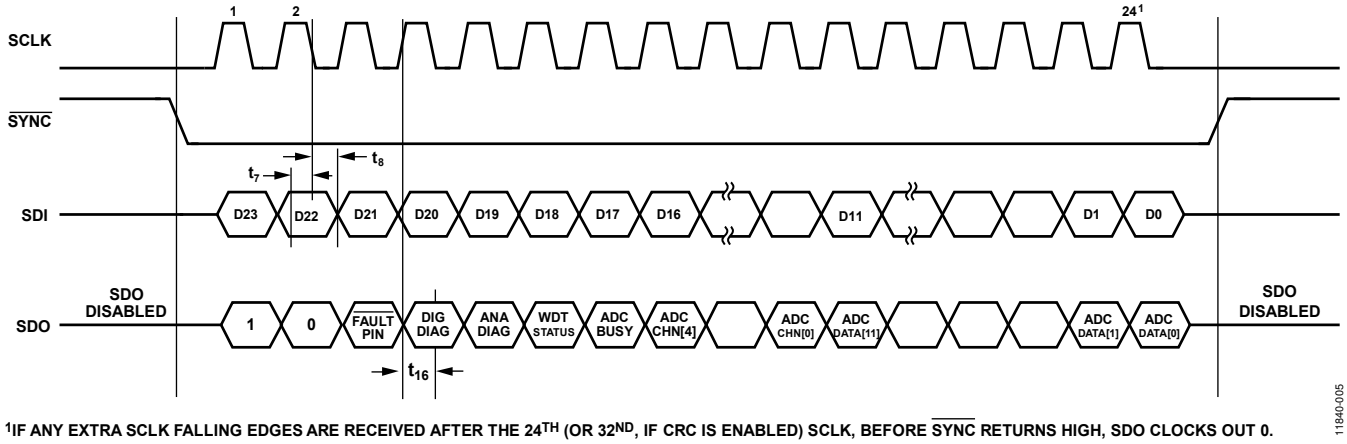


Figure 3. Readback Timing Diagram



[1]IF ANY EXTRA SCLK FALLING EDGES ARE RECEIVED AFTER THE 24TH (OR 32ND, IF CRC IS ENABLED) SCLK, BEFORE $\overline{SYNC}$ RETURNS HIGH, SDO CLOCKS OUT 0.

Figure 4. Autostatus Readback Timing Diagram

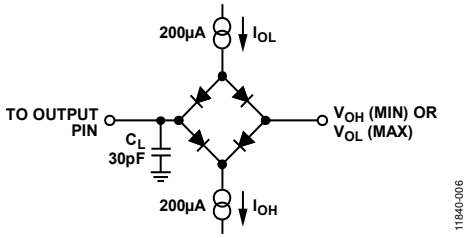


Figure 5. Load Circuit for SDO Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Table 4.

Parameter	Rating
AV_{DD1} to AGND, DGND	−0.3 V to +44 V
AV_{SS} to AGND, DGND	+0.3 V to −33 V
AV_{DD1} to AV_{SS}	−0.3 V to +66 V
AV_{DD2}, V_{DPC+} to AGND, DGND	−0.3 V to +35 V
AV_{DD2}, V_{DPC+} to AV_{SS}	−0.3 V to +55 V
V_{LOGIC} to DGND	−0.3 V to +7 V
Digital Inputs to DGND (SCLK, SDI, SYNC, AD0, AD1, RESET, LDAC)	−0.3 V to V_{LOGIC} + 0.3 V or +7 V (whichever is less)
Digital Outputs to DGND (FAULT, SDO, CLKOUT)	−0.3 V to V_{LOGIC} + 0.3 V or +7 V (whichever is less)
REFIN, REFOUT, V_{LDO}, C_{HART} to AGND	−0.3 V to AV_{DD2} + 0.3 V or +7 V (whichever is less)
R_A to AGND	−0.3 V to +4.5 V
R_B to AGND	−0.3 V to +4.5 V
VI_{OUT} to AGND	±35 V
VI_{OUT_INT} to AGND	±35 V
$+V_{SENSE}$ to AGND	±35 V
$-V_{SENSE}$ to AGND	±35 V
C_{COMP} to AGND	AV_{SS} − 0.3 V to V_{DPC+} + 0.3 V
SW+ to AGND	−0.3 V to AV_{DD1} + 0.3 V or +33 V (whichever is less)
AGND, DGND to REFGND	−0.3 V to +0.3 V
AGND, DGND to PGND1	−0.3 V to +0.3 V
Industrial Operating Temperature Range (T_A)[1]	−40°C to +115°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}
Lead Temperature Soldering	JEDEC industry standard J-STD-020

[1] Power dissipated on the chip must be derated to keep the junction temperature below 125°C.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-32-30[1]	46	18	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

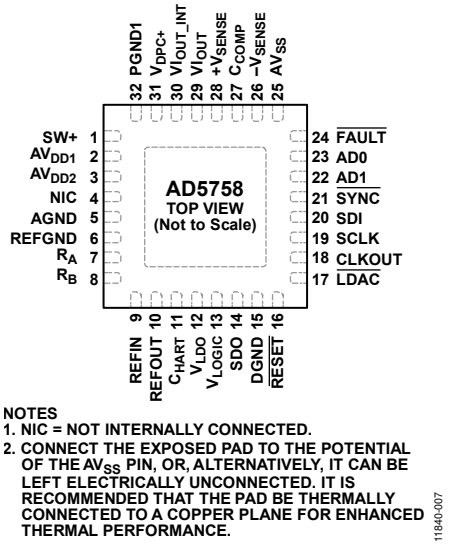


Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SW+	Switching Output for the DC-to-DC Circuitry. To use the dc-to-dc feature of the device, connect as shown in Figure 77.
2	AV_{DD1}	Positive Analog Supply. The voltage range is from 7 V to 33 V.
3	AV_{DD2}	Positive Low Voltage Analog Supply. The voltage range is from 5 V to 33 V.
4	NIC	Not Internally Connected. This pin is not internally connected.
5	AGND	Ground Reference Point for the Analog Circuitry. This pin must be connected to 0 V.
6	REFGND	Ground Reference Point for Internal Reference. This pin must be connected to 0 V.
7	R_A	External Current Setting Resistor. An external, precision, low drift 13.7 kΩ current setting resistor can be connected between R_A and R_B to improve the current output temperature drift performance. It is recommended that the external resistor be placed as close as possible to the AD5758.
8	R_B	External Current Setting Resistor. An external, precision, low drift 13.7 kΩ current setting resistor can be connected between R_A and R_B to improve the current output temperature drift performance. It is recommended that the external resistor be placed as close as possible to the AD5758.
9	REFIN	External 2.5 V Reference Voltage Input.
10	REFOUT	Internal 2.5 V Reference Voltage Output. REFOUT must be connected to REFIN to use the internal reference. A capacitor between REFOUT and REFGND is not recommended.
11	C_{HART}	HART Input Connection. The HART signal must be ac-coupled to this pin. If HART is not being used, leave this pin unconnected. This pin is disconnected from the HART summing node by default and can be connected via the HART_EN bit in the GP_CONFIG1 register.
12	V_{LDO}	3.3 V LDO Output Voltage. V_{LDO} must be decoupled to AGND with a 0.1 µF capacitor.
13	V_{LOGIC}	Digital Supply. The voltage range is from 1.71 V to 5.5 V. V_{LOGIC} must be decoupled to DGND with a 0.1 µF capacitor.
14	SDO	Serial Data Output. This pin clocks data from the serial register in readback mode. The maximum SCLK speed for readback mode is 15 MHz (depending on the V_{LOGIC} voltage). See Table 3.
15	DGND	Digital Ground.
16	$\overline{\text{RESET}}$	Hardware $\overline{\text{Reset}}$. Active low input. Do not write an SPI command within 100 µs of issuing a reset (using the hardware $\overline{\text{RESET}}$ pin or via software).
17	$\overline{\text{LDAC}}$	Load $\overline{\text{DAC}}$. Active low input. This pin updates the DAC_OUTPUT register and, consequently, the DAC output. Do not assert $\overline{\text{LDAC}}$ within the window of 500 ns before the rising edge of $\overline{\text{SYNC}}$ or 1.5 µs after the rising edge of $\overline{\text{SYNC}}$ (see Table 3 for the timing specifications).
18	CLKOUT	Optional Clock Output Signal (Disabled by Default). This pin is a divided down version of the internal 10 MHz oscillator (MCLK) and is configured in the GP_CONFIG1 register.

Pin No.	Mnemonic	Description
19	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. In write mode, this pin operates at clock speeds of up to 50 MHz (depending on the V_{LOGIC} voltage). In read mode, the maximum SCLK speed is 15 MHz (depending on the V_{LOGIC} voltage). See Table 3 for the timing specifications.
20	SDI	Serial Data Input. Data must be valid on the falling edge of SCLK.
21	$\overline{\text{SYNC}}$	Frame Synchronization Signal for the Serial Interface. Active low input. While $\overline{\text{SYNC}}$ is low, data is transferred in on the falling edge of SCLK.
22	AD1	Address Decode 1 for the DUT on the Board.
23	AD0	Address Decode 0 for the DUT on the Board.
24	$\overline{\text{FAULT}}$	Fault Pin. Active low, open-drain output. This pin is high impedance when no faults are detected and is asserted low when certain faults are detected, for example, an open circuit in current mode, a short circuit in voltage mode, a CRC error, or an overtemperature error (see the Output Fault section). This pin must be connected to V_{LOGIC} with a 10 kΩ pull-up resistor.
25	AV_{SS}	Negative Analog Supply. The voltage range is from 0 V to −33 V. If using the device solely for unipolar current output purposes, AV_{SS} can be 0 V. For a unipolar voltage output, AV_{SS} (maximum) is −2.5 V. When using bipolar output ranges, V_{OUT}/I_{OUT} headroom must be obeyed when calculating the AV_{SS} maximum, for example, for a ±10 V output, the AV_{SS} maximum is −12.5 V. See the AVSS Considerations section for an important note on power supply sequencing.
26	$-V_{SENSE}$	Sense Connection for the Negative Voltage Output Load Connection for V_{OUT} Mode. This pin must stay within ±10 V of AGND for specified operation. For specified operation, AV_{SS} tracks $-V_{SENSE}$ with respect to AGND. If remote sensing is not being used, short this pin to AGND.
27	C_{COMP}	Optional Compensation Capacitor Connection for the Voltage Output Buffer. Connecting a 220 pF capacitor between this pin and the VI_{OUT} pin allows the voltage output to drive up to 2 µF. The addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
28	$+V_{SENSE}$	Sense Connection for the Positive Voltage Output Load Connection for Voltage Output Mode. If remote sensing is not being used, short this pin to VI_{OUT} via a series 1 kΩ resistor.
29	VI_{OUT}	Voltage/Current Output Pin. VI_{OUT} is a shared pin, providing either a buffered output voltage or current.
30	VI_{OUT_INT}	Fault Protect Switch Internal Node. The inside of the fault protect switch is routed to this pin.
31	V_{DPC+}	Positive Supply for Current and Voltage Output Stage. To use the dc-to-dc feature of the device, connect as shown in Figure 77.
32	PGND1	Power Ground.
	EPAD	Exposed Pad. Connect the exposed pad to the potential of the AV_{SS} pin, or, alternatively, it can be left electrically unconnected. It is recommended that the pad be thermally connected to a copper plane for enhanced thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE OUTPUT

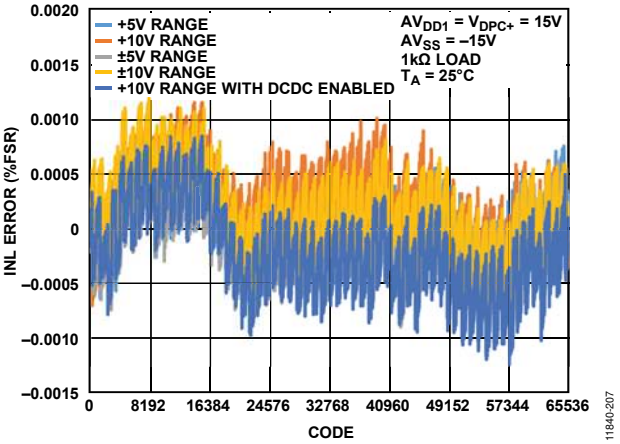


Figure 7. INL Error vs. DAC Code

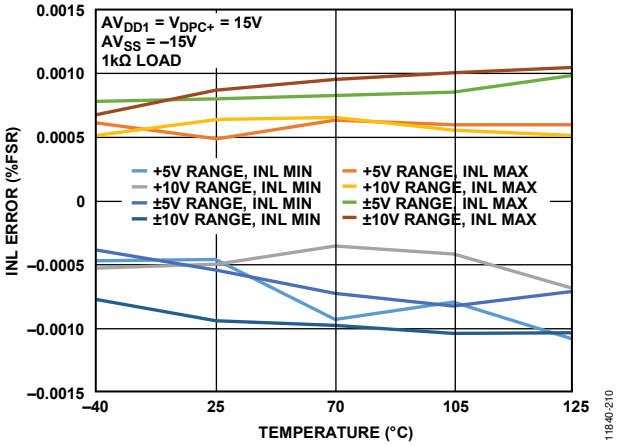


Figure 10. INL Error vs. Temperature

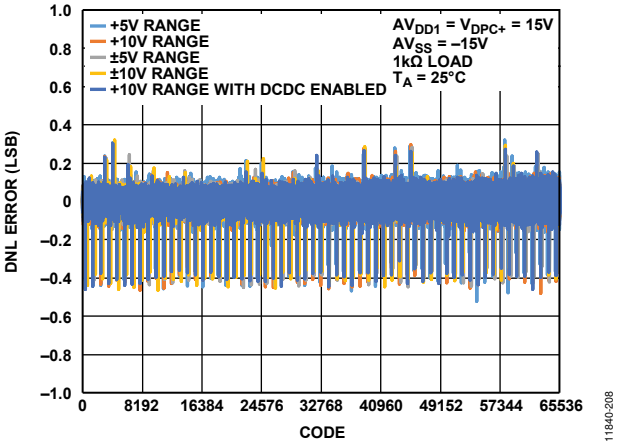


Figure 8. DNL Error vs. DAC Code

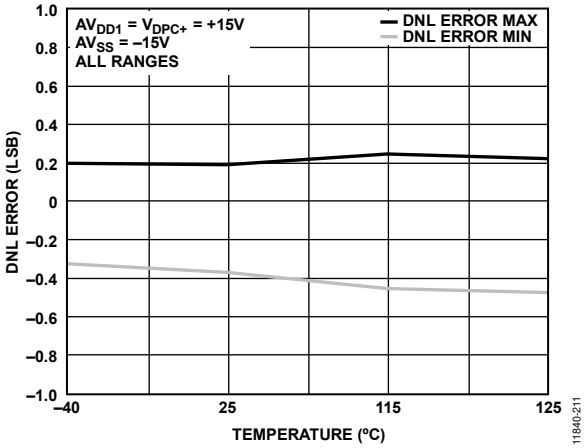


Figure 11. DNL Error vs Temperature

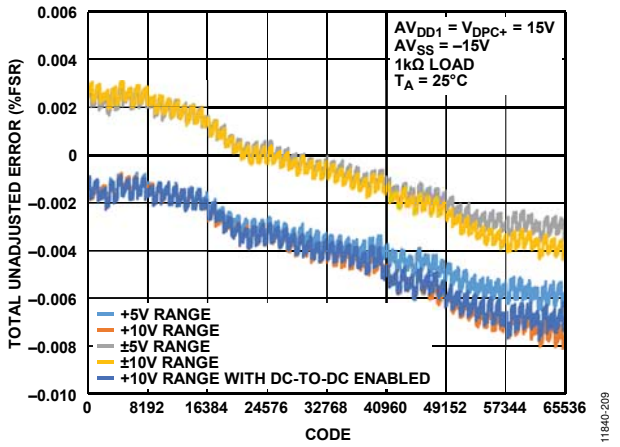


Figure 9. Total Unadjusted Error vs. DAC Code

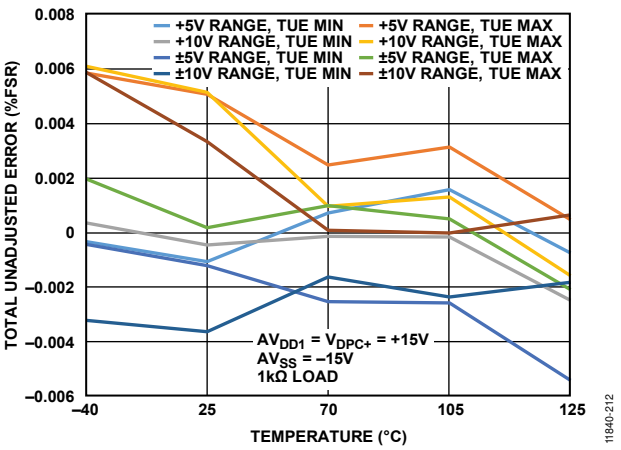


Figure 12. Total Unadjusted Error vs. Temperature

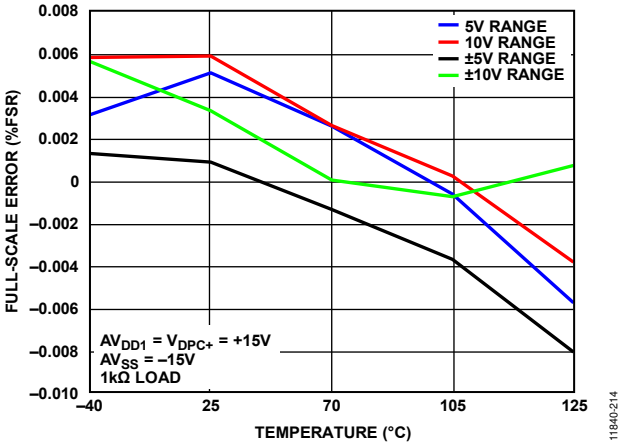


Figure 13. Full-Scale Error vs. Temperature

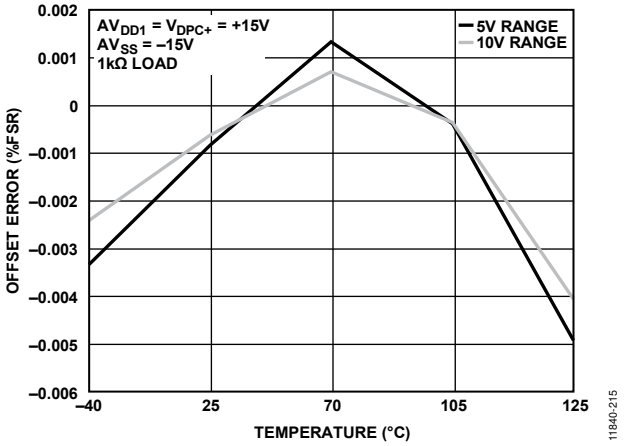


Figure 14. Offset Error vs. Temperature

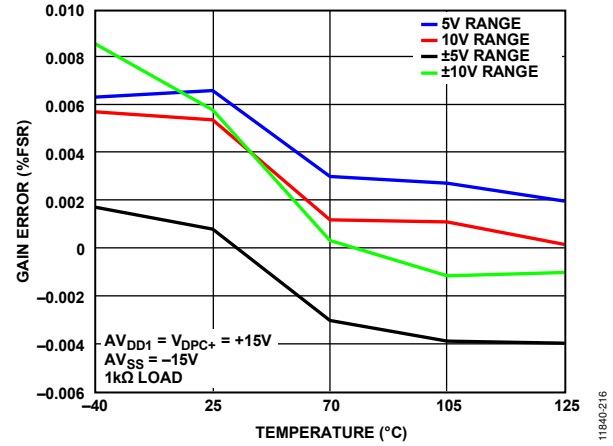


Figure 15. Gain Error vs. Temperature

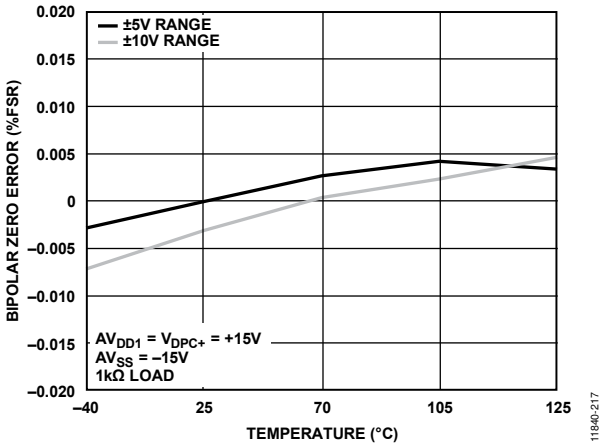


Figure 16. Bipolar Zero Error vs. Temperature

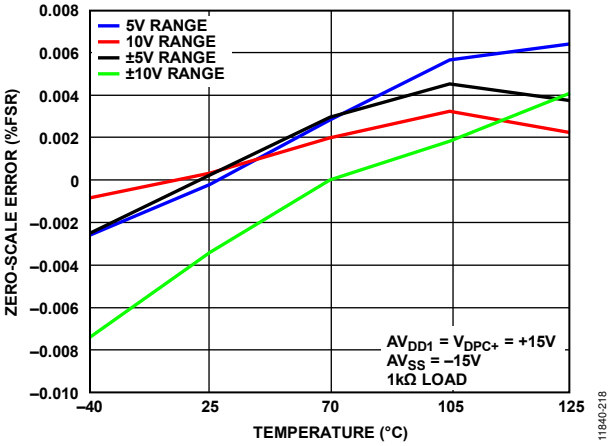


Figure 17. Zero-Scale Error vs. Temperature

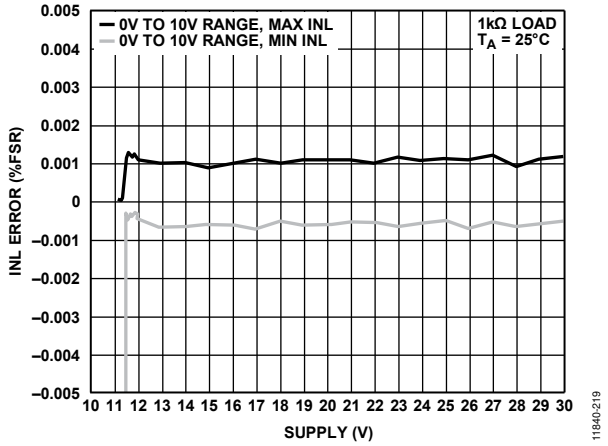


Figure 18. INL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply

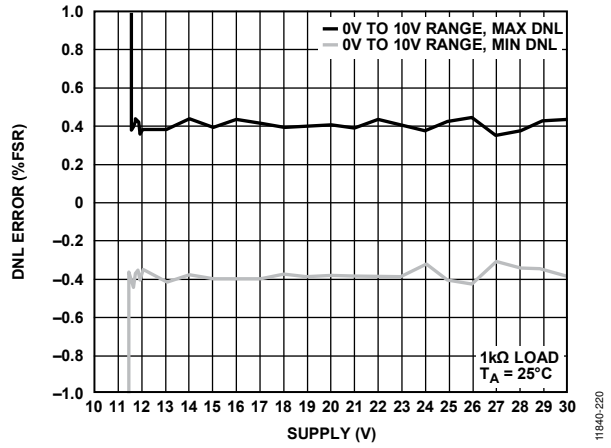


Figure 19. DNL Erorr vs. AV_{DD1}/|AV_{SS}| Supply

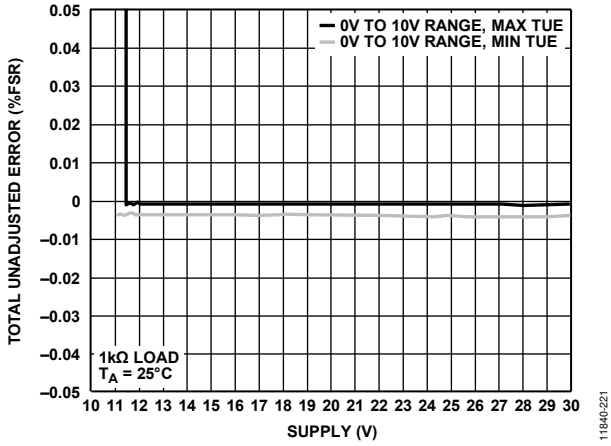


Figure 20. Total Unadjusted Error vs. AV_{DD1}/|AV_{SS}| Supply

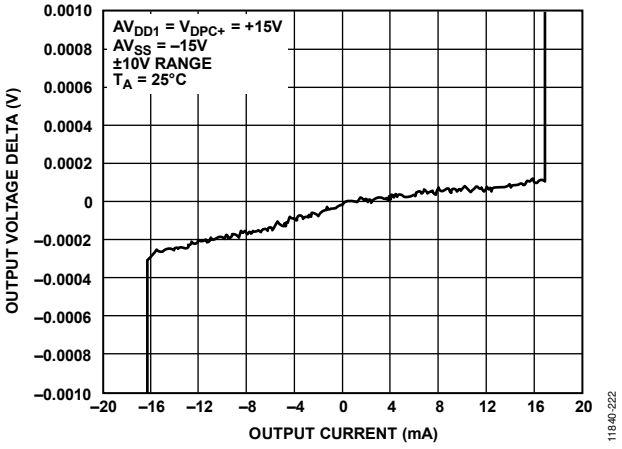


Figure 21. Sink and Source Capability of the Output Amplifier

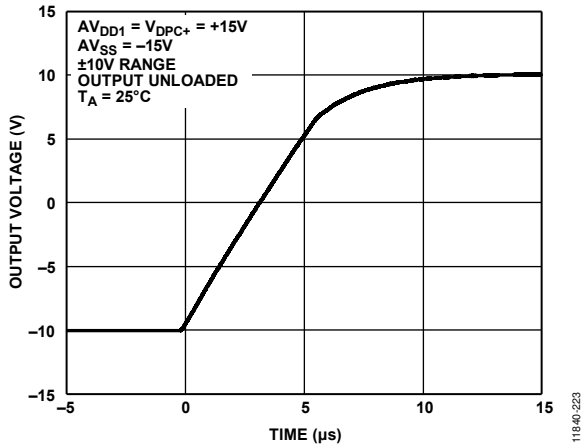


Figure 22. Full-Scale Positive Step

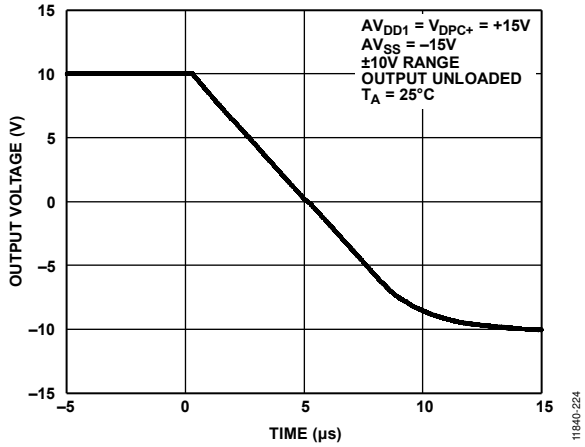


Figure 23. Full-Scale Negative Step

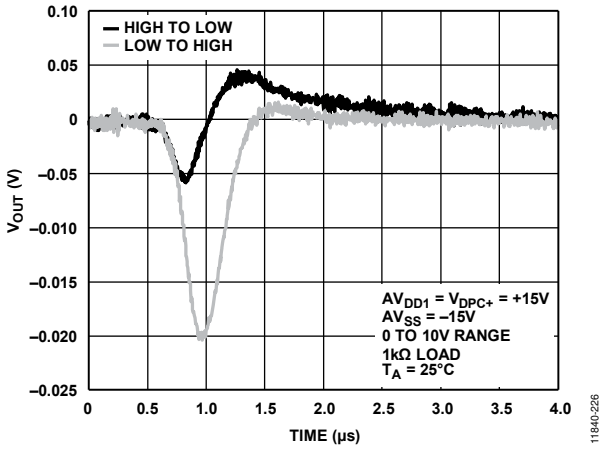


Figure 24. Digital-to-Analog Glitch Major Code Transition

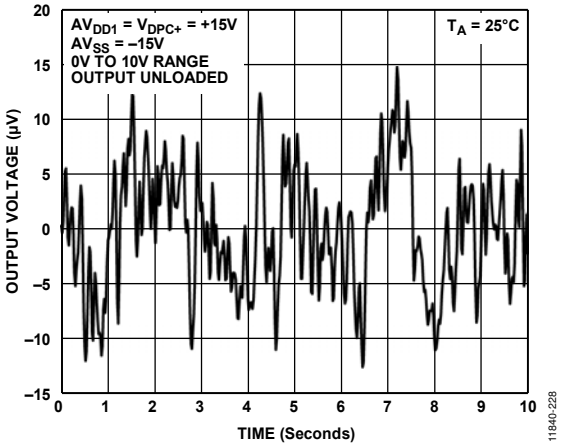


Figure 25. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

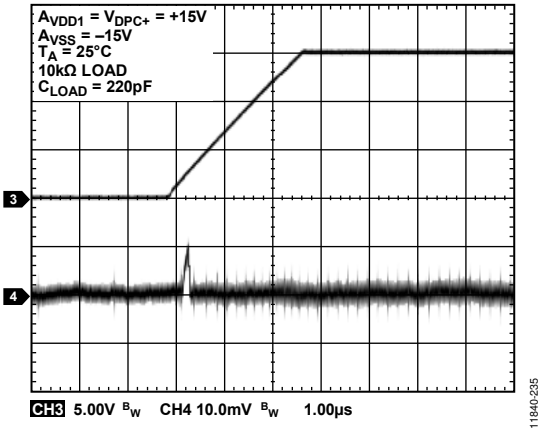


Figure 28. V_{OUT} vs. Time on Power-Up

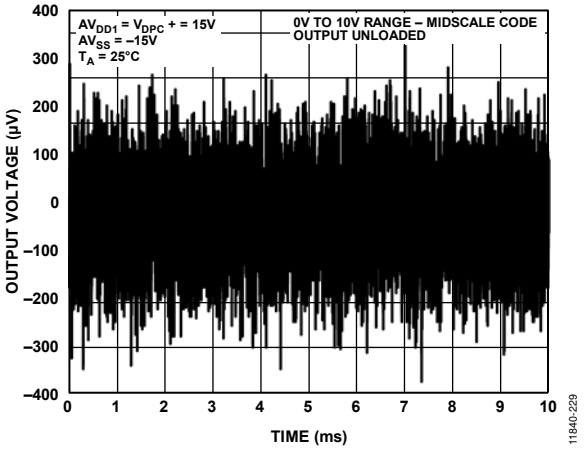


Figure 26. Peak-to-Peak Noise (100 kHz Bandwidth)

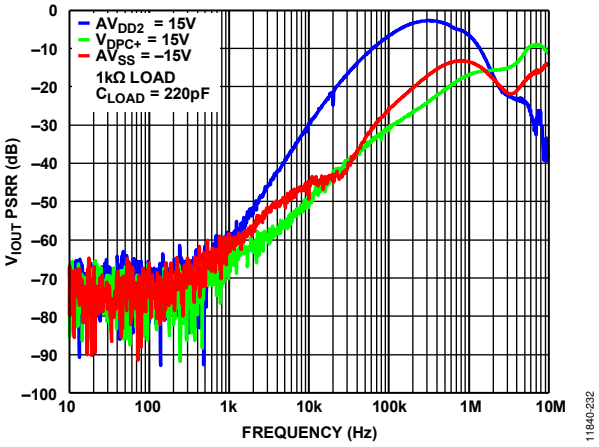


Figure 29. V_{OUT} PSRR vs. Frequency

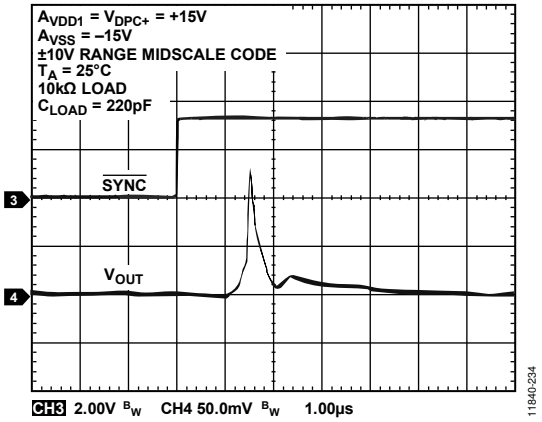


Figure 27. V_{OUT} vs. Time on Output Enable

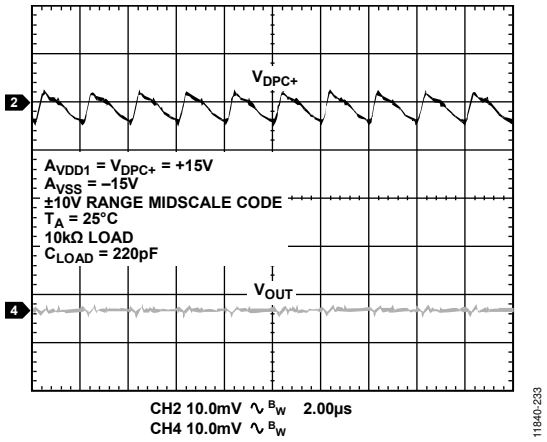


Figure 30. Voltage Output Ripple

CURRENT OUTPUTS

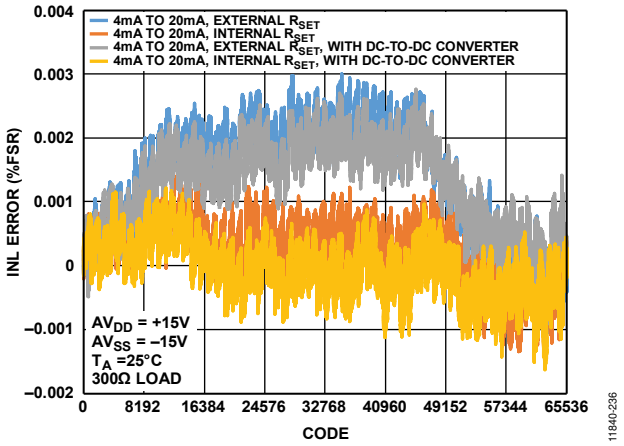


Figure 31. INL Error vs. DAC Code

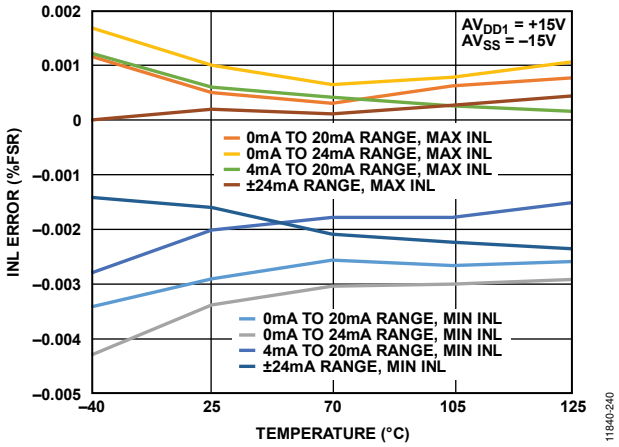


Figure 34. INL Error vs. Temperature, Internal R_{SET}

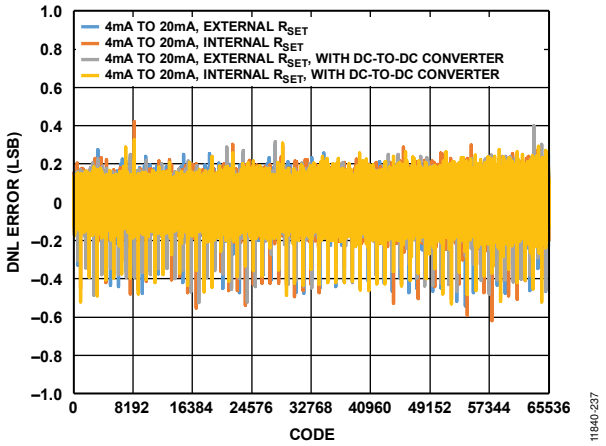


Figure 32. DNL Error vs. DAC Code

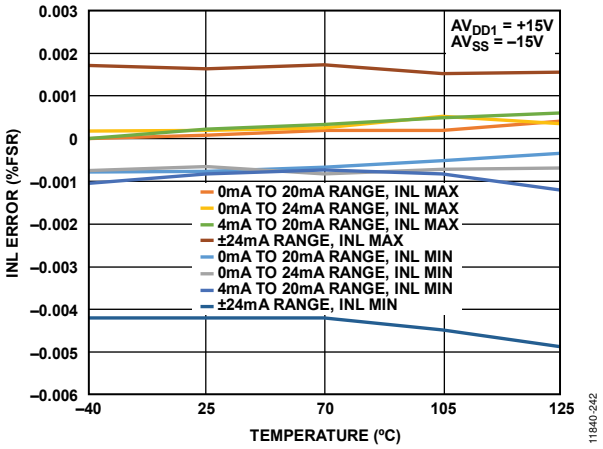


Figure 35. INL Error vs. Temperature, External R_{SET}

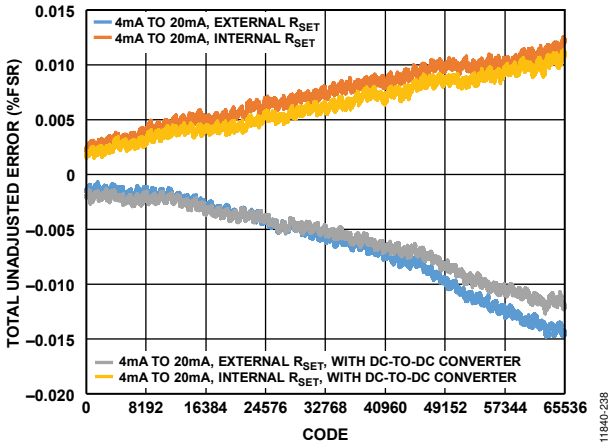


Figure 33. Total Unadjusted Error vs. DAC Code

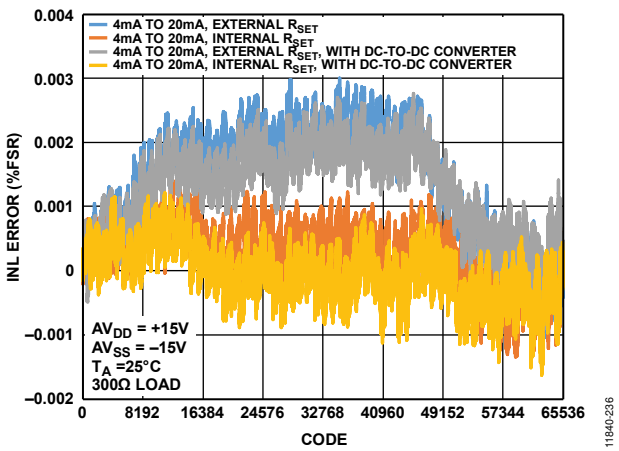


Figure 36. DNL vs. Temperature

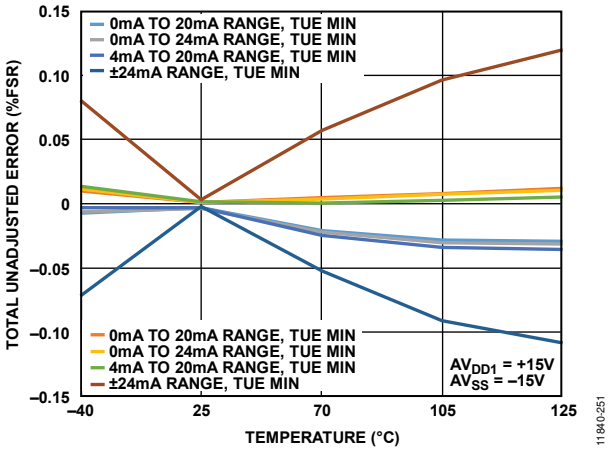


Figure 37. Total Unadjusted Error vs. Temperature, Internal R_{SET}

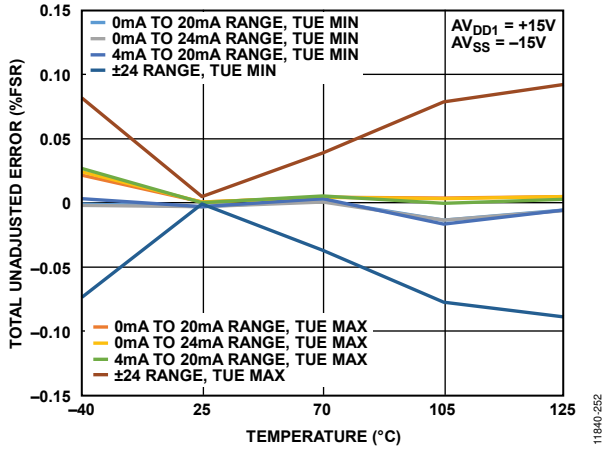


Figure 38. Total Unadjusted Error vs. Temperature, External R_{SET}

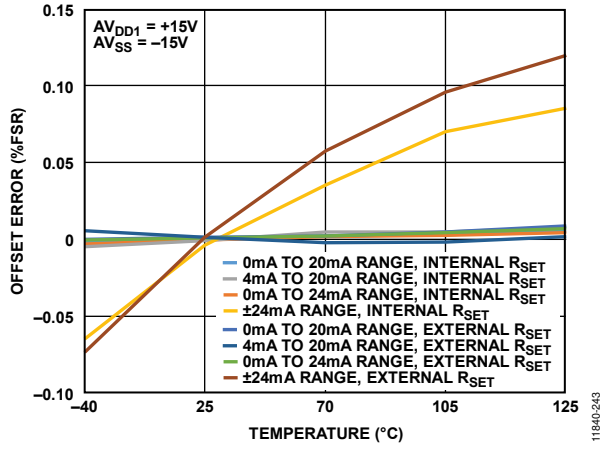


Figure 39. Offset Error vs. Temperature

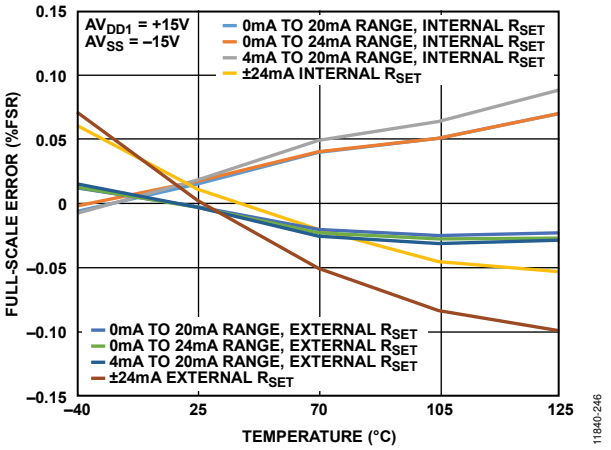


Figure 40. Full-Scale Error vs. Temperature

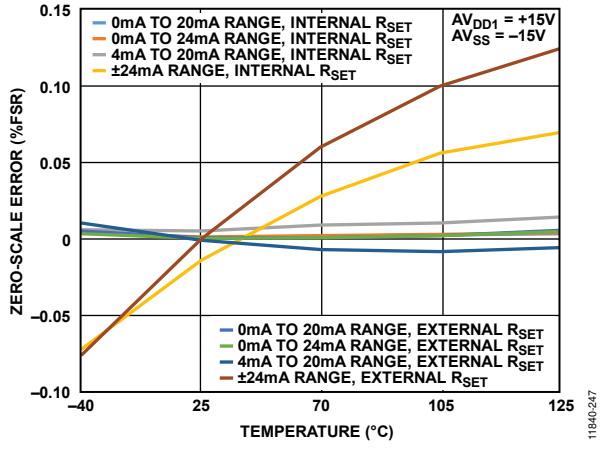


Figure 41. Zero-Scale Error vs. Temperature

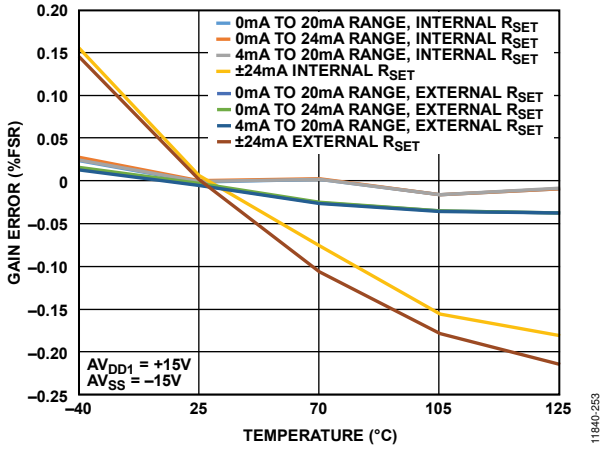


Figure 42. Gain Error vs. Temperature

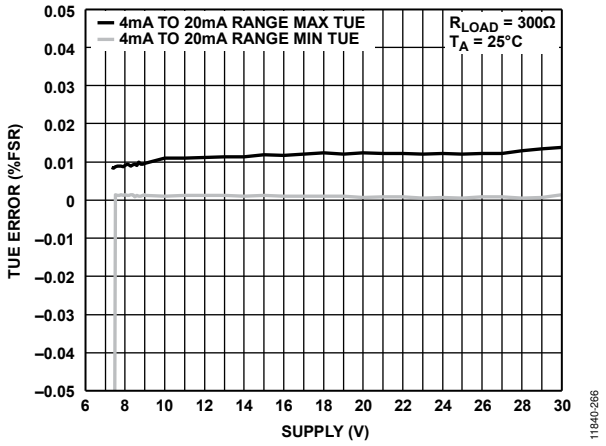


Figure 43. Total Unadjusted Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, Internal R_{SET}

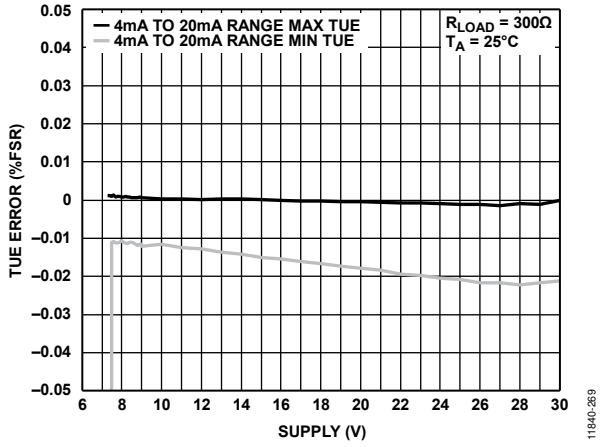


Figure 44. Total Unadjusted Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, External R_{SET}

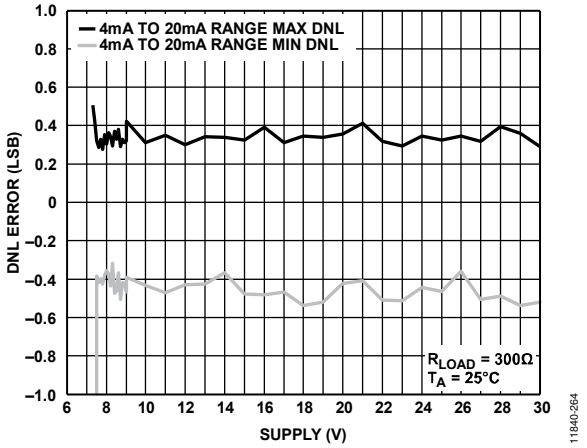


Figure 45. DNL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, Internal R_{SET}

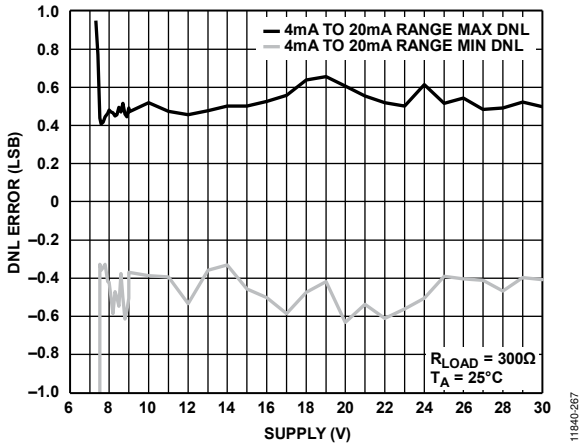


Figure 46. DNL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, External R_{SET}

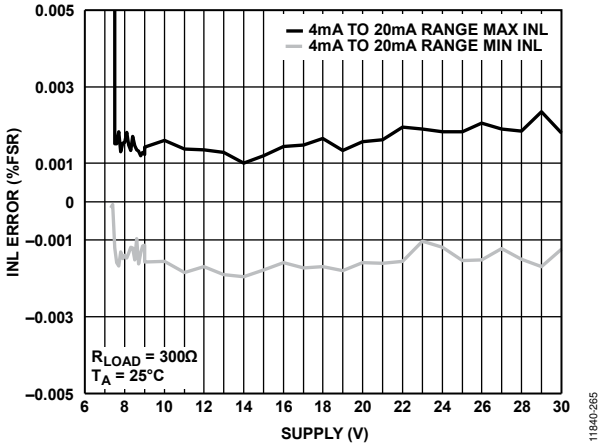


Figure 47. INL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, Internal R_{SET}

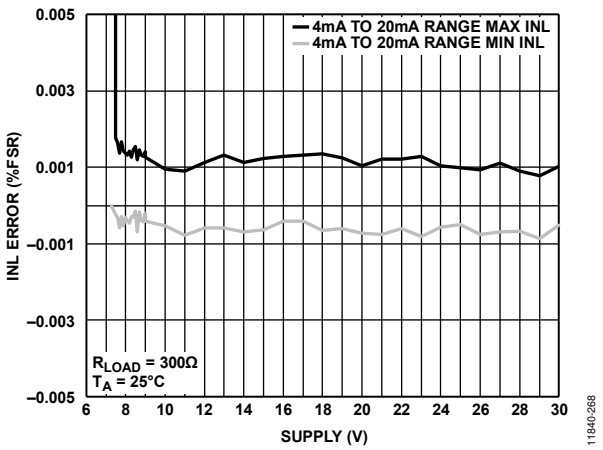


Figure 48. INL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, External R_{SET}

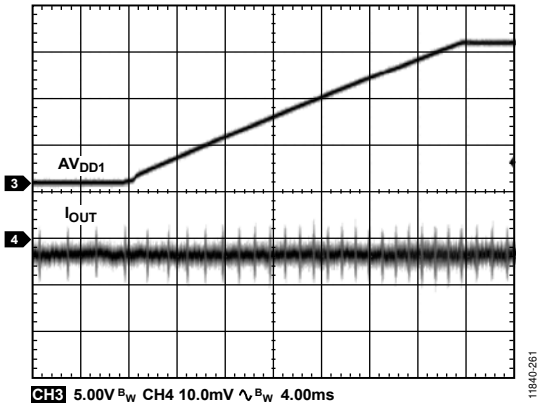


Figure 49. Output Current vs. Time on Power-Up

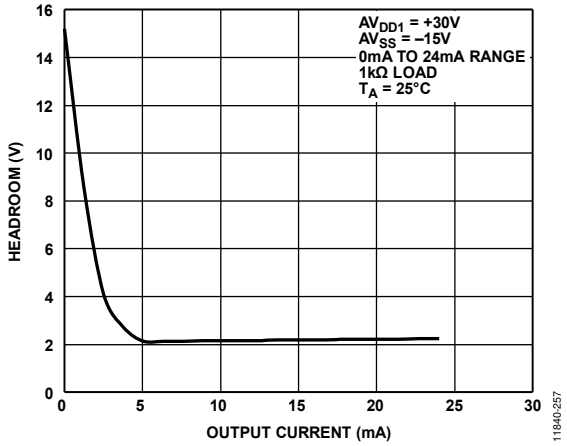


Figure 51. DC-to-DC Converter Headroom vs. Output Current

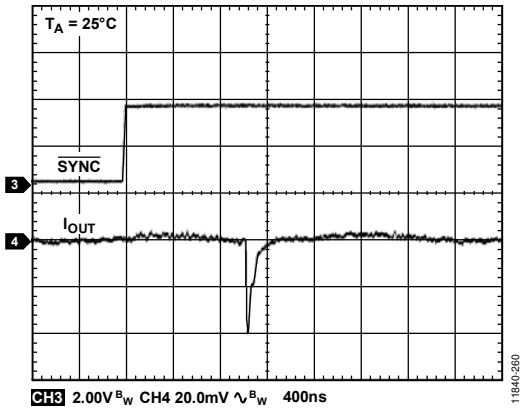


Figure 50. Output Current vs. Time on Output Enable

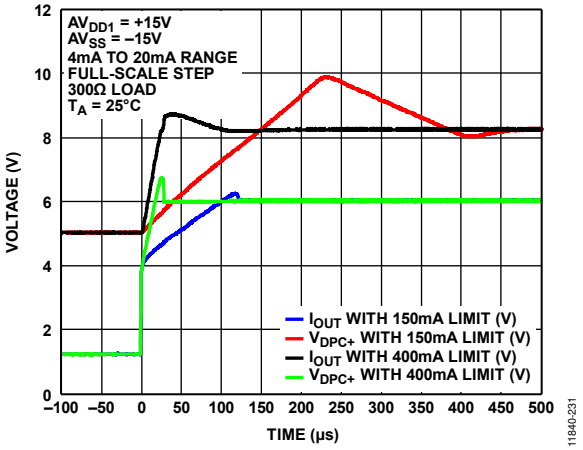


Figure 52. Output Current and V_{DPC+} Settling Time

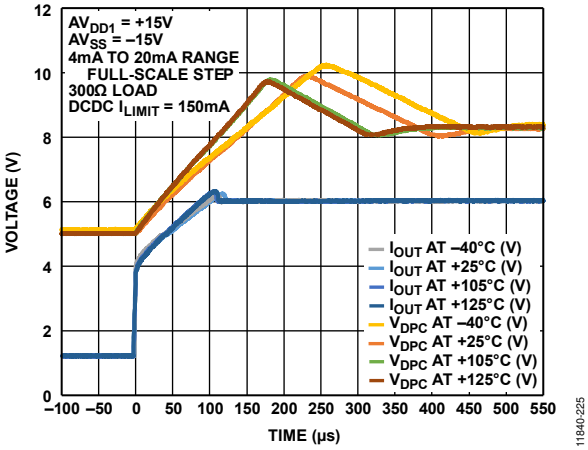


Figure 53. Output Current and V_{DPC+} Settling Time vs. Temperature

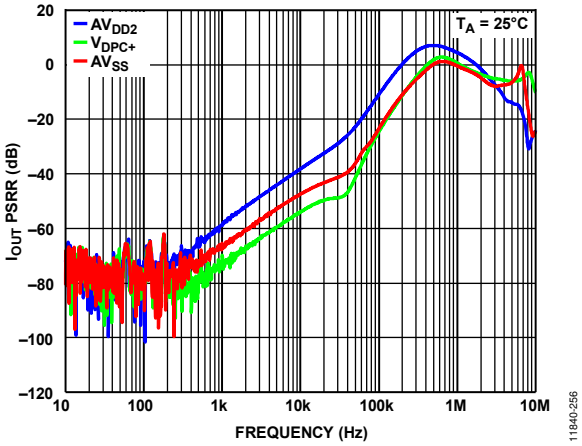


Figure 55. I_{OUT} PSRR vs. Frequency

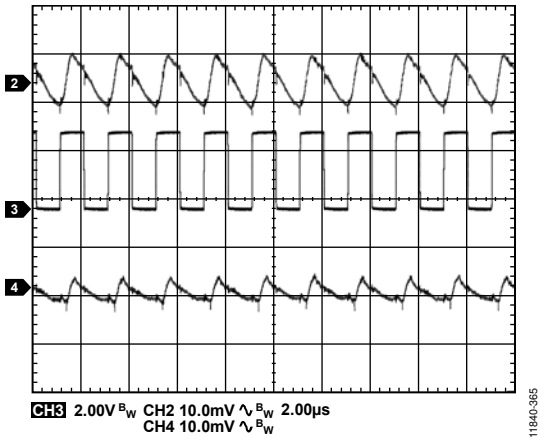


Figure 54. Output Current Ripple vs. Time with DC-to-DC Converter