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Multiple Range, 16-/12-Bit, Bipolar/Unipolar, Voltage Output DACs

Data Sheet

AD5761/AD5721

FEATURES

- 8 software-programmable output ranges: 0 V to 5 V, 0 V to 10 V, 0 V to 16 V, 0 V to 20 V, ±3 V, ±5 V, ±10 V, −2.5 V to +7.5 V; 5% overrange
- Total unadjusted error (TUE): 0.1% FSR maximum
- 16-bit resolution: ±2 LSB maximum INL
- Guaranteed monotonicity: ±1 LSB maximum
- Single channel, 16-/12-bit DACs
- Settling time: 7.5 µs typical
- Integrated reference buffers
- Low noise: 35 nV/√Hz
- Low glitch: 1 nV-sec
- 1.8 V logic compatibility
- Asynchronous updating via $\overline{\text{LDAC}}$
- Asynchronous $\overline{\text{RESET}}$ to zero scale/midscale
- DSP/microcontroller-compatible serial interface
- Robust 4 kV HBM ESD rating
- Available in 16-lead TSSOP and 16-lead LFCSP
- Operating temperature range: −40°C to +125°C

APPLICATIONS

- Industrial automation
- Instrumentation, data acquisition
- Open-/closed-loop servo control, process control
- Programmable logic controllers

GENERAL DESCRIPTION

The AD5761/AD5721 are single channel, 16-/12-bit serial input, voltage output, digital-to-analog converters (DACs). They operate from single supply voltages from 4.75 V to 30 V or dual supply voltages from −16.5 V to 0 V V_{SS} and 4.75 V to 16.5 V V_{DD}. The integrated output amplifier and reference buffer provide a very easy to use, universal solution.

The devices offer guaranteed monotonicity, integral nonlinearity (INL) of ±2 LSB maximum, 35 nV/√Hz noise, and 7.5 µs settling time on selected ranges.

The AD5761/AD5721 use a serial interface that operates at clock rates of up to 50 MHz and are compatible with DSP and microcontroller interface standards. Double buffering allows the asynchronous updating of the DAC output. The input coding is user-selectable twos complement or straight binary. The asynchronous reset function resets all registers to their default state. The output range is user selectable, via the RA[2:0] bits in the control register.

The devices available in the 16-lead TSSOP and in the 16-lead LFCSP offer guaranteed specifications over the −40°C to +125°C industrial temperature range.

Table 1. Pin-Compatible Devices

Device	Description
AD5761R/AD5721R	AD5761/AD5721 with internal reference

FUNCTIONAL BLOCK DIAGRAM

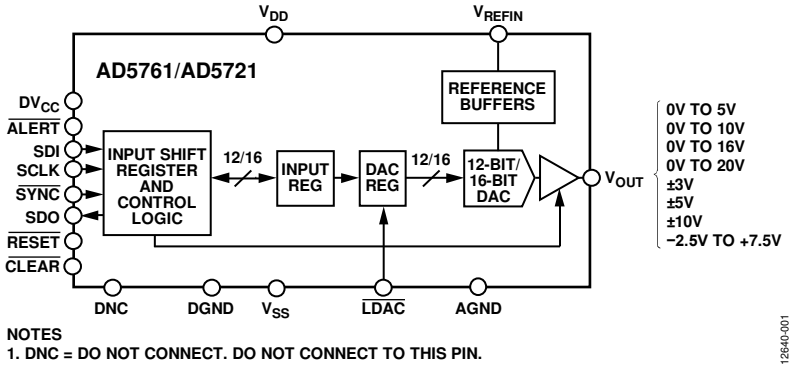

Figure 1.

Rev. B

Document Feedback

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Added Grade A Parameter, Table 2 ... 3
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1/15—Revision 0: Initial Version

SPECIFICATIONS

V_{DD}[1] = 4.75 V to 30 V, V_{SS}[1] = −16.5 V to 0 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V external, DV_{CC} = 1.7 V to 5.5 V, R_{LOAD} = 1 kΩ for all ranges except 0 V to 16 V and 0 V to 20 V for which R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[2]	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					External reference[3], outputs unloaded
Programmable Output Ranges	0		5	V	
	0		10	V	
	0		16	V	
	0		20	V	
	−2.5		+7.5	V	
	−3		+3	V	
	−5		+5	V	
	−10		+10	V	
AD5761					
Resolution	16			Bits	
Relative Accuracy, INL					
A Grade	−8		+8	LSB	External reference[3]
B Grade[4]	−2		+2	LSB	All ranges except 0 V to 16 V and 0 V to 20 V, V_{REFIN} = 2.5 V external reference
Differential Nonlinearity, DNL	−1		+1	LSB	
AD5721					
Resolution	12			Bits	
Relative Accuracy, INL					
B Grade	−0.5		+0.5	LSB	External reference[3]
Differential Nonlinearity, DNL	−0.5		+0.5	LSB	
Zero-Scale Error	−6		+6	mV	All ranges except ±10 V and 0 V to 20 V, external reference[3]
	−10		+10	mV	0 V to 20 V, ±10 V ranges, external reference[3]
Zero-Scale Temperature Coefficient (TC)[5]		±5		µV/°C	Unipolar ranges, external reference[3]
		±15		µV/°C	Bipolar ranges, external reference[3]
Bipolar Zero Error	−5		+5	mV	All bipolar ranges except ±10 V
	−7		+7	mV	±10 V output range
Bipolar Zero TC[5]		±2		µV/°C	±3 V range, external reference[3]
		±5		µV/°C	All bipolar ranges except ±3 V, external reference[3]
Offset Error	−6		+6	mV	All ranges except ±10 V and 0 V to 20 V, external reference[3]
	−10		+10	mV	0 V to 20 V, ±10 V ranges; external reference[3]
Offset Error TC[5]		±5		µV/°C	Unipolar ranges, external reference[3]
		±15		µV/°C	Bipolar ranges, external reference[3]
Gain Error	−0.1		+0.1	% FSR	External reference[3]
Gain Error TC[5]		±1.5		ppm FSR/°C	External reference[3]
Total Unadjusted Error (TUE)	−0.1		+0.1	% FSR	External reference[3]
REFERENCE INPUT[5]					
Reference Input Voltage (V_{REF})		2.5		V	±1% for specified performance
Input Current	−2	±0.5	+2	µA	
Reference Range	2		3	V	
OUTPUT CHARACTERISTICS[5]					
Output Voltage Range	$-V_{OUT}$		$+V_{OUT}$		Refer to Table 7 for the different output voltage ranges available
	−10		+10	V	V_{DD}/V_{SS} = ±11 V, ±10 V output range
	−10.5		+10.5	V	V_{DD}/V_{SS} = ±11 V, ±10 V output range with 5% overrange

Parameter[2]	Min	Typ	Max	Unit	Test Conditions/Comments
Capacitive Load Stability			1	nF	
Headroom		0.5	1	V	R_{LOAD} = 1 kΩ for all ranges except 0 V to16 V and 0 V to 20 V ranges (R_{LOAD} = 2 kΩ)
Output Voltage TC		±3		ppm FSR/°C	±10 V range, external reference
Short-Circuit Current		25		mA	Short on the V_{OUT} pin
Resistive Load			1	kΩ	All ranges except 0 V to16 V and 0 V to 20 V
			2	kΩ	0 V to16 V, 0 V to 20 V ranges
Load Regulation		0.3		mV/mA	Outputs unloaded
DC Output Impedance		0.5		Ω	Outputs unloaded
LOGIC INPUTS[5]					DV_{CC} = 1.7 V to 5.5 V, JEDEC compliant
Input Voltage					
High, V_{IH}	0.7 × DV_{CC}			V	
Low, V_{IL}			0.3 × DV_{CC}	V	
Input Current					
Leakage Current	−1		+1	µA	SDI, SCLK, $\overline{SYNC}$
	−1		+1	µA	$\overline{LDAC}$, $\overline{CLEAR}$, $\overline{RESET}$ pins held high
	−55			µA	$\overline{LDAC}$, $\overline{CLEAR}$, $\overline{RESET}$ pins held low
Pin Capacitance		5		pF	Per pin, outputs unloaded
LOGIC OUTPUTS (SDO, $\overline{ALERT}$)[5]					
Output Voltage					
Low, V_{OL}			0.4	V	DV_{CC} = 1.7 V to 5.5 V, sinking 200 µA
High, V_{OH}	DVCC − 0.5			V	DV_{CC} = 1.7 V to 5.5 V, sourcing 200 µA
High Impedance, SDO Pin					
Leakage Current	−1		+1	µA	
Pin Capacitance		5		pF	
POWER REQUIREMENTS					
V_{DD}	4.75		30	V	
V_{SS}	−16.5		0	V	
DV_{CC}	1.7		5.5	V	
I_{DD}		5.1	6.5	mA	Outputs unloaded, external reference
I_{SS}		1	3	mA	Outputs unloaded
DI_{CC}		0.005	1	µA	V_{IH} = DV_{CC}, V_{IL} = DGND
Power Dissipation		67.1		mW	±11 V operation, outputs unloaded
DC Power Supply Rejection Ratio (PSRR)[5]		0.1		mV/V	V_{DD} ± 10%, V_{SS} = −15 V
		0.1		mV/V	V_{SS} ±10%, V_{DD} = +15 V
AC PSRR[5]		80		dB	V_{DD} ±200 mV, 50 Hz/60 Hz, V_{SS} = −15 V; external reference; C_{LOAD} = unloaded
		80		dB	V_{SS} ±200 mV, 50 Hz/60 Hz, V_{DD} = +15 V; external reference; C_{LOAD} = unloaded

[1] For specified performance, headroom requirement is 1 V.
[2] Temperature range: −40°C to +125°C, typical at +25°C.
[3] External reference means 2 V to 2.85 V with overrange and 2 V to 3 V without overrange.
[4] Integral nonlinearity error is specified at ±4 LSB (minimum/maximum) for 0 V to 16 V and 0 V to 20 V ranges with V_{REFIN} = 2.5 V external reference, and for all ranges with V_{REFIN} = 2 V to 2.85 V with overrange and 2 V to 3 V without overrange.
[5] Guaranteed by design and characterization, not production tested.

AC PERFORMANCE CHARACTERISTICS

V_{DD}[1] = 4.75 V to 30 V, V_{SS}[1]= −16.5 V to 0 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V external, DV_{CC} = 1.7 V to 5.5 V, R_{LOAD} = 1 kΩ for all ranges except 0 V to 16 V and 0 V to 20 V for which R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[2]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[3]					
Output Voltage Settling Time		9	12.5	µs	20 V step to 1 LSB at 16-bit resolution
		7.5	8.5	µs	10 V step to 1 LSB at 16-bit resolution
			5	µs	512 LSB step to 1 LSB at 16-bit resolution
Digital-to-Analog Glitch Impulse		8		nV-sec	±10 V range
		1		nV-sec	0 V to 5 V range
Glitch Impulse Peak Amplitude		15		mV	±10 V range
		10		mV	0 V to 5 V range
Power-On Glitch		100		mV p-p	
Digital Feedthrough		0.6		nV-sec	
Output Noise					
0.1 Hz to 10 Hz Bandwidth (BW)		15		µV p-p	
100 kHz BW		45		µV rms	0 V to 20 V and 0 V to 16 V ranges, 2.5 V external reference
		35		µV rms	0 V to 10 V, ±10 V, −2.5 V to +7.5 V ranges, 2.5 V external reference
		25		µV rms	±5 V range, 2.5 V external reference
		15		µV rms	+5 V, ±3 V ranges; 2.5 V external reference
Output Noise Spectral Density (at 10 kHz)		80		nV/√Hz	±10 V range, 2.5 V external reference
		35		nV/√Hz	±3 V range, 2.5 V external reference
		70		nV/√Hz	±5 V, 0 V to 10 V, and −2.5 V to +7.5 V ranges; 2.5 V external reference
		110		nV/√Hz	0 V to 20 V range, 2.5 V external reference
		90		nV/√Hz	0 V to 16 V range, 2.5 V external reference
		45		nV/√Hz	0 V to 5 V range, 2.5 V external reference
Total Harmonic Distortion (THD)[4]		−87		dB	2.5 V external reference, 1 kHz tone
Signal-to-Noise Ratio (SNR)		92		dB	At ambient, 2.5 V external reference, BW = 20 kHz, f_{OUT} = 1 kHz
Peak Harmonic or Spurious Noise (SFDR)		92		dB	At ambient, 2.5 V external reference, BW = 20 kHz, f_{OUT} = 1 kHz
Signal-to-Noise-and-Distortion (SINAD) Ratio		85		dB	At ambient, 2.5 V external reference, BW = 20 kHz, f_{OUT} = 1 kHz

[1] For specified performance, headroom requirement is 1 V.
[2] Temperature range: −40°C to +125°C, typical at +25°C.
[3] Guaranteed by design and characterization; not production tested.
[4] Digitally generated sine wave at 1 kHz.

TIMING CHARACTERISTICS

DV_{CC} = 1.7 V to 5.5 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Description
t_1[1]	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	15	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	10	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge time
t_6	20	ns min	Minimum $\overline{SYNC}$ high time (write mode)
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	10	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ falling edge
t_{10}	20	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{11}	20	ns min	$\overline{LDAC}$ pulse width low
t_{12}	9	µs typ	DAC output settling time, 20 V step to 1 LSB at 16-bit resolution (see Table 3)
	7.5	µs typ	DAC output settling time, 10 V step to 1 LSB at 16-bit resolution
t_{13}	20	ns min	$\overline{CLEAR}$ pulse width low
t_{14}	200	ns typ	$\overline{CLEAR}$ pulse activation time
t_{15}	10	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
t_{16}	40	ns max	SCLK rising edge to SDO valid (C_{L_SDO} = 15 pF, where C_{L_SDO} is the capacitive load on the SDO output)
t_{17}	50	ns min	Minimum $\overline{SYNC}$ high time (readback/daisy-chain mode)

[1] Maximum SCLK frequency is 50 MHz for write mode and 33 MHz for readback mode.

Timing Diagrams

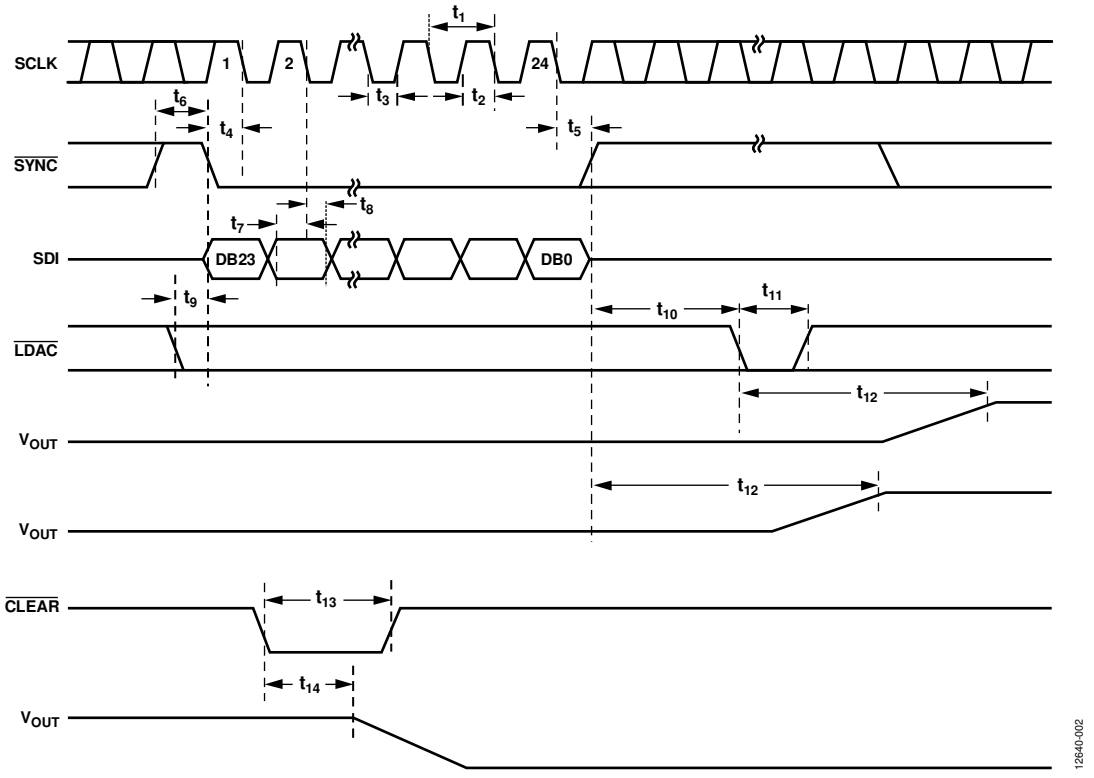


Figure 2. Serial Interface Timing Diagram

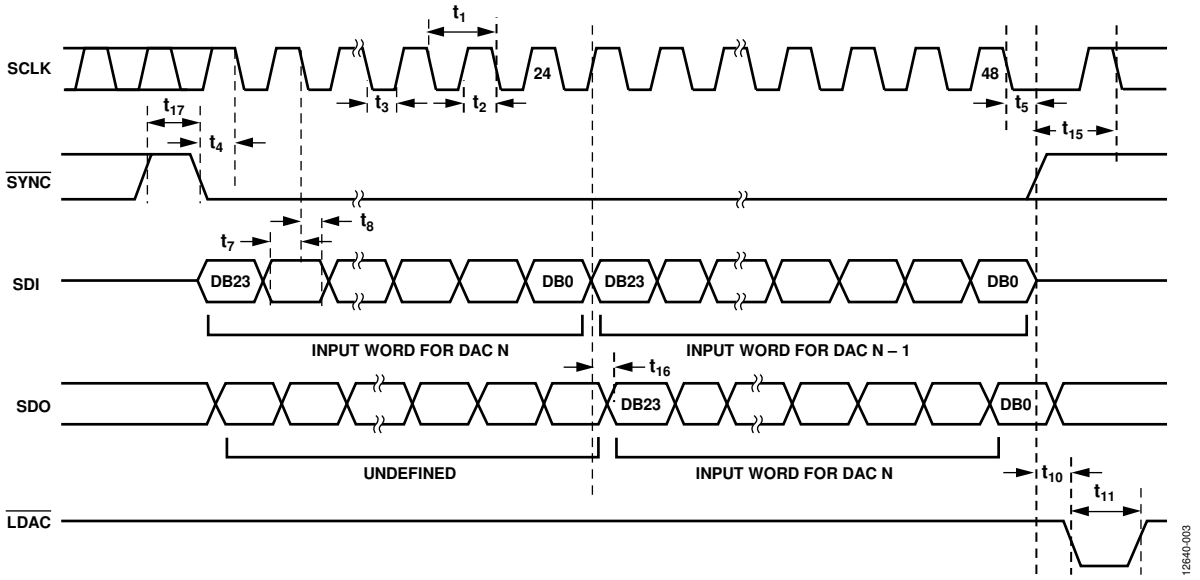


Figure 3. Daisy-Chain Timing Diagram

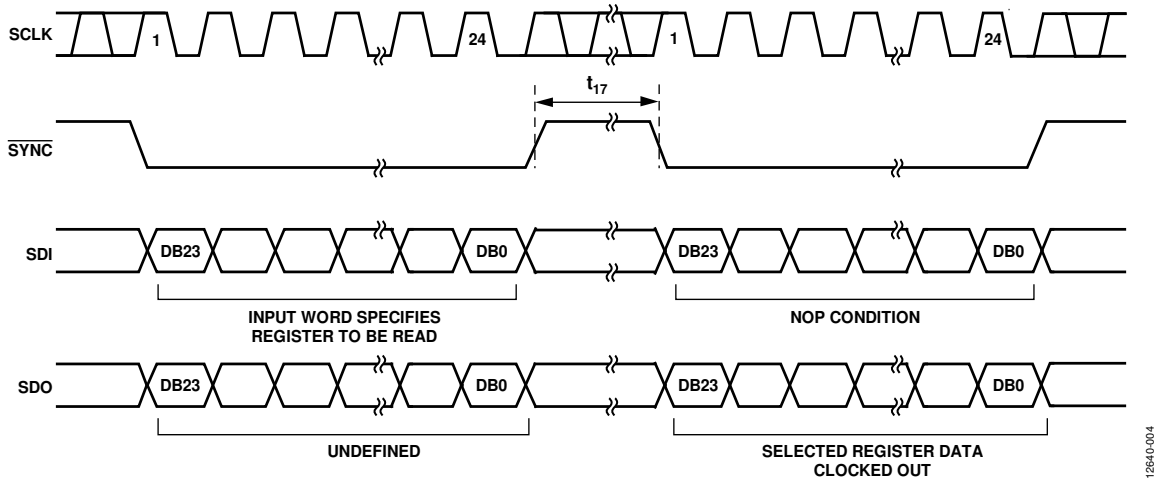


Figure 4. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 200 mA do not cause silicon controlled rectifier (SCR) latch-up.

Table 5.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +34 V
V_{SS} to AGND	+0.3 V to −17 V
V_{DD} to V_{SS}	−0.3 V to +34 V
DV_{CC} to DGND	−0.3 V to +7 V
Digital Inputs[1] to DGND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital Outputs[2] to DGND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
V_{REFIN} to DGND	−0.3 V to +7 V
V_{OUT} to AGND	V_{SS} to V_{DD}
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range, T_A Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature, $T_{J\,MAX}$	150°C
Thermal Impedance	
16-Lead TSSOP	
θ_{JA}	113°C/W[3]
θ_{JC}	28°C/W
16-Lead LFCSP	
θ_{JA}	75°C/W[3]
θ_{JC}	4.5°C/W[4]
Power Dissipation	$(T_{J\,MAX} - T_A)/\theta_{JA}$
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD (Human Body Model)	4 kV

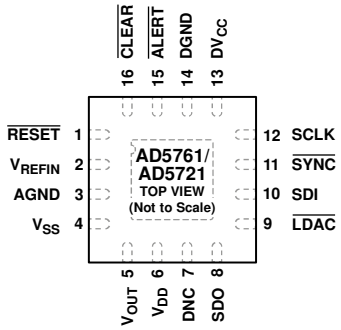
[1] The digital inputs include $\overline{\text{CLEAR}}$, $\overline{\text{RESET}}$, SCLK, $\overline{\text{SYNC}}$, SDI, and $\overline{\text{LDAC}}$.
[2] The digital outputs include $\overline{\text{ALERT}}$ and SDO.
[3] JEDEC 2S2P test board, still air (0 m/sec airflow).
[4] Measured to exposed paddle, with infinite heat sink on package top surface.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

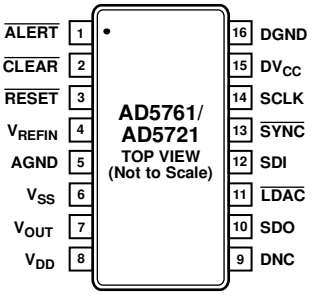
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.
2. EXPOSED PAD. ENSURE THAT THE EXPOSED PAD IS MECHANICALLY CONNECTED TO A PCB COPPER PLANE FOR OPTIMAL THERMAL PERFORMANCE. THE EXPOSED PAD CAN BE LEFT ELECTRICALLY FLOATING.

12640-106

Figure 5. LFCSP Pin Configuration



DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

12640-006

Figure 6. TSSOP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
LFCSP	**TSSOP**	**Mnemonic**	**Description**
1	3	$\overline{\text{RESET}}$	Active Low Reset Input. Asserting this pin returns the AD5761/AD5721 to their default power-on status where the output is clamped to ground and the output buffer is powered down. This pin can be left floating because there is an internal pull-up resistor.
2	4	V_{REFIN}	External Reference Voltage Input. For specified performance, V_{REFIN} = 2.5 V.
3	5	AGND	Ground Reference for Analog Circuitry.
4	6	V_{SS}	Negative Analog Supply Connection. A voltage in the range of −16.5 V to 0 V can be connected to this pin. For unipolar output ranges, connect this pin to 0 V. V_{SS} must be decoupled to AGND.
5	7	V_{OUT}	Analog Output Voltage of the DAC. The output amplifier is capable of directly driving a 2 kΩ, 1 nF load.
6	8	V_{DD}	Positive Analog Supply Connection. A voltage in the range of 4.75 V to 30 V can be connected to this pin for unipolar output ranges. Bipolar output ranges accept a voltage in the range of 4.75 V to 16.5 V. V_{DD} must be decoupled to AGND.
7	9	DNC	Do Not Connect. Do not connect to this pin.
8	10	SDO	Serial Data Output. This pin clocks data from the serial register in daisy-chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
9	11	$\overline{\text{LDAC}}$	Load DAC. This logic input updates the DAC register and, consequently, the analog output. When tied permanently low, the DAC register is updated when the input register is updated. If $\overline{\text{LDAC}}$ is held high during the write to the input register, the DAC output register is not updated, and the DAC output update is held off until the falling edge of $\overline{\text{LDAC}}$. This pin can be left floating because there is an internal pull-up resistor.
10	12	SDI	Serial Data Input. Data must be valid on the falling edge of SCLK.
11	13	$\overline{\text{SYNC}}$	Active Low Synchronization Input. This pin is the frame synchronization signal for the serial interface. While $\overline{\text{SYNC}}$ is low, data is transferred in on the falling edge of SCLK. Data is latched on the rising edge of $\overline{\text{SYNC}}$.
12	14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This pin operates at clock speeds of up to 50 MHz.
13	15	DV_{CC}	Digital Supply. The voltage range is from 1.7 V to 5.5 V. The applied voltage sets the voltage at which the digital interface operates.
14	16	DGND	Digital Ground.
15	1	$\overline{\text{ALERT}}$	Active Low Alert. This pin is asserted low when the die temperature exceeds approximately 150°C, or when an output short circuit or a brownout occurs. This pin is also asserted low during power-up, a full software reset, or a hardware reset, for which a write to the control register asserts the pin high.
16	2	$\overline{\text{CLEAR}}$	Falling Edge Clear Input. Asserting this pin sets the DAC register to zero-scale, midscale, or full-scale code (user selectable) and updates the DAC output. This pin can be left floating because there is an internal pull-up resistor.
17	N/A[1]	EPAD	Exposed Pad. Ensure that the exposed pad is mechanically connected to a PCB copper plane for optimal thermal performance. The exposed pad can be left electrically floating.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERSTICS

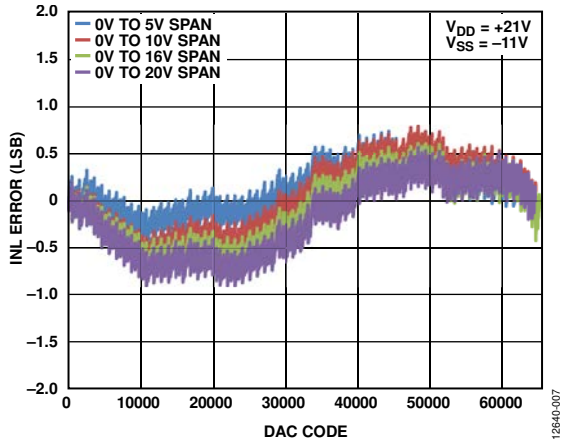


Figure 7. AD5761 INL Error vs. DAC Code, Unipolar Output

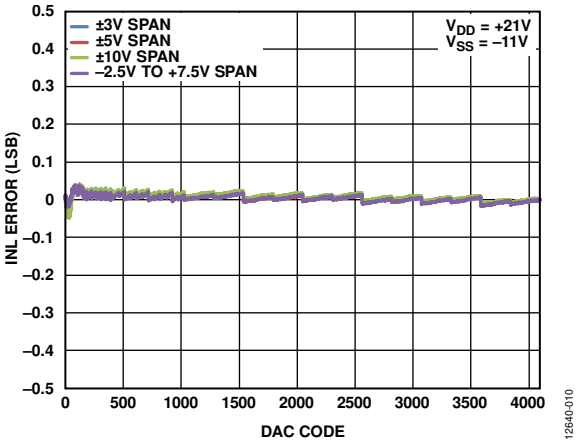


Figure 10. AD5721 INL Error vs. DAC Code, Bipolar Output

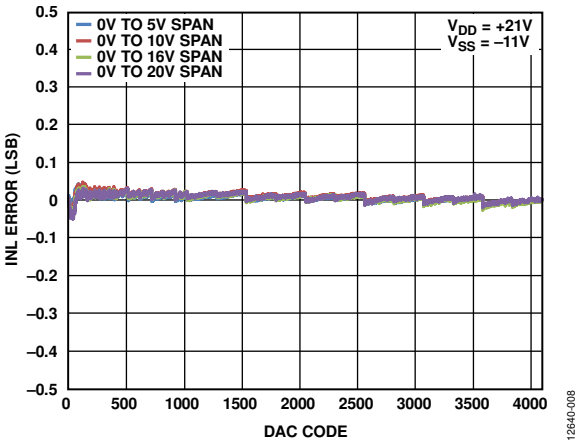


Figure 8. AD5721 INL Error vs. DAC Code, Unipolar Output

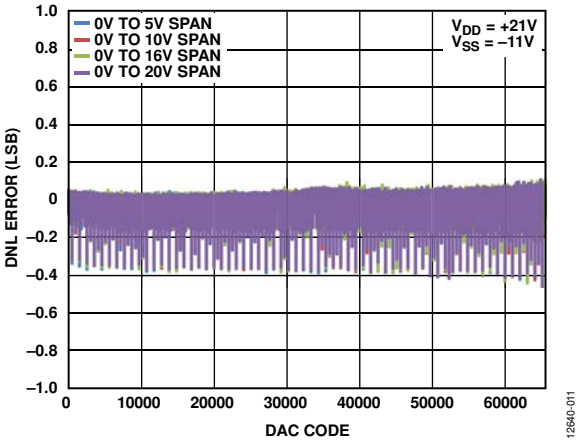


Figure 11. AD5761 DNL Error vs. DAC Code, Unipolar Output

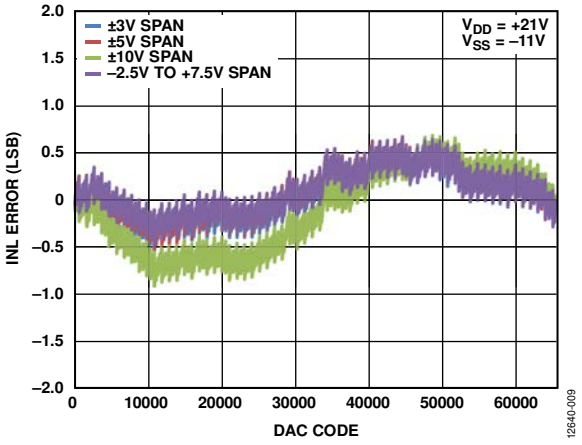


Figure 9. AD5761 INL Error vs. DAC Code, Bipolar Output

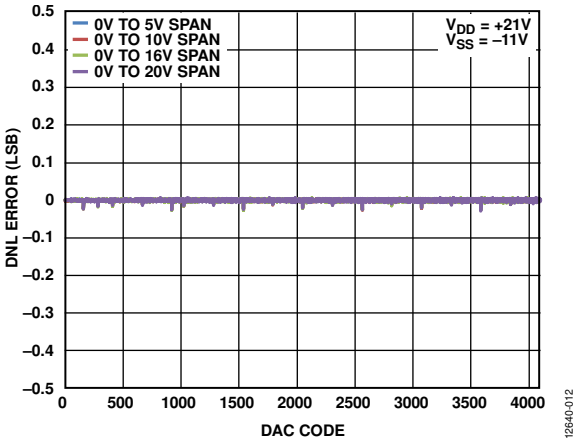


Figure 12. AD5721 DNL Error vs. DAC Code, Unipolar Output

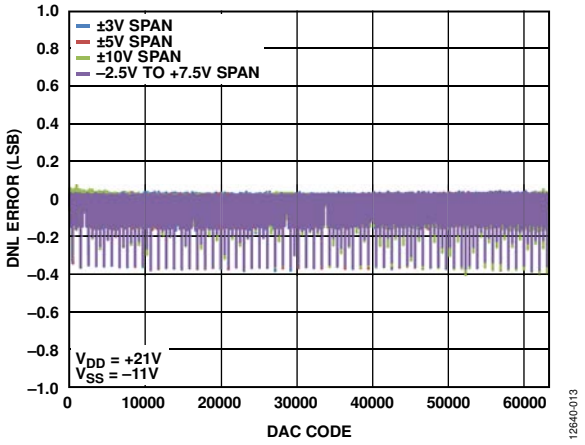


Figure 13. AD5761 DNL Error vs. DAC Code, Bipolar Output

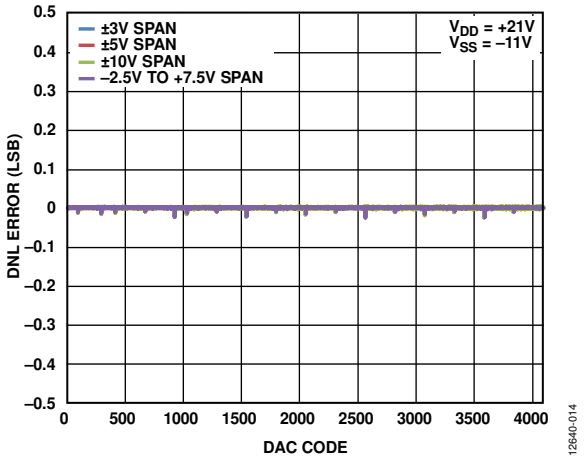


Figure 14. AD5721 DNL Error vs. DAC Code, Bipolar Output

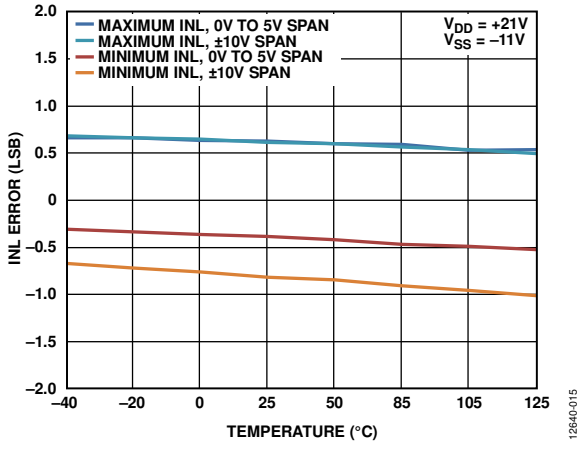


Figure 15. INL Error vs. Temperature

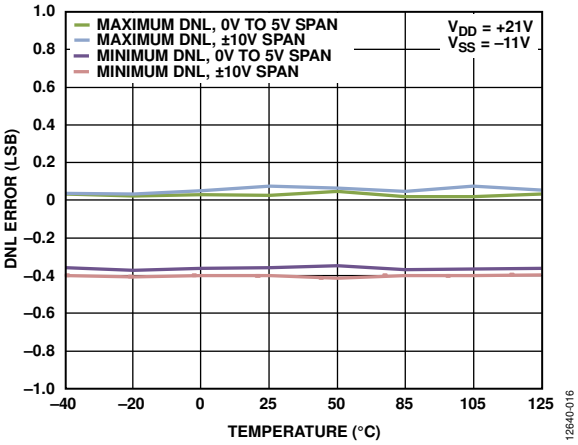


Figure 16. DNL Error vs. Temperature

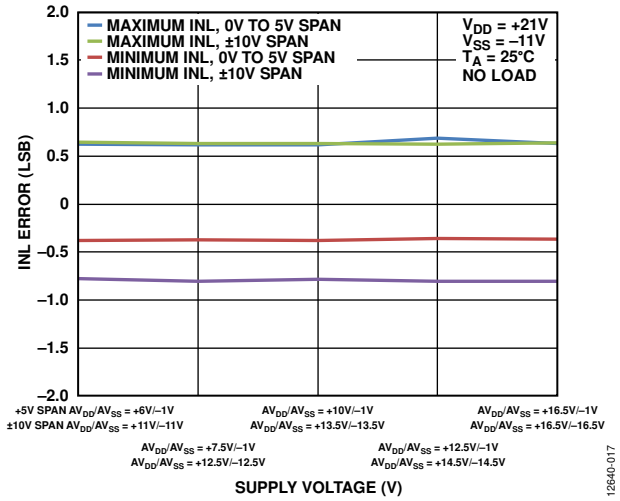


Figure 17. INL Error vs. Supply Voltage

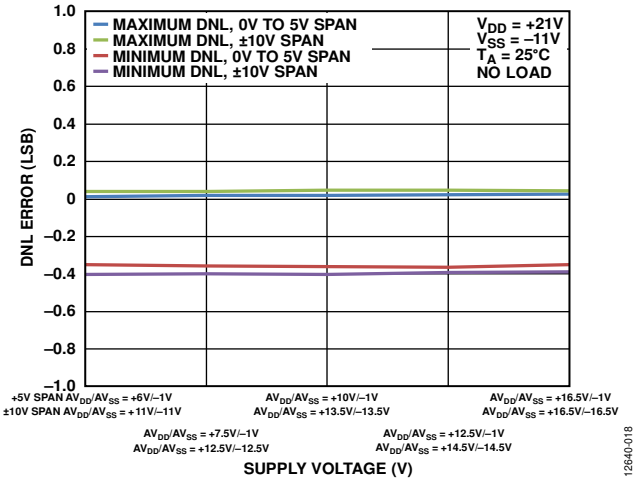


Figure 18. DNL Error vs. Supply Voltage

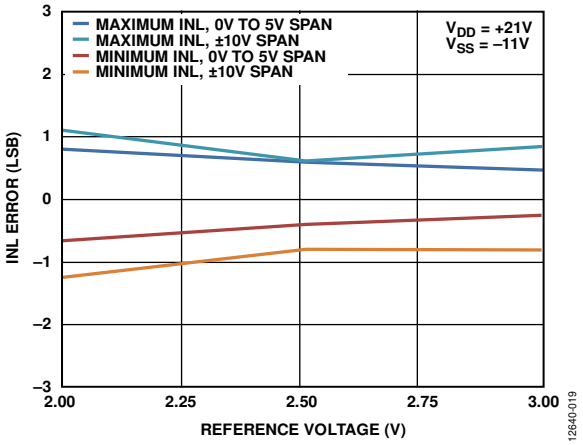


Figure 19. INL Error vs. Reference Voltage

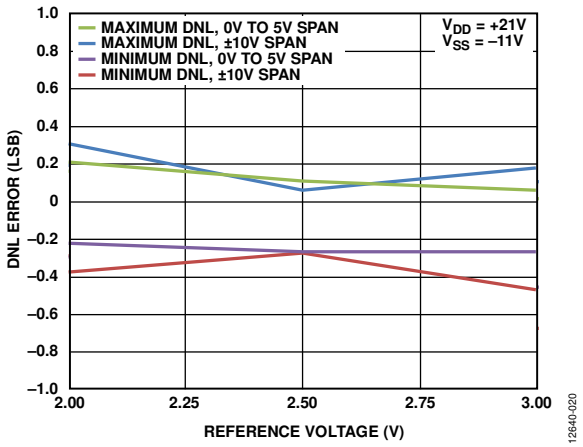


Figure 20. DNL Error vs. Reference Voltage

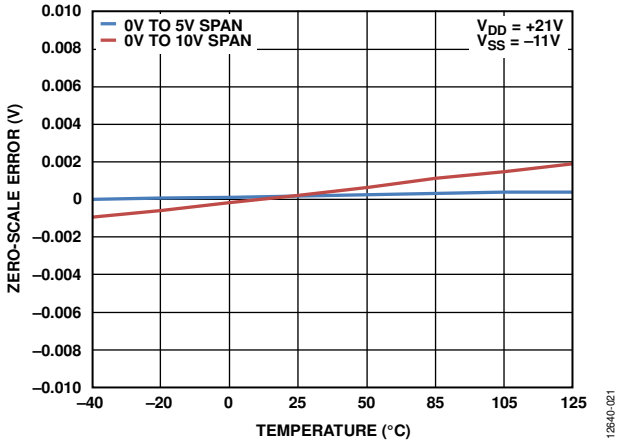


Figure 21. Zero-Scale Error vs. Temperature

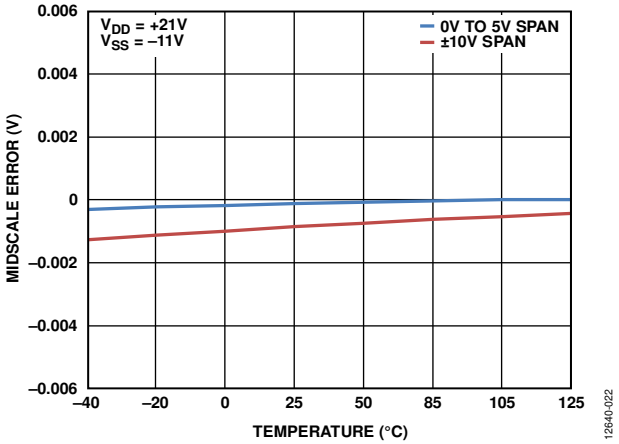


Figure 22. Midscale Error vs. Temperature

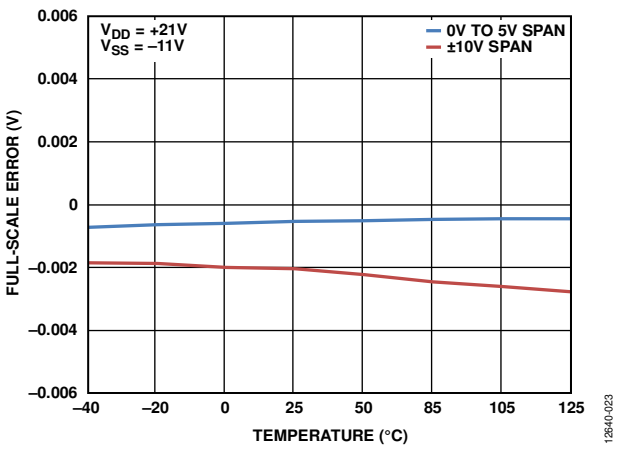


Figure 23. Full-Scale Error vs. Temperature

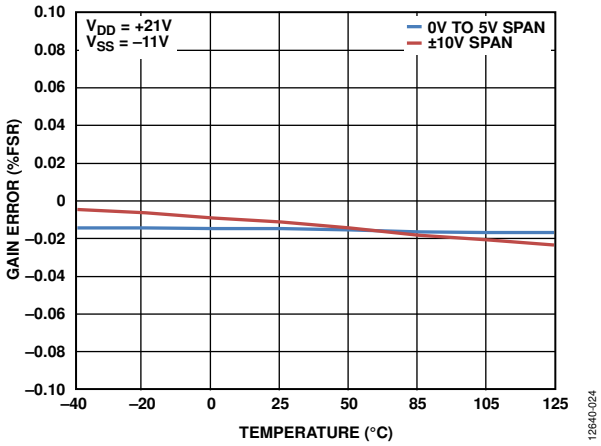


Figure 24. Gain Error vs. Temperature

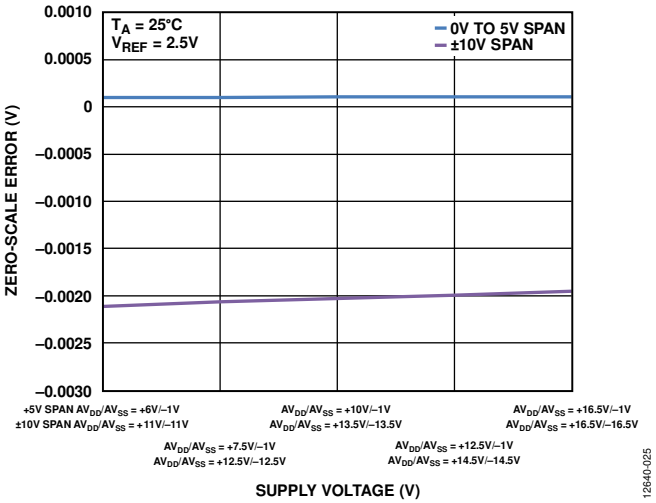


Figure 25. Zero-Scale Error vs. Supply Voltage

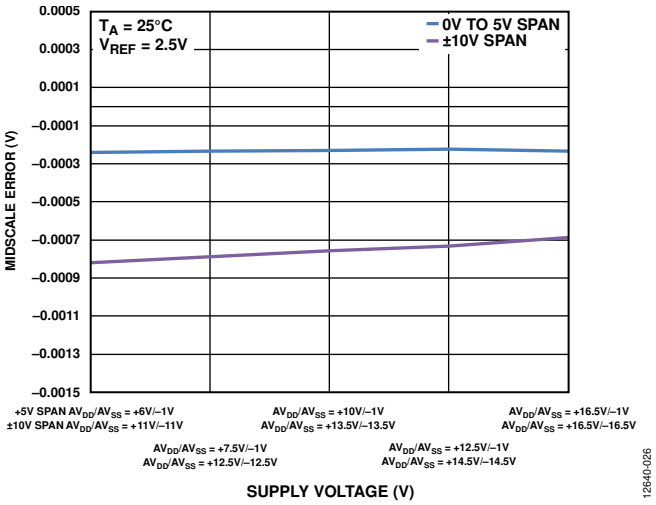


Figure 26. Midscale Error vs. Supply Voltage

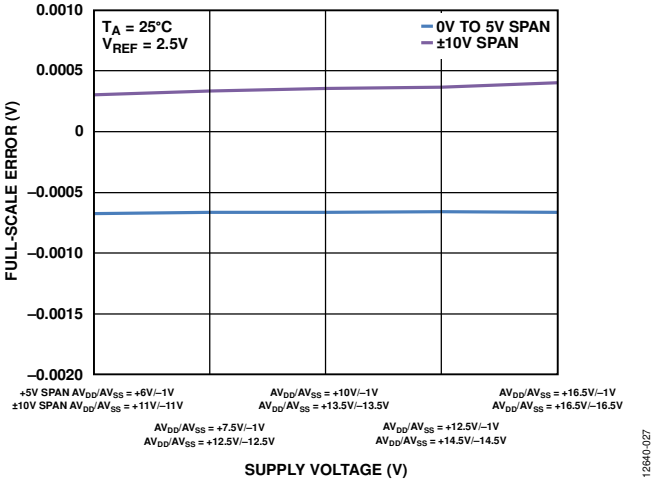


Figure 27. Full-Scale Error vs. Supply Voltage

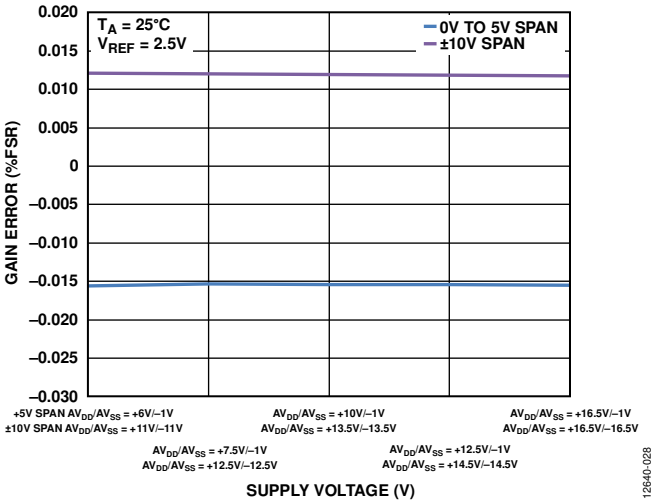


Figure 28. Gain Error vs. Supply Voltage

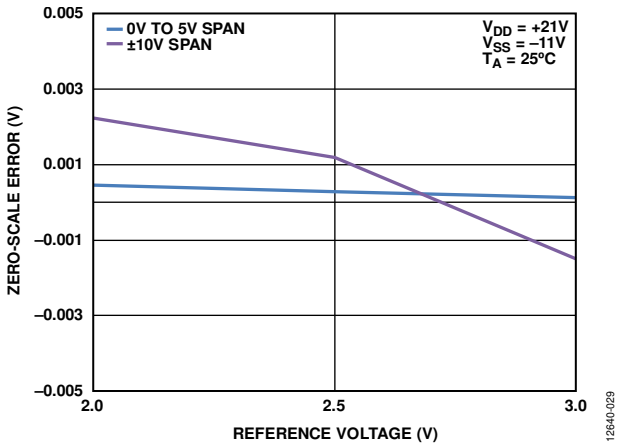


Figure 29. Zero-Scale Error vs. Reference Voltage

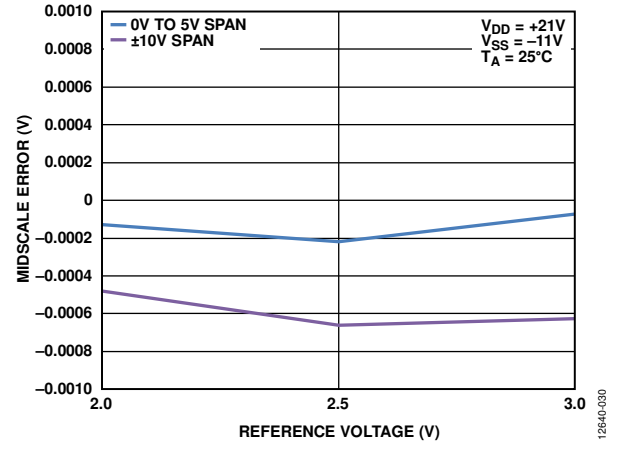


Figure 30. Midscale Error vs. Reference Voltage

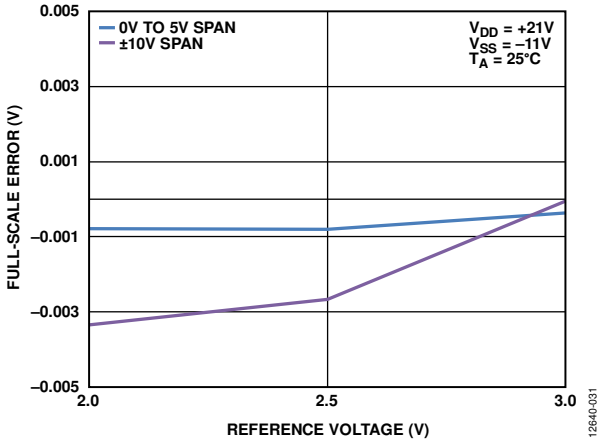


Figure 31. Full-Scale Error vs. Reference Voltage

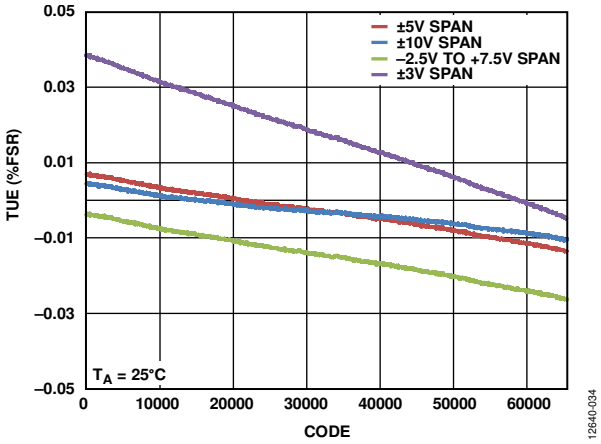


Figure 34. TUE vs. Code, Bipolar Output

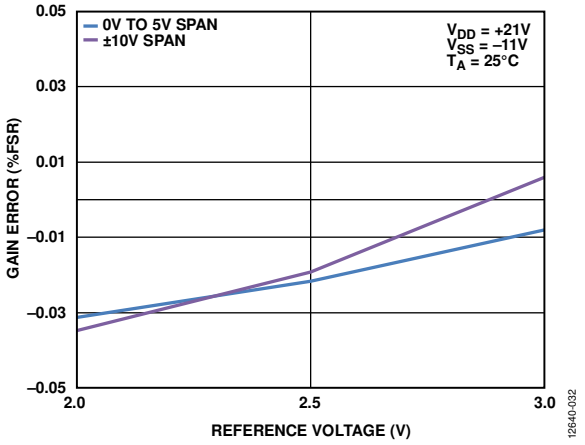


Figure 32. Gain Error vs. Reference Voltage

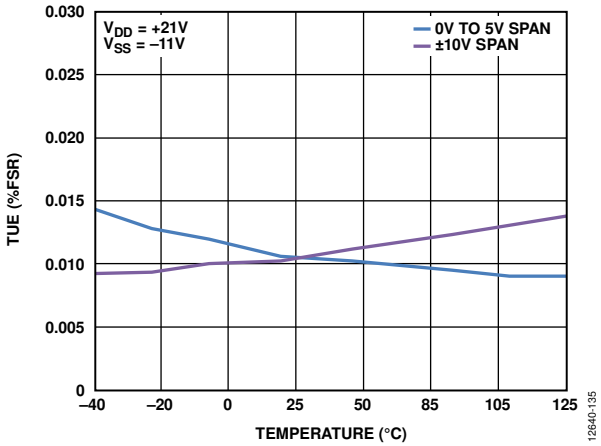


Figure 35. TUE vs. Temperature

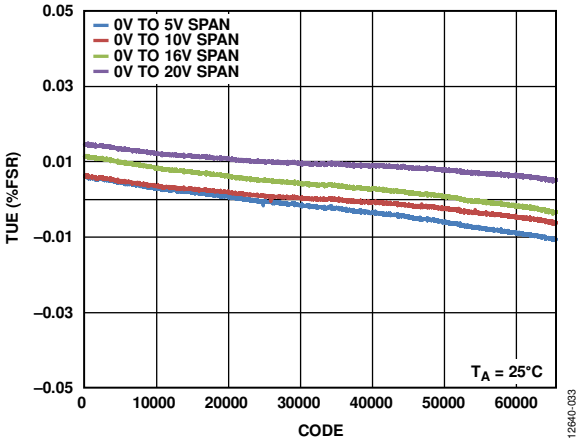


Figure 33. TUE vs. Code, Unipolar Output

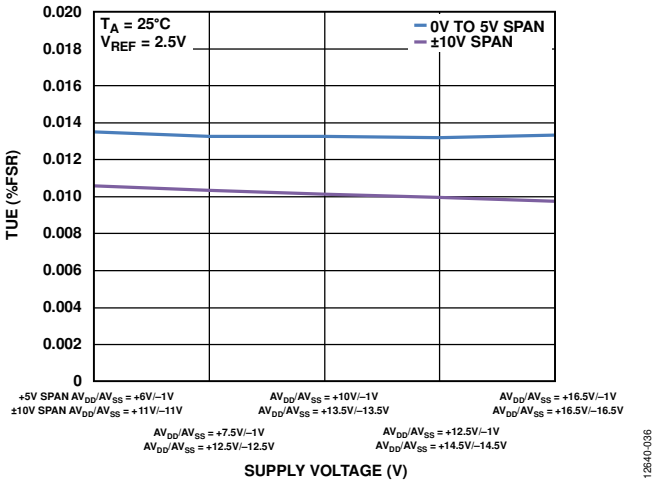


Figure 36. TUE vs. Supply Voltage

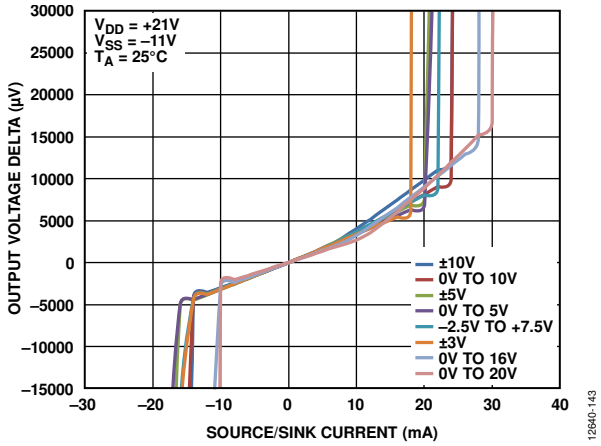


Figure 37. Source and Sink Capability of Output Amplifier with Positive Full Scale Loaded

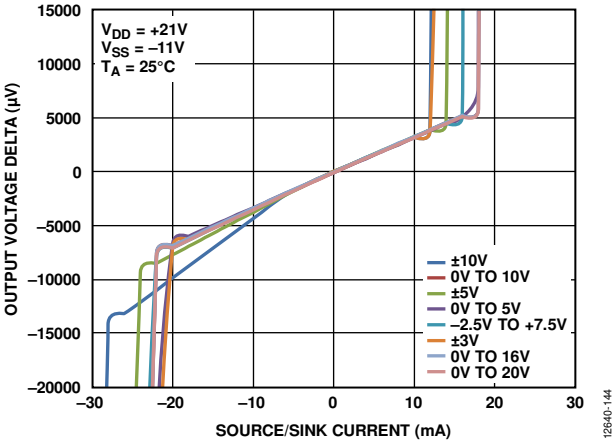


Figure 38. Source and Sink Capability of Output Amplifier with Negative Full Scale Loaded

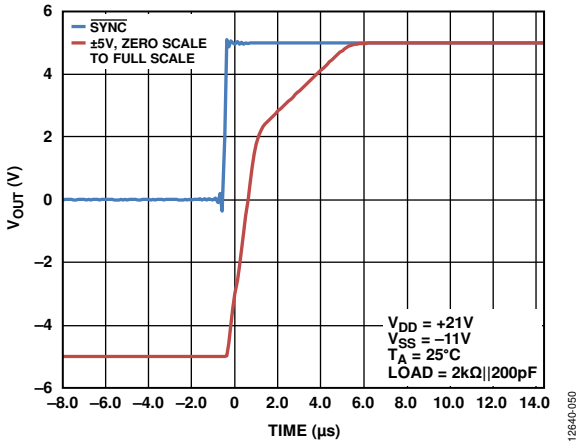


Figure 39. Full-Scale Settling Time (Rising Voltage Step), ±5 V Range

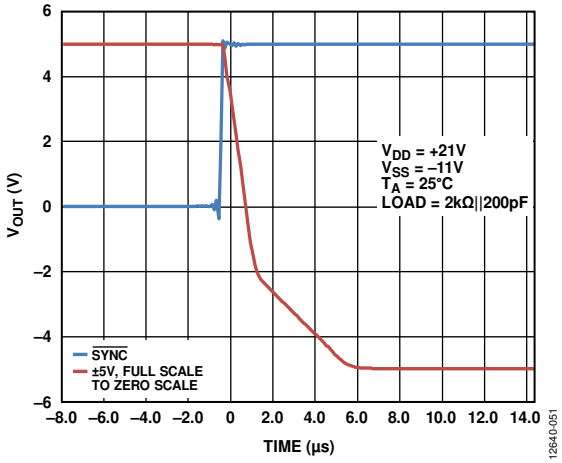


Figure 40. Full-Scale Settling Time (Falling Voltage Step), ±5 V Range

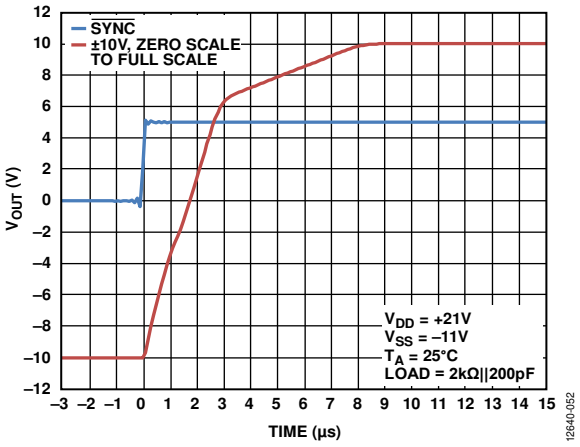


Figure 41. Full-Scale Settling Time (Rising Voltage Step), ±10 V Range

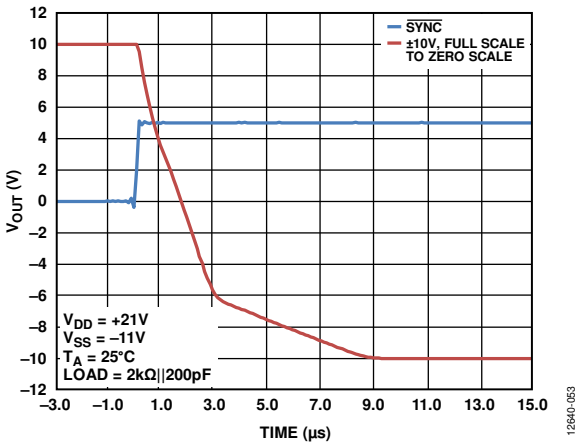


Figure 42. Full-Scale Settling Time (Falling Voltage Step), ±10 V Range

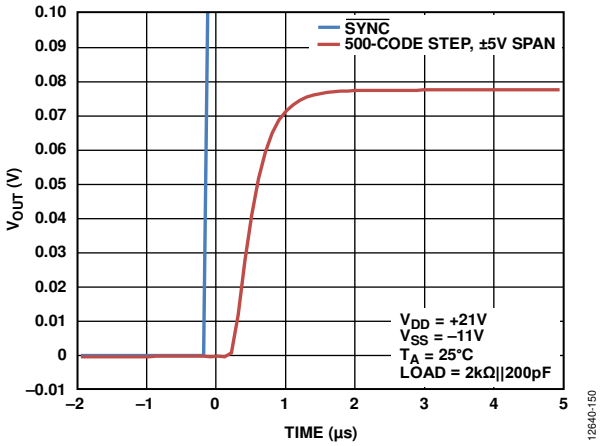


Figure 43. 500-Code Step Settling Time, ±5 V Range

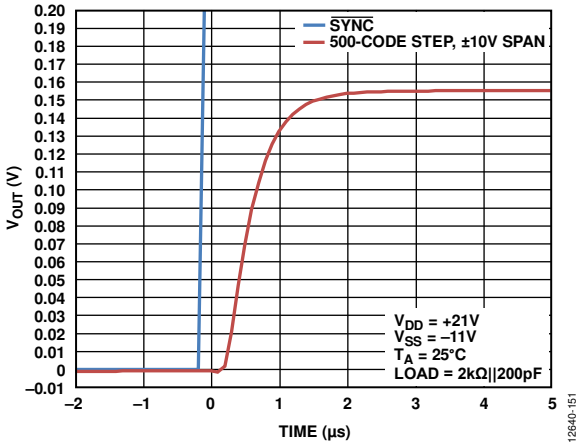


Figure 44. 500-Code Step Settling Time, ±10 V Range

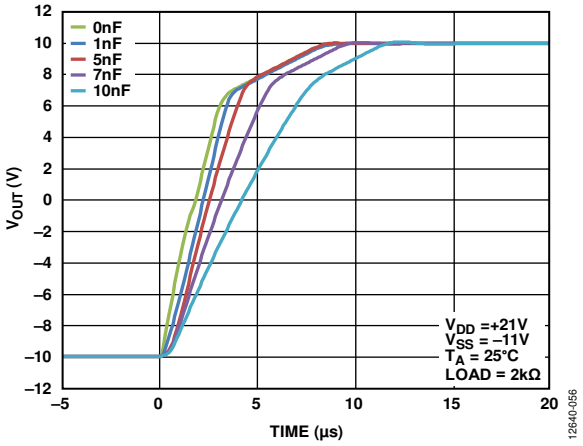


Figure 45. Settling Time vs. Capacitive Load, ±10 V Range

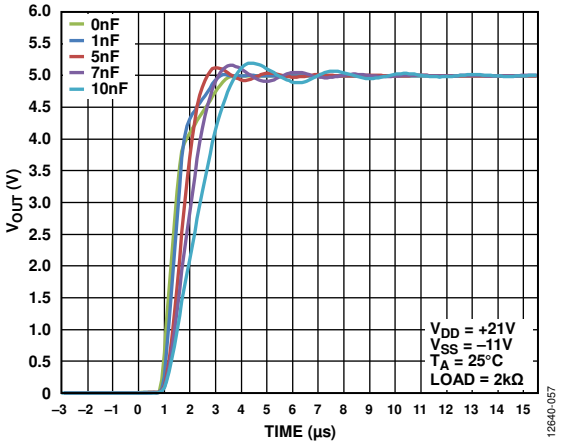


Figure 46. Settling Time vs. Capacitive Load, 0 V to 5 V Range

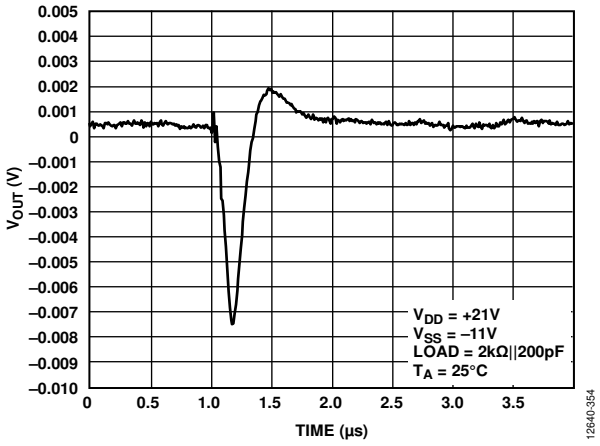


Figure 47. Digital-to-Analog Glitch Energy, 0 V to 5 V Range

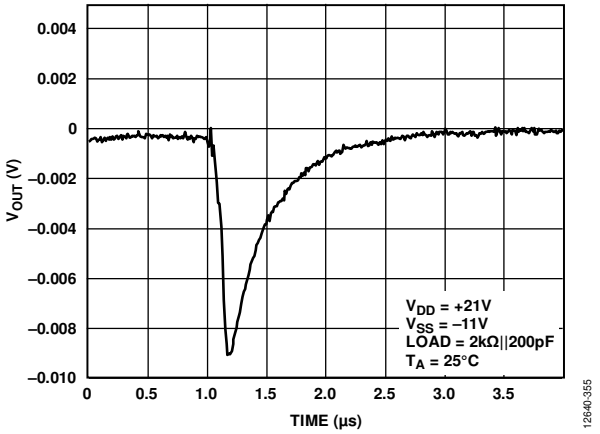


Figure 48. Digital-to-Analog Glitch Energy, ±10 V Range

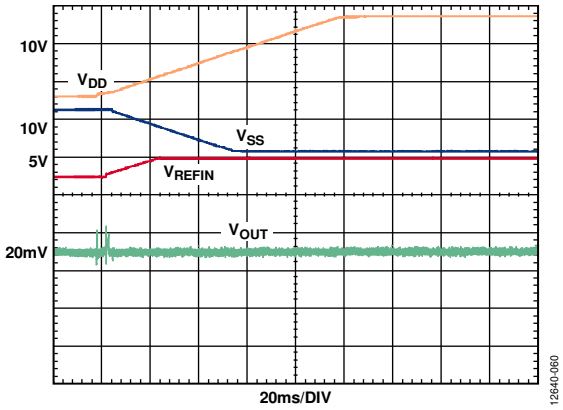


Figure 49. Power-Up Glitch

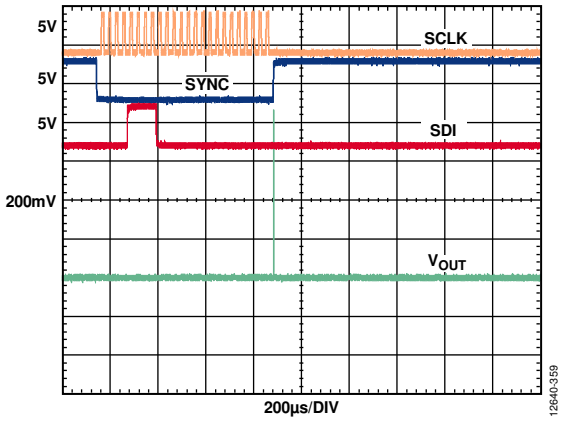


Figure 52. Software Full Reset Glitch from Zero Scale with Output Loaded, 0 V to 5 V Range

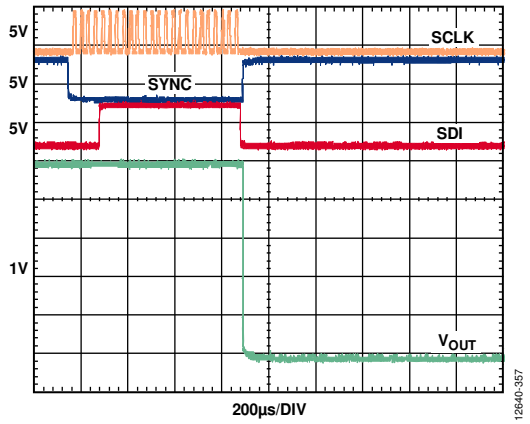


Figure 50. Software Full Reset Glitch from Full Scale with Output Loaded, 0 V to 5 V Range

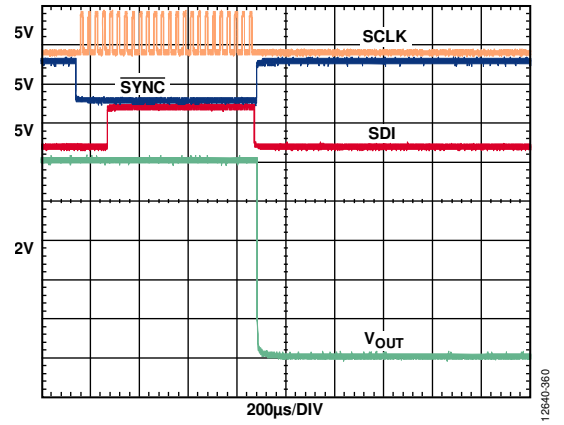


Figure 53. Software Full Reset Glitch from Full Scale with Output Loaded, ±10 V Range

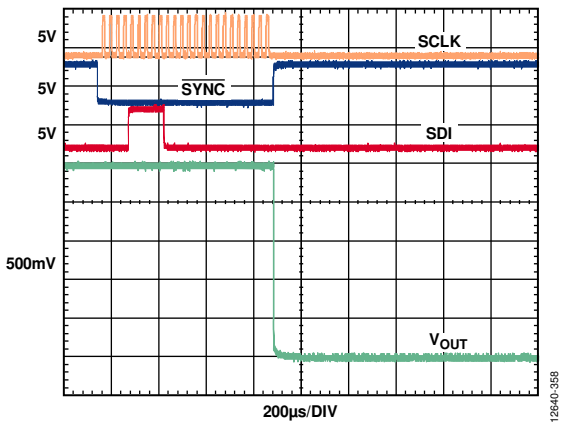


Figure 51. Software Full Reset Glitch from Midscale with Output Loaded, 0 V to 5 V Range

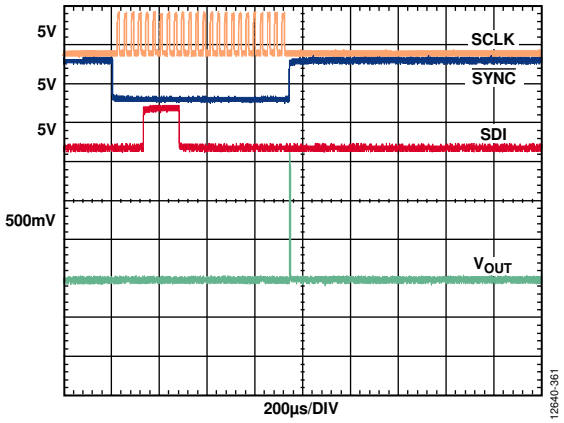


Figure 54. Software Full Reset Glitch from Midscale with Output Loaded, ±10 V Range

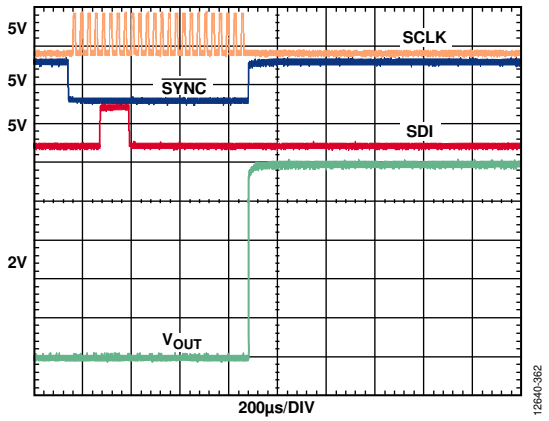


Figure 55. Software Full Reset Glitch from Zero Scale with Output Loaded, ±10 V Range

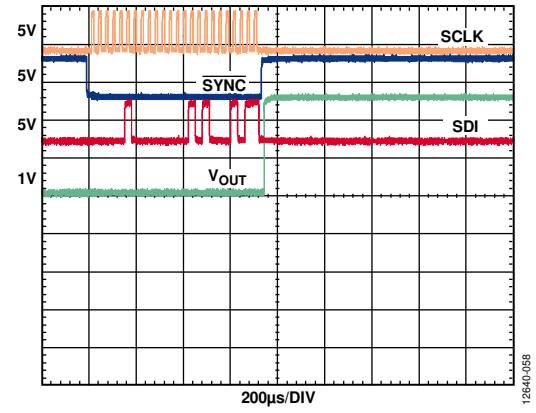


Figure 56. Output Range Change Glitch, 0 V to 5 V Range

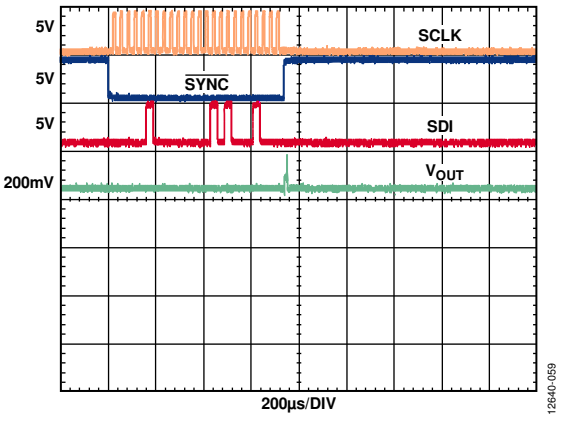


Figure 57. Output Range Change Glitch, ±10 V Range

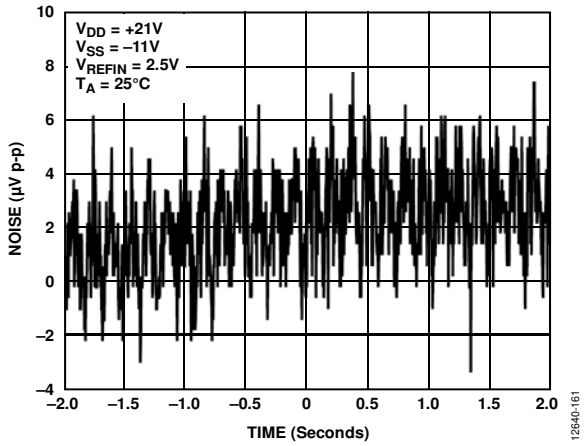


Figure 58. Peak-to-Peak Noise (Voltage Output Noise), 0.1 Hz to 10 Hz Bandwidth

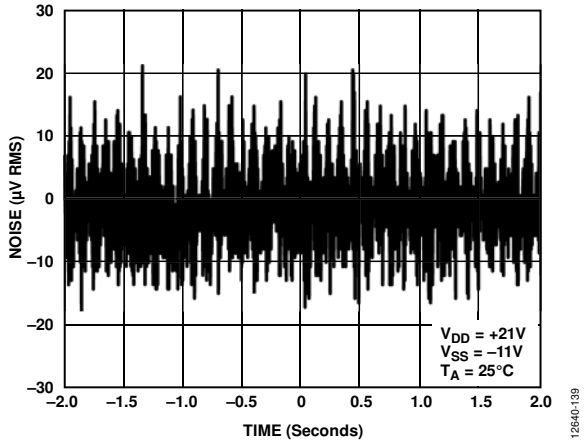


Figure 59. Peak-to-Peak Noise (Voltage Output Noise), 100 kHz Bandwidth

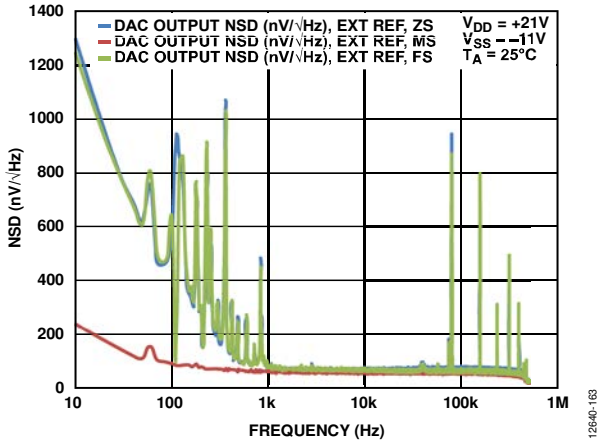


Figure 60. DAC Output Noise Spectral Density vs. Frequency, ±10 V Range

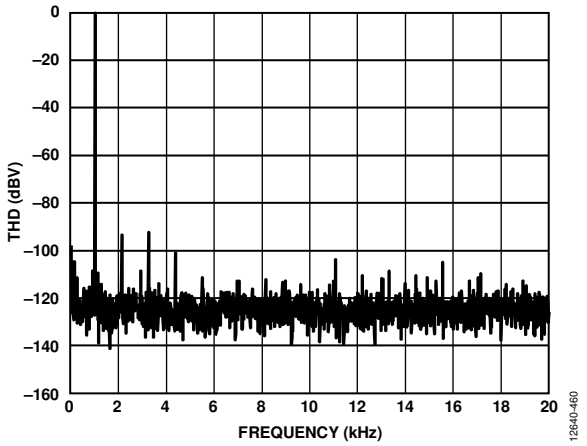


Figure 61. Total Harmonic Distortion at 1 kHz

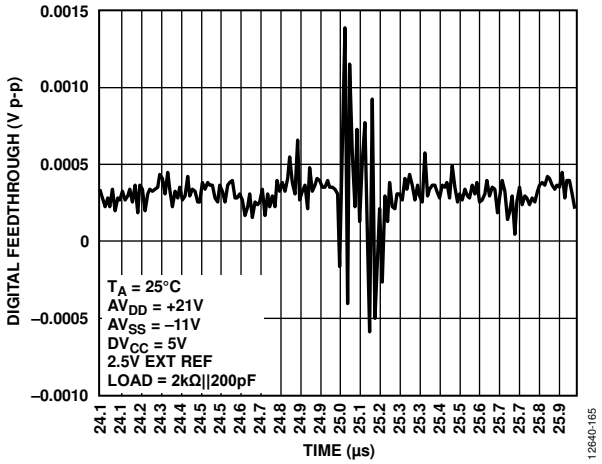


Figure 62. Digital Feedthrough

TERMINOLOGY

Total Unadjusted Error (TUE)
Total unadjusted error is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy, or integral nonlinearity, is a measure of the maximum deviation, in LSB, from a straight line passing through the endpoints of the DAC transfer function. A typical INL error vs. DAC code plot is shown in Figure 7.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic. A typical DNL error vs. code plot is shown in Figure 11.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5761/AD5721 are monotonic over their full operating temperature range.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (straight binary coding) or 0x0000 (twos complement coding) for the AD5761/AD5721.

Bipolar Zero Temperature Coefficient (TC)
Bipolar zero TC is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in µV/°C.

Zero-Scale Error
Zero-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) or 0x8000 (twos complement coding) is loaded to the DAC register. Ideally, the output voltage is negative full scale. A plot of zero-scale error vs. temperature is shown in Figure 21.

Zero-Scale Error Temperature Coefficient (TC)
Zero-scale error TC is a measure of the change in zero-scale error with a change in temperature. It is expressed in µV/°C.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function.

Offset Error Temperature Coefficient (TC)
Offset error TC is a measurement of the change in offset error with a change in temperature. It is expressed in µV/°C.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed in % FSR. A plot of gain error vs. temperature is shown in Figure 24.

Gain Error Temperature Coefficient (TC)
Gain error TC is a measure of the change in gain error with changes in temperature. It is expressed in ppm FSR/°C.

DC Power Supply Rejection Ratio (DC PSRR)
DC power supply rejection ratio is a measure of the rejection of the output voltage to dc changes in the power supplies applied to the DAC. It is measured for a given dc change in power supply voltage and is expressed in mV/V.

AC Power Supply Rejection Ratio (AC PSRR)
AC power supply rejection ratio is a measure of the rejection of the output voltage to ac changes in the power supplies applied to the DAC. It is measured for a given amplitude and frequency change in power supply voltage and is expressed in decibels.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change. Full-scale settling time is shown in Figure 39 to Figure 42.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (see Figure 47 and Figure 48).

Glitch Impulse Peak Amplitude
Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the amplitude of the glitch in mV and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

Noise Spectral Density
Noise spectral density is a measurement of the internally generated random noise characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to full scale and measuring noise at the output. It is measured in nV/√Hz. A plot of noise spectral density is shown in Figure 60.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental.

For the AD5761/AD5721, it is defined as

$$THD\ (\text{dB}) = 20 \times \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5761/AD5721 are single channel 16-/12-bit voltage output DACs. The AD5761/AD5721 output ranges are software selectable and can be configured as follows:

- Unipolar output voltage: 0 V to 5 V, 0 V to 10 V, 0 V to 16 V, 0 V to 20 V
- Bipolar output voltage: −2.5 V to +7.5 V, ±3 V, ±5 V, ±10 V

Data is written to the AD5761/AD5721 in a 24-bit word format via a 4-wire digital interface that is serial peripheral interface (SPI) compatible. The devices also offer an SDO pin to facilitate daisy-chaining and readback.

TRANSFER FUNCTION

The input coding to the DAC can be straight binary or twos complement (bipolar ranges case only). Therefore, the transfer function is given by

$$V_{OUT} = V_{REF} \times \left[\left(M \times \frac{D}{65{,}536} \right) - C \right]$$

where:

V_{REF} is 2.5 V.
M is the slope for a given output range (see Table 7).
D is the decimal equivalent of the code loaded to the DAC register as follows:
0 to 4095 for the 12-bit device.
0 to 65,535 for the 16-bit device.
C is the offset for a given output range (see Table 7).

Table 7. M and C Values for Various Output Ranges

Range	M	C
±10 V	8	4
±5 V	4	2
±3 V	2.4	1.2
−2.5 V to +7.5 V	4	1
0 V to 20 V	8	0
0 V to 16 V	6.4	0
0 V to 10 V	4	0
0 V to 5 V	2	0

DAC ARCHITECTURE

The DAC architecture consists of an R/2R DAC followed by an output buffer amplifier. Figure 63 shows a block diagram of the DAC architecture. Note that the reference input is buffered prior to being applied to the DAC.

The output voltage range obtained from the configurable output amplifier is selected by writing to the 3 LSBs, (RA[2:0]), in the control register.

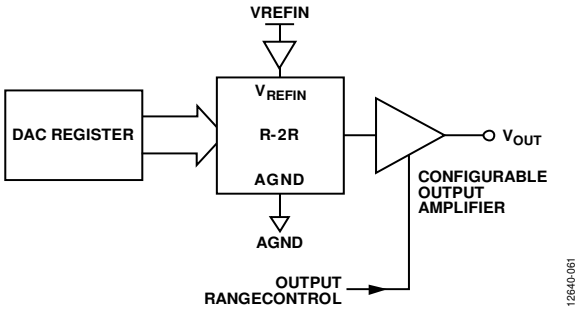


Figure 63. DAC Architecture

R/2R DAC

The architecture of the AD5761/AD5721 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 64. The six MSBs of the 16-bit data-word are decoded to drive 63 switches, E0 to E62, whereas the remaining 10 bits of the data-word drive the S0 to S9 switches of a 10-bit voltage mode R/2R ladder network.

The code loaded into the DAC register determines which arms of the ladder are switched between V_{REFIN} and ground (AGND). The output voltage is taken from the end of the ladder and amplified afterwards to provide the selected output voltage.

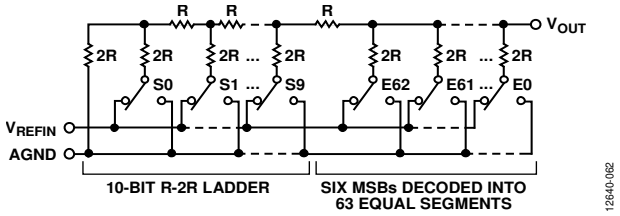


Figure 64. DAC Ladder Structure

Reference Buffer

The AD5761/AD5721 operate with an external reference. The reference input has an input range of 2 V to 3 V with 2.5 V for specified performance. This input voltage is then buffered before it is applied to the DAC core.

DAC Output Amplifier

The output amplifier is capable of generating both unipolar and bipolar output voltages. It is capable of driving a load of 2 kΩ in parallel with 1 nF to AGND. The source and sink capabilities of the output amplifier are shown in Figure 37.

SERIAL INTERFACE

The AD5761/AD5721 4-wire (SYNC, SCLK, SDI, and SDO) digital interface is SPI compatible. The write sequence begins after bringing the SYNC line low, maintaining this line low until the complete data-word is loaded from the SDI pin. Data is loaded in at the SCLK falling edge transition (see Figure 2). When SYNC is brought high again, the serial data-word is decoded according to the instructions in Table 10. The AD5761/AD5721 contain an SDO pin to allow the user to daisy-chain multiple devices together or to read back the contents of the registers.

Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can be used only when SYNC is held low for the correct number of clock cycles.

In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and SYNC must be taken high after the final clock to latch the data. The first falling edge of SYNC starts the write cycle. Exactly 24 falling clock edges must be applied to SCLK before SYNC is brought high again. If SYNC is brought high before the 24th falling SCLK edge, the data written is invalid. If more than 24 falling SCLK edges are applied before SYNC is brought high, the input data is also invalid.

The input shift register is updated on the rising edge of SYNC. For another serial transfer to take place, SYNC must be brought low again. After the end of the serial data transfer, data is automatically transferred from the input shift register to the addressed register. When the write cycle is complete, the output can be updated by taking LDAC low while SYNC is high.

Readback Operation

The contents of the input, DAC, and control registers can be read back via the SDO pin. Figure 4 shows how the registers are decoded. After a register has been addressed for a read, the next 24 clock cycles clock the data out on the SDO pin. The clocks must be applied while SYNC is low. When SYNC is returned high, the SDO pin is placed in tristate. For a read of a single register, the no operation (NOP) function clocks out the data. Alternatively, if more than one register is to be read, the data of the first register to be addressed clocks out at the same time that the second register to be read is being addressed. The SDO pin must be enabled to complete a readback operation. The SDO pin is enabled by default.

Daisy-Chain Operation

For systems that contain several devices, use the SDO pin to daisy-chain several devices together. Daisy-chain mode is useful in system diagnostics and in reducing the number of serial interface lines. The first falling edge of SYNC starts the write cycle. SCLK is continuously applied to the input shift register when SYNC is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge.

By connecting the SDO of the first device to the SDI input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × N, where N is the total number of AD5761/AD5721 devices in the chain. When the serial transfer to all devices is complete, SYNC is taken high, which latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register.

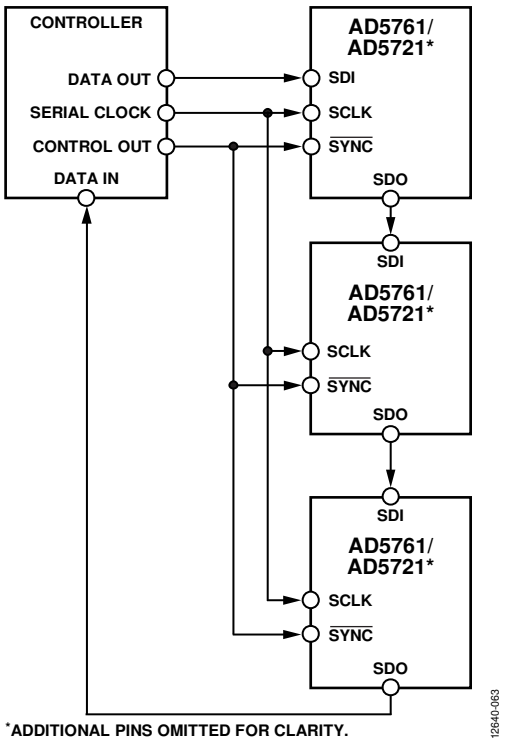


Figure 65. Daisy-Chain Block Diagram

HARDWARE CONTROL PINS

Load DAC Function (LDAC)

After data transfers into the input register of the DAC, there are two ways to update the DAC register and DAC output. Depending on the status of both SYNC and LDAC, one of two update modes is selected: synchronous DAC update or asynchronous DAC update.

Synchronous DAC Update

In synchronous DAC update mode, LDAC is held low while data is being clocked into the input shift register. The DAC output is updated on the rising edge of SYNC.

Asynchronous DAC Update

In asynchronous DAC update mode, $\overline{\text{LDAC}}$ is held high while data is being clocked into the input shift register. The DAC output is asynchronously updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ is taken high. The update then occurs on the falling edge of $\overline{\text{LDAC}}$.

Reset Function ($\overline{\text{RESET}}$)

The AD5761/AD5721 can be reset to its power-on state by two means: either by asserting the $\overline{\text{RESET}}$ pin or by using the software full reset registers (see Table 26).

Asynchronous Clear Function ($\overline{\text{CLEAR}}$)

The $\overline{\text{CLEAR}}$ pin is a falling edge active input that allows the output to be cleared to a user defined value. The clearcode value is programmed by writing to Bit 10 and Bit 9 in the control register (see Table 11 and Table 12). It is necessary to maintain $\overline{\text{CLEAR}}$ low for a minimum amount of time to complete the operation (see Figure 2). When the $\overline{\text{CLEAR}}$ signal is returned high, the output remains at the clear value until a new value is loaded to the DAC register.

Alert Function ($\overline{\text{ALERT}}$)

When the $\overline{\text{ALERT}}$ pin is asserted low, a readback from the control register is required to clarify whether a short-circuit or brownout condition occurred, depending on the values of Bit 12 and Bit 11, SC and BO bits, respectively (see Table 15 and Table 16). If neither of these conditions occurred, the temperature exceeded approximately 150°C.

The $\overline{\text{ALERT}}$ pin is low during power-up, a software full reset, or a hardware reset. After the first write to the control register to configure the DAC, the $\overline{\text{ALERT}}$ pin is asserted high.

In the event of the die temperature exceeding approximately 150°C, the $\overline{\text{ALERT}}$ pin is low and the value of the ETS bit determines the state of the digital supply of the device, whether the internal digital supply is powered on or powered down. If the ETS bit is set to 0, the internal digital supply is powered on when the internal die temperature exceeds approximately 150°C. If the ETS bit is set to 1, the internal digital supply is powered down when the internal die temperature exceeds approximately 150°C and the device becomes nonfunctional (see Table 11 and Table 12).

The AD5761/AD5721 temperature at power-up must be less than 150°C for proper operation of the devices.

REGISTER DETAILS

INPUT SHIFT REGISTER

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK, which can operate at rates of up to 50 MHz. The input shift register consists of three don't care bits, one fixed value bit (DB20 = 0), four address bits, and a 16-bit or 12-bit data-word as shown in Table 8 and Table 9, respectively.

Table 8. AD5761 16-Bit Input Shift Register Format

MSB **LSB**

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB0
X[1]	X[1]	X[1]	0	Register address				Register data

[1] X means don't care.

Table 9. AD5721 12-Bit Input Shift Register Format

MSB **LSB**

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB4	DB3 to DB0
X[1]	X[1]	X[1]	0	Register address				Register data	XXXX[1]

[1] X means don't care.

Table 10. Input Shift Register Commands

Register Address				
DB19	DB18	DB17	DB16	Command
0	0	0	0	No operation
0	0	0	1	Write to input register (no update)
0	0	1	0	Update DAC register from input register
0	0	1	1	Write and update DAC register
0	1	0	0	Write to control register
0	1	0	1	No operation
0	1	1	0	No operation
0	1	1	1	Software data reset
1	0	0	0	Reserved
1	0	0	1	Disable daisy-chain functionality
1	0	1	0	Readback input register
1	0	1	1	Readback DAC register
1	1	0	0	Readback control register
1	1	0	1	No operation
1	1	1	0	No operation
1	1	1	1	Software full reset

CONTROL REGISTER

The control register controls the mode of operation of the AD5761/AD5721. The control register options are shown in Table 11 and Table 12.

On power-up, after a full reset, or after a hardware reset, the output of the DAC is clamped to ground through a 1 kΩ resistor and the output buffer remains in power-down mode. A write to the control register is required to configure the device, remove the clamp to ground, and power up the output buffer.

When the DAC output range is reconfigured during operation, a software full reset command (see Table 26) must be written to the device before writing to the control register.

Table 11. Write to Control Register

MSB **LSB**

DB[23:21]	DB20	DB[19:16]	DB[15:11]	DB[10:9]	DB8	DB7	DB6	DB5	DB[4:3]	DB[2:0]
XXX[1]	0	Register address	Register data							
XXX[1]	0	0100	XXXX[1]	CV[1:0]	OVR	B2C	ETS	0	PV[1:0]	RA[2:0]

[1] X means don't care.

Table 12. Control Register Functions

Bit Name	Description
CV[1:0]	$\overline{\text{CLEAR}}$ voltage selection. 00: zero scale. 01: midscale. 10, 11: full scale.
OVR	5% overrange. 0: 5% overrange disabled. 1: 5% overrange enabled.
B2C	Bipolar range. 0: DAC input for bipolar output range is straight binary coded. 1: DAC input for bipolar output range is twos complement coded.
ETS	Thermal shutdown alert. The alert may not work correctly if the device powers on with temperature conditions >150°C (greater than the maximum rating of the device). 0: internal digital supply does not power down if die temperature exceeds 150°C. 1: internal digital supply powers down if die temperature exceeds 150°C.
PV[1:0]	Power-up voltage. 00: zero scale. 01: midscale. 10, 11: full scale.
RA[2:0]	Output range. After an output range configuration, the device must be reset. 000: −10 V to +10 V. 001: 0 V to +10 V. 010: −5 V to +5 V. 011: 0 V to 5 V. 100: −2.5 V to +7.5 V. 101: −3 V to +3 V. 110: 0 V to 16 V. 111: 0 V to 20 V.

Table 13. Bipolar Output Range Possible Codes

Straight Binary	Decimal Code	Twos Complement
1111	+7	0111
1110	+6	0110
1101	+5	0101
1100	+4	0100
1011	+3	0011
1010	+2	0010
1001	+1	0001
1000	0	0000
0111	−1	1111
0110	−2	1110
0101	−3	1101
0100	−4	1100
0011	−5	1011
0010	−6	1010
0001	−7	1001
0000	−8	1000