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Complete Quad, 16-Bit, High Accuracy, Serial Input, Bipolar Voltage Output DAC

Data Sheet

AD5764R

FEATURES

Complete quad, 16-bit digital-to-analog converter (DAC)
Programmable output range: ±10 V, ±10.2564 V, or ±10.5263 V
±1 LSB maximum INL error, ±1 LSB maximum DNL error
Low noise: 60 nV/√Hz
Settling time: 10 µs maximum
Integrated reference buffers
Internal reference: 10 ppm/°C maximum
On-chip die temperature sensor
Output control during power-up/brownout
Programmable short-circuit protection
Simultaneous updating via $\overline{\text{LDAC}}$
Asynchronous $\overline{\text{CLR}}$ to zero code
Digital offset and gain adjust
Logic output control pins
DSP-/microcontroller-compatible serial interface
Temperature range: −40°C to +85°C
***i*CMOS process technology**

APPLICATIONS

Industrial automation
Open-loop/closed-loop servo control
Process control
Data acquisition systems
Automatic test equipment
Automotive test and measurement
High accuracy instrumentation

GENERAL DESCRIPTION

The AD5764R is a quad, 16-bit, serial input, bipolar voltage output DAC that operates from supply voltages of ±11.4 V to ±16.5 V. Nominal full-scale output range is ±10 V. The AD5764R provides integrated output amplifiers, reference buffers, and proprietary power-up/power-down control circuitry. The part also features a digital I/O port, programmed via the serial interface, and an analog temperature sensor. The part incorporates digital offset and gain adjust registers per channel.

The AD5764R is a high performance converter that provides guaranteed monotonicity, integral nonlinearity (INL) of ±1 LSB, low noise, and 10 µs settling time. The AD5764R includes an on-chip 5 V reference with a reference temperature coefficient of 10 ppm/°C maximum. During power-up when the supply voltages are changing, VOUTx is clamped to 0 V via a low impedance path.

The AD5764R is based on the *i*CMOS® technology platform, which is designed for analog systems designers within industrial/instrumentation equipment OEMs who need high performance ICs at higher voltage levels. *i*CMOS enables the development of analog ICs capable of 30 V and operation at ±15 V supplies, while allowing reductions in power consumption and package size, coupled with increased ac and dc performance.

The AD5764R uses a serial interface that operates at clock rates of up to 30 MHz and is compatible with DSP and microcontroller interface standards. Double buffering allows the simultaneous updating of all DACs. The input coding is programmable to either twos complement or offset binary formats. The asynchronous clear function clears all data registers to either bipolar zero or zero scale, depending on the coding used. The AD5764R is ideal for both closed-loop servo control and open-loop control applications. The AD5764R is available in a 32-lead TQFP and offers guaranteed specifications over the −40°C to +85°C industrial temperature range (see Figure 1 for the functional block diagram).

Rev. D

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- AD5764R Evaluation Board

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- AD5764R: Complete Quad, 16-Bit, High Accuracy, Serial Input, Bipolar Voltage Output DAC Data Sheet

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- AD5764 IIO Quad-Channel DAC Linux Driver
- AD5764R Software Evaluation

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

DESIGN RESOURCES

- AD5764R Material Declaration
- PCN-PDN Information
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FUNCTIONAL BLOCK DIAGRAM

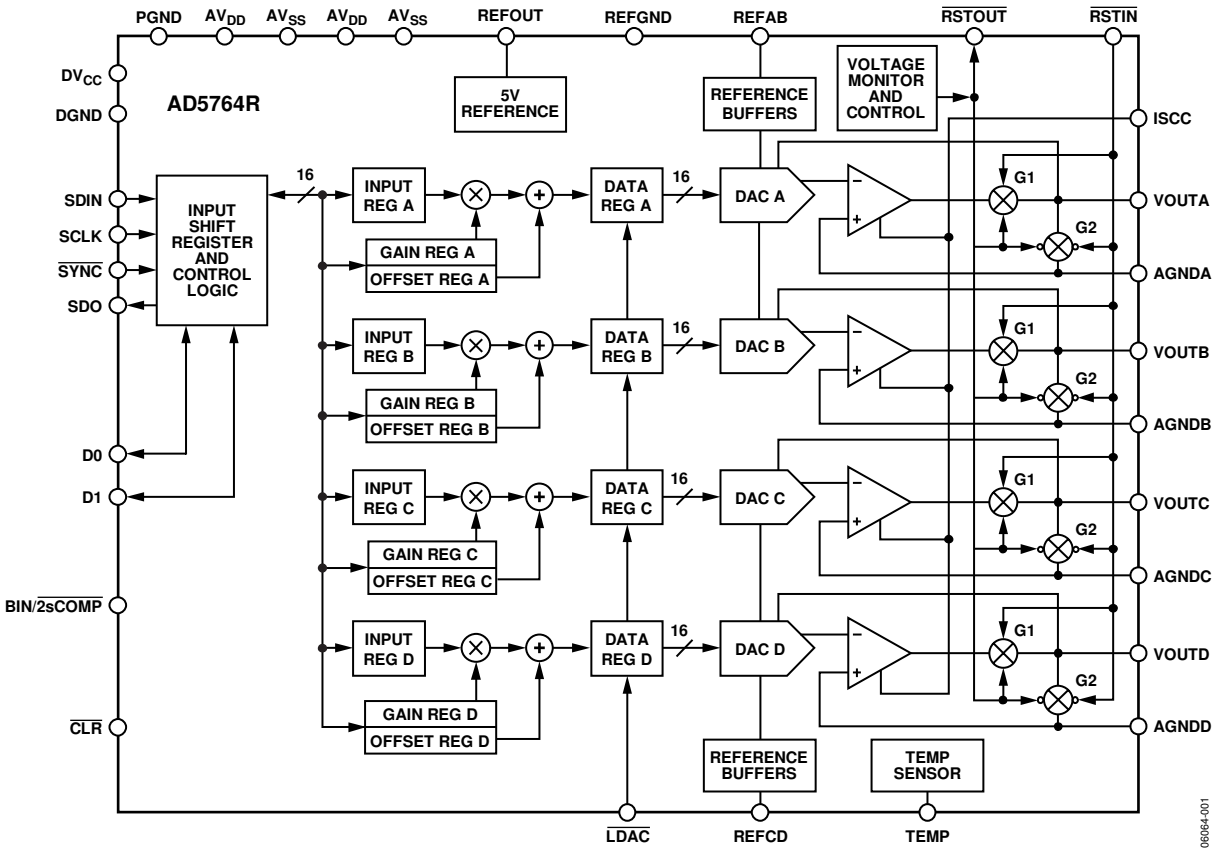

Figure 1.

SPECIFICATIONS

AV_{DD} = 11.4 V to 16.5 V, AV_{SS} = −11.4 V to −16.5 V, AGND = DGND = REFGND = PGND = 0 V; REFAB = REFCD = 5 V external; DV_{CC} = 2.7 V to 5.25 V, R_{LOAD} = 10 kΩ, C_L = 200 pF. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Grade[1]	C Grade[1]	Unit	Test Conditions/Comments
ACCURACY				Outputs unloaded
Resolution	16	16	Bits	
Relative Accuracy (INL)	±2	±1	LSB max	
Differential Nonlinearity (DNL)	±1	±1	LSB max	Guaranteed monotonic
Bipolar Zero Error	±2	±2	mV max	25°C; error at other temperatures obtained using bipolar zero tempco
	±3	±3	mV max	
Bipolar Zero Tempco[2]	±2	±2	ppm FSR/°C max	
Zero-Scale Error	±2	±2	mV max	25°C; error at other temperatures obtained using zero-scale tempco
	±2.5	±2.5	mV max	
Zero-Scale Tempco[2]	±2	±2	ppm FSR/°C max	
Gain Error	±0.02	±0.02	% FSR max	
Gain Tempco[2]	±2	±2	ppm FSR/°C max	
DC Crosstalk[2]	0.5	0.5	LSB max	
REFERENCE INPUT/OUTPUT				
Reference Input[2]				
Reference Input Voltage	5	5	V nominal	±1% for specified performance
DC Input Impedance	1	1	MΩ min	Typically 100 MΩ
Input Current	±10	±10	µA max	Typically ±30 nA
Reference Range	1/7	1/7	V min/V max	
Reference Output				
Output Voltage	4.995/5.005	4.995/5.005	V min/V max	At 25°C, AV_{DD}/AV_{SS} = ±13.5 V
Reference Tempco[2]	±10	±10	ppm/°C max	Typically 1.7ppm/°C
R_{LOAD}[2]	1	1	MΩ min	
Power Supply Sensitivity[2]	300	300	µV/V typ	
Output Noise[2]	18	18	µV p-p typ	0.1 Hz to 10 Hz
Noise Spectral Density[2]	75	75	nV/√Hz typ	At 10 kHz
Output Voltage Drift vs. Time[2]	±40	±40	ppm/500 hr typ	
	±50	±50	ppm/1000 hr typ	
Thermal Hysteresis[2]	70	70	ppm typ	First temperature cycle
	30	30	ppm typ	Subsequent temperature cycles
OUTPUT CHARACTERISTICS[2]				
Output Voltage Range[3]	±10.5263	±10.5263	V min/V max	AV_{DD}/AV_{SS} = ±11.4 V, V_{REFIN} = 5 V
	±14	±14	V min/V max	AV_{DD}/AV_{SS} = ±16.5 V, V_{REFIN} = 7 V
Output Voltage Drift vs. Time	±13	±13	ppm FSR/500 hr typ	
	±15	±15	ppm FSR/1000 hr typ	
Short-Circuit Current	10	10	mA typ	R_{ISCC} = 6 kΩ, see Figure 31
Load Current	±1	±1	mA max	For specified performance
Capacitive Load Stability				
R_{LOAD} = ∞	200	200	pF max	
R_{LOAD} = 10 kΩ	1000	1000	pF max	
DC Output Impedance	0.3	0.3	Ω max	

Parameter	B Grade[1]	C Grade[1]	Unit	Test Conditions/Comments
DIGITAL INPUTS[2]				DV_{CC} = 2.7 V to 5.25 V
Input High Voltage, V_{IH}	2.4	2.4	V min	
Input Low Voltage, V_{IL}	0.8	0.8	V max	
Input Current	±1.2	±1.2	µA max	Per pin
Pin Capacitance	10	10	pF max	Per pin
DIGITAL OUTPUTS (D0, D1, SDO)[2]				
Output Low Voltage	0.4	0.4	V max	DV_{CC} = 5 V ± 5%, sinking 200 µA
Output High Voltage	DV_{CC} − 1	DV_{CC} − 1	V min	DV_{CC} = 5 V ± 5%, sourcing 200 µA
Output Low Voltage	0.4	0.4	V max	DV_{CC} = 2.7 V to 3.6 V, sinking 200 µA
Output High Voltage	DV_{CC} − 0.5	DV_{CC} − 0.5	V min	DV_{CC} = 2.7 V to 3.6 V, sourcing 200 µA
High Impedance Leakage Current	±1	±1	µA max	SDO only
High Impedance Output Capacitance	5	5	pF typ	SDO only
DIE TEMPERATURE SENSOR[2]				
Output Voltage at 25°C	1.47	1.47	V typ	Die temperature
Output Voltage Scale Factor	5	5	mV/°C typ	
Output Voltage Range	1.175/1.9	1.175/1.9	V min/V max	−40°C to +105°C
Output Load Current	200	200	µA max	Current source only
Power-On Time	10	10	ms typ	
POWER REQUIREMENTS				
AV_{DD}/AV_{SS}	11.4/16.5	11.4/16.5	V min/V max	
DV_{CC}	2.7/5.25	2.7/5.25	V min/V max	
Power Supply Sensitivity[2]				
$\Delta V_{OUT}/\Delta AV_{DD}$	−85	−85	dB typ	
AI_{DD}	3.55	3.55	mA/channel max	Outputs unloaded
AI_{SS}	2.8	2.8	mA/channel max	Outputs unloaded
DI_{CC}	1.2	1.2	mA max	$V_{IH} = DV_{CC}$, V_{IL} = DGND, 750 µA typ
Power Dissipation	275	275	mW typ	±12 V operation output unloaded

[1] Temperature range: −40°C to +85°C; typical at +25°C. Device functionality is guaranteed to +105°C with degraded performance.
[2] Guaranteed by design and characterization; not production tested.
[3] Output amplifier headroom requirement is 1.4 V minimum.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = 11.4 V to 16.5 V, AV_{SS} = −11.4 V to −16.5 V, AGND = DGND = REFGND = PGND = 0 V; REFAB = REFCD = 5 V external; DV_{CC} = 2.7 V to 5.25 V, R_{LOAD} = 10 kΩ, C_L = 200 pF. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	B Grade	C Grade	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]				
Output Voltage Settling Time	8	8	µs typ	Full-scale step to ±1 LSB
	10	10	µs max	
	2	2	µs typ	512 LSB step settling
Slew Rate	5	5	V/µs typ	
Digital-to-Analog Glitch Energy	8	8	nV-sec typ	
Glitch Impulse Peak Amplitude	25	25	mV max	
Channel-to-Channel Isolation	80	80	dB typ	
DAC-to-DAC Crosstalk	8	8	nV-sec typ	
Digital Crosstalk	2	2	nV-sec typ	
Digital Feedthrough	2	2	nV-sec typ	Effect of input bus activity on DAC outputs
Output Noise (0.1 Hz to 10 Hz)	0.1	0.1	LSB p-p typ	
Output Noise (0.1 Hz to 100 kHz)	45	45	µV rms max	
1/f Corner Frequency	1	1	kHz typ	
Output Noise Spectral Density	60	60	nV/√Hz typ	Measured at 10 kHz
Complete System Output Noise Spectral Density[2]	80	80	nV/√Hz typ	Measured at 10 kHz

[1] Guaranteed by design and characterization; not production tested.
[2] Includes noise contributions from integrated reference buffers, a 16-bit DAC, and an output amplifier.

TIMING CHARACTERISTICS

AV_{DD} = 11.4 V to 16.5 V, AV_{SS} = −11.4 V to −16.5 V, AGND = DGND = REFGND = PGND = 0 V; REFAB = REFCD = 5 V external; DV_{CC} = 2.7 V to 5.25 V, R_{LOAD} = 10 kΩ, C_L = 200 pF. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5[4]	13	ns min	24th SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	90	ns min	Minimum $\overline{SYNC}$ high time
t_7	2	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	1.7	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (all DACs updated)
	480	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (single DAC updated)
t_{10}	10	ns min	$\overline{LDAC}$ pulse width low
t_{11}	500	ns max	$\overline{LDAC}$ falling edge to DAC output response time
t_{12}	10	µs max	DAC output settling time
t_{13}	10	ns min	$\overline{CLR}$ pulse width low
t_{14}	2	µs max	$\overline{CLR}$ pulse activation time
t_{15}[5, 6]	25	ns max	SCLK rising edge to SDO valid
t_{16}	13	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
t_{17}	2	µs max	$\overline{SYNC}$ rising edge to DAC output response time (LDAC = 0)
t_{18}	170	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, and Figure 4.
[4] Standalone mode only.
[5] Measured with the load circuit of Figure 5.
[6] Daisy-chain mode only.

Timing Diagrams

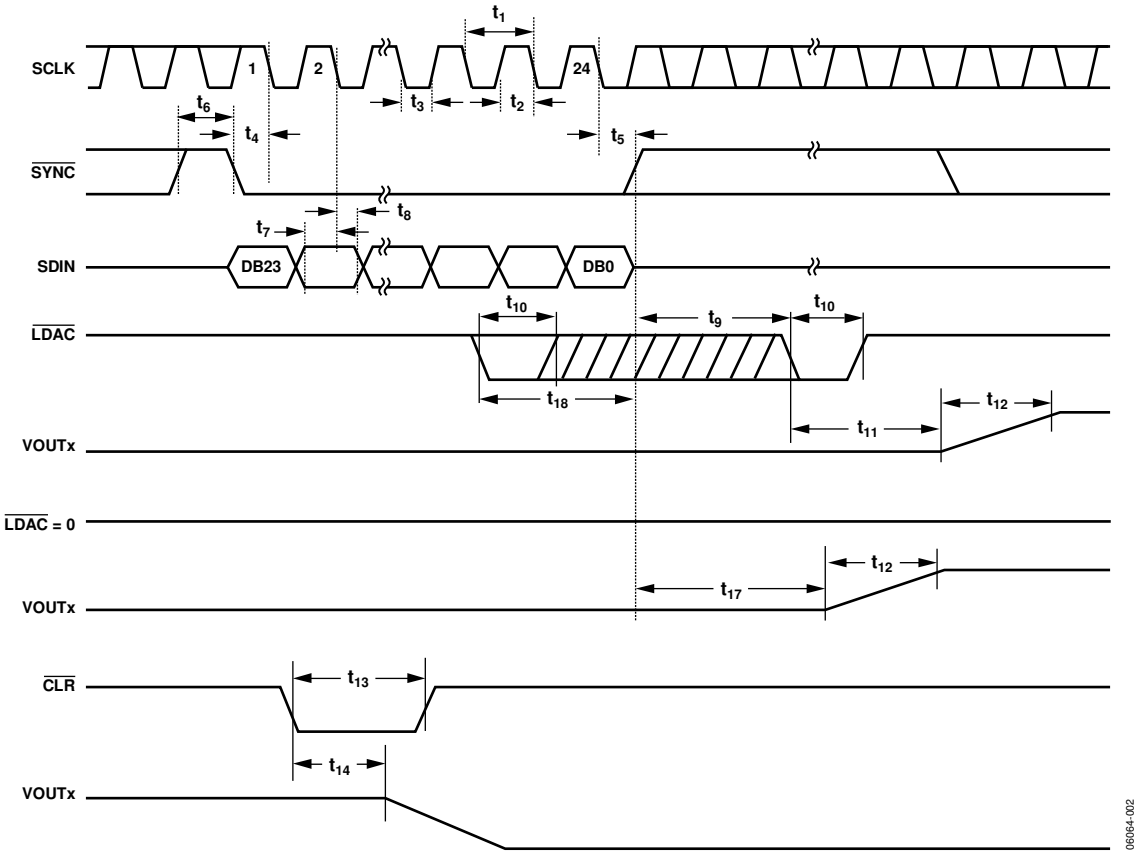

Figure 2. Serial Interface Timing Diagram

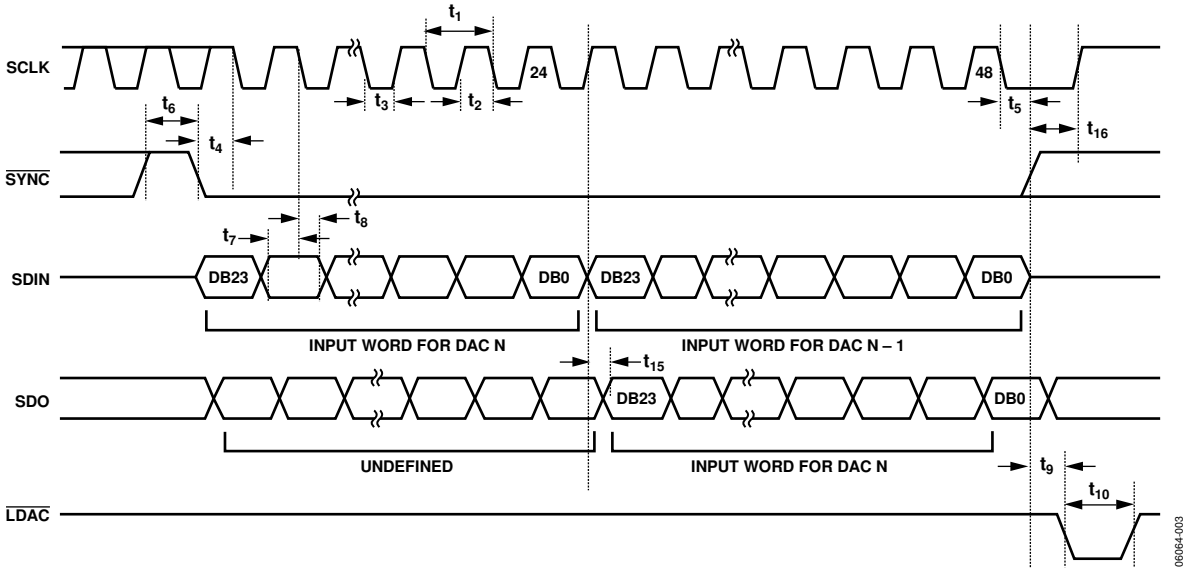

Figure 3. Daisy-Chain Timing Diagram

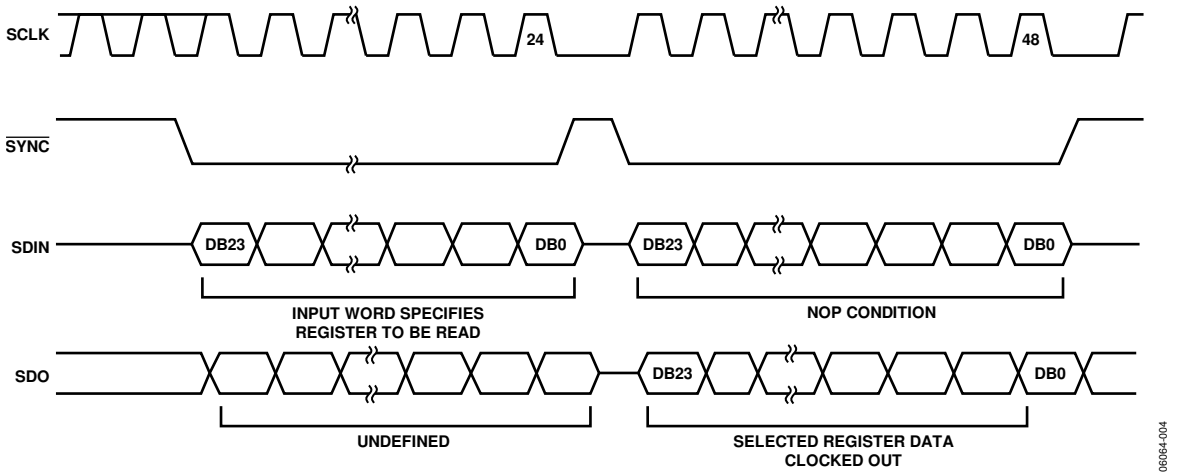

Figure 4. Readback Timing Diagram

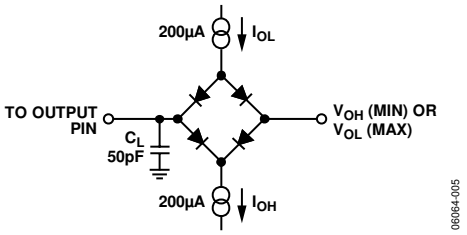

Figure 5. Load Circuit for SDO Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4.

Parameter	Rating
AV_{DD} to AGND, DGND	−0.3 V to +17 V
AV_{SS} to AGND, DGND	+0.3 V to −17 V
DV_{CC} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to (DV_{CC} + 0.3 V) or +7 V, whichever is less
Digital Outputs to DGND	−0.3 V to DV_{CC} + 0.3 V
REFAB, REFCD to AGND, PGND	−0.3 V to AV_{DD} + 0.3 V
REFOUT to AGND	AV_{SS} to AV_{DD}
TEMP	AV_{SS} to AV_{DD}
VOUTx to AGND	AV_{SS} to AV_{DD}
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Lead Temperature (Soldering)	JEDEC industry standard J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead TQFP	65	12	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

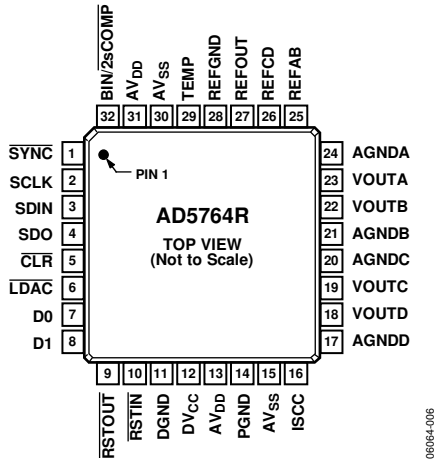

Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{SYNC}}$	Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{\text{SYNC}}$ is low, data is transferred in on the falling edge of SCLK.
2	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This operates at clock speeds of up to 30 MHz.
3	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
4	SDO	Serial Data Output. This pin is used to clock data from the serial register in daisy-chain or readback mode.
5	$\overline{\text{CLR}}$	Negative Edge Triggered Input.[1] Asserting this pin sets the data registers to 0x0000.
6	$\overline{\text{LDAC}}$	Load DAC. This logic input is used to update the data registers and, consequently, the analog outputs. When tied permanently low, the addressed data register is updated on the rising edge of $\overline{\text{SYNC}}$. If $\overline{\text{LDAC}}$ is held high during the write cycle, the DAC input register is updated but the output update is held off until the falling edge of $\overline{\text{LDAC}}$. In this mode, all analog outputs can be updated simultaneously on the falling edge of $\overline{\text{LDAC}}$. The $\overline{\text{LDAC}}$ pin must not be left unconnected.
7, 8	D0, D1	Digital I/O Port. D0 and D1 form a digital I/O port. The user can set up these pins as inputs or outputs that are configurable and readable over the serial interface. When configured as inputs, these pins have weak internal pull-ups to DV_{CC}. When programmed as outputs, D0 and D1 are referenced by DV_{CC} and DGND.
9	$\overline{\text{RSTOUT}}$	Reset Logic Output. This is the output from the on-chip voltage monitor used in the reset circuit. If desired, it can be used to control other system components.
10	$\overline{\text{RSTIN}}$	Reset Logic Input. This input allows external access to the internal reset logic. Applying a Logic 0 to this input clamps the DAC outputs to 0 V. In normal operation, $\overline{\text{RSTIN}}$ should be tied to Logic 1. Register values remain unchanged.
11	DGND	Digital Ground Pin.
12	DV_{CC}	Digital Supply Pin. Voltage ranges from 2.7 V to 5.25 V.
13, 31	AV_{DD}	Positive Analog Supply Pins. Voltage ranges from 11.4 V to 16.5 V.
14	PGND	Ground Reference Point for Analog Circuitry.
15, 30	AV_{SS}	Negative Analog Supply Pins. Voltage ranges from −11.4 V to −16.5 V.
16	ISCC	This pin is used in association with an optional external resistor to AGND to program the short-circuit current of the output amplifiers. Refer to the Design Features section for more information.
17	AGNDD	Ground Reference Pin for DAC D Output Amplifier.
18	VOUTD	Analog Output Voltage of DAC D. Buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
19	VOUTC	Analog Output Voltage of DAC C. Buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
20	AGNDC	Ground Reference Pin for DAC C Output Amplifier.
21	AGNDB	Ground Reference Pin for DAC B Output Amplifier.

Pin No.	Mnemonic	Description
22	VOUTB	Analog Output Voltage of DAC B. Buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
23	VOUTA	Analog Output Voltage of DAC A. Buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
24	AGNDA	Ground Reference Pin for DAC A Output Amplifier.
25	REFAB	External Reference Voltage Input for Channel A and Channel B. The reference input range is 1 V to 7 V, and it programs the full-scale output voltage. V_{REFIN} = 5 V for specified performance.
26	REFCD	External Reference Voltage Input for Channel C and Channel D. The reference input range is 1 V to 7 V, and it programs the full-scale output voltage. V_{REFIN} = 5 V for specified performance.
27	REFOUT	Reference Output. This is the reference output from the internal voltage reference. The internal reference is 5 V ± 3 mV at 25°C, with a reference temperature coefficient of 10 ppm/°C.
28	REFGND	Reference Ground Return for the Reference Generator and Buffers.
29	TEMP	This pin provides an output voltage proportional to temperature. The output voltage is 1.47 V typical at 25°C die temperature; variation with temperature is 5 mV/°C.
32	BIN/$\overline{2sCOMP}$	This pin determines the DAC coding. This pin should be hardwired to either DV_{CC} or DGND. When hardwired to DV_{CC}, input coding is offset binary (see Table 7). When hardwired to DGND, input coding is twos complement (see Table 8).

[1] Internal pull-up device on this logic input. Therefore, it can be left floating; and it defaults to a logic high condition.

TYPICAL PERFORMANCE CHARACTERISTICS

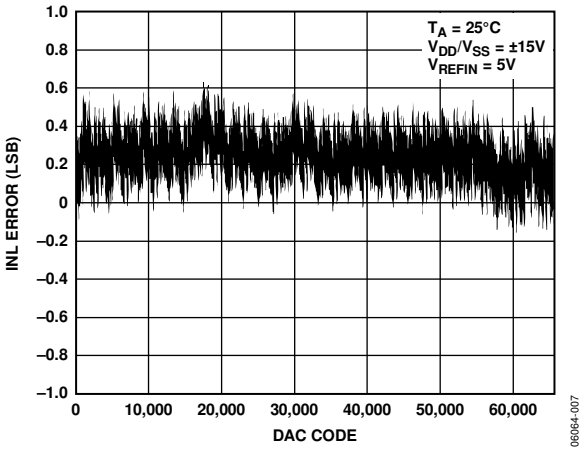

Figure 7. Integral Nonlinearity Error vs. DAC Code, V_{DD}/V_{SS} = ±15 V

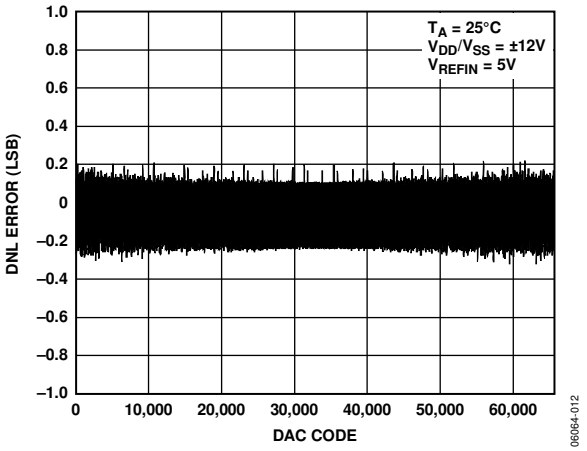

Figure 10. Differential Nonlinearity Error vs. DAC Code, V_{DD}/V_{SS} = ±12 V

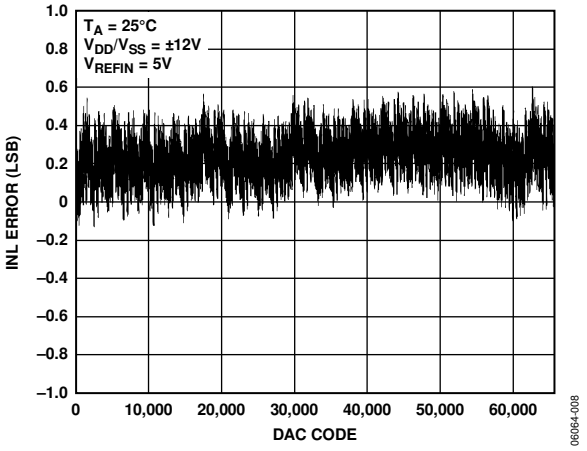

Figure 8. Integral Nonlinearity Error vs. DAC Code, V_{DD}/V_{SS} = ±12 V

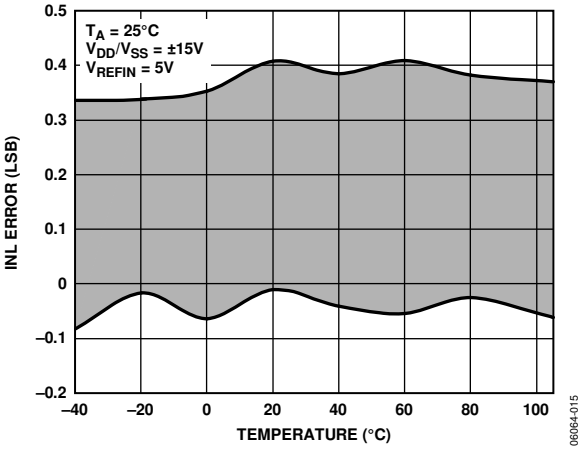

Figure 11. Integral Nonlinearity Error vs. Temperature, V_{DD}/V_{SS} = ±15 V

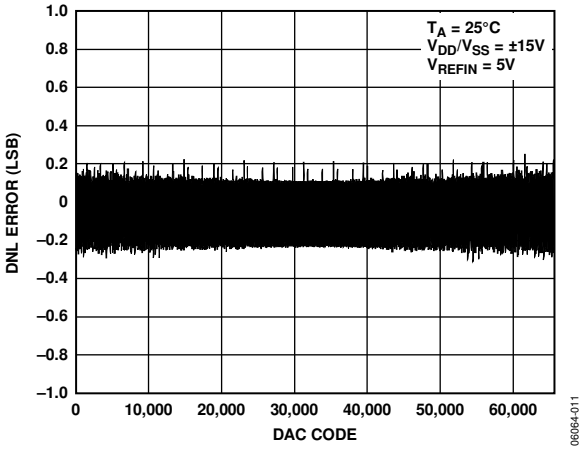

Figure 9. Differential Nonlinearity Error vs. DAC Code, V_{DD}/V_{SS} = ±15 V

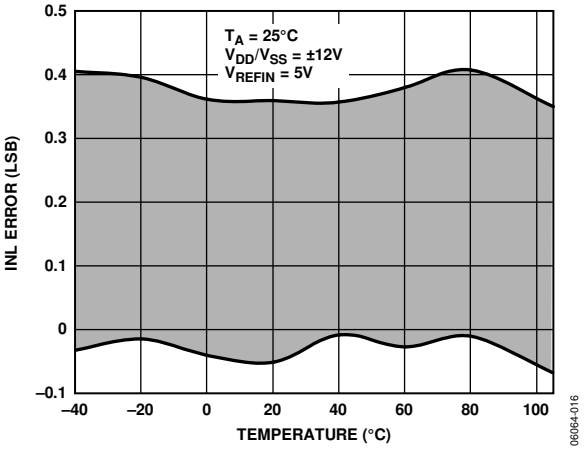

Figure 12. Integral Nonlinearity Error vs. Temperature, V_{DD}/V_{SS} = ±12 V

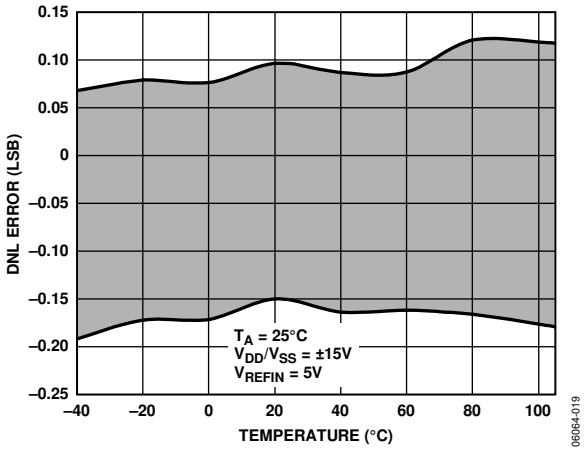

Figure 13. Differential Nonlinearity Error vs. Temperature, V_{DD}/V_{SS} = ±15 V

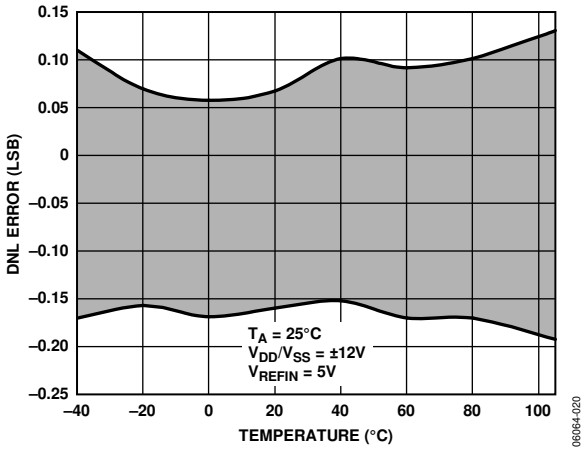

Figure 14. Differential Nonlinearity Error vs. Temperature, V_{DD}/V_{SS} = ±12 V

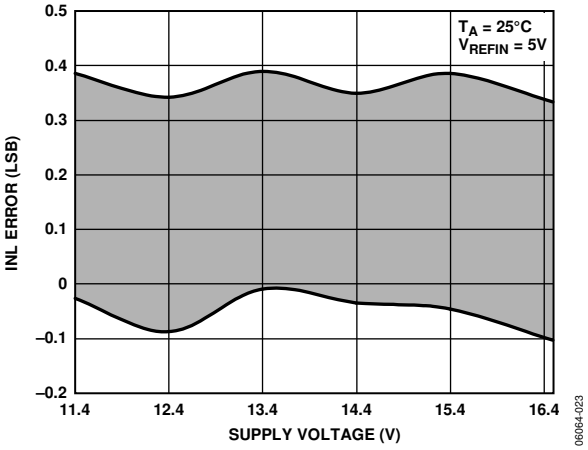

Figure 15. Integral Nonlinearity Error vs. Supply Voltage

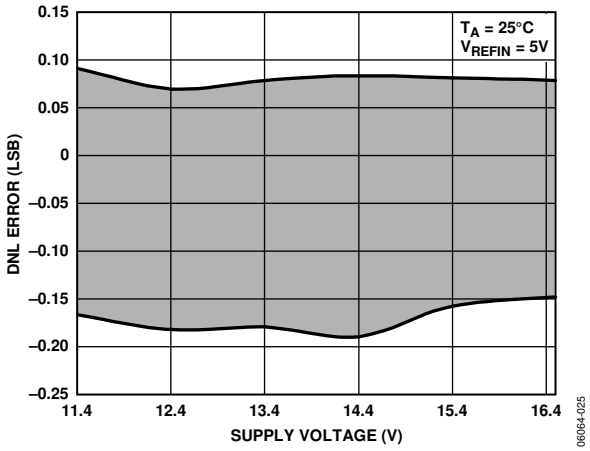

Figure 16. Differential Nonlinearity Error vs. Supply Voltage

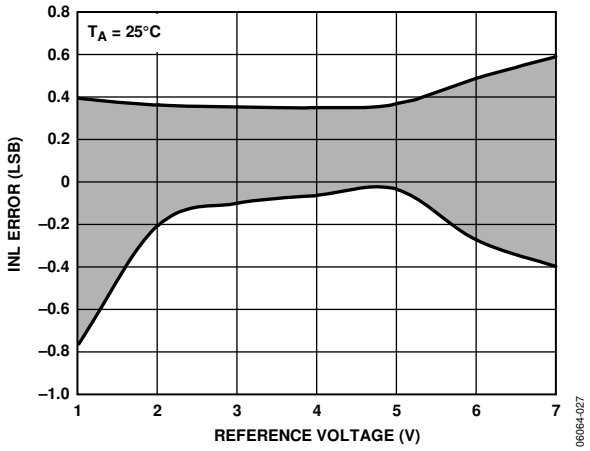

Figure 17. Integral Nonlinearity Error vs. Reference Voltage, V_{DD}/V_{SS} = ±16.5 V

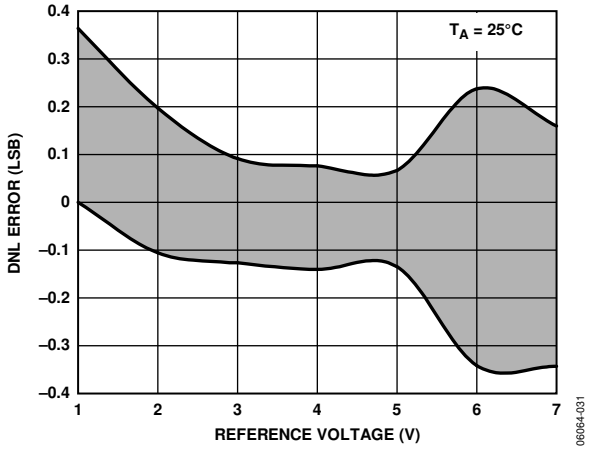

Figure 18. Differential Nonlinearity Error vs. Reference Voltage, V_{DD}/V_{SS} = ±16.5 V

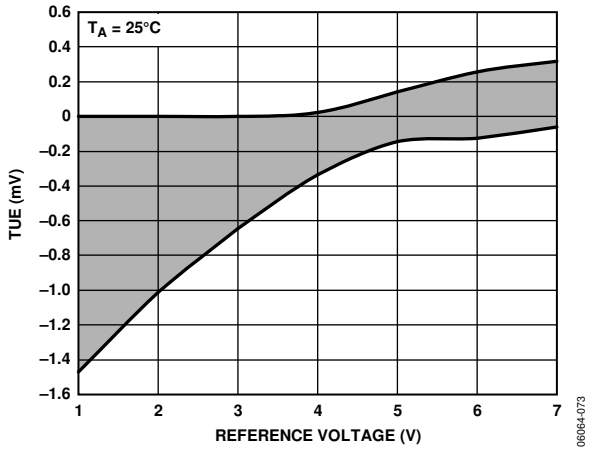

Figure 19. Total Unadjusted Error vs. Reference Voltage, V_{DD}/V_{SS} = ±16.5 V

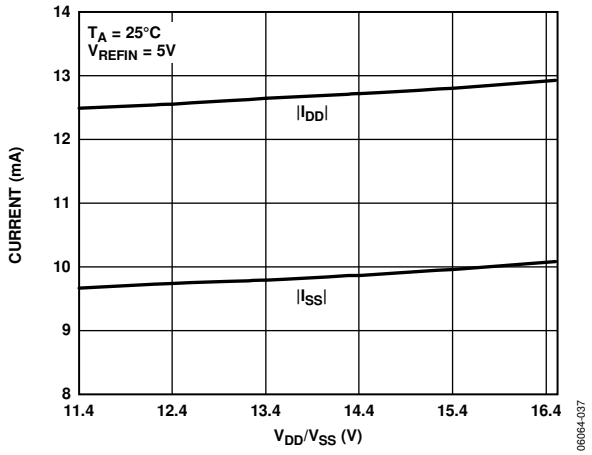

Figure 20. I_{DD}/I_{SS} vs. V_{DD}/V_{SS}

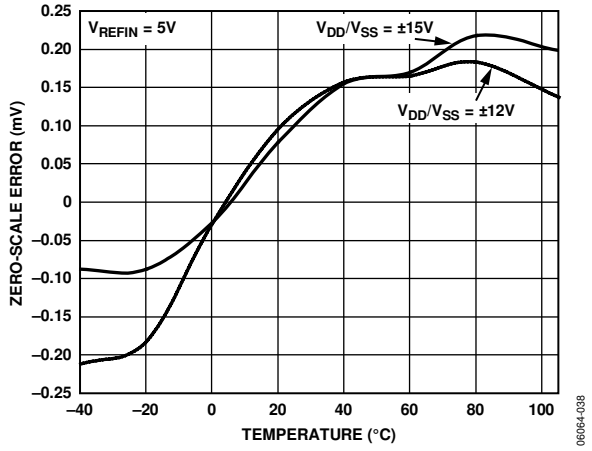

Figure 21. Zero-Scale Error vs. Temperature

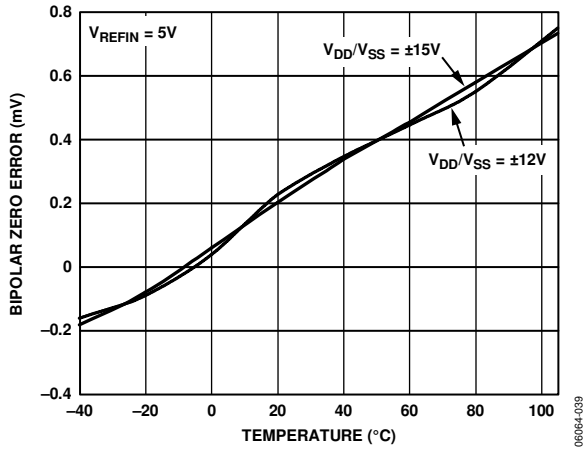

Figure 22. Bipolar Zero Error vs. Temperature

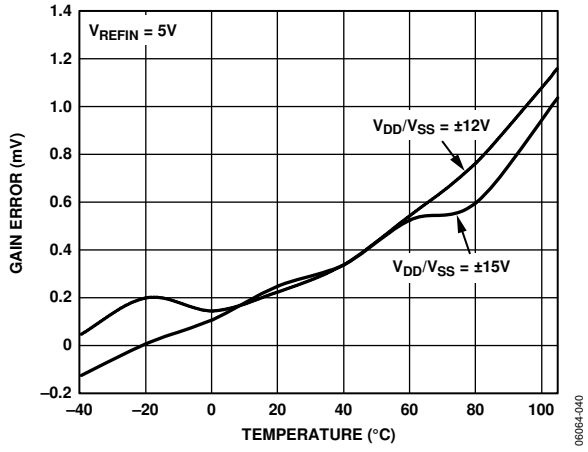

Figure 23. Gain Error vs. Temperature

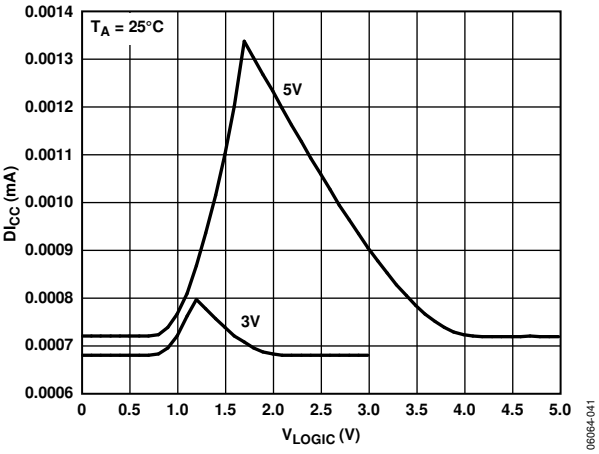

Figure 24. DI_{CC} vs. Logic Input Voltage

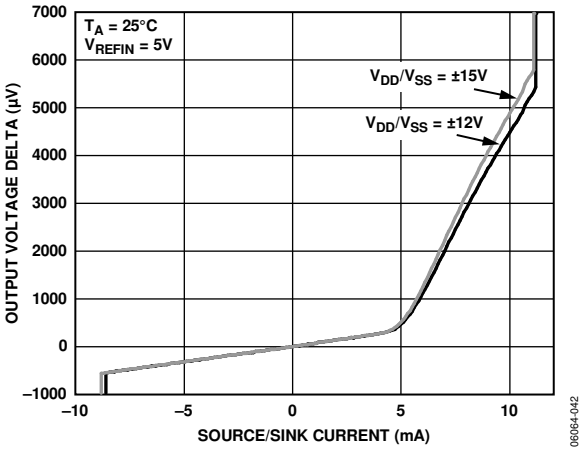

Figure 25. Source and Sink Capability of Output Amplifier with Positive Full Scale Loaded

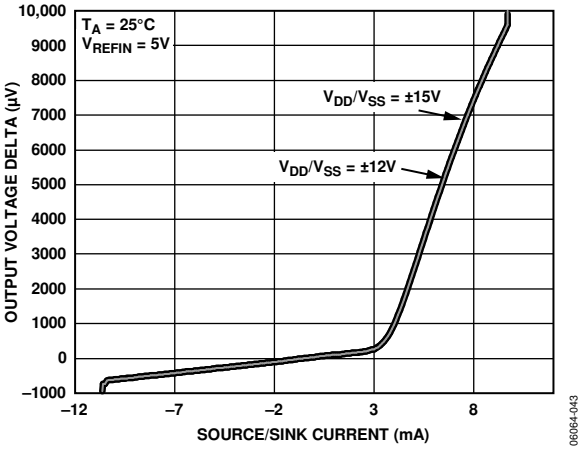

Figure 26. Source and Sink Capability of Output Amplifier with Negative Full Scale Loaded

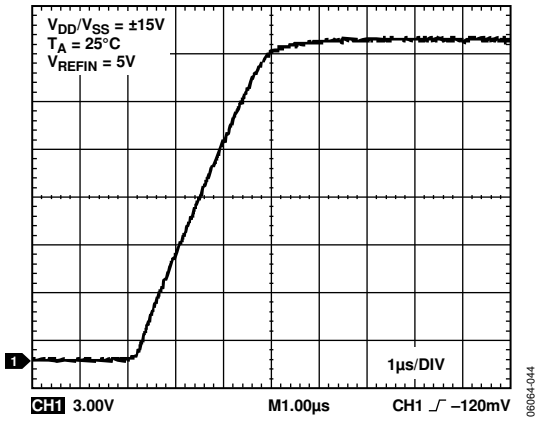

Figure 27. Full-Scale Settling Time

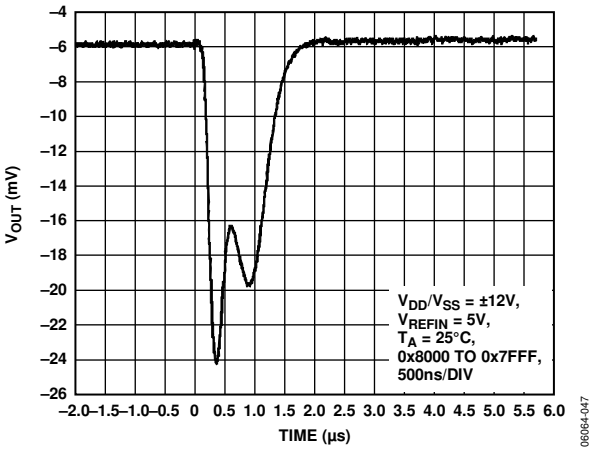

Figure 28. Major Code Transition Glitch Energy, V_{DD}/V_{SS} = ±12 V

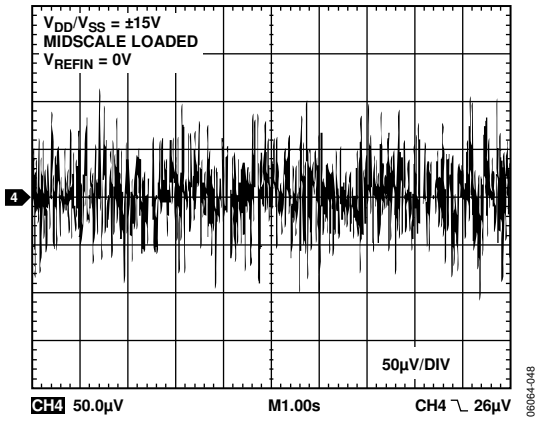

Figure 29. Peak-to-Peak Noise (100 kHz Bandwidth)

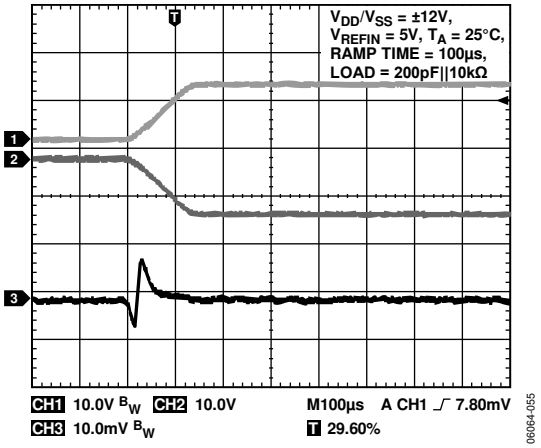

Figure 30. VOUTx vs. V_{DD}/V_{SS} on Power-Up

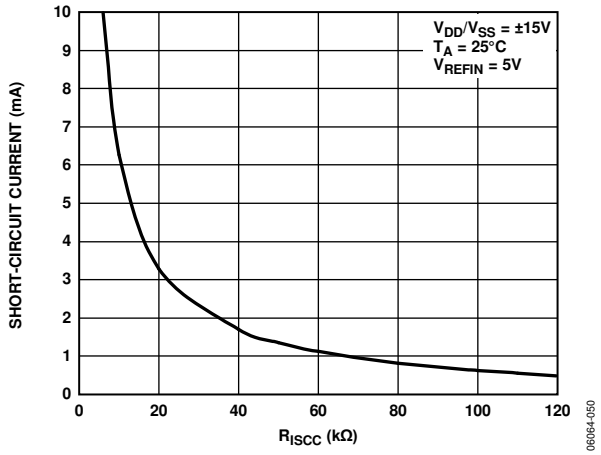

Figure 31. Short-Circuit Current vs. R_{ISCC}

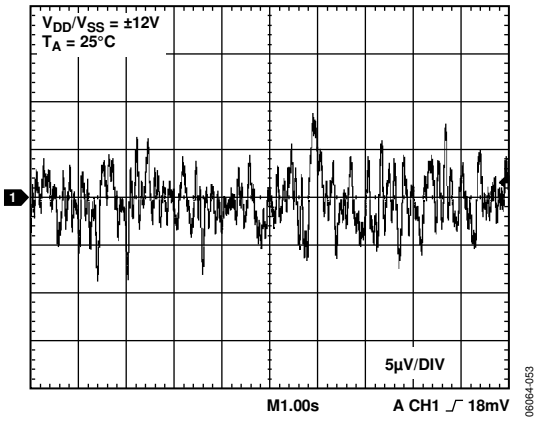

Figure 34. REFOUT Output Noise 0.1 Hz to 10 Hz

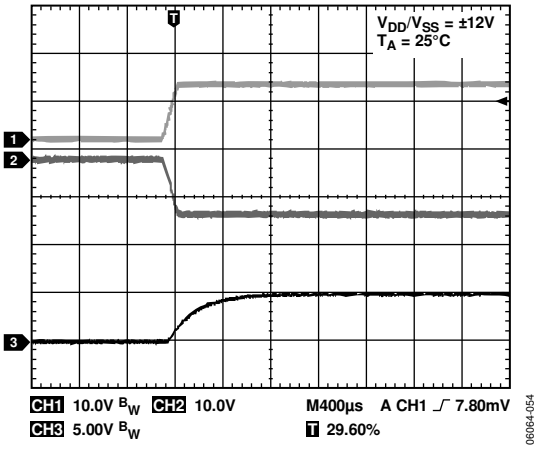

Figure 32. REFOUT Turn-On Transient

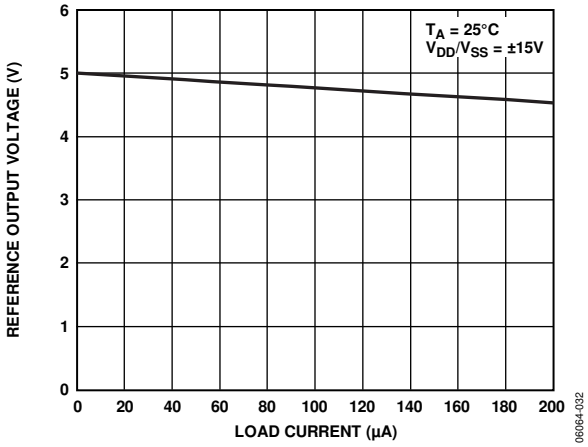

Figure 35. REFOUT Load Regulation

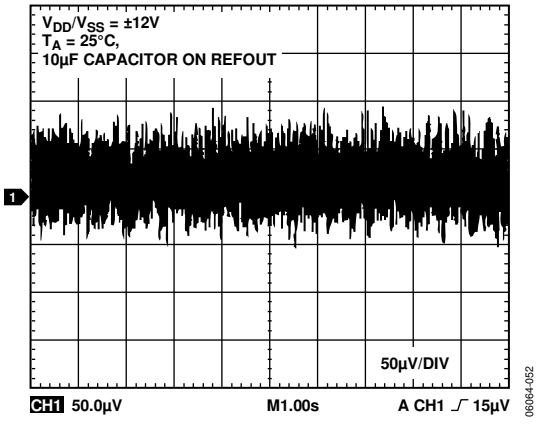

Figure 33. REFOUT Output Noise 100 kHz Bandwidth

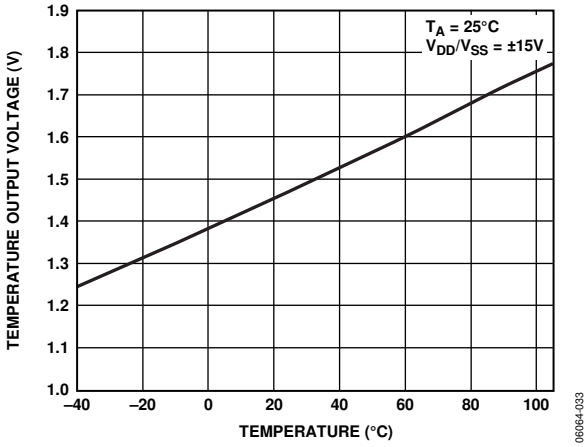

Figure 36. Temperature Output Voltage vs. Temperature

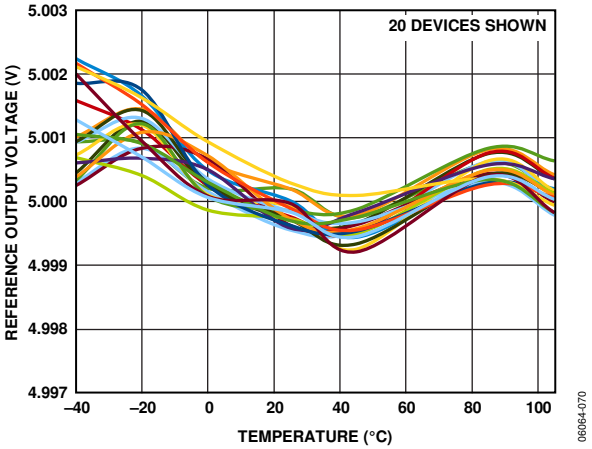

Figure 37. Reference Output Voltage vs. Temperature

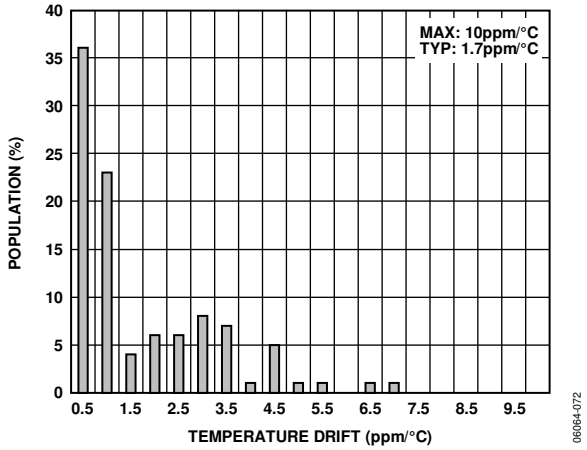

Figure 38. Reference Output Temperature Drift (–40°C to +85°C)

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)
The difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5744R is monotonic over its full operating temperature range.

Bipolar Zero Error
The deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (offset binary coding) or 0x0000 (twos complement coding). Figure 22 shows a plot of bipolar zero error vs. temperature.

Bipolar Zero Temperature Coefficient
The measure of the change in the bipolar zero error with a change in temperature. It is expressed as parts per million of full-scale range per degree Celsius (ppm FSR/°C).

Full-Scale Error
The measure of the output error when full-scale code is loaded to the data register. Ideally, the output voltage should be $2 \times V_{REFIN} - 1$ LSB. Full-scale error is expressed as a percentage of full-scale range (% FSR).

Negative Full-Scale Error/Zero-Scale Error
The error in the DAC output voltage when 0x0000 (offset binary coding) or 0x8000 (twos complement coding) is loaded to the data register. Ideally, the output voltage should be $-2 \times V_{REFIN}$. Figure 21 shows a plot of zero-scale error vs. temperature.

Output Voltage Settling Time
The amount of time it takes for the output to settle to a specified level for a full-scale input change.

Slew Rate
A limitation in the rate of change of the output voltage. The output slewing speed of a voltage-output DAC is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is given in volts per microsecond (V/µs).

Gain Error
A measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range (% FSR). Figure 23 shows a plot of gain error vs. temperature.

Total Unadjusted Error (TUE)
A measure of the output error, considering all the various errors. Figure 19 shows a plot of total unadjusted error vs. reference voltage.

Zero-Scale Error Temperature Coefficient
A measure of the change in zero-scale error with a change in temperature. It is expressed as parts per million of full-scale range per degree Celsius (ppm FSR/°C).

Gain Error Temperature Coefficient
A measure of the change in gain error with changes in temperature. It is expressed as parts per million of full-scale range per degree Celsius (ppm FSR/°C).

Digital-to-Analog Glitch Energy
The impulse injected into the analog output when the input code in the data register changes state. It is normally specified as the area of the glitch in nanovolt-seconds (nV-sec) and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000), as seen in Figure 28.

Digital Feedthrough
A measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but measured when the DAC output is not updated. It is specified in nanovolt-seconds (nV-sec) and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s, and vice versa.

Power Supply Sensitivity
Indicates how the output of the DAC is affected by changes in the power supply voltage.

DC Crosstalk
The dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC, and is expressed in least significant bits (LSBs).

DAC-to-DAC Crosstalk
The glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (from all 0s to all 1s, and vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nanovolt-seconds (nV-sec).

Channel-to-Channel Isolation
The ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in decibels (dB).

Reference Temperature Coefficient
A measure of the change in the reference output voltage with a change in temperature. It is expressed in parts per million per degree Celsius (ppm/°C).

Digital Crosstalk
A measure of the impulse injected into the analog output of one DAC from the digital inputs of another DAC but is measured when the DAC output is not updated. It is specified in nanovolt-seconds (nV-sec) and measured with a full-scale code change on the data bus; that is, from all 0s to all 1s, and vice versa.

Thermal Hysteresis
The change of reference output voltage after the device is cycled through temperatures from −40°C to +85°C and back to −40°C. This is a typical value from a sample of parts put through such a cycle.

THEORY OF OPERATION

The AD5764R is a quad, 16-bit, serial input, bipolar voltage output DAC that operates from supply voltages of ±11.4 V to ±16.5 V and has a buffered output voltage of up to ±10.5263 V. Data is written to the AD5764R in a 24-bit word format via a 3-wire serial interface. The AD5764R also offers an SDO pin that is available for daisy chaining or readback.

The AD5764R incorporates a power-on reset circuit that ensures that the data registers are loaded with 0x0000 at power-up. The AD5764R features a digital I/O port that can be programmed via the serial interface, an analog die temperature sensor, on-chip 10 ppm/°C voltage reference, on-chip reference buffers, and per channel digital gain and offset registers.

DAC ARCHITECTURE

The DAC architecture of the AD5764R consists of a 16-bit, current mode, segmented R-2R DAC. The simplified circuit diagram for the DAC section is shown in Figure 39.

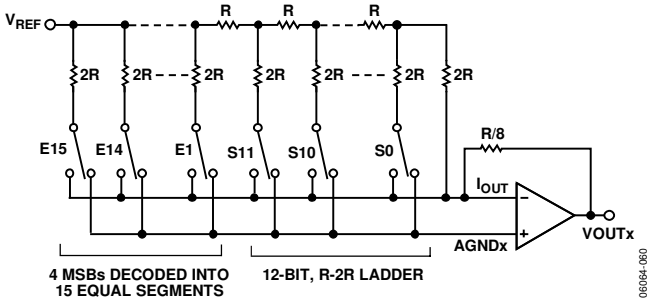

Figure 39. DAC Ladder Structure

The four MSBs of the 16-bit data-word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of the 15 matched resistors to either AGNDx or I_{OUT}. The remaining 12 bits of the data-word drive Switch S0 to Switch S11 of the 12-bit R-2R ladder network.

REFERENCE BUFFERS

The AD5764R can operate with either an external or an internal reference. The reference inputs (REFAB and REFCD) have an input range of up to 7 V. This input voltage is then used to provide a buffered positive and negative reference for the DAC cores. The positive reference is given by

$$+V_{REF} = 2 \times V_{REFIN}$$

The negative reference to the DAC cores is given by

$$-V_{REF} = -2 \times V_{REFIN}$$

These positive and negative reference voltages (along with the gain register values) define the output ranges of the DACs.

SERIAL INTERFACE

The AD5764R is controlled over a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device, MSB first, as a 24-bit word under the control of a serial clock input, SCLK. The input register consists of a read/write bit, a reserved bit that must be set to 0, three register select bits, three DAC address bits, and 16 data bits, as shown in Table 9. The timing diagram for this operation is shown in Figure 2.

Upon power-up, the data registers are loaded with zero code (0x0000) and the outputs are clamped to 0 V via a low impedance path. The outputs can be updated with the zero code value by asserting either $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$. The corresponding output voltage depends on the state of the BIN/$\overline{\text{2sCOMP}}$ pin. If the BIN/$\overline{\text{2sCOMP}}$ pin is tied to DGND, the data coding is twos complement and the outputs update to 0 V. If the BIN/$\overline{\text{2sCOMP}}$ pin is tied to DV_{CC}, the data coding is offset binary and the outputs update to negative full scale. To have the outputs power up with zero code loaded to the outputs, hold the $\overline{\text{CLR}}$ pin low during power-up.

Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can be used only if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. Exactly 24 falling clock edges must be applied to SCLK before $\overline{\text{SYNC}}$ is brought high again. If $\overline{\text{SYNC}}$ is brought high before the 24th falling SCLK edge, then the data written is invalid. If more than 24 falling SCLK edges are applied before $\overline{\text{SYNC}}$ is brought high, the input data is also invalid. The input register addressed is updated on the rising edge of $\overline{\text{SYNC}}$. For another serial transfer to take place, $\overline{\text{SYNC}}$ must be brought low again. After the end of the serial data transfer, data is automatically transferred from the input shift register to the addressed register.

When the data has been transferred into the chosen register of the addressed DAC, all data registers and outputs can be updated by taking $\overline{\text{LDAC}}$ low.

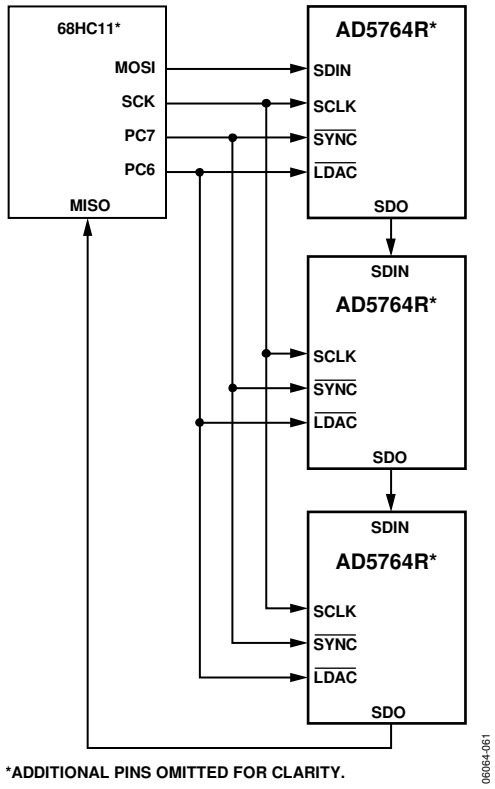

Figure 40. Daisy-Chaining the AD5764R

Daisy-Chain Operation

For systems that contain several devices, the SDO pin can be used to daisy-chain several devices together. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the input shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed.

Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24*n*, where *n* is the total number of AD5764R devices in the chain. When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register. The serial clock can be a continuous or a gated clock.

A continuous SCLK source can be used only if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data.

Readback Operation

Before a readback operation is initiated, the SDO pin must be enabled by writing to the function register and clearing the SDO disable bit; this bit is cleared by default. Readback mode is invoked by setting the R/$\overline{\text{W}}$ bit to 1 in the serial input register write. With R/$\overline{\text{W}}$ set to 1, Bit A2 to Bit A0, in association with Bit REG2 to Bit REG0, select the register to be read. The remaining data bits in the write sequence are don't care. During the next SPI write, the data appearing on the SDO output contains the data from the previously addressed register. For a read of a single register, the NOP command can be used in clocking out the data from the selected register on SDO. The readback diagram in Figure 4 shows the readback sequence. For example, to read back the fine gain register of Channel A, implement the following sequence:

1. Write 0xA0XXXX to the input shift register. This write configures the AD5764R for read mode with the fine gain register of Channel A selected. Note that all the data bits, DB15 to DB0, are don't care.
2. Follow with a second write: an NOP condition, 0x00XXXX. During this write, the data from the fine gain register is clocked out on the SDO line; that is, data clocked out contains the data from the fine gain register in Bit DB5 to Bit DB0.

SIMULTANEOUS UPDATING VIA $\overline{\text{LDAC}}$

Depending on the status of both $\overline{\text{SYNC}}$ and $\overline{\text{LDAC}}$, and after data has been transferred into the input register of the DACs, there are two ways to update the data registers and DAC outputs.

Individual DAC Updating

In individual DAC updating mode, $\overline{\text{LDAC}}$ is held low while data is being clocked into the input shift register. The addressed DAC output is updated on the rising edge of $\overline{\text{SYNC}}$.

Simultaneous Updating of All DACs

In simultaneous updating of all DACs mode, $\overline{\text{LDAC}}$ is held high while data is being clocked into the input shift register. All DAC outputs are updated by taking $\overline{\text{LDAC}}$ low any time after $\overline{\text{SYNC}}$ has been taken high. The update then occurs on the falling edge of $\overline{\text{LDAC}}$.

See Figure 41 for a simplified block diagram of the DAC load circuitry.

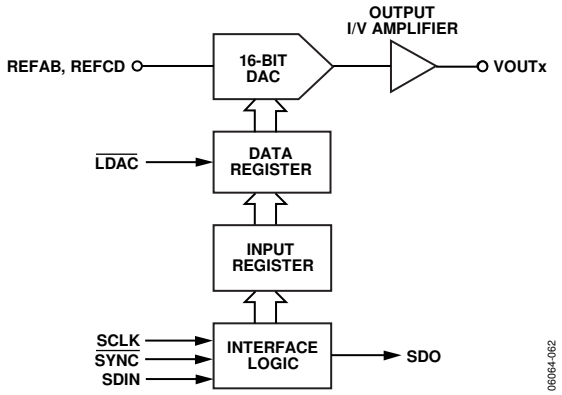

Figure 41. Simplified Serial Interface of Input Loading Circuitry for One DAC Channel

TRANSFER FUNCTION

Table 7 and Table 8 show the ideal input code to output voltage relationship for offset binary data coding and twos complement data coding, respectively.

The output voltage expression for the AD5764R is given by

$$V_{OUT} = -2 \times V_{REFIN} + 4 \times V_{REFIN} \left[\frac{D}{65{,}536} \right]$$

where:
D is the decimal equivalent of the code loaded to the DAC.
V_{REFIN} is the reference voltage applied at the REFAB and REFCD pins.

ASYNCHRONOUS CLEAR ($\overline{\text{CLR}}$)

$\overline{\text{CLR}}$ is a negative edge triggered clear that allows the outputs to be cleared to either 0 V (twos complement coding) or negative full scale (offset binary coding). It is necessary to maintain $\overline{\text{CLR}}$ low for a minimum amount of time for the operation to complete (see Figure 2). When the $\overline{\text{CLR}}$ signal is returned high, the output remains at the cleared value until a new value is programmed. If $\overline{\text{CLR}}$ is at 0 V at power-on, all DAC outputs are updated with the clear value. A clear can also be initiated through software by writing the command of 0x04XXXX.

Table 7. Ideal Output Voltage to Input Code Relationship—Offset Binary Data Coding

Digital Input				Analog Output
MSB			LSB	V_{OUT}
1111	1111	1111	1111	+2 V_{REFIN} × (32,767/32,768)
1000	0000	0000	0001	+2 V_{REFIN} × (1/32,768)
1000	0000	0000	0000	0 V
0111	1111	1111	1111	−2 V_{REFIN} × (1/32,768)
0000	0000	0000	0000	−2 V_{REFIN} × (32,767/32,768)

Table 8. Ideal Output Voltage to Input Code Relationship—Twos Complement Data Coding

Digital Input				Analog Output
MSB			LSB	V_{OUT}
0111	1111	1111	1111	+2 V_{REFIN} × (32,767/32,768)
0000	0000	0000	0001	+2 V_{REFIN} × (1/32,768)
0000	0000	0000	0000	0 V
1111	1111	1111	1111	−2 V_{REFIN} × (1/32,768)
1000	0000	0000	0000	−2 V_{REFIN} × (32,767/32,768)

REGISTERS

Table 9. Input Shift Register Format

MSB									LSB
DB23	**DB22**	**DB21**	**DB20**	**DB19**	**DB18**	**DB17**	**DB16**	**DB15 to DB1**	**DB0**
R/$\overline{W}$	0	REG2	REG1	REG0	A2	A1	A0	Data	

Table 10. Input Shift Register Bit Function Descriptions

Register Bit	Description			
R/$\overline{W}$	Indicates a read from or a write to the addressed register			
REG2, REG1, REG0	Used in association with the address bits, determines if a read or write operation is to the data register, offset register, gain registers, or function register			
	REG2	**REG1**	**REG0**	**Function**
	0	0	0	Function register
	0	1	0	Data register
	0	1	1	Coarse gain register
	1	0	0	Fine gain register
	1	0	1	Offset register
A2, A1, A0	Decodes the DAC channels			
	A2	**A1**	**A0**	**Channel Address**
	0	0	0	DAC A
	0	0	1	DAC B
	0	1	0	DAC C
	0	1	1	DAC D
	1	0	0	All DACs
Data	Data bits			

FUNCTION REGISTER

The function register is addressed by setting the three REG bits to 000. The values written to the address bits and the data bits determine the function addressed. The functions available via the function register are outlined in Table 11 and Table 12.

Table 11. Function Register Options

REG2	REG1	REG0	A2	A1	A0	DB15 to DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	NOP, data = don't care						
0	0	0	0	0	1	Don't care	Local ground offset adjust	D1 direction	D1 value	D0 direction	D0 value	SDO disable
0	0	0	1	0	0	Clear, data = don't care						
0	0	0	1	0	1	Load, data = don't care						

Table 12. Explanation of Function Register Options

Option	Description
NOP	No operation instruction used in readback operations.
Local Ground Offset Adjust	Set by the user to enable the local ground offset adjust function. Cleared by the user to disable the local ground offset adjust function (default). See the Design Features section for more information.
D0, D1 Direction	Set by the user to enable the D0 and D1 pins as outputs. Cleared by the user to enable the D0 and D1 pins as inputs (default). See the Design Features section for more information.
D0, D1 Value	I/O port status bits. Logic values written to these locations determine the logic outputs on the D0 and D1 pins when configured as outputs. These bits indicate the status of the D0 and D1 pins when the I/O port is active as an input. When enabled as inputs, these bits are don't cares during a write operation.
SDO Disable	Set by the user to disable the SDO output. Cleared by the user to enable the SDO output (default).
Clear	Addressing this function resets the DAC outputs to 0 V in twos complement mode and negative full scale in binary mode.
Load	Addressing this function updates the DAC registers and consequently the analog outputs.