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1 MSPS, 12-Bit Impedance Converter, Network Analyzer

Data Sheet

AD5933

FEATURES

- Programmable output peak-to-peak excitation voltage to a maximum frequency of 100 kHz
- Programmable frequency sweep capability with serial I²C interface
- Frequency resolution of 27 bits (<0.1 Hz)
- Impedance measurement range from 1 kΩ to 10 MΩ
- Capable of measuring of 100 Ω to 1 kΩ with additional circuitry
- Internal temperature sensor (±2°C)
- Internal system clock option
- Phase measurement capability
- System accuracy of 0.5%
- 2.7 V to 5.5 V power supply operation
- Temperature range: −40°C to +125°C
- 16-lead SSOP package
- Qualified for automotive applications

APPLICATIONS

- Electrochemical analysis
- Bioelectrical impedance analysis
- Impedance spectroscopy
- Complex impedance measurement
- Corrosion monitoring and protection equipment
- Biomedical and automotive sensors
- Proximity sensing
- Nondestructive testing
- Material property analysis
- Fuel/battery cell condition monitoring

GENERAL DESCRIPTION

The AD5933 is a high precision impedance converter system solution that combines an on-board frequency generator with a 12-bit, 1 MSPS, analog-to-digital converter (ADC). The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on-board ADC and a discrete Fourier transform (DFT) is processed by an on-board DSP engine. The DFT algorithm returns a real (R) and imaginary (I) data-word at each output frequency.

Once calibrated, the magnitude of the impedance and relative phase of the impedance at each frequency point along the sweep is easily calculated. This is done off chip using the real and imaginary register contents, which can be read from the serial I²C interface.

A similar device, also available from Analog Devices, Inc., is the AD5934, a 2.7 V to 5.5 V, 250 kSPS, 12-bit impedance converter, with an internal temperature sensor and is packaged in a 16-lead SSOP.

FUNCTIONAL BLOCK DIAGRAM

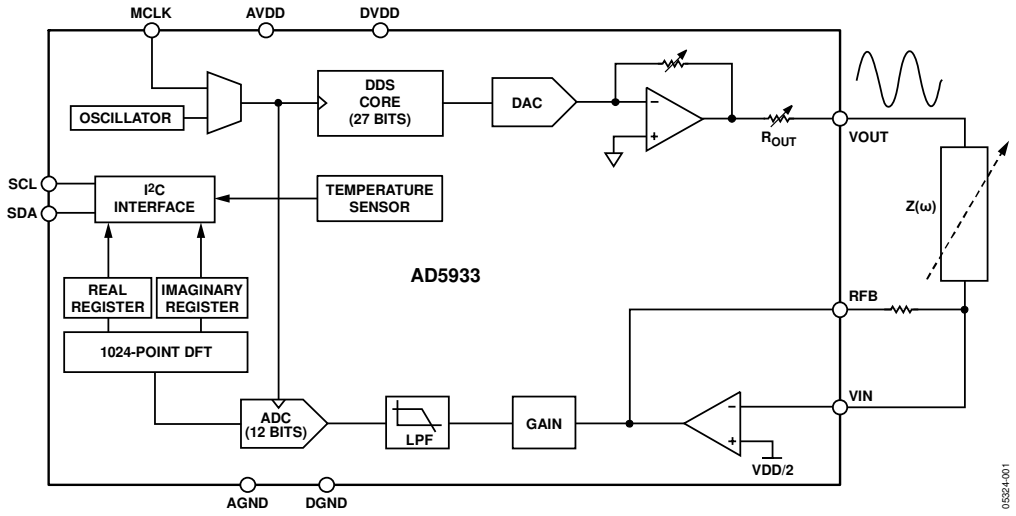

Figure 1.

Rev. F

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

AD5933* PRODUCT PAGE QUICK LINKS

Last Content Update: 04/25/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD5933 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1053: AD5933 Evaluation Board Example Measurement
- AN-1252: How to Configure the AD5933/AD5934
- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-280: Mixed Signal Circuit Technologies
- AN-342: Analog Signal-Handling for High Speed and Accuracy
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-419: A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850
- AN-423: Amplitude Modulation of the AD9850 Direct Digital Synthesizer
- AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
- AN-557: An Experimenter's Project:
- AN-587: Synchronizing Multiple AD9850/AD9851 DDS-Based Synthesizers
- AN-605: Synchronizing Multiple AD9852 DDS-Based Synthesizers
- AN-621: Programming the AD9832/AD9835
- AN-632: Provisionary Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-843: Measuring a Loudspeaker Impedance Profile Using the AD5933
- AN-847: Measuring a Grounded Impedance Profile Using the AD5933
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design

- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal
- AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

Data Sheet

- AD5933: 1 MSPS, 12-Bit Impedance Converter, Network Analyzer Data Sheet

Product Highlight

- Impedance-to-Digital Converters—Compact and Easy to Use
- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

User Guides

- UG-364: Evaluating the AD5933 1 MSPS, 12-Bit Impedance Converter Network Analyzer

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD5933 - No-OS Driver for Microchip Microcontroller Platforms
- AD5933 - No-OS Driver for Renesas Microcontroller Platforms
- AD5933 IIO Impedance Converter and Network Analyzer Linux Driver
- AD5933 Software Evaluation
- AD5933 Pmod Xilinx FPGA Reference Design

REFERENCE DESIGNS

- CN0217

REFERENCE MATERIALS

Technical Articles

- 400-MSample DDSs Run On Only +1.8 VDC
- ADI Buys Korean Mobile TV Chip Maker
- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Applications
- DDS Circuit Generates Precise PWM Waveforms
- DDS Design
- DDS Device Produces Sawtooth Waveform
- DDS Device Provides Amplitude Modulation
- DDS IC Initiates Synchronized Signals
- DDS IC Plus Frequency-To-Voltage Converter Make Low-Cost DAC
- DDS Simplifies Polar Modulation
- Digital Potentiometers Vary Amplitude In DDS Devices
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Waveform Generator Provides Flexible Frequency Tuning for Sensor Measurement
- Improved DDS Devices Enable Advanced Comm Systems
- Integrated DDS Chip Takes Steps To 2.7 GHz
- Simple Circuit Controls Stepper Motors
- Speedy A/Ds Demand Stable Clocks
- Synchronized Synthesizers Aid Multichannel Systems
- The Year of the Waveform Generator
- Two DDS ICs Implement Amplitude-shift Keying
- Video Portables and Cameras Get HDMI Outputs

DESIGN RESOURCES

- AD5933 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD5933 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

4/2017—Rev E to Rev F

Changes to Table 4 8
Changes to Table 12 25

5/2013—Rev. D to Rev. E

Added Automotive Information (Throughout) 1
Changed Sampling Rate from 250 kSPS to 1 MSPS 5
Changes to Table 7 21
Deleted Choosing a Reference for the AD5933 Section 34
Changes to Ordering Guide 40

12/2011—Rev. C to Rev. D

Changes to Impedance Error Section 19
Removed Figure 26 and Figure 27;
Renumbered Sequentially 19
Removed Figure 28, Figure 29, Figure 30, Figure 31 20
Changes to Figure 39 37
Changes to Figure 40 38
Changes to Figure 41 39
Changes to Figure 42 40

8/2010—Rev. B to Rev. C

Changes to Impedance Error Section 19
Changes to Figure 45 38
Changes to U4 Description in Table 19 42

2/2010—Rev. A to Rev. B

Changes to General Description 1

5/2008—Rev. 0 to Rev. A

Changes to Layout ..... Universal
Changes to Figure 1 1
Changes to Table 1 4
Changes to Figure 17 13
Changes to System Description Section 13
Changes to Figure 19 14
Changes to Figure 24 18
Changes to Impedance Error Section 19
Added Measuring the Phase Across an Impedance Section 21
Changes to Register Map Section 24
Added Measuring Small Impedances Section 31
Changes to Table 18 35
Added Evaluation Board Section 37
Changes to Ordering Guide 43

9/2005—Revision 0: Initial Version

SPECIFICATIONS

VDD = 3.3 V, MCLK = 16.776 MHz, 2 V p-p output excitation voltage @ 30 kHz, 200 kΩ connected between Pin 5 and Pin 6; feedback resistor = 200 kΩ connected between Pin 4 and Pin 5; PGA gain = ×1, unless otherwise noted.

Table 1.

	Y Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SYSTEM					
Impedance Range	1 K		10 M	Ω	100 Ω to 1 kΩ requires extra buffer circuitry, see the Measuring Small Impedances section
Total System Accuracy		0.5		%	2 V p-p output excitation voltage at 30 kHz, 200 kΩ connected between Pin 5 and Pin 6
System Impedance Error Drift		30		ppm/°C	
TRANSMIT STAGE					
Output Frequency Range[2]	1		100	kHz	
Output Frequency Resolution		0.1		Hz	<0.1 Hz resolution achievable using DDS techniques
MCLK Frequency			16.776	MHz	Maximum system clock frequency
Internal Oscillator Frequency[3]		16.776		MHz	Frequency of internal clock
Internal Oscillator Temperature Coefficient		30		ppm/°C	
TRANSMIT OUTPUT VOLTAGE					
Range 1					
AC Output Excitation Voltage[4]		1.98		V p-p	See Figure 4 for output voltage distribution
DC Bias[5]		1.48		V	DC bias of the ac excitation signal; see Figure 5
DC Output Impedance		200		Ω	T_A = 25°C
Short-Circuit Current to Ground at VOUT		±5.8		mA	T_A = 25°C
Range 2					
AC Output Excitation Voltage[4]		0.97		V p-p	See Figure 6
DC Bias[5]		0.76		V	DC bias of output excitation signal; see Figure 7
DC Output Impedance		2.4		kΩ	
Short-Circuit Current to Ground at VOUT		±0.25		mA	
Range 3					
AC Output Excitation Voltage[4]		0.383		V p-p	See Figure 8
DC Bias[5]		0.31		V	DC bias of output excitation signal; see Figure 9
DC Output Impedance		1		kΩ	
Short-Circuit Current to Ground at VOUT		±0.20		mA	
Range 4					
AC Output Excitation Voltage[4]		0.198		V p-p	See Figure 10
DC Bias[5]		0.173		V	DC bias of output excitation signal. See Figure 11
DC Output Impedance		600		Ω	
Short-Circuit Current to Ground at VOUT		±0.15		mA	
SYSTEM AC CHARACTERISTICS					
Signal-to-Noise Ratio		60		dB	
Total Harmonic Distortion		−52		dB	
Spurious-Free Dynamic Range					
Wide Band (0 MHz to 1 MHz)		−56		dB	
Narrow Band (±5 kHz)		−85		dB	

Parameter	Y Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVE STAGE					
Input Leakage Current		1		nA	To VIN pin
Input Capacitance[6]		0.01		pF	Pin capacitance between VIN and GND
Feedback Capacitance (C_{FB})		3		pF	Feedback capacitance around current-to-voltage amplifier; appears in parallel with feedback resistor
ANALOG-TO-DIGITAL CONVERTER[6]					
Resolution		12		Bits	
Sampling Rate		1		MSPS	ADC throughput rate
TEMPERATURE SENSOR					
Accuracy		±2.0		°C	−40°C to +125°C temperature range
Resolution		0.03		°C	
Temperature Conversion Time		800		µs	Conversion time of single temperature measurement
LOGIC INPUTS					
Input High Voltage (V_{IH})	0.7 × VDD				
Input Low Voltage (V_{IL})			0.3 × VDD		
Input Current[7]			1	µA	T_A = 25°C
Input Capacitance			7	pF	T_A = 25°C
POWER REQUIREMENTS					
VDD	2.7		5.5	V	
IDD (Normal Mode)		10	15	mA	VDD = 3.3 V
		17	25	mA	VDD = 5.5 V
IDD (Standby Mode)		11		mA	VDD = 3.3 V; see the Control Register (Register Address 0X80, Register Address 0X81) section
		16		mA	VDD = 5.5 V
IDD (Power-Down Mode)		0.7	5	µA	VDD = 3.3 V
		1	8	µA	VDD = 5.5 V

[1] Temperature range for Y version = −40°C to +125°C, typical at 25°C.
[2] The lower limit of the output excitation frequency can be lowered by scaling the clock supplied to the AD5933.
[3] Refer to Figure 14, Figure 15, and Figure 16 for the internal oscillator frequency distribution with temperature.
[4] The peak-to-peak value of the ac output excitation voltage scales with supply voltage according to the following formula:
Output Excitation Voltage (V p-p) = [2/3.3] × *VDD*
where *VDD* is the supply voltage.
[5] The dc bias value of the output excitation voltage scales with supply voltage according to the following formula:
Output Excitation Bias Voltage (V) = [2/3.3] × *VDD*
where *VDD* is the supply voltage.
[6] Guaranteed by design or characterization, not production tested. Input capacitance at the VOUT pin is equal to pin capacitance divided by open-loop gain of current-to-voltage amplifier.
[7] The accumulation of the currents into Pin 8, Pin 15, and Pin 16.

I²C SERIAL INTERFACE TIMING CHARACTERISTICS

VDD = 2.7 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter[2]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU, DAT}$, data setup time
t_6[3]	0.9	µs max	$t_{HD, DAT}$, data hold time
	0	µs min	$t_{HD, DAT}$, data hold time
t_7	0.6	µs min	$t_{SU, STA}$, setup time for repeated start
t_8	0.6	µs min	$t_{SU, STO}$, stop condition setup time
t_9	1.3	µs min	t_{BUF}, bus free time between a stop and a start condition
t_{10}	300	ns max	t_F, rise time of SDA when transmitting
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS compatible)
t_{11}	300	ns max	t_F, fall time of SCL and SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS compatible)
	250	ns max	t_F, fall time of SDA when receiving
	20 + 0.1 C_b[4]	ns min	t_F, fall time of SCL and SDA when transmitting
C_b	400	pF max	Capacitive load for each bus line

[1] See Figure 2.
[2] Guaranteed by design and characterization, not production tested.
[3] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to $V_{IH\ MIN}$ of the SCL signal) to bridge the undefined falling edge of SCL.
[4] C_b is the total capacitance of one bus line in picofarads. Note that t_R and t_F are measured between 0.3 VDD and 0.7 VDD.

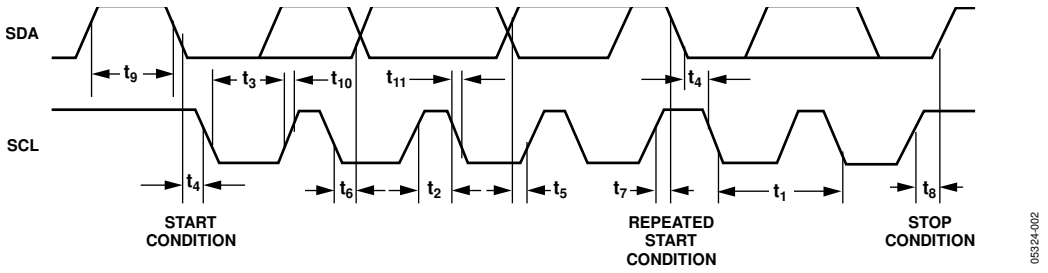

Figure 2. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
DVDD to GND	−0.3 V to +7.0 V
AVDD1 to GND	−0.3 V to +7.0 V
AVDD2 to GND	−0.3 V to +7.0 V
SDA/SCL to GND	−0.3 V to VDD + 0.3 V
VOUT to GND	−0.3 V to VDD + 0.3 V
VIN to GND	−0.3 V to VDD + 0.3 V
MCLK to GND	−0.3 V to VDD + 0.3 V
Operating Temperature Range	
Extended Industrial (Y Grade)	−40°C to +125°C
Storage Temperature Range	−65°C to +160°C
Maximum Junction Temperature	150°C
SSOP Package, Thermal Impedance	
θ_{JA}	139°C/W
θ_{JC}	136°C/W
Reflow Soldering (Pb-Free)	
Peak Temperature	260°C
Time at Peak Temperature	10 sec to 40 sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND DESCRIPTIONS

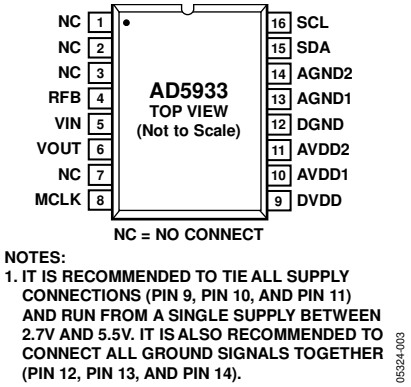

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3, 7	NC	No Connect. Do not connect to this pin.
4	RFB	External Feedback Resistor. Connected from Pin 4 to Pin 5 and used to set the gain of the current-to-voltage amplifier on the receive side.
5	VIN	Input to Receive Transimpedance Amplifier. Presents a virtual earth voltage of VDD/2.
6	VOUT	Excitation Voltage Signal Output.
8	MCLK	The master clock for the system is supplied by the user.
9	DVDD	Digital Supply Voltage.
10	AVDD1	Analog Supply Voltage 1.
11	AVDD2	Analog Supply Voltage 2.
12	DGND	Digital Ground.
13	AGND1	Analog Ground 1.
14	AGND2	Analog Ground 2.
15	SDA	I^2C Data Input. Open-drain pins requiring 10 kΩ pull-up resistors to VDD.
16	SCL	I^2C Clock Input. Open-drain pins requiring 10 kΩ pull-up resistors to VDD.

TYPICAL PERFORMANCE CHARACTERISTICS

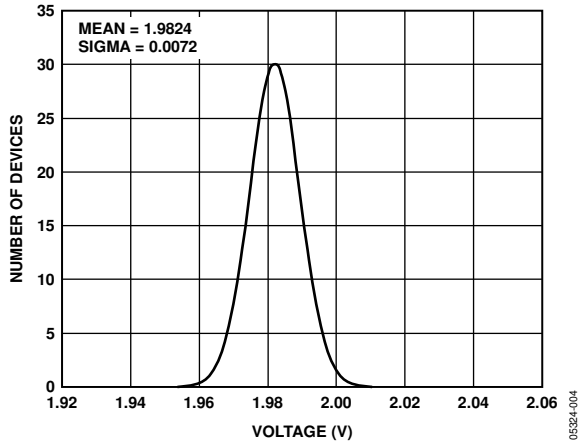

Figure 4. Range 1 Output Excitation Voltage Distribution, VDD = 3.3 V

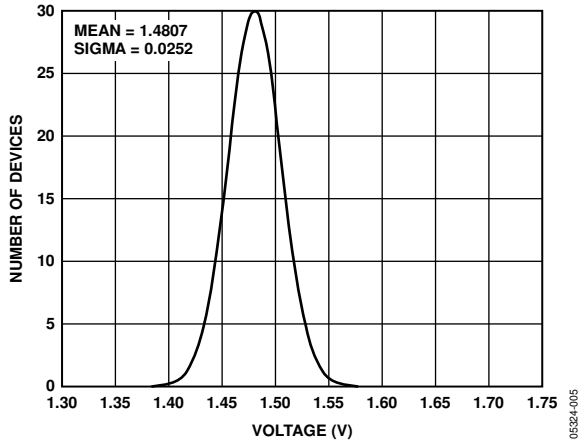

Figure 5. Range 1 DC Bias Distribution, VDD = 3.3 V

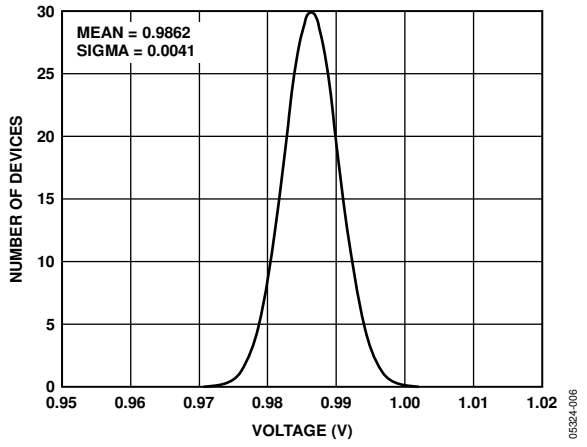

Figure 6. Range 2 Output Excitation Voltage Distribution, VDD = 3.3 V

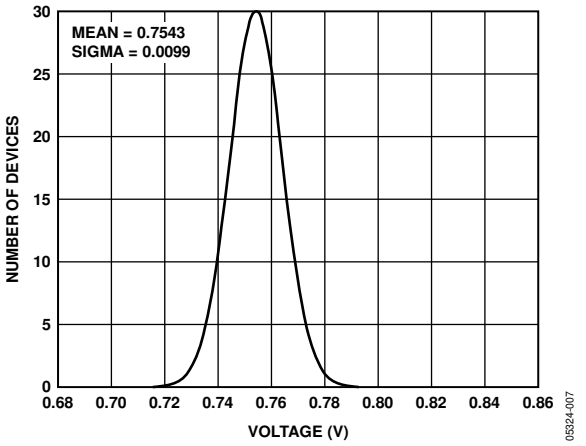

Figure 7. Range 2 DC Bias Distribution, VDD = 3.3 V

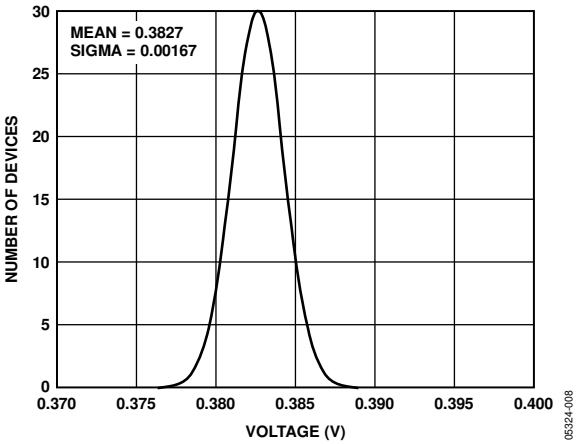

Figure 8. Range 3 Output Excitation Voltage Distribution, VDD = 3.3 V

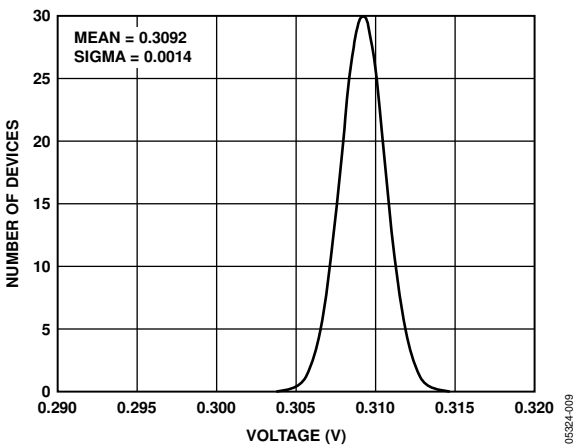

Figure 9. Range 3 DC Bias Distribution, VDD = 3.3 V

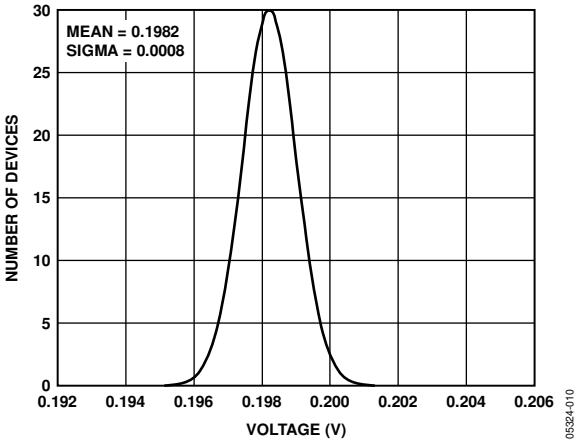

Figure 10. Range 4 Output Excitation Voltage Distribution, VDD = 3.3 V

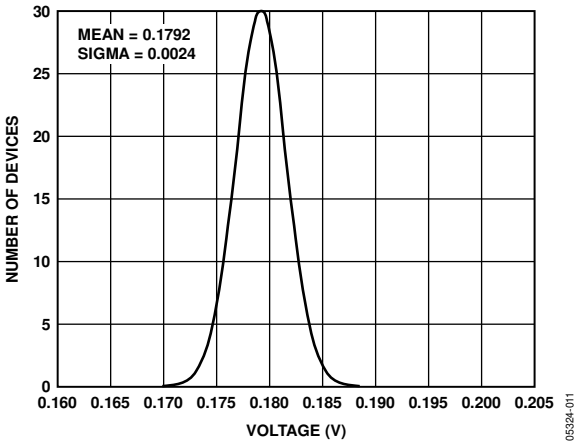

Figure 11. Range 4 DC Bias Distribution, VDD = 3.3 V

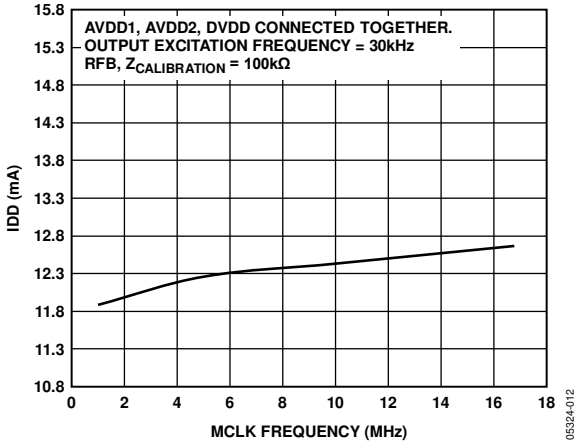

Figure 12. Typical Supply Current vs. MCLK Frequency

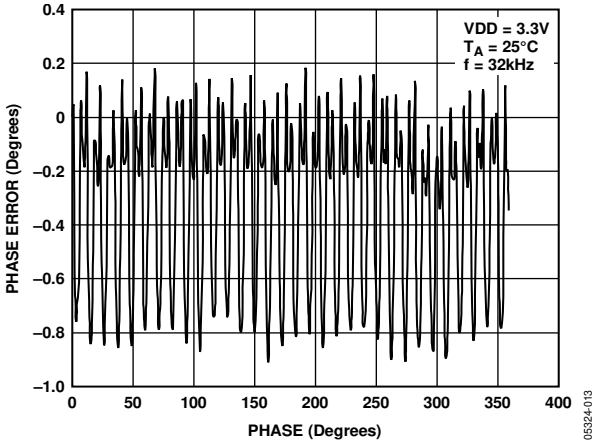

Figure 13. Typical Phase Error

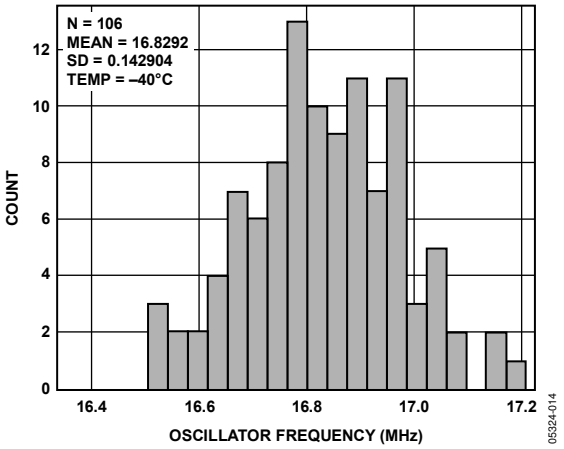

Figure 14. Frequency Distribution of Internal Oscillator at −40°C

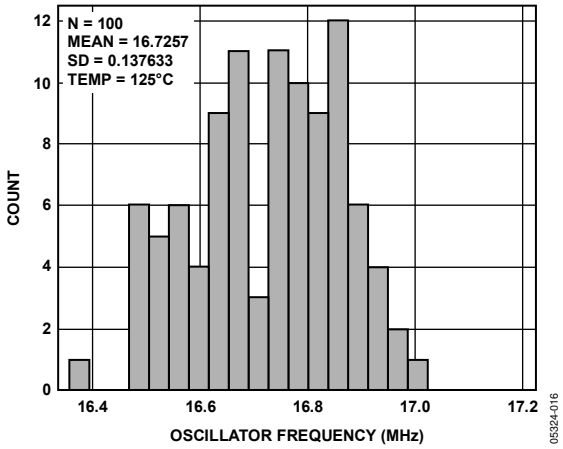

Figure 16. Frequency Distribution of Internal Oscillator at 125°C

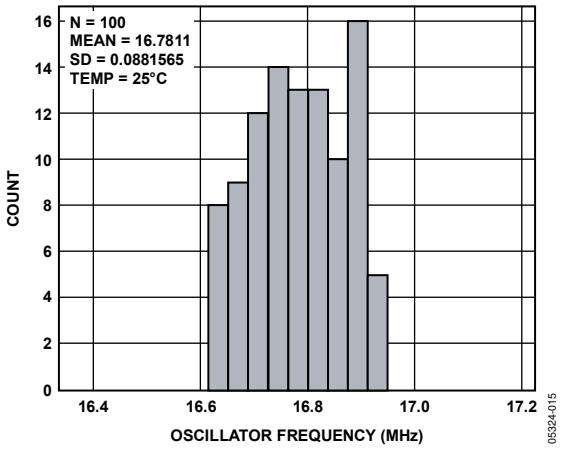

Figure 15. Frequency Distribution of Internal Oscillator at 25°C

TERMINOLOGY

Total System Accuracy
The AD5933 can accurately measure a range of impedance values to less than 0.5% of the correct impedance value for supply voltages between 2.7 V to 5.5 V.

Spurious-Free Dynamic Range (SFDR)
Along with the frequency of interest, harmonics of the fundamental frequency and images of these frequencies are present at the output of a DDS device. The spurious-free dynamic range refers to the largest spur or harmonic present in the band of interest. The wideband SFDR gives the magnitude of the largest harmonic or spur relative to the magnitude of the fundamental frequency in the 0 Hz to Nyquist bandwidth. The narrow-band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±200 kHz, about the fundamental frequency.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental, where V1 is the rms amplitude of the fundamental and V2, V3, V4, V5, and V6 are the rms amplitudes of the second through the sixth harmonics. For the AD5933, THD is defined as

$$THD\,(\text{dB}) = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + V5^2\ V6^2}}{V1}$$

SYSTEM DESCRIPTION

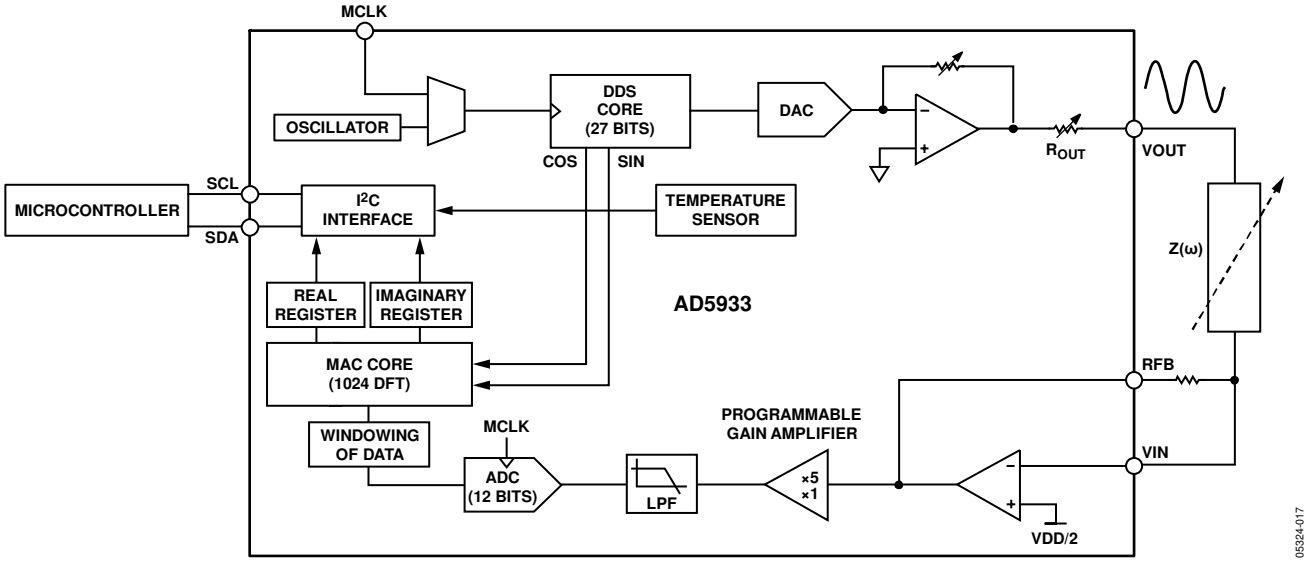

Figure 17. Block Overview

The AD5933 is a high precision impedance converter system solution that combines an on-board frequency generator with a 12-bit, 1 MSPS ADC. The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on-board ADC and DFT processed by an on-board DSP engine. The DFT algorithm returns both a real (R) and imaginary (I) data-word at each frequency point along the sweep. The impedance magnitude and phase are easily calculated using the following equations:

$$Magnitude = \sqrt{R^2 + I^2}$$

$$Phase = \tan^{-1}(I/R)$$

To characterize an impedance profile Z(ω), generally a frequency sweep is required, like that shown in Figure 18.

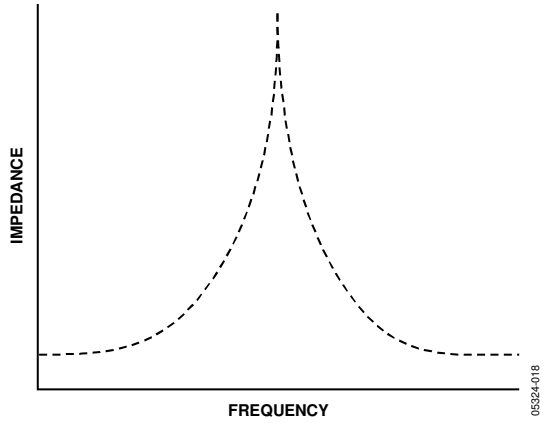

Figure 18. Impedance vs. Frequency Profile

The AD5933 permits the user to perform a frequency sweep with a user-defined start frequency, frequency resolution, and number of points in the sweep. In addition, the device allows the user to program the peak-to-peak value of the output sinusoidal signal as an excitation to the external unknown impedance connected between the VOUT and VIN pins.

Table 5 gives the four possible output peak-to-peak voltages and the corresponding dc bias levels for each range for 3.3 V. These values are ratiometric with VDD. So for a 5 V supply

$$Output\ Excitation\ Voltage\ for\ Range\ 1 = 1.98 \times \frac{5.0}{3.3} = 3\ \text{V p-p}$$

$$Output\ DC\ Bias\ Voltage\ for\ Range\ 1 = 1.48 \times \frac{5.0}{3.3} = 2.24\ \text{V p-p}$$

Table 5. Voltage Levels Respective Bias Levels for 3.3 V

Range	Output Excitation Voltage Amplitude	Output DC Bias Level
1	1.98 V p-p	1.48 V
2	0.97 V p-p	0.76 V
3	383 mV p-p	0.31 V
4	198 mV p-p	0.173 V

The excitation signal for the transmit stage is provided on-chip using DDS techniques that permit subhertz resolution. The receive stage receives the input signal current from the unknown impedance, performs signal processing, and digitizes the result. The clock for the DDS is generated from either an external reference clock, which is provided by the user at MCLK, or by the internal oscillator. The clock for the DDS is determined by the status of Bit D3 in the control register (see Register Address 0x81 in the Register Map section).

TRANSMIT STAGE

As shown in Figure 19, the transmit stage of the AD5933 is made up of a 27-bit phase accumulator DDS core that provides the output excitation signal at a particular frequency. The input to the phase accumulator is taken from the contents of the start frequency register (see Register Address 0x82, Register Address 0x83, and Register Address 0x84). Although the phase accumulator offers 27 bits of resolution, the start frequency register has the three most significant bits (MSBs) set to 0 internally; therefore, the user has the ability to program only the lower 24 bits of the start frequency register.

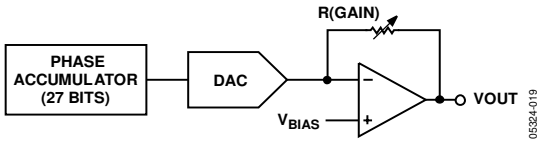

Figure 19. Transmit Stage

The AD5933 offers a frequency resolution programmable by the user down to 0.1 Hz. The frequency resolution is programmed via a 24-bit word loaded serially over the I²C interface to the frequency increment register.

The frequency sweep is fully described by the programming of three parameters: the start frequency, the frequency increment, and the number of increments.

Start Frequency

This is a 24-bit word that is programmed to the on-board RAM at Register Address 0x82, Register Address 0x83, and Register Address 0x84 (see the Register Map section). The required code loaded to the start frequency register is the result of the formula shown in Equation 1, based on the master clock frequency and the required start frequency output from the DDS.

$$Start\ Frequency\ Code = \left(\frac{Required\ Output\ Start\ Frequency}{\left(\frac{MCLK}{4} \right)} \right) \times 2^{27} \quad (1)$$

For example, if the user requires the sweep to begin at 30 kHz and has a 16 MHz clock signal connected to MCLK, the code that needs to be programmed is given by

$$Start\ Frequency\ Code = \left(\frac{30\ \text{kHz}}{\left(\frac{16\ \text{MHz}}{4} \right)} \right) \times 2^{27} \equiv 0\text{x}0\text{F}5\text{C}28$$

The user programs the value of 0x0F to Register Address 0x82, the value of 0x5C to Register Address 0x83, and the value of 0x28 to Register Address 0x84.

Frequency Increment

This is a 24-bit word that is programmed to the on-board RAM at Register Address 0x85, Register Address 0x86, and Register Address 0x87 (see the Register Map). The required code loaded to the frequency increment register is the result of the formula shown in Equation 2, based on the master clock frequency and the required increment frequency output from the DDS.

$$Frequency\ Increment\ Code = \left(\frac{Required\ Frequency\ Increment}{\left(\frac{MCLK}{4} \right)} \right) \times 2^{27} \quad (2)$$

For example, if the user requires the sweep to have a resolution of 10 Hz and has a 16 MHz clock signal connected to MCLK, the code that needs to be programmed is given by

$$Frequency\ Increment\ Code = \left(\frac{10\ \text{Hz}}{\left(\frac{16\ \text{MHz}}{4} \right)} \right) \equiv 0\text{x}00014\text{F}$$

The user programs the value of 0x00 to Register Address 0x85, the value of 0x01 to Register Address 0x86, and the value of 0x4F to Register Address 0x87.

Number of Increments

This is a 9-bit word that represents the number of frequency points in the sweep. The number is programmed to the on-board RAM at Register Address 0x88 and Register Address 0x89 (see the Register Map section). The maximum number of points that can be programmed is 511.

For example, if the sweep needs 150 points, the user programs the value of 0x00 to Register Address 0x88 and the value of 0x96 to Register Address 0x89.

Once the three parameter values have been programmed, the sweep is initiated by issuing a start frequency sweep command to the control register at Register Address 0x80 and Register Address 0x81 (see the Register Map section). Bit D2 in the status register (Register Address 0x8F) indicates the completion of the frequency measurement for each sweep point. Incrementing to the next frequency sweep point is under the control of the user. The measured result is stored in the two register groups that follow: 0x94, 0x95 (real data) and 0x96, 0x97 (imaginary data) that should be read before issuing an increment frequency command to the control register to move to the next sweep point. There is the facility to repeat the current frequency point measurement by issuing a repeat frequency command to the control register. This has the benefit of allowing the user to average successive readings. When the frequency sweep has completed all frequency points, Bit D3 in the status register is set, indicating completion of the sweep. Once this bit is set, further increments are disabled.

FREQUENCY SWEEP COMMAND SEQUENCE

The following sequence must be followed to implement a frequency sweep:

1. Enter standby mode. Prior to issuing a start frequency sweep command, the device must be placed in a standby mode by issuing an enter standby mode command to the control register (Register Address 0x80 and Register Address 0x81). In this mode, the VOUT and VIN pins are connected internally to ground so there is no dc bias across the external impedance or between the impedance and ground.
2. Enter initialize mode. In general, high Q complex circuits require a long time to reach steady state. To facilitate the measurement of such impedances, this mode allows the user full control of the settling time requirement before entering start frequency sweep mode where the impedance measurement takes place.
   An initialize with a start frequency command to the control register enters initialize mode. In this mode the impedance is excited with the programmed start frequency, but no measurement takes place. The user times out the required settling time before issuing a start frequency sweep command to the control register to enter the start frequency sweep mode.
3. Enter start frequency sweep mode. The user enters this mode by issuing a start frequency sweep command to the control register. In this mode, the ADC starts measuring after the programmed number of settling time cycles has elapsed. The user can program an integer number of output frequency cycles (settling time cycles) to Register Address 0x8A and Register Address 0x8B before beginning the measurement at each frequency point (see Figure 28).

The DDS output signal is passed through a programmable gain stage to generate the four ranges of peak-to-peak output excitation signals listed in Table 5. The peak-to-peak output excitation voltage is selected by setting Bit D10 and Bit D9 in the control register (see the Control Register (Register Address 0X80, Register Address 0X81) section) and is made available at the VOUT pin.

RECEIVE STAGE

The receive stage comprises a current-to-voltage amplifier, followed by a programmable gain amplifier (PGA), antialiasing filter, and ADC. The receive stage schematic is shown in Figure 20. The unknown impedance is connected between the VOUT and VIN pins. The first stage current-to-voltage amplifier configuration means that a voltage present at the VIN pin is a virtual ground with a dc value set at VDD/2. The signal current that is developed across the unknown impedance flows into the VIN pin and develops a voltage signal at the output of the current-to-voltage converter. The gain of the current-to voltage amplifier is determined by a user-selectable feedback resistor connected between Pin 4 (RFB) and Pin 5 (VIN). It is important for the user to choose a feedback resistance value that, in conjunction with the selected gain of the PGA stage, maintains the signal within the linear range of the ADC (0 V to VDD).

The PGA allows the user to gain the output of the current-to-voltage amplifier by a factor of 5 or 1, depending upon the status of Bit D8 in the control register (see the Register Map section, Register Address 0x80). The signal is then low-pass filtered and presented to the input of the 12-bit, 1 MSPS ADC.

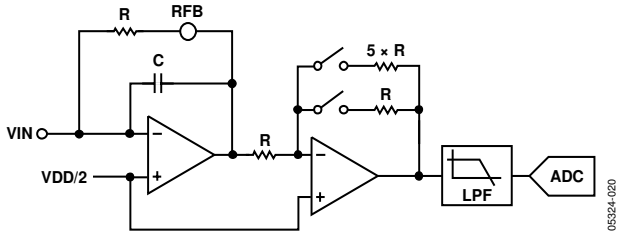

Figure 20. Receive Stage

The digital data from the ADC is passed directly to the DSP core of the AD5933, which performs a DFT on the sampled data.

DFT OPERATION

A DFT is calculated for each frequency point in the sweep. The AD5933 DFT algorithm is represented by

$$X(f) = \sum_{n=0}^{1023} (x(n)(\cos(n) - j\sin(n)))$$

where:
X(f) is the power in the signal at the Frequency Point f.
x(n) is the ADC output.
cos(*n*) and sin(*n*) are the sampled test vectors provided by the DDS core at the Frequency Point f.

The multiplication is accumulated over 1024 samples for each frequency point. The result is stored in two, 16-bit registers representing the real and imaginary components of the result. The data is stored in twos complement format.

SYSTEM CLOCK

The system clock for the AD5933 can be provided in one of two ways. The user can provide a highly accurate and stable system clock at the external clock pin (MCLK). Alternatively, the AD5933 provides an internal clock with a typical frequency of 16.776 MHz by means of an on-chip oscillator.

The user can select the preferred system clock by programming Bit D3 in the control register (Register Address 0x81, see Table 11). The default clock option on power-up is selected to be the internal oscillator.

The frequency distribution of the internal clock with temperature can be seen in Figure 14, Figure 15, and Figure 16.

TEMPERATURE SENSOR

The temperature sensor is a 13-bit digital temperature sensor with a 14th bit that acts as a sign bit. The on-chip temperature sensor allows an accurate measurement of the ambient device temperature to be made.

The measurement range of the sensor is −40°C to +125°C. At +150°C, the structural integrity of the device starts to deteriorate when operated at voltage and temperature maximum specifications. The accuracy within the measurement range is ±2°C.

TEMPERATURE CONVERSION DETAILS

The conversion clock for the part is internally generated; no external clock is required except when reading from and writing to the serial port. In normal mode, an internal clock oscillator runs an automatic conversion sequence.

The temperature sensor block defaults to a power-down state. To perform a measurement, a measure temperature command is issued by the user to the control register (Register Address 0x80 and Register Address 0x81). After the temperature operation is complete (typically 800 µs later), the block automatically powers down until the next temperature command is issued.

The user can poll the status register (Register Address 0x8F) to see if a valid temperature conversion has taken place, indicating that valid temperature data is available to read at Register Address 0x92 and Register Address 0x93 (see the Register Map section).

TEMPERATURE VALUE REGISTER

The temperature value register is a 16-bit, read-only register that stores the temperature reading from the ADC in 14-bit, twos complement format. The two MSB bits are don't cares. D13 is the sign bit. The internal temperature sensor is guaranteed to a low value limit of −40°C and a high value limit of +150°C. The digital output stored in Register Address 0x92 and Register Address 0x93 for the various temperatures is outlined in Table 6. The temperature sensor transfer characteristic is shown in Figure 21.

Table 6. Temperature Data Format

Temperature	Digital Output D13…D0
−40°C	11, 1011, 0000, 0000
−30°C	11, 1100, 0100, 0000
−25°C	11, 1100, 1110, 0000
−10°C	11, 1110, 1100, 0000
−0.03125°C	11, 1111, 1111, 1111
0°C	00, 0000, 0000, 0000
+0.03125°C	00, 0000, 0000, 0001
+10°C	00, 0001, 0100, 0000
+25°C	00, 0011, 0010, 0000
+50°C	00, 0110, 0100, 0000
+75°C	00, 1001, 0110, 0000
+100°C	00, 1100, 1000, 0000
+125°C	00, 1111, 1010, 0000
+150°C	01, 0010, 1100, 0000

TEMPERATURE CONVERSION FORMULA

Positive Temperature = ADC Code (D)/32

Negative Temperature = (*ADC Code* (*D*) – 16384)/32

where *ADC Code* uses all 14 bits of the data byte, including the sign bit.

Negative Temperature = (*ADC Code* (*D*) – 8192)/32

where *ADC Code (D)* is D13, the sign bit, and is removed from the ADC code.)

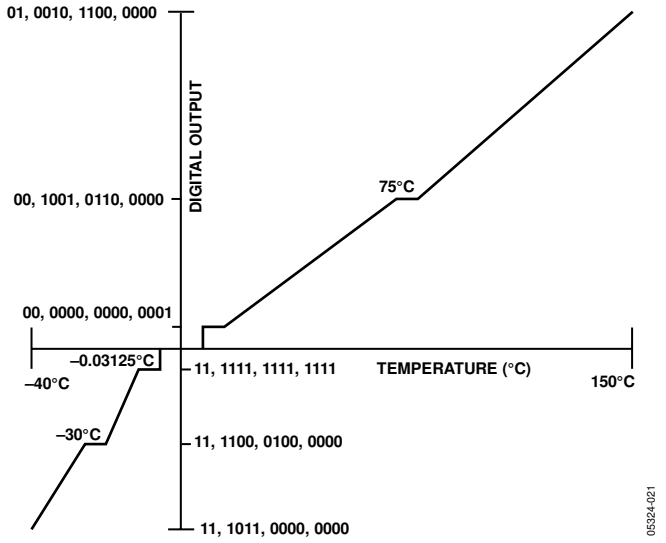

Figure 21. Temperature Sensor Transfer Function

IMPEDANCE CALCULATION

MAGNITUDE CALCULATION

The first step in impedance calculation for each frequency point is to calculate the magnitude of the DFT at that point.

The DFT magnitude is given by

$$Magnitude = \sqrt{R^2 + I^2}$$

where:
R is the real number stored at Register Address 0x94 and Register Address 0x95.
I is the imaginary number stored at Register Address 0x96 and Register Address 0x97.

For example, assume the results in the real data and imaginary data registers are as follows at a frequency point:

Real data register = 0x038B = 907 decimal

Imaginary data register = 0x0204 = 516 decimal

$$Magnitude = \sqrt{(907^2 + 516^2)} = 1043.506$$

To convert this number into impedance, it must be multiplied by
a scaling factor called the gain factor. The gain factor is calculated during the calibration of the system with a known impedance connected between the VOUT and VIN pins.

Once the gain factor has been calculated, it can be used in the calculation of any unknown impedance between the VOUT and VIN pins.

GAIN FACTOR CALCULATION

An example of a gain factor calculation follows, with the following assumptions:

Output excitation voltage = 2 V p-p

Calibration impedance value, $Z_{CALIBRATION}$ = 200 kΩ

PGA Gain = ×1

Current-to-voltage amplifier gain resistor = 200 kΩ

Calibration frequency = 30 kHz

Then typical contents of the real data and imaginary data registers after a frequency point conversion are:

Real data register = 0xF064 = −3996 decimal

Imaginary data register = 0x227E = +8830 decimal

$$Magnitude = \sqrt{(-3996)^2 + (8830)^2} = 9692.106$$

$$Gain\ Factor = \left(\frac{Admittance}{Code}\right) = \frac{\left(\frac{1}{Impedance}\right)}{Magnitude}$$

$$Gain\ Factor = \left(\frac{\frac{1}{200\ k\Omega}}{9692.106}\right) = 515.819 \times 10^{-12}$$

IMPEDANCE CALCULATION USING GAIN FACTOR

The next example illustrates how the calculated gain factor derived previously is used to measure an unknown impedance. For this example, assume that the unknown impedance = 510 kΩ.

After measuring the unknown impedance at a frequency of 30 kHz, assume that the real data and imaginary data registers contain the following data:

Real data register = 0xFA3F = −1473 decimal

Imaginary data register = 0x0DB3 = +3507 decimal

$$Magnitude = \sqrt{((-1473)^2 + (3507)^2)} = 3802.863$$

Then the measured impedance at the frequency point is given by

$$Impedance = \frac{1}{Gain\ Factor \times Magnitude}$$

$$= \frac{1}{515.819273 \times 10^{-12} \times 3802.863}\ \Omega = 509.791\ k\Omega$$

GAIN FACTOR VARIATION WITH FREQUENCY

Because the AD5933 has a finite frequency response, the gain factor also shows a variation with frequency. This variation in gain factor results in an error in the impedance calculation over a frequency range. Figure 22 shows an impedance profile based on a single-point gain factor calculation. To minimize this error, the frequency sweep should be limited to as small a frequency range as possible.

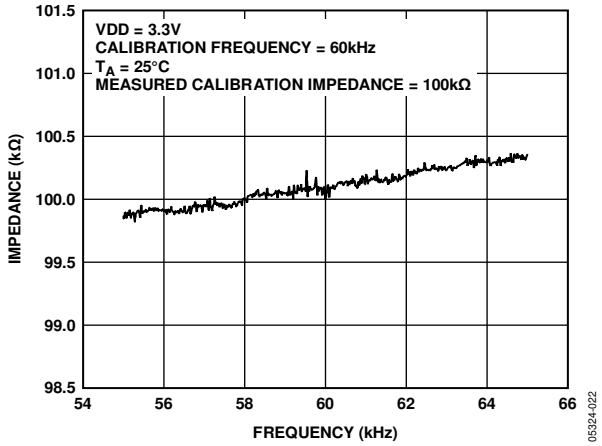

Figure 22. Impedance Profile Using a Single-Point Gain Factor Calculation

TWO-POINT CALIBRATION

Alternatively, it is possible to minimize this error by assuming that the frequency variation is linear and adjusting the gain factor with a two-point calibration. Figure 23 shows an impedance profile based on a two-point gain factor calculation.

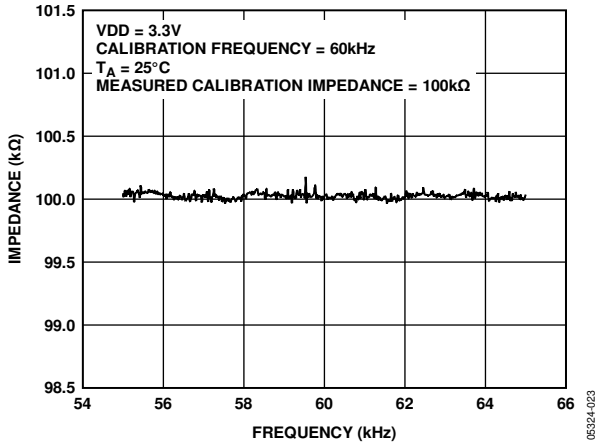

Figure 23. Impedance Profile Using a Two-Point Gain Factor Calculation

TWO-POINT GAIN FACTOR CALCULATION

This is an example of a two-point gain factor calculation assuming the following:

Output excitation voltage = 2 V (p-p)

Calibration impedance value, $Z_{UNKNOWN}$ = 100.0 kΩ

PGA gain = ×1

Supply voltage = 3.3 V

Current-to-voltage amplifier gain resistor = 100 kΩ

Calibration frequencies = 55 kHz and 65 kHz

Typical values of the gain factor calculated at the two calibration frequencies read

Gain factor calculated at 55 kHz is 1.031224E-09

Gain factor calculated at 65 kHz is 1.035682E-09

Difference in gain factor (ΔGF) is 1.035682E-09 – 1.031224E-09 = 4.458000E-12

Frequency span of sweep (ΔF) = 10 kHz

Therefore, the gain factor required at 60 kHz is given by

$$\left(\frac{4.458000\text{E-}12}{10\text{ kHz}} \times 5\text{ kHz}\right) + 1.031224 \times 10^{-9}$$

The required gain factor is 1.033453E-9.

The impedance is calculated as previously described.

GAIN FACTOR SETUP CONFIGURATION

When calculating the gain factor, it is important that the receive stage operate in its linear region. This requires careful selection of the excitation signal range, current-to-voltage gain resistor, and PGA gain.

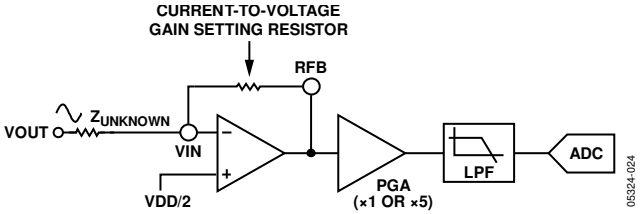

Figure 24. System Voltage Gain

The gain through the system shown in Figure 24 is given by

$$Ouput\ Excitation\ Voltage\ Range \times \frac{Gain\ Setting\ Resistor}{Z_{UNKNOWN}} \times PGA\ Gain$$

For this example, assume the following system settings:

VDD = 3.3 V

Gain setting resistor = 200 kΩ

$Z_{UNKNOWN}$ = 200 kΩ

PGA setting = ×1

The peak-to-peak voltage presented to the ADC input is 2 V p-p. However, if a PGA gain of ×5 was chose, the voltage would saturate the ADC.

GAIN FACTOR RECALCULATION

The gain factor must be recalculated for a change in any of the following parameters:

- Current-to-voltage gain setting resistor
- Output excitation voltage
- PGA gain

GAIN FACTOR TEMPERATURE VARIATION

The typical impedance error variation with temperature is in the order of 30 ppm/°C. Figure 25 shows an impedance profile with a variation in temperature for 100 kΩ impedance using a two-point gain factor calibration.

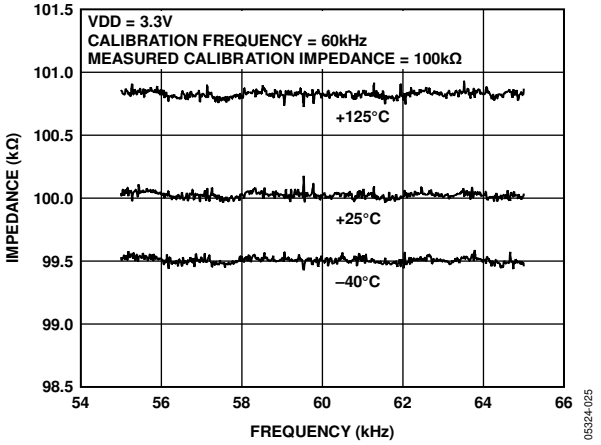

Figure 25. Impedance Profile Variation with Temperature Using a Two-Point Gain Factor Calibration

IMPEDANCE ERROR

It is important when reading the following section to note that the output impedance associated with the excitation voltages was actually measured and then calibrated out for each impedance error measurement. This was done using a Keithley current source/sink and measuring the voltage.

R_{OUT} (for example ,200 Ω specified for a 1.98 V p-p in the specification table) is only a typical specification and can vary from part to part. This method may not be achievable for large volume applications and in such cases, it is advised to use an extra low impedance output amplifier, as shown in Figure 4, to improve accuracy.

Please refer to CN-0217 for impedance accuracy examples on the AD5933 product web-page.

MEASURING THE PHASE ACROSS AN IMPEDANCE

The AD5933 returns a complex output code made up of separate real and imaginary components. The real component is stored at Register Address 0x94 and Register Address 0x95 and the imaginary component is stored at Register Address 0x96 and Register Address 0x97 after each sweep measurement. These correspond to the real and imaginary components of the DFT and not the resistive and reactive components of the impedance under test.

For example, it is a very common misconception to assume that if a user is analyzing a series RC circuit, the real value stored in Register Address 0x94 and Register Address 0x95 and the imaginary value stored at Register Address 0x96 and Register Address 0x97 correspond to the resistance and capacitive reactance, respectfully. However, this is incorrect because the magnitude of the impedance (|Z|) can be calculated by calculating the magnitude of the real and imaginary components of the DFT given by the following formula:

$$Magnitude = \sqrt{R^2 + I^2}$$

After each measurement, multiply it by the calibration term and invert the product. The magnitude of the impedance is, therefore, given by the following formula:

$$Impedance = \frac{1}{Gain\ Factor \times Magnitude}$$

Where gain factor is given by

$$Gain\ Factor = \left(\frac{Admittance}{Code}\right) = \frac{\left(\frac{1}{Impedance}\right)}{Magnitude}$$

The user must calibrate the AD5933 system for a known impedance range to determine the gain factor before any valid measurement can take place. Therefore, the user must know the impedance limits of the complex impedance ($Z_{UNKNOWN}$) for the sweep frequency range of interest. The gain factor is determined by placing a known impedance between the input/output of the AD5933 and measuring the resulting magnitude of the code. The AD5933 system gain settings need to be chosen to place the excitation signal in the linear region of the on-board ADC.

Because the AD5933 returns a complex output code made up of real and imaginary components, the user can also calculate the phase of the response signal through the AD5933 signal path. The phase is given by the following formula:

$$Phase(\text{rads}) = \tan^{-1}(I/R) \quad (3)$$

The phase measured by Equation 3 accounts for the phase shift introduced to the DDS output signal as it passes through the internal amplifiers on the transmit and receive side of the AD5933 along with the low-pass filter and also the impedance connected between the VOUT and VIN pins of the AD5933.

The parameters of interest for many users are the magnitude of the impedance ($|Z_{UNKNOWN}|$) and the impedance phase (ZØ). The measurement of the impedance phase (ZØ) is a two step process.

The first step involves calculating the AD5933 system phase. The AD5933 system phase can be calculated by placing a resistor across the VOUT and VIN pins of the AD5933 and calculating the phase (using Equation 3) after each measurement point in the sweep. By placing a resistor across the VOUT and VIN pins, there is no additional phase lead or lag introduced to the AD5933 signal path and the resulting phase is due entirely to the internal poles of the AD5933, that is, the system phase.

Once the system phase has been calibrated using a resistor, the second step involves calculating the phase of any unknown impedance by inserting the unknown impedance between the VIN and VOUT terminals of the AD5933 and recalculating the

new phase (including the phase due to the impedance) using the same formula. The phase of the unknown impedance (ZØ) is given by the following formula:

$$Z\text{Ø} = (\Phi\, unknown - \nabla system)$$

where:

$\nabla system$ is the phase of the system with a calibration resistor connected between VIN and VOUT.

Φ*unknown* is the phase of the system with the unknown impedance connected between VIN and VOUT.

ZØ is the phase due to the impedance, that is, the impedance phase.

Note that it is possible to calculate the gain factor and to calibrate the system phase using the same real and imaginary component values when a resistor is connected between the VOUT and VIN pins of the AD5933, for example, measuring the impedance phase (ZØ) of a capacitor.

The excitation signal current leads the excitation signal voltage across a capacitor by −90 degrees. Therefore, an approximate −90 degree phase difference exists between the system phase responses measured with a resistor and that of the system phase responses measured with a capacitive impedance.

As previously outlined, if the user would like to determine the phase angle of capacitive impedance (ZØ), the user first has to determine the system phase response (∇system) and subtract this from the phase calculated with the capacitor connected between VOUT and VIN (Φunknown).

A plot showing the AD5933 system phase response calculated using a 220 kΩ calibration resistor (R_{FB} = 220 kΩ, PGA = ×1) and the repeated phase measurement with a 10 pF capacitive impedance is shown in Figure 26.

One important point to note about the phase formula used to plot Figure 26 is that it uses the arctangent function that returns a phase angle in radians and, therefore, it is necessary to convert from radians to degrees.

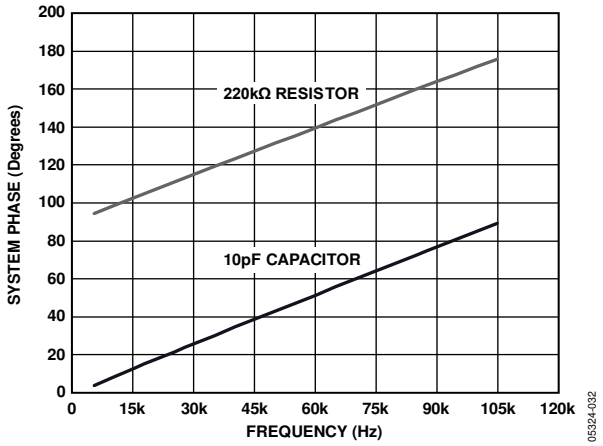

Figure 26. System Phase Response vs. Capacitive Phase

The phase difference (that is, ZØ) between the phase response of a capacitor and the system phase response using a resistor is the impedance phase of the capacitor, ZØ (see Figure 27).

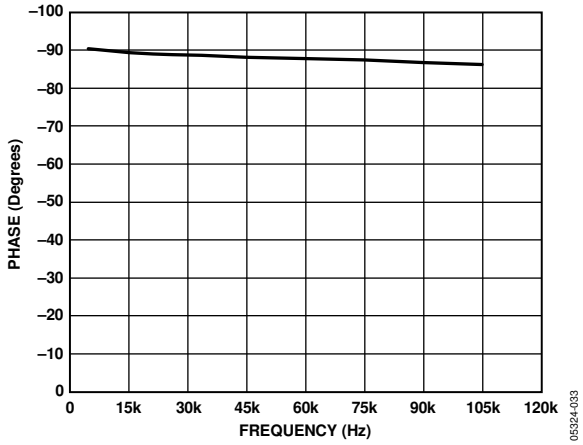

Figure 27. Phase Response of a Capacitor

Also when using the real and imaginary values to interpret the phase at each measurement point, take care when using the arctangent formula. The arctangent function returns the correct standard phase angle only when the sign of the real and imaginary values are positive, that is, when the coordinates lie in the first quadrant. The standard angle is the angle taken counterclockwise from the positive real x-axis. If the sign of the real component is positive and the sign of the imaginary component is negative, that is, the data lies in the second quadrant, then the arctangent formula returns a negative angle and it is necessary to add a further 180 degrees to calculate the correct standard angle. Likewise, when the real and imaginary components are both negative, that is, when the coordinates lie in the third quadrant, then the arctangent formula returns a positive angle and it is necessary to add 180 degrees from the angle to return the correct standard phase. Finally, when the real component is positive and the imaginary component is negative, that is, the data lies in the fourth quadrant, then the arctangent formula returns a negative angle. It is necessary to add 360 degrees to the angle to calculate the correct phase angle.

Therefore, the correct standard phase angle is dependent upon the sign of the real and imaginary component and is summarized in Table 7.

Once the magnitude of the impedance (|Z|) and the impedance phase angle (ZØ, in radians) are correctly calculated, it is possible to determine the magnitude of the real (resistive) and imaginary (reactive) component of the impedance ($Z_{UNKNOWN}$) by the vector projection of the impedance magnitude onto the real and imaginary impedance axis using the following formulas:

The real component is given by

$$|Z_{REAL}| = |Z| \times \cos(Z\text{Ø})$$

The imaginary component is given by

$$|Z_{IMAG}| = |Z| \times \sin(Z\text{Ø})$$

Table 7. Phase Angle

Real	Imaginary	Quadrant	Phase Angle
Positive	Positive	First	$\tan^{-1}(I/R) \times \frac{180^\circ}{\pi}$
Negative	Positive	Second	$180^\circ + \left(\tan^{-1}(I/R) \times \frac{180^\circ}{\pi} \right)$
Negative	Negative	Third	$180^\circ + \left(\tan^{-1}(I/R) \times \frac{180^\circ}{\pi} \right)$
Positive	Negative	Fourth	$360^\circ + \left(\tan^{-1}(I/R) \times \frac{180^\circ}{\pi} \right)$

PERFORMING A FREQUENCY SWEEP

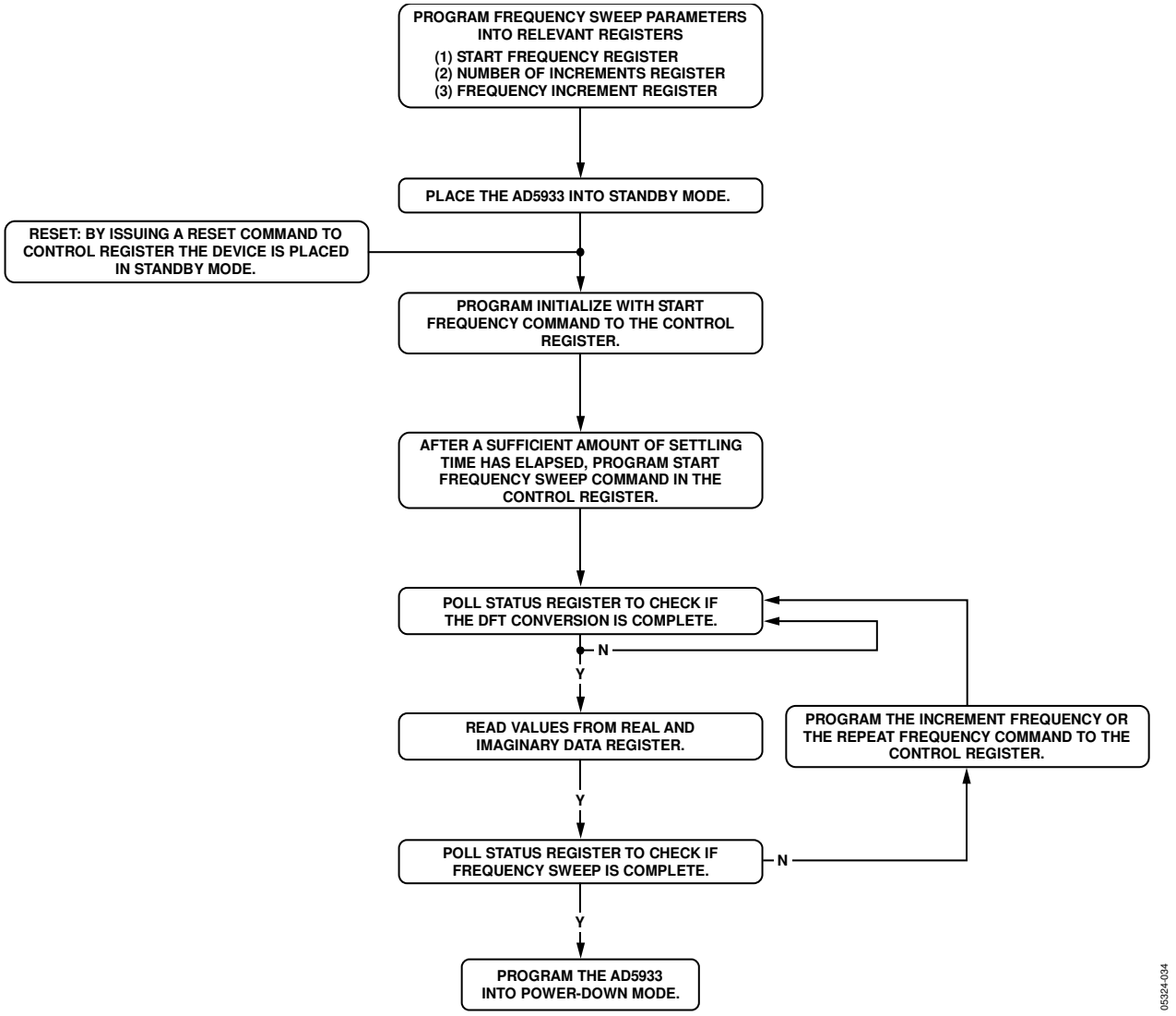

Figure 28. Frequency Sweep Flow Chart