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67 MSPS Digital Receive Signal Processor

AD6620

FEATURES

High Input Sample Rate
- 67 MSPS Single Channel Real
- 33.5 MSPS Diversity Channel Real
- 33.5 MSPS Single Channel Complex

NCO Frequency Translation
- Worst Spur Better than –100 dBc
- Tuning Resolution Better than 0.02 Hz

2nd Order Cascaded Integrator Comb FIR Filter
- Linear Phase, Fixed Coefficients
- Programmable Decimation Rates: 2, 3 . . . 16

5th Order Cascaded Integrator Comb FIR Filter
- Linear Phase, Fixed Coefficients
- Programmable Decimation Rates: 1, 2, 3 . . . 32

Programmable Decimating RAM Coefficient FIR Filter
- Up to 134 Million Taps per Second
- 256 20-Bit Programmable Coefficients
- Programmable Decimation Rates: 1, 2, 3 . . . 32

Bidirectional Synchronization Circuitry
- Phase Aligns NCOs
- Synchronizes Data Output Clocks

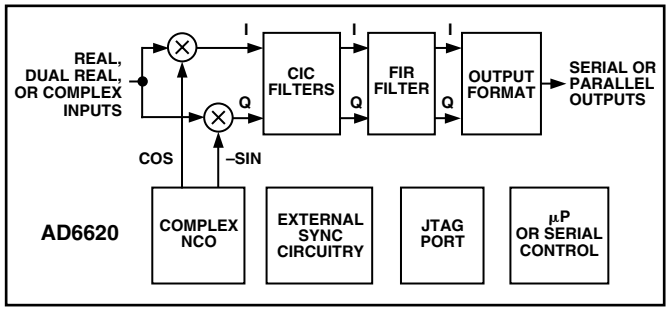
Serial or Parallel Baseband Outputs
- Pin Selectable Serial or Parallel
- Serial Works with SHARC®, ADSP-21xx, Most Other DSPs
- 16-Bit Parallel Port, Interleaved I and Q Outputs

Two Separate Control and Configuration Ports
- Generic µP Port, Serial Port

3.3 V Optimized CMOS Process

JTAG Boundary Scan

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD6620 is a digital receiver with four cascaded signal-processing elements: a frequency translator, two fixed-coefficient decimating filters, and a programmable coefficient decimating filter. All inputs are 3.3 V LVCMOS compatible. All outputs are LVCMOS and 5 V TTL compatible.

As ADCs achieve higher sampling rates and dynamic range, it becomes increasingly attractive to accomplish the final IF stage of a receiver in the digital domain. Digital IF Processing is less expensive, easier to manufacture, more accurate, and more flexible than a comparable highly selective analog stage.

The AD6620 diversity channel decimating receiver is designed to bridge the gap between high-speed ADCs and general purpose DSPs. The high resolution NCO allows a single carrier to be selected from a high speed data stream. High dynamic range decimation filters with a wide range of decimation rates allow both narrowband and wideband carriers to be extracted. The RAM-based architecture allows easy reconfiguration for multi-mode applications.

The decimating filters remove unwanted signals and noise from the channel of interest. When the channel of interest occupies less bandwidth than the input signal, this rejection of out-of-band noise is called "processing gain." By using large decimation factors, this "processing gain" can improve the SNR of the ADC by 36 dB or more. In addition, the programmable RAM Coefficient filter allows antialiasing, matched filtering, and static equalization functions to be combined in a single, cost-effective filter.

The input port accepts a 16-bit Mantissa, a 3-bit Exponent, and an A/B Select pin. These allow direct interfacing with the AD6600, AD6640, AD6644, AD9042 and most other high-speed ADCs. Three input modes are provided: Single Channel Real, Single Channel Complex, and Diversity Channel Real.

When paired with an interleaved sampler such as the AD6600, the AD6620 can process two data streams in the Diversity Channel Real input mode. Each channel is processed with coherent frequency translation and output sample clocks. In addition, external synchronization pins are provided to facilitate coherent frequency translation and output sample clocks among several AD6620s. These features can ease the design of systems with diversity antennas or antenna arrays.

Units are packaged in an 80-lead PQFP (plastic quad flatpack) and specified to operate over the industrial temperature range (–40°C to +85°C).

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REV. A

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AD6620* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-502: Designing A Superheterodyne Receiver Using an IF Sampling Diversity Chipset
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design

Data Sheet

- AD6620: 65 MSPS Digital Receive Signal Processor Data Sheet

Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

REFERENCE MATERIALS

Technical Articles

- Basics of Designing a Digital Radio Receiver (Radio 101)
- Designing a Super-Heterodyne Multi-Channel Digital Receiver
- Designing Filters with the AD6620
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Smart Partitioning Eyes 3G Basestation

DESIGN RESOURCES

- AD6620 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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TABLE OF CONTENTS

ARCHITECTURE

As shown in Figure 1, the AD6620 has four main signal processing stages: a Frequency Translator, two Cascaded Integrator Comb FIR Filters (CIC2, CIC5), and a RAM Coefficient FIR Filter (RCF). Multiple modes are supported for clocking data into and out of the chip. Programming and control is accomplished via serial and microprocessor interfaces.

Input data to the chip may be real or complex. If the input data is real, it may be clocked in as a single channel or interleaved with a second channel. The two-channel input mode, called Diversity Channel Real, is typically used in diversity receiver applications. Input data is clocked in 16-bit parallel words, IN[15:0]. This word may be combined with exponent input bits EXP[2:0] when the AD6620 is being driven by floating-point or gain-ranging analog-to-digital converters such as the AD6600.

Frequency translation is accomplished with a 32-bit complex Numerically Controlled Oscillator (NCO). Real data entering this stage is separated into in-phase (I) and quadrature (Q) components. This stage translates the input signal from a digital intermediate frequency (IF) to baseband. Phase and amplitude dither may be enabled on-chip to improve spurious performance of the NCO. A phase offset word is available to create a known phase relationship between multiple AD6620s.

Following frequency translation is a fixed coefficient, high speed decimating filter that reduces the sample rate by a programmable ratio between 2 and 16. This is a second order, cascaded integrator comb FIR filter shown as CIC2 in Figure 1. (Note: Decimation of 1 in CIC2 requires 2× or greater clock into AD6620). The data rate into this stage equals the input data rate, f_{SAMP}. The data rate out of CIC2, f_{SAMP2}, is determined by the decimation factor, M_{CIC2}.

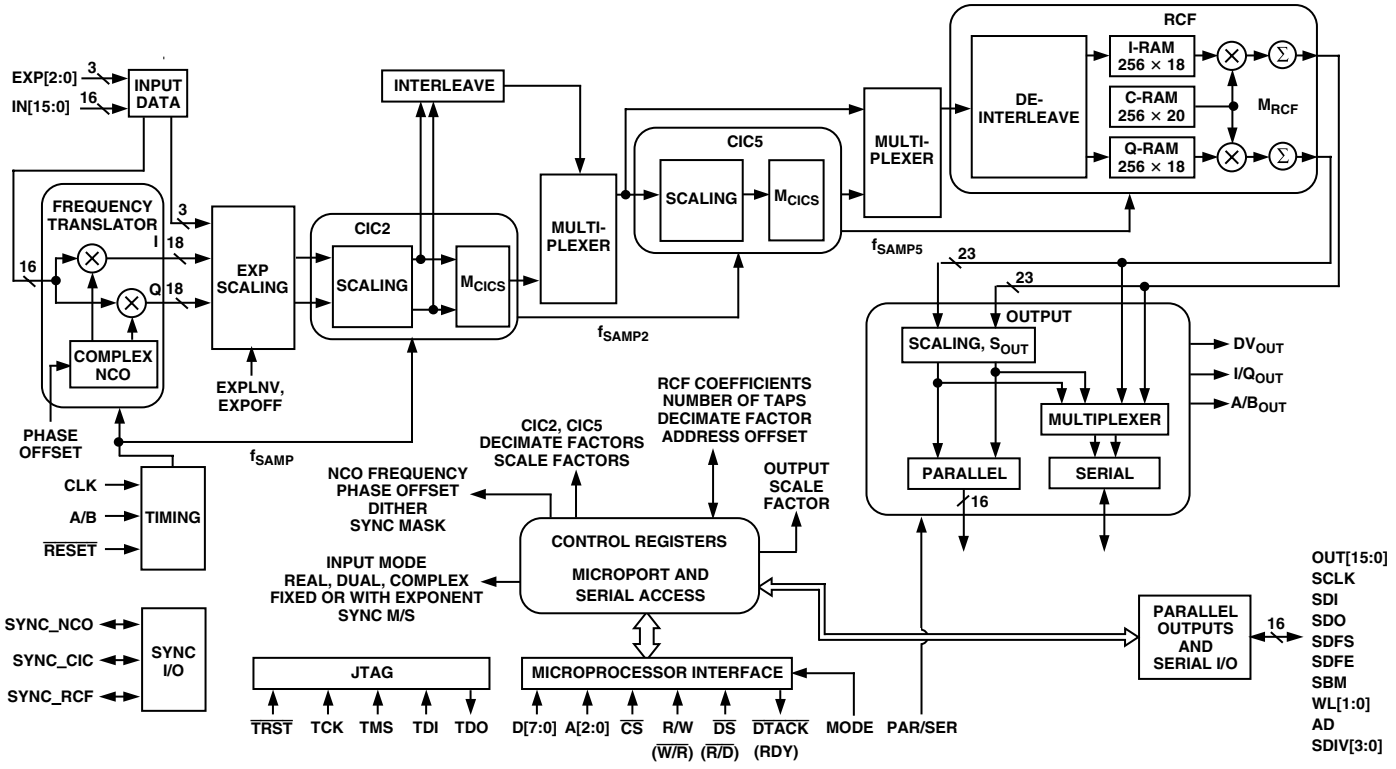


Figure 1. Block Diagram

Following CIC2 is the second fixed-coefficient decimating filter. This filter, CIC5, further reduces the sample rate by a programmable ratio from 1 to 32. The data rate out of CIC5, f_{SAMP5}, is determined by the decimation factors of M_{CIC5} and M_{CIC2}.

Each CIC stage is a FIR filter whose response is defined by the decimation rate. The purpose of these filters is to reduce the data rate of the incoming signal so that the final filter stage, a FIR RAM coefficient sum-of-products filter (RCF), can calculate more taps per output. As shown in Figure 1, on-chip multiplexers allow both CIC filters to be bypassed if a multirate clock is used.

The fourth stage is a sum-of-products FIR filter with programmable 20-bit coefficients, and decimation rates programmable from 1 to 32. The RAM Coefficient FIR Filter (RCF in Figure 1) can handle a maximum of 256 taps.

The overall filter response for the AD6620 is the composite of all three cascaded decimating filters: CIC2, CIC5, and RCF. Each successive filter stage is capable of narrower transition bandwidths but requires a greater number of CLK cycles to calculate the output. More decimation in the first filter stage will minimize overall power consumption. Data comes out via a parallel port or a serial interface.

Figure 2 illustrates the basic function of the AD6620: to select and filter a single channel from a wide input spectrum. The frequency translator "tunes" the desired carrier to baseband. CIC2 and CIC5 have fixed order responses; the RCF filter provides the sharp transitions. More detail is provided in later sections of the data sheet.

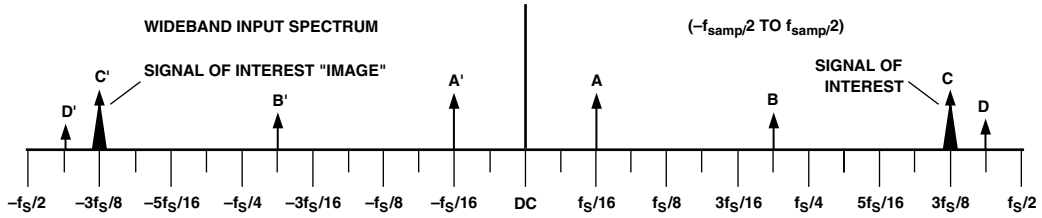


Figure 2a. Wideband Input Spectrum (e.g., 30 MHz from High-Speed ADC)

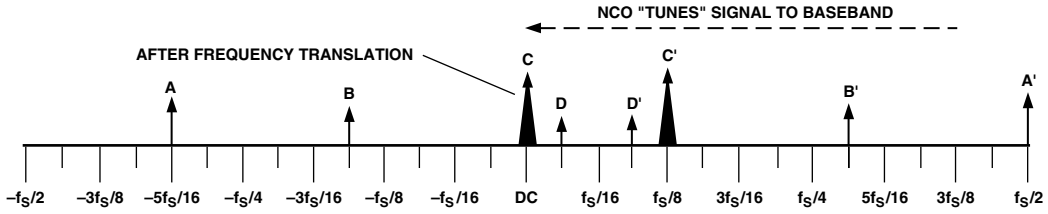


Figure 2b. Frequency Translation (e.g., Single 1 MHz Channel Tuned to Baseband)

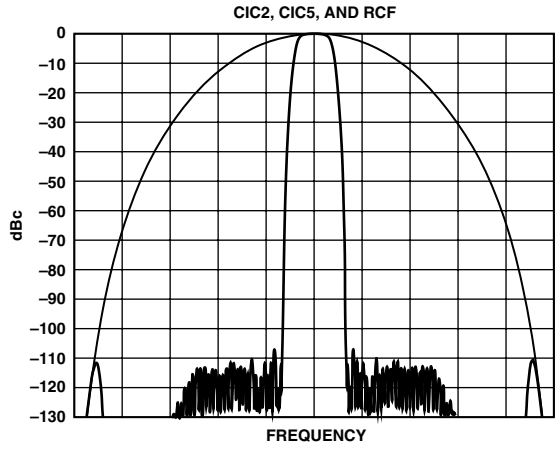


Figure 2c. Baseband Signal is Decimated and Filtered by CIC2, CIC5, RCF

AD6620–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Test Level	AD6620AS Min	Typ	Max	Unit
VDD	I	3.0	3.3	3.6	V
$T_{AMBIENT}$	IV	–40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter (Conditions)	Temp	Test Level	AD6620AS Min	Typ	Max	Unit
LOGIC INPUTS[1, 2, 3, 4, 5, 6, 7] (NOT 5 V TOLERANT)						
Logic Compatibility	Full			3.3 V CMOS		
Logic "1" Voltage	Full	I	2.0		VDD + 0.3	V
Logic "0" Voltage	Full	I	–0.3		0.8	V
Logic "1" Current	Full	I		1	10	µA
Logic "0" Current	Full	I		1	10	µA
Input Capacitance	25°C	V		4		pF
LOGIC OUTPUTS[2, 4, 7, 8, 9, 10, 11]						
Logic Compatibility	Full			3.3 V CMOS/TTL		
Logic "1" Voltage (I_{OH} = 0.5 mA)	Full	I	2.4	VDD – 0.2		V
Logic "0" Voltage (I_{OL} = 1.0 mA)	Full	I		0.2	0.4	V
IDD SUPPLY CURRENT						
CLK = 20 MHz[12]	Full	V		52		mA
CLK = 65 MHz[13]	Full	I		167	227	mA
Reset Mode[14]	Full	I			1	mA
POWER DISSIPATION						
CLK = 20 MHz[12]	Full	V		170		mW
CLK = 65 MHz[13]	Full	I		550	750	mW
Reset Mode[14]	Full	I			3.3	mW

NOTES
[1]Input-Only Pins: CLK, $\overline{\text{RESET}}$, IN[15:0], EXP[2:0], A/B, PAR/SEL.
[2]Bidirectional Pins: SYNC_NCO, SYNC_CIC, SYNC_RCF.
[3]Microinterface Input Pins: $\overline{\text{DS}}$ ($\overline{\text{RD}}$), R/$\overline{\text{W}}$ ($\overline{\text{WR}}$), $\overline{\text{CS}}$.
[4]Microinterface Bidirectional Pins: A[2:0], D[7:0].
[5]JTAG Input Pins: $\overline{\text{TRST}}$, TCK, TMS, TDI.
[6]Serial Mode Input Pins: SDI, SBM, WL[1:0], AD, SDIV[3:0].
[7]Serial Mode Bidirectional Pins: SCLK, SDFS.
[8]Output Pins: OUT[15:0], DV_{OUT}, A/B_{OUT}, I/Q_{OUT}.
[9]Microinterface Output Pins: $\overline{\text{DTACK}}$ (RDY).
[10]JTAG Output Pins: TDO.
[11]Serial Mode Output Pins: SDO, SDFE.
[12]Conditions for IDD @ 20 MHz. M_{CIC2} = 2, M_{CIC5} = 2, M_{RCF} = 1, 4 RCF taps of alternating positive and negative full scale.
[13]Conditions for IDD @ 65 MHz. M_{CIC2} = 2, M_{CIC5} = 2, M_{RCF} = 1, 4 RCF taps of alternating positive and negative full scale.
[14]Conditions for IDD in Reset ($\overline{\text{RESET}}$ = 0).

Specifications subject to change without notice.

TIMING CHARACTERISTICS (C_{LOAD} = 40 pF All Outputs)

Parameter (Conditions)		Temp	Test Level	AD6620AS Min	Typ	Max	Unit
CLK Timing Requirements:							
t_{CLK}	CLK Period	Full	I	14.93[1]			ns
t_{CLK}	CLK Period	Full	I	15.4			ns
t_{CLKL}	CLK Width Low	Full	IV	7.0	$0.5 \times t_{CLK}$		ns
t_{CLKH}	CLK Width High	Full	IV	7.0	$0.5 \times t_{CLK}$		ns
Reset Timing Requirements:							
t_{RESL}	$\overline{\text{RESET}}$ Width Low	Full	I	30.0			ns
Input Data Timing Requirements:							
t_{SI}	Input[2] to CLK Setup Time	Full	IV	–1.0			ns
t_{HI}	Input[2] to CLK Hold Time	Full	IV	6.5			ns
Parallel Output Switching Characteristics:							
t_{DPR}	CLK to OUT[15:0] Rise Delay	Full	IV	8.0		19.5	ns
t_{DPF}	CLK to OUT[15:0] Fall Delay	Full	IV	7.5		19.5	ns
t_{DPR}	CLK to DV_{OUT} Rise Delay	Full	IV	6.5		19.0	ns
t_{DPF}	CLK to DV_{OUT} Fall Delay	Full	IV	5.5		11.5	ns
t_{DPR}	CLK to IQ_{OUT} Rise Delay	Full	IV	7.0		19.5	ns
t_{DPF}	CLK to IQ_{OUT} Fall Delay	Full	IV	6.0		13.5	ns
t_{DPR}	CLK to AB_{OUT} Rise Delay	Full	IV	7.0		19.5	ns
t_{DPF}	CLK to AB_{OUT} Fall Delay	Full	IV	5.5		13.5	ns
SYNC Timing Requirements:							
t_{SY}	SYNC[3] to CLK Setup Time	Full	IV	–1.0			ns
t_{HY}	SYNC[3] to CLK Hold Time	Full	IV	6.5			ns
SYNC Switching Characteristics:							
t_{DY}	CLK to SYNC[4] Delay Time	Full	V	7.0		23.5	ns
Serial Input Timing:							
t_{SSI}	SDI to SCLK↓ Setup Time	Full	IV	1.0			ns
t_{HSI}	SDI to SCLK↓ Hold Time	Full	IV	2.0			ns
t_{HSRF}	SDFS to SCLK↑ Hold Time	Full	IV	4.0			ns
t_{SSF}	SDFS to SCLK↓ Setup Time[5]	Full	IV	1.0			ns
t_{HSF}	SDFS to SCLK↓ Hold Time[5]	Full	IV	2.0			ns
Serial Frame Output Timing:							
t_{DSE}	SCLK↑ to SDFE Delay Time	Full	IV	3.5		11.0	ns
t_{SDFEH}	SDFE Width High	Full	V		t_{SCLK}		ns
t_{DSO}	SCLK↑ to SDO Delay Time	Full	IV	4.5		11.0	ns
SCLK Switching Characteristics, SBM = "1":							
t_{SCLK}	SCLK Period[4]	Full	I	$2 \times t_{CLK}$			ns
t_{SCLKL}	SCLK Width Low	Full	V		$0.5 \times t_{SCLK}$		ns
t_{SCLKH}	SCLK Width High	Full	V		$0.5 \times t_{SCLK}$		ns
t_{SCLKD}	CLK to SCLK Delay Time	Full	V	6.5		13.0	ns
Serial Frame Timing, SBM = "1":							
t_{DSF}	SCLK↑ to SDFS Delay Time	Full	IV	1.0		4.0	ns
t_{SDFSH}	SDFS Width High	Full	V		t_{SCLK}		ns
SCLK Timing Requirements, SBM = "0":							
t_{SCLK}	SCLK Period	Full	I	15.4			ns
t_{SCLKL}	SCLK Width Low	Full	IV	$0.4 \times t_{SCLK}$	$0.5 \times t_{SCLK}$		ns
t_{SCLKH}	SCLK Width High	Full	IV	$0.4 \times t_{SCLK}$	$0.5 \times t_{SCLK}$		ns

NOTES
[1]This specification valid for VDD >= 3.3 V. t_{CLKL} and t_{CLKH} still apply.
[2]Specification pertains to: IN[15:0], EXP[2:0], A/B.
[3]Specification pertains to: SYNC_NCO, SYNC_CIC, SYNC_RCF.
[4]SCLK period will be $\geq 2 \times t_{CLK}$ when AD6620 is Serial Bus Master (SBM = 1) depending on the SDIV word.
[5]SDFS setup and hold time must be met, even when configured as outputs, since internally the signal is sampled at the pad.

Specifications subject to change without notice.

AD6620
TIMING CHARACTERISTICS (C_{LOAD} = 40 pF All Outputs)

Parameter (Conditions)		Temp	Test Level	AD6620AS Min	Typ	Max	Unit
MICROPROCESSOR PORT, MODE = 0							
MODE0 Input Timing Requirements:							
t_{SC}	Control[1] to CLK Setup Time	Full	IV	3.0			ns
t_{HC}	Control[1] to CLK Hold Time	Full	IV	5.0			ns
t_{HA}	Address[2] to CLK Hold Time	Full	IV	3.0			ns
t_{ZR}	$\overline{CS}$ to Data Enabled Time	Full	IV		5.0		ns
t_{ZD}	$\overline{CS}$ to Data Disabled Time	Full	IV		5.0		ns
t_{SAM}	$\overline{CS}$ to Address/Data Setup Time	Full	IV	0.0			ns
MODE0 Read Switching Characteristics:							
t_{DD}	CLK to Data Valid Time	Full	I	10.0	15.0	30.0	ns
t_{RDY}	$\overline{RD}$ to RDY Time	Full	IV	4.0		19.5	ns
MODE0 Write Timing Requirements:							
t_{SC}	Control[1] to CLK Setup Time	Full	IV	3.0			ns
t_{HC}	Control[1] to CLK Hold Time	Full	IV	5.0			ns
t_{HM}	Micro Data[3] to CLK Hold Time	Full	IV	3.0			ns
t_{HA}	Address[2] to CLK Hold Time	Full	IV	3.0			ns
t_{SAM}	Address/Data Setup Time to $\overline{CS}$	Full	IV	0.0			ns
MODE0 Write Switching Characteristics:							
t_{RDY}	$\overline{RD}$ to RDY Time	Full	IV	4.0		19.5	ns
MICROPROCESSOR PORT, MODE = 1							
MODE1 Input Timing Requirements:							
t_{SC}	Control[1] to CLK Setup Time	Full	IV	3.0			ns
t_{HC}	Control[1] to CLK Hold Time	Full	IV	5.0			ns
t_{HA}	Address[2] to CLK Hold Time	Full	IV	3.0			ns
t_{ZR}	$\overline{CS}$ to Data Enabled Time	Full	IV		5.0		ns
t_{ZD}	$\overline{CS}$ to Data Disabled Time	Full	IV		5.0		ns
t_{SAM}	Address/Data Setup Time to $\overline{CS}$	Full	IV	0.0			ns
MODE1 Read Switching Characteristics:							
t_{DD}	CLK to Data Valid Time	Full	I	10.0		30.0	ns
t_{DTACK}	CLK to DTACK Time	Full	V	5.5		15.5	ns
MODE1 Write Timing Requirements:							
t_{SC}	Control[1] to CLK Setup Time	Full	IV	0.0			ns
t_{HC}	Control[1] to CLK Hold Time	Full	IV	5.0			ns
t_{HM}	Micro Data[3] to CLK Hold Time	Full	IV	6.5			ns
t_{HA}	Address[2] to CLK Hold Time	Full	IV	3.0			ns
t_{SAM}	Address/Data Setup Time to $\overline{CS}$	Full	IV	0.0			ns
MODE1 Write Switching Characteristic:							
t_{DTACK}	CLK to DTACK Time	Full	V	5.5		15.5	ns

NOTES
[1]Specification pertains to: R/W ($\overline{WR}$), $\overline{DS}$ ($\overline{RD}$), $\overline{CS}$.
[2]Specification pertains to: A[2:0].
[3]Specification pertains to: D[7:0].

Specifications subject to change without notice.

TIMING DIAGRAMS

CLK, INPUTS, PARALLEL OUTPUTS

RESET with PAR/SER = "1" establishes Parallel Outputs active.

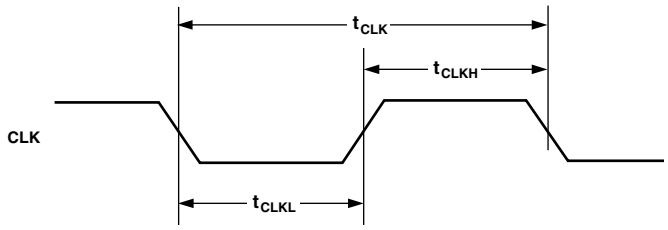


Figure 3. CLK Timing Requirements

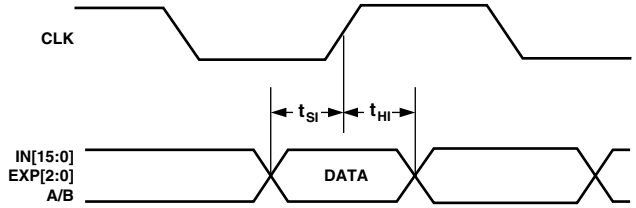


Figure 4. Input Data Timing Requirements

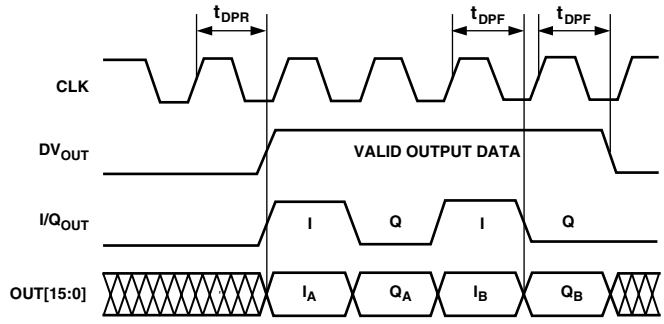
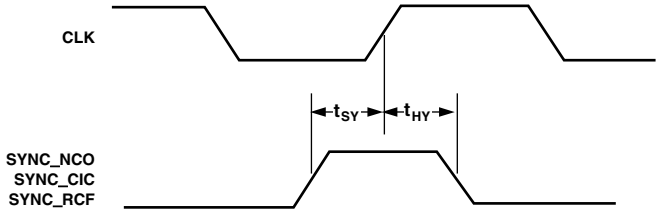


Figure 5. Parallel Output Switching Characteristics

SYNC PULSES: SLAVE OR MASTER



NOTE:
IN THE SLAVE MODE WITH SINGLE CHANNEL OPERATION, THE WIDTH OF THE SYNC_NCO SHOULD BE ONE SAMPLE CLOCK CYCLE. IN DUAL CHANNEL MODE, THE PULSEWIDTH SHOULD BE TWO SAMPLE CLOCK CYCLES. IF A PULSE LONGER THAN SPECIFIED IS USED, THE NCO WILL BE INHIBITED AND NOT INCREMENT PROPERLY.

Figure 6. SYNC Slave Timing Requirements

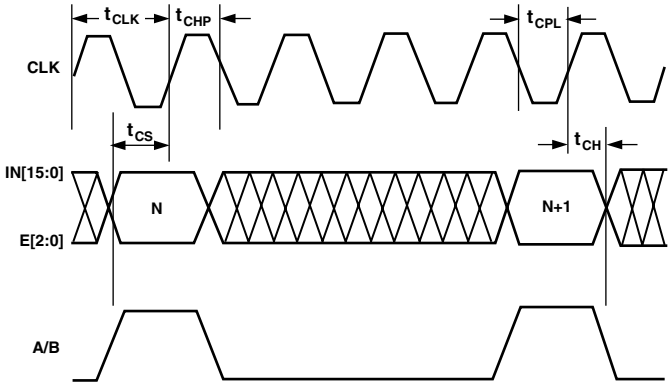


Figure 7. SYNC Master Delay

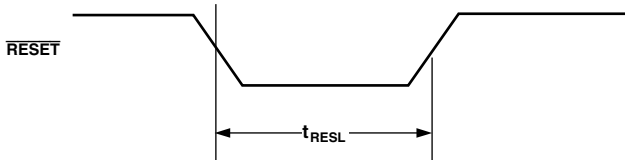


Figure 8. Reset Timing Requirements

SERIAL PORT: BUS MASTER

RESET with PAR/SER = "0" establishes Serial Port active. SBM = "1" puts AD6620 in Serial Bus Master mode SCLK is output; SDFS is output.

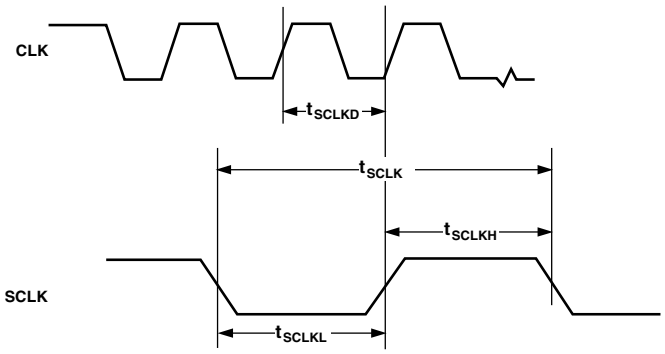


Figure 9. SCLK Switching Characteristics

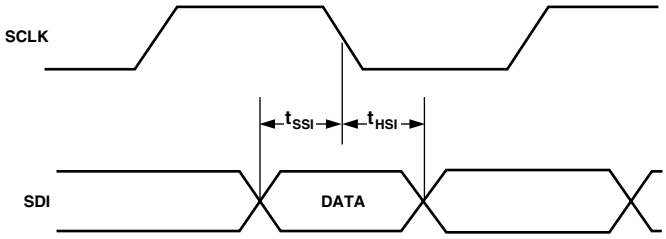


Figure 10. Serial Input Data Timing Requirements

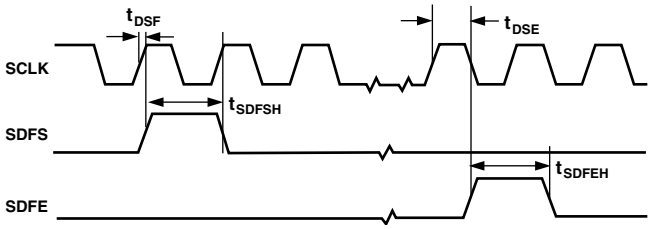


Figure 11. Serial Frame Switching Characteristics

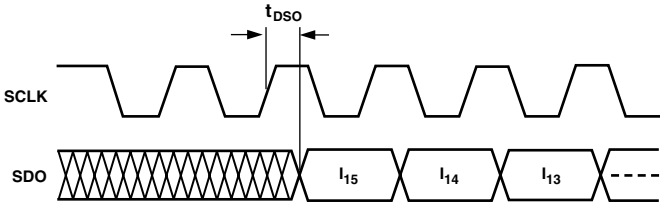


Figure 12. Serial Output Data Switching Characteristics

SERIAL PORT: CASCADE MODE

RESET with PAR/SER = "0" establishes Serial Port active. SBM = "0" puts AD6620 in Serial Port Cascade mode, SCLK is input; SDFS is input.

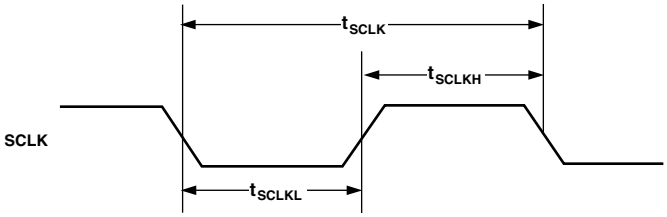


Figure 13. SCLK Timing Requirements

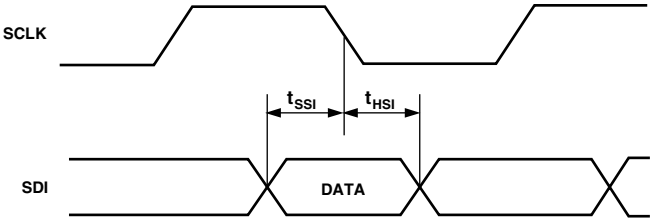


Figure 14. Serial Input Data Timing Requirements

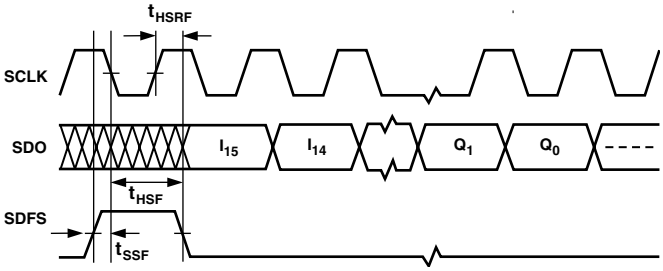


Figure 15. SDO/SDFS Timing Requirements

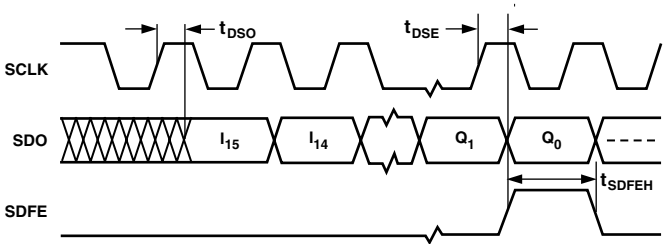
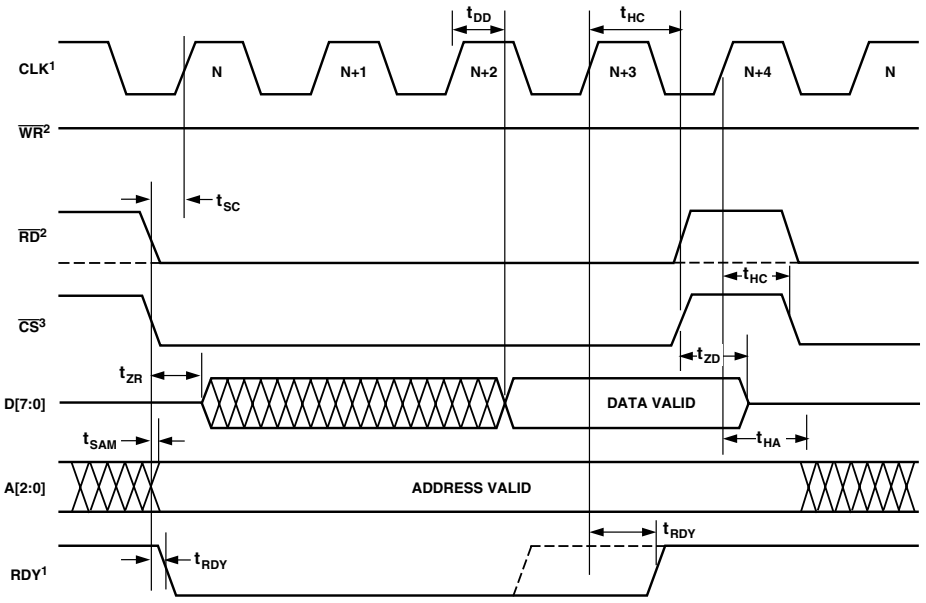


Figure 16. SDO, SDFE Switching Characteristics

MICROPORT MODE0, READ

Timing is synchronous to CLK; MODE = 0.



NOTES:

[1] RDY IS DRIVEN LOW ASYNCHRONOUSLY BY $\overline{RD}$ AND $\overline{CS}$ GOING LOW AND RETURNS HIGH ON THE RISING EDGE OF CLK "N+3" FOR INTERNAL ACCESS (A[2:0] = 000), CLK "N+2" OTHERWISE.

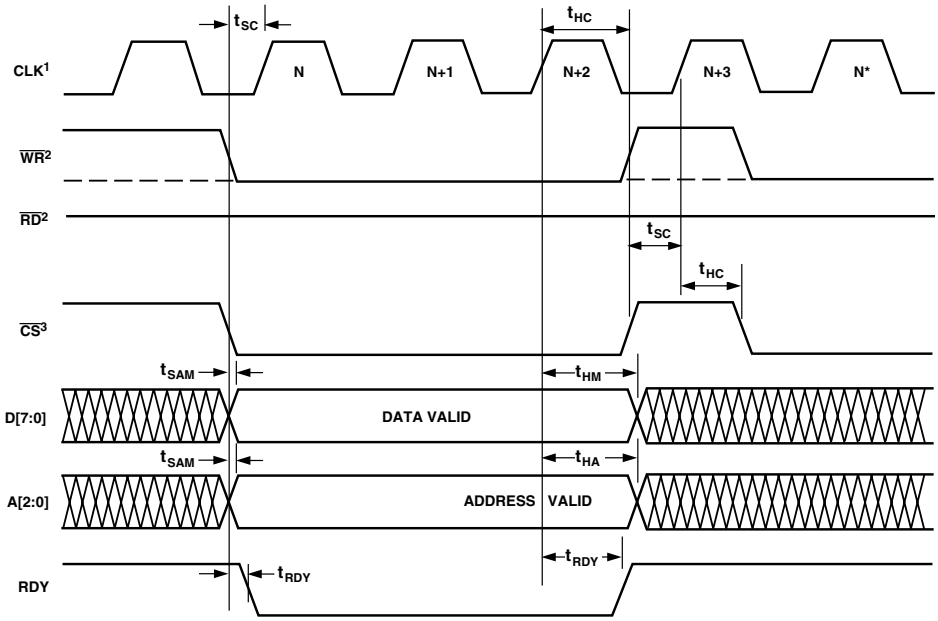
[2] THE SIGNAL, $\overline{WR}$, MAY REMAIN HIGH AND $\overline{RD}$ MAY REMAIN LOW TO CONTINUE READ MODE.

[3] $\overline{CS}$ MUST RETURN TO HIGH STATE AND BE SAMPLED BY CLK (N+4 SHOWN) TO COMPLETE READ.

Figure 17. MODE0 Read Timing Requirements and Switching Characteristics

MICROPORT MODE0, WRITE

Timing is synchronous to CLK; MODE = 0.



NOTES:

[1] RDY IS DRIVEN LOW ASYNCHRONOUSLY BY $\overline{WR}$ AND $\overline{CS}$ GOING LOW AND RETURNS HIGH ON THE RISING EDGE OF CLK "N+2".

[2] THESE SIGNALS (R/W AND $\overline{DS}$) MAY REMAIN IN LOW STATE TO CONTINUE WRITING DATA.

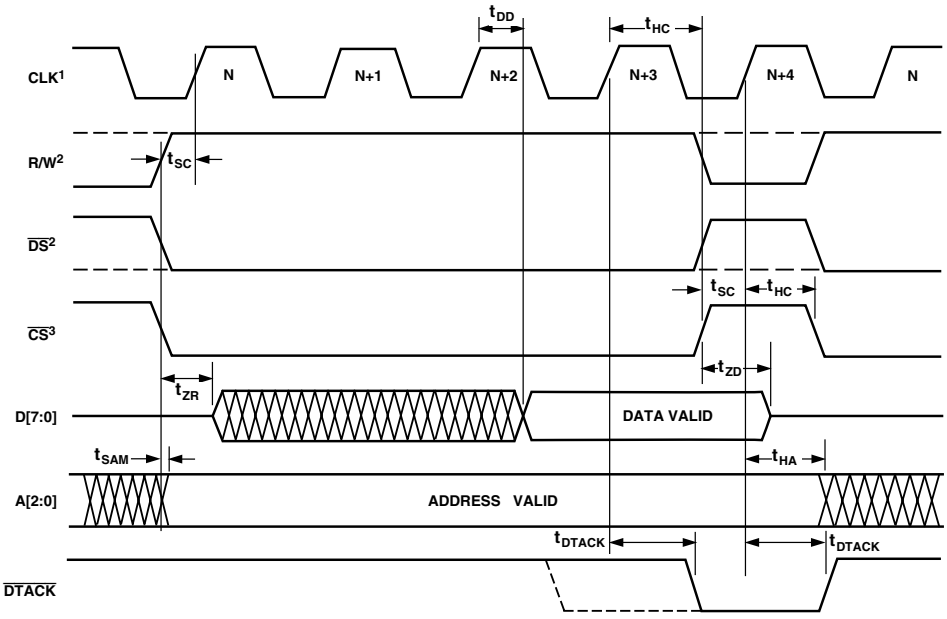
[3] $\overline{CS}$ MUST RETURN TO HIGH STATE AND BE SAMPLED BY CLK (N+3 SHOWN) TO COMPLETE WRITE.

* THE NEXT WRITE MAY BE INITIATED ON CLK, N*.

Figure 18. MODE0 Write Timing Requirements and Switching Characteristics

MICROPORT MODE1, READ

Timing is synchronous to CLK; MODE = 1.



NOTES:

1 $\overline{DTACK}$ IS DRIVEN LOW ON THE RISING EDGE OF CLK "N+3" FOR INTERNAL ACCESS (A[2:0] = 000), CLK "N=2" OTHERWISE.

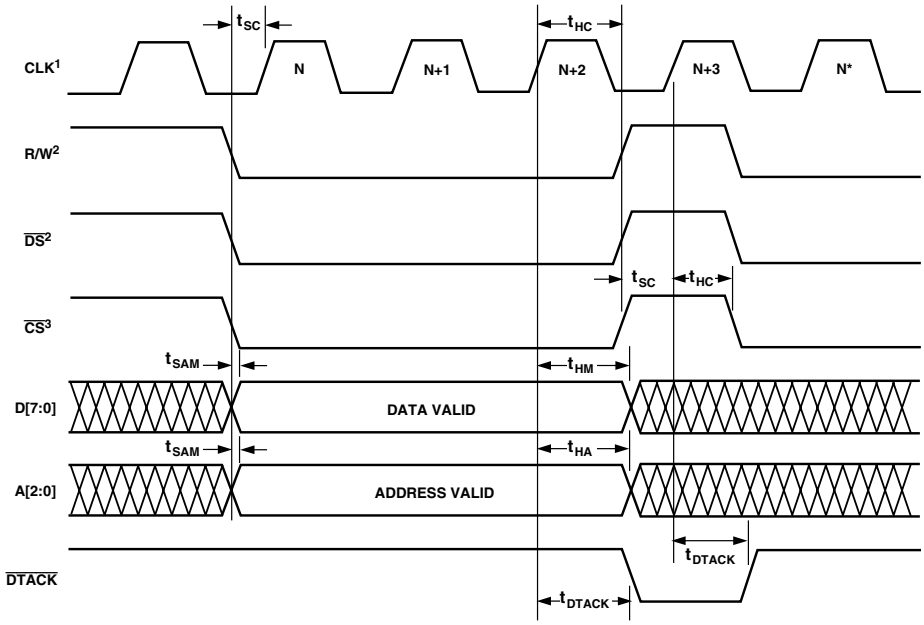
2 THE SIGNAL, R/W MAY REMAIN HIGH AND $\overline{DS}$ MAY REMAIN LOW TO CONTINUE READ MODE.

3 $\overline{CS}$ MUST RETURN TO HIGH STATE AND BE SAMPLED BY CLK (N+4 SHOWN) TO COMPLETE ACCESS AND FORCE $\overline{DTACK}$ HIGH.

Figure 19. MODE1 Read Timing Requirements and Switching Characteristics

MICROPORT MODE1, WRITE

Timing is synchronous to CLK; MODE = 1.



NOTES:

1 ON RISING EDGE OF "N+3" CLK, $\overline{DTACK}$ IS DRIVEN LOW.

2 THESE SIGNALS (R/W AND $\overline{DS}$) MAY REMAIN IN LOW STATE TO CONTINUE WRITING DATA.

3 $\overline{CS}$ MUST RETURN TO HIGH STATE AND BE SAMPLED BY CLK (N+3 SHOWN) TO COMPLETE WRITE AND FORCE $\overline{DTACK}$ HIGH.

* THE NEXT WRITE MAY BE INITIATED ON CLK, N*.

Figure 20. MODE1 Write Timing Requirements and Switching Characteristics

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.5 V
Input Voltage . . . –0.3 V to VDD + 0.3 V (Not 5 V Tolerant)
Output Voltage Swing . . . . . –0.3 V to VDD + 0.3 V
Load Capacitance . . . . . 200 pF
Junction Temperature Under Bias . . . . . 130°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) . . . . . 280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

80-Lead Plastic Quad Flatpack:
θ_{JA} = 44°C/W
θ_{JC} = 11°C/W

EXPLANATION OF TEST LEVELS

I. 100% Production Tested.

II. 100% Production Tested at 25°C, and Sampled Tested at Specified Temperatures.

III. Sample Tested Only.

IV. Parameter Guaranteed by Design and Analysis.

V. Parameter is Typical Value Only.

VI. 100% Production Tested at 25°C, and Sampled Tested at Temperature Extremes.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6620AS	–40°C to +85°C (Ambient)	80-Lead PQFP (Plastic Quad Flatpack)	S-80A
AD6620S/PCB		Evaluation Board with AD6620AS and Software	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6620 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Name	Type	Description
VDD	P	3.3 V Supply
VSS	G	Ground
CLK	I	Input Clock
$\overline{\text{RESET}}$	I	Active Low Reset Pin
IN[15:0]	I	Input Data (Mantissa)
EXP[2:0]	I	Input Data (Exponent)
A/B	I	Channel (A/B) Select
SYNC_NCO	I/O	Sync Signal for NCO
SYNC_CIC	I/O	Sync Signal for CIC Stages
SYNC_RCF	I/O	Sync Signal for RCF
MODE	I	Sets Microport Mode: Mode 1, (MODE = 1), Mode 0, (MODE = 0)
A[2:0]	I	Microprocessor Interface Address
D[7.0]	I/O/T	Microprocessor Interface Data
$\overline{\text{DS}}$ or $\overline{\text{RD}}$	I	Mode 1: Data Strobe Line, Mode 0: Read Signal
R/W or $\overline{\text{WR}}$	I	Read/Write Line (Write Signal)
$\overline{\text{CS}}$	I	Chip Select, Enables the Chip for µP Access
$\overline{\text{DTACK}}$ or RDY	O	Acknowledgment of a Completed Transaction (Signals when µP Port Is Ready for an Access)
PAR/SER	I	Parallel/Serial Control Select (PAR = 1, SER = 0)
DV_{OUT}	O	Data Valid Pin for the Parallel Output Data
A/B_{OUT}	O	Signals to Which Channel the Output Belongs to (A = 1, B = 0)
I/Q_{OUT}	O	Signals Whether I or Q Data Is Present (I = 1, Q = 0)
$\overline{\text{TRST}}$	I	Test Reset Pin
TCK	I	Test Clock Input
TMS	I	Test Mode Select Input
TDI	I	Test Data Input
TDO	I	Test Data Output

Pin Types: I = Input, O = Output, P = Power Supply, G = Ground, T = Three-state.

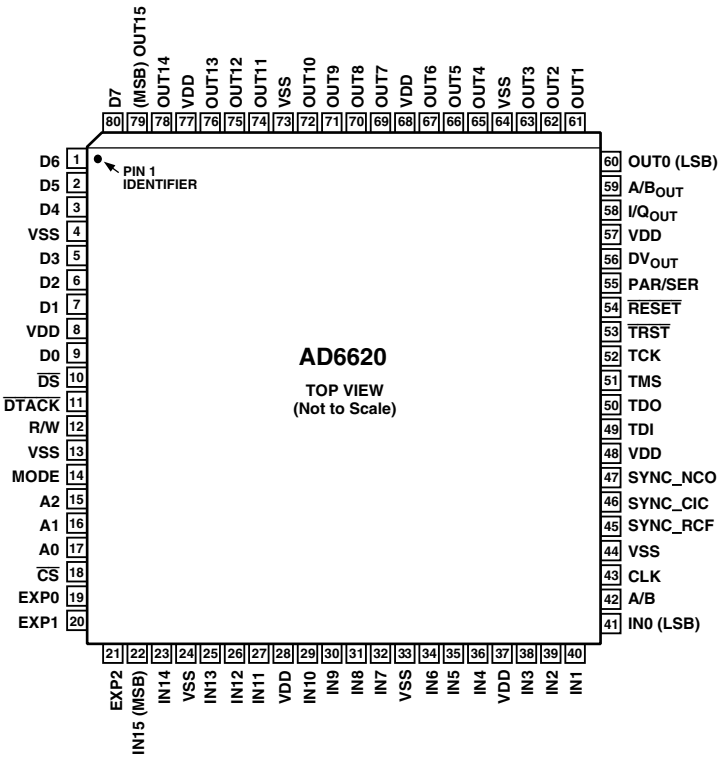
SHARED PINS

Parallel Outputs (PAR/SER = 1 at RESET)			Serial Port (PAR/SER = 0 at RESET)		
Name	**Type**	**Description**	**Name**	**Type**	**Description**
OUT15	O	Parallel Output Data	SCLK	I/O	Serial Clock Input (SBM =0) Serial Clock Output (SBM = 1)
OUT14	O	Parallel Output Data	SDI	I	Serial Data Input
OUT13	O	Parallel Output Data	SDO	O/T	Serial Data Output
OUT12	O	Parallel Output Data	SDFS	I/O	Serial Data Frame Sync Input (SBM = 0) Serial Data Frame Sync Output (SBM = 1)
OUT11	O	Parallel Output Data	SDFE	O	Serial Data Frame End
OUT10	O	Parallel Output Data	SBM	I	Serial Bus Master (Master = 1, Cascade = 0)
OUT9	O	Parallel Output Data	WL1	I	Serial Port Word Length, Bit 1
OUT8	O	Parallel Output Data	WL0	I	Serial Port Word Length, Bit 0
OUT7	O	Parallel Output Data	AD	I	Append Data
OUT[6:4]	O	Parallel Output Data	NC	NC	Unused, Do Not Connect
OUT3	O	Parallel Output Data	SDIV3	I	SCLK Divide Value, Bit 3
OUT2	O	Parallel Output Data	SDIV2	I	SCLK Divide Value, Bit 2
OUT1	O	Parallel Output Data	SDIV1	I	SCLK Divide Value, Bit 1
OUT0	O	Parallel Output Data (LSB)	SDIV0	I	SCLK Divide Value, Bit 0

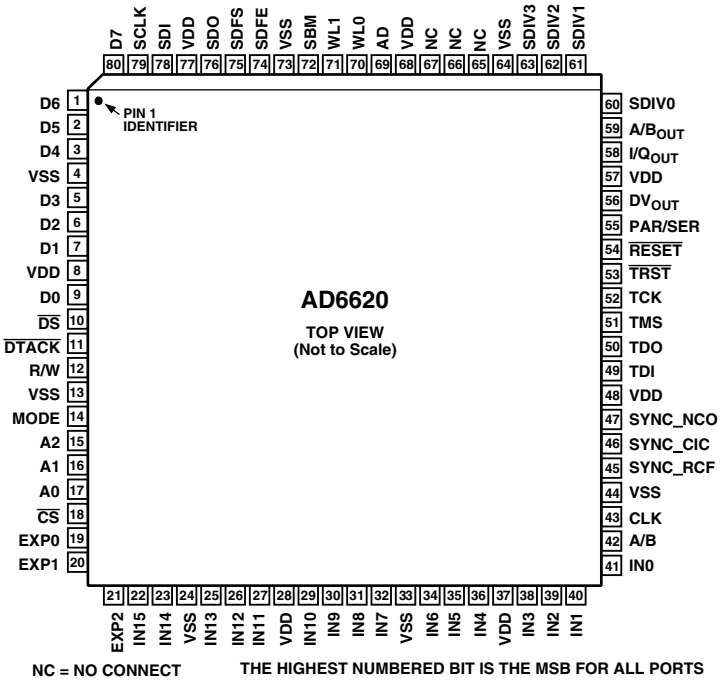
Pin Types: I = Input, O = Output, P = Power Supply, G = Ground, T = Three-state.

PIN CONFIGURATIONS

Parallel Output Data



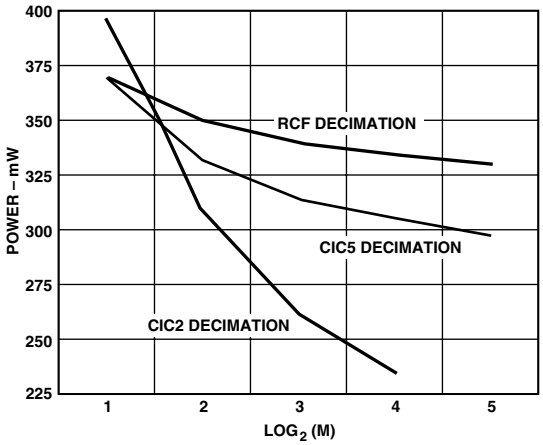
Serial Port



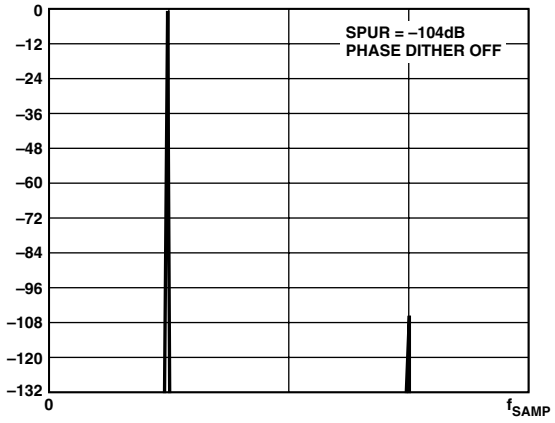
NC = NO CONNECT

THE HIGHEST NUMBERED BIT IS THE MSB FOR ALL PORTS

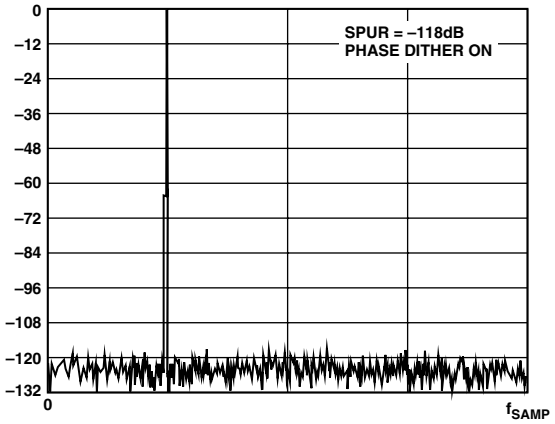
AD6620–Typical Performance Characteristics



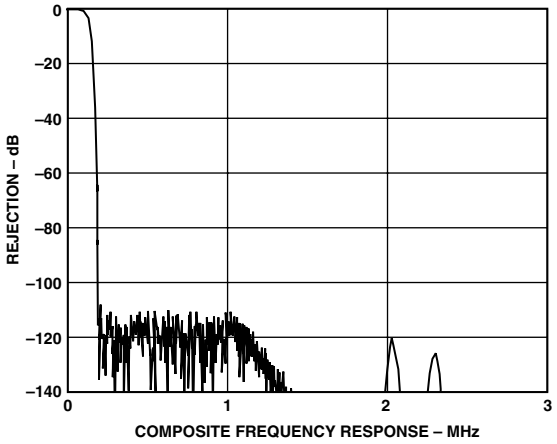
TPC 1. Typical Power vs. Decimation Rates



TPC 2. Typical NCO Spur Without Dither

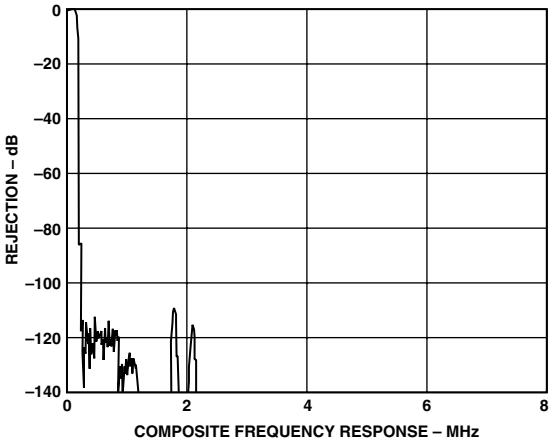


TPC 3. Typical NCO Spur with Dither



TPC 4. High Decimation GSM Filter

Input sample rate 65 MSPS, decimation is 240, FIR taps is 240. Unshown spectrum is below that shown. Decimation distribution is 3, 10, 8, respectively.



TPC 5. High Decimation AMPS Filter

Input sample rate 58.32 MSPS, decimation is 300, FIR taps is 128. Unshown spectrum is below that shown. Decimation distribution among CIC2, CIC5, and RCF is 10, 30 and 1, respectively.

INPUT DATA PORT

The input data port accepts a clock (CLK), a 16-bit mantissa IN[15:0], a 3-bit exponent EXP[2:0], and channel select Pin A/B. These pins allow direct interfacing to both standard fixed-point ADCs such as the AD9225 and AD6640, as well as to gain-ranging ADCs such as the AD6600. These inputs are not 5 V tolerant and the ADC I/O should be set to 3.3 V.

The input data port accepts data in one of three input modes: Single Channel Real, Diversity Channel Real, or Single Channel Complex. The input mode is selected by programming the Input Mode Control Register located at internal address space 300h.

Single Channel Real mode is used when a single channel ADC drives the input to the AD6620. Diversity Channel Real mode is the two channel mode used primarily for diversity receiver applications. Single Channel Complex mode accepts complex data in conjunction with the A/B input which identifies in-phase and quadrature samples (primarily for cascaded 6620s).

The input data port is sampled on the rising edge of CLK at a maximum rate of 67 MSPS. The 16-bit mantissa, IN[15:0] is interpreted as a *twos complement integer*. For most applications with ADCs having fewer than 16 bits, the active bits should be MSB justified and the unused LSBs should be tied low.

The 3-bit exponent, EXP[2:0] is interpreted as an unsigned integer. The exponent can be modified by the 3-bit exponent offset ExpOff (Control Register 0x305, Bits (7–5)) and an exponent invert ExpInv (Control Register 0x305, Bit 4).

ExpOff sets the offset of the input exponent, EXP[2:0]. ExpInv determines the direction of this offset. Equations below show how the exponent is handled.

$$scaled\_input = IN \times 2^{-\bmod(Exp+ExpOff,\,8)},\ ExpInv = 0$$

$$scaled\_input = IN \times 2^{-\bmod(7-Exp+ExpOff,\,8)},\ ExpInv = 1$$

where: *IN* is the value of IN[15:0], *Exp* is the value of EXP[2:0], and *ExpOff* is the value of ExpOff.

Input Scaling

In general there are two reasons for scaling digital data. The first is to avoid "clipping" or, in the case of the AD6620 register, "wrap-around" in subsequent stages. Wrap-around is not a concern for the input data since the NCO is designed to accept the largest possible input at the AD6620 data port.

The second use of scaling is to preserve maximum dynamic range through the chip. As data flows from one stage to the next it is important to keep the math functions performed in the MSBs. This will keep the desired signal as far above the noise floor as possible, thus maximizing signal-to-noise ratio.

Scaling with Fixed-Point ADCs

For fixed-point ADCs, the AD6620 exponent inputs EXP[2:0] are typically not used and should be tied low. The ADC outputs are tied directly to the AD6620 Inputs, MSB-justified. The exponent offset (ExpOff) and exponent invert (ExpInv) should both be programmed to 0. Thus the input equation,

$$scaled\_input = IN \times 2^{-\bmod(Exp+ExpOff,\,8)},\ ExpInv = 0$$

where: *IN* is the value of IN[15:0], Exp is the value of EXP[0:2], and ExpOff is the value of ExpOff, simplifies to,

$$scaled\_input = IN \times 2^{-\bmod(0,\,8)}$$

Thus for fixed-point ADCs, the exponents are typically static and no input scaling is used in the AD6620.

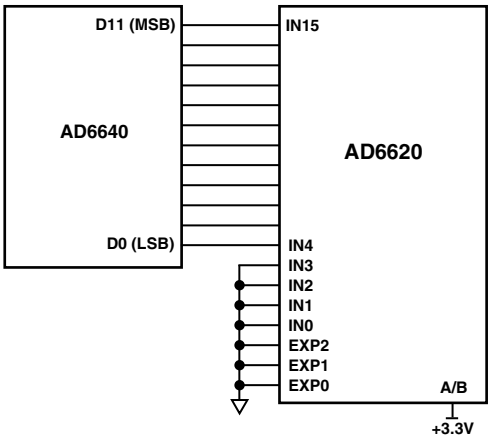


Figure 21. Typical Interconnection of the AD6640 Fixed Point ADC and the AD6620

Scaling with Floating-Point ADCs

An example of the exponent control feature combines the AD6600 and the AD6620. The AD6600 is an 11-bit ADC with three bits of gain ranging. In effect, the 11-bit ADC provides the mantissa, and the three bits of relative signal strength indicator (RSSI) are the exponent. Only five of the eight available steps are used by the AD6600. See the AD6600 data sheet for additional details.

For gain-ranging ADCs such as the AD6600,

$$scaled\_input = IN \times 2^{-\bmod(7-Exp+ExpOff,\,8)},\ ExpInv = 1$$

where: *IN* is the value of IN[15:0], *Exp* is the value of EXP[2:0], and *ExpOff* is the value of ExpOff.

The RSSI output of the AD6600 numerically grows with increasing signal strength of the analog input (RSSI = 5 for a large signal, RSSI = 0 for a small signal). With the Exponent Offset equal to zero and the Exponent Invert Bit equal to zero, the AD6620 would consider the smallest signal at the parallel input (EXP = 0) the largest and, as the signal and EXP word increase, it shifts the data down internally (EXP = 5, will shift the 11-bit data right by 5 bits internally before going into the CIC2). The AD6620 regards the largest signal possible on the AD6600 as the smallest signal. Thus the Exponent Invert Bit is used to make the AD6620 exponent agree with the AD6600 RSSI. When it is set high, it forces the AD6620 to shift the data up for growing EXP instead of down. The exponent invert bit should always be set high for use with the AD6600.

Table I. AD6600 Transfer Function with AD6620 ExpInv = 1, and No ExpOff

ADC Input Level	AD6600 RSSI[2.0]	AD6620 Data	Signal Reduction
Largest	101 (5)	÷ 4 (>> 2)	–12 dB
	100 (4)	÷ 8 (>> 3)	–18 dB
	011 (3)	÷ 16 (>> 4)	–24 dB
	010 (2)	÷ 32 (>> 5)	–30 dB
	001 (1)	÷ 64 (>> 6)	–36 dB
Smallest	000 (0)	÷ 128 (>> 7)	–42 dB

(ExpInv = 1, ExpOff = 0)

The Exponent Offset is used to shift the data right. For example, Table I shows that with no ExpOff shift, 12 dB of range is lost when the ADC input is at the largest level. This is undesired because it lowers the Dynamic Range and SNR of the system by reducing the signal of interest relative to the quantization noise floor.

To avoid this automatic attenuation of the full-scale ADC signal, the Exponent Offset is used to move the largest signal (RSSI = 5) up to the point where there is no downshift. In other words, once the Exponent Invert bit has been set, the Exponent Offset should be adjusted so that mod(7–5 + ExpOff,8) = 0. This is the case when Exponent Offset is set to 6 since mod(8, 8) = 0. Table II illustrates the use of ExpInv and ExpOff when used with the AD6600 ADC.

Table II. AD6600 Transfer Function with AD6620 ExpInv = 1, and ExpOff = 6

ADC Input Level	AD6600 RSSI[2.0]	AD6620 Data	Signal Reduction
Largest	101 (5)	÷ 1 (>> 0)	–0 dB
	100 (4)	÷ 2 (>> 1)	–6 dB
	011 (3)	÷ 4 (>> 2)	–12 dB
	010 (2)	÷ 8 (>> 3)	–18 dB
	001 (1)	÷ 16 (>> 4)	–24 dB
Smallest	000 (0)	÷ 32 (>> 5)	–30 dB

(ExpInv = 1, ExpOff = 6)

This flexibility in handling the exponent allows the AD6620 to interface with other gain ranging ADCs besides the AD6600. The Exponent Offset can be adjusted to allow up to seven RSSI(EXP) ranges to be used as opposed to the AD6600s five. It also allows the AD6620 to be tailored in a system that employs the AD6600, but does not utilize all of its signal range. For example, if only the first four RSSI ranges are expected to occur then the Exponent Offset could be adjusted to five, which would then make RSSI = 4 correspond to the 0 dB point of the AD6620.

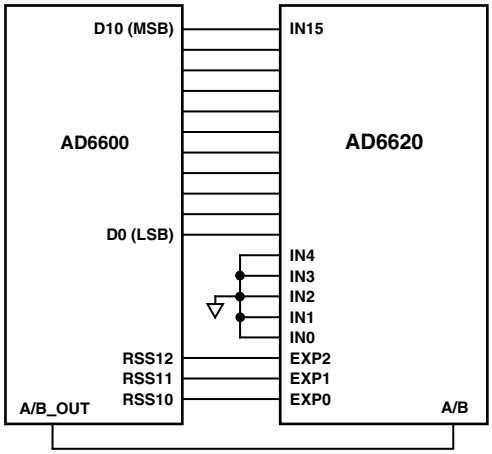


Figure 22. Typical Interconnection of the AD6600 Gain-Ranging ADC and the AD6620 in a Diversity Application

Input Timing

The CLK signal is used to sample the input port and clock the synchronous signal processing stages that follow. The CLK signal can operate up to 67 MHz and have a duty cycle of 45% to 55%. In applications using high speed ADCs, the ADC sample clock is typically used to clock the AD6620. Applications that require a faster signal processing clock than the ADC sample clock, may employ fractional rate input timing as shown in the following sections. The input timing requirements vary according to the mode of operation. Fractional rate input timing creates a longer "don't care" time for the input data so that slower ADCs need only meet the setup-and-hold conditions for their data with respect to their own sample clock cycle, rather than the faster signal processing clock. The ADC sample clock may be any integer fraction of CLK up to and including 1, as long as the clock and data rate are less than or equal to 67 MSPS.

Single Channel Real Mode

In the Single Channel Real mode the A/B input pin functions as an active high input enable. If the A/D sample clock is fast enough to perform the necessary filter functions, full rate input timing can be used and A/B should be tied high as shown in Figure 23.

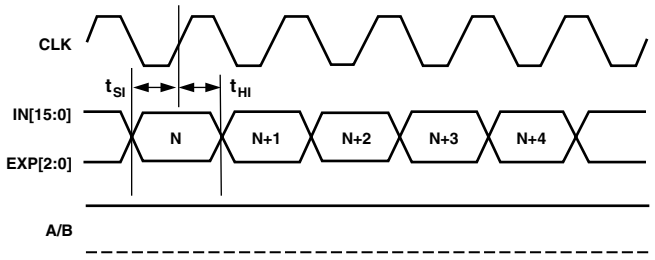


Figure 23. Full Rate Input Timing, Single Channel Real Mode

When a faster processing clock is used to achieve better filter performance, the A/D data must be synchronized with the faster AD6620 CLK signal. This is achieved by having the ADC clock rate an integer fraction of the AD6620 clock rate. AD6620 input data is sampled at the slower ADC clock rate. In the Single Channel Real Mode this is achieved by dynamically controlling the A/B input and bringing it high before each rising CLK edge that data is to be sampled on. A/B must be returned low before the next high speed clock pulse and the duty cycle of the A/B signal will therefore be equal to the data-to-clock ratio.

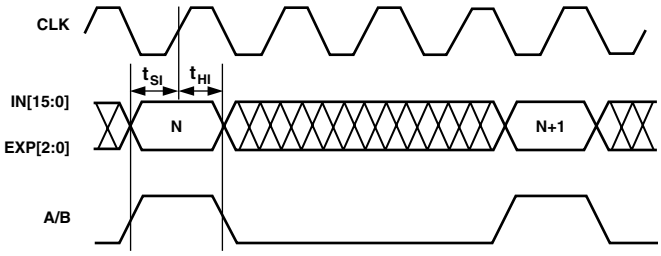


Figure 24. Fractional Rate Input Timing (4× CLK), Single Channel Real Mode

Diversity Channel Real Mode

In the Diversity Channel Real mode the A/B pin serves not only as an input enable but also to determine which channel is being sampled on a given CLK edge. A high on the A/B pin marks channel A data and a low on A/B marks channel B data. The AD6620 only accepts the first sample after an A/B transition. All subsequent samples are disregarded until A/B changes again.

When full rate input timing is employed in the Diversity Channel Real mode, A/B must toggle on every rising edge of CLK for new data to be clocked into the AD6620.

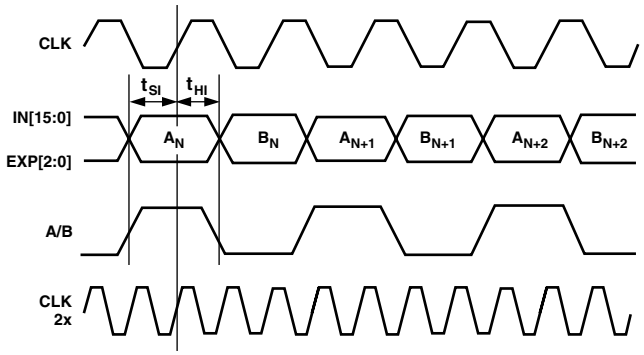


Figure 25. Full Rate Input Timing, Diversity Channel Real Mode

If fractional rate input timing is necessary in the Diversity Channel Real Mode, the A/B pin must toggle at half the rate of the A/D sample clock. The timing diagram below shows a 3× processing clock. In this situation there will be one ADC encode pulse for every three AD6620 CLK pulses and data must be taken on every third CLK pulse. The CLK edges that correspond to the latching of A and B channel data are shown in Figure 26.

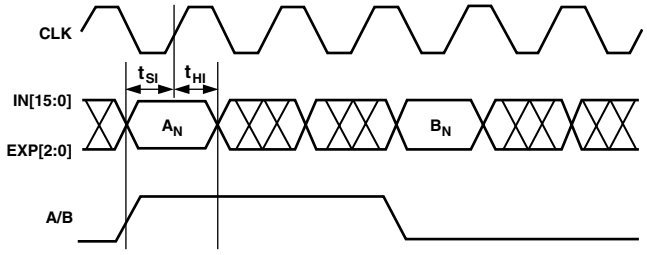


Figure 26. Fractional Rate Input Timing (3× CLK), Diversity Channel Real Mode

Single Channel Complex Mode

In the Single Channel Complex input mode, A/B high identifies the in-phase samples and A/B low identifies quadrature samples. The quadrature samples are paired with the previous in-phase samples. The timing for this mode is the same as that of the Diversity Channel Real Mode. This mode is useful for accepting complex output data from another AD6620 or another source to increase filtering and or decimation rates.

In the Single Channel Complex Mode the CIC2 decimation must be set to two (M_{CIC2} = 2). This is necessary in order to allow enough CLK cycles to process the complex input data as described below.

First clock cycle: (A/B high).
- I data loaded from the input port.
- The I data-path gets I × cosine.
- The Q data-path gets I × sine.
- The first integrator of the CIC2 adds these values to its previous sums.
- The rest of the CIC2 is idle.

Second clock cycle: (A/B low).
- Q data loaded from the input port.
- The I data-path gets Q × sine.
- The Q data-path gets Q × cosine.
- The first integrator of the I path of the CIC2 completes the sum (I × cosine - Q × sine) and the first integrator of the Q path of the CIC2 completes the sum j(I × sine + Q × cosine).
- The rest of the CIC2 operates on these sums, which is the complete complex multiply. The data is then multiplexed through the rest of the chip as if it were single channel real data.

Simplified Input Data Port Schematic

Figure 27 details a simplified schematic for the input data port. The first thing to note is that IN[15:0], EXP[2:0] and A/B are all synchronously latched with CLK. Note also that upon soft reset, a seven pipeline delay (sample clock delay) exists in the data path. This delay is synchronous with CLK, but is in fact seven valid sample data delays. For instance, in single channel

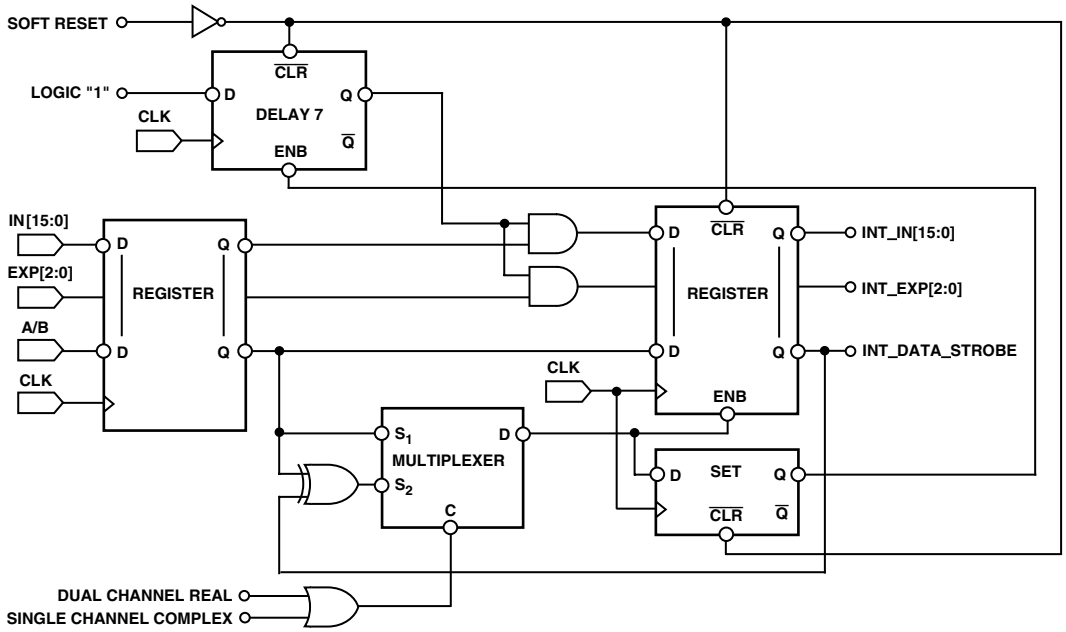


Figure 27. Simplified Input Data Port Schematic for the AD6620

real mode with full rate timing the delay is seven CLKs. If instead the data rate is one-fourth CLK, then 28 CLKs (i.e., seven sample data delays, gated via A/B) occur before valid data is passed to the NCO stage.

Interfacing AD6620 Inputs to 5 V Logic Gates
None of the inputs to the AD6620 are tolerant of 5 V logic signals. When interfacing 5 V devices to this product, an interface gate such as the 74LCX2244 is recommended. If latching must be performed, 74LCX574 latches may be used. This gate runs from the 3.3 V supply and is tolerant of 5 V inputs.

OUTPUT DATA PORT

Parallel Output Data Port

The AD6620 provides a choice of two output ports: a 16-bit parallel port and a synchronous serial port. Output operation using the serial port is discussed in the next section. The parallel port is limited to 16 bits. Because pins are shared between the parallel and serial output ports, only one output mode can be used. The output mode must be set with a hard reset generated by at least a 30 ns low time on the $\overline{\text{RESET}}$ pin. If the PAR/SER line is high (Logic "1"), then parallel output data is activated. The PAR/SER pin should remain static after the output mode has been set (i.e., PAR/SER should only change when $\overline{\text{RESET}}$ is low). *Data out of the AD6620 is two's complement.*

A scale factor is associated with the output port, which allows the signal level to be adjusted. This scale factor is mapped to location 309h, Bits 2–0 in the AD6620 internal address space. This scalar controls the weight of the 16-bit data going to the parallel port. The scale factor is discussed in the RAM Coefficient Filter (RCF) section.

The Parallel Mode provides a 16-bit output port, which constitutes the I and Q data for either one or both channels. This port can run at a maximum of 67 MHz (33.5 MHz I, 33.5 MHz Q).

This rate assumes that there is a minimum decimation of 2 in the first filter stage (CIC2) or a 2× or greater CLK is used. This decimation is required because for every input word there is both an I and a Q output. When the data rate and clock rate are the same (Full Rate Input Timing), the minimum decimation of 2 must occur in CIC2. Refer to CIC2 for more detail.

DV_{OUT}
DV_{OUT} is provided to signal that valid data is present. If this pin is high, there is a valid data word on the bus. DV_{OUT} remains high for two high-speed clock cycles in Single Channel Real and Single Channel Complex Mode and for four high-speed clock cycles in Diversity Channel Real mode. After DV_{OUT} returns low the Q data will remain until the next data sample.

I/Q_{OUT}
When this pin is high the data word represents I data; when I/Q_{OUT} is low Q data is present. This signal will also be low when DV_{OUT} is low since the last word of every data phase is Q data.

A/B_{OUT}
If DV_{OUT} is low, A/B_{OUT} is always low. When A/B_{OUT} is high, A Channel data is available on the output. If DV_{OUT} remains high while A/B_{OUT} is low, then B Channel data is on the output pins of the chip OUT[15:0].

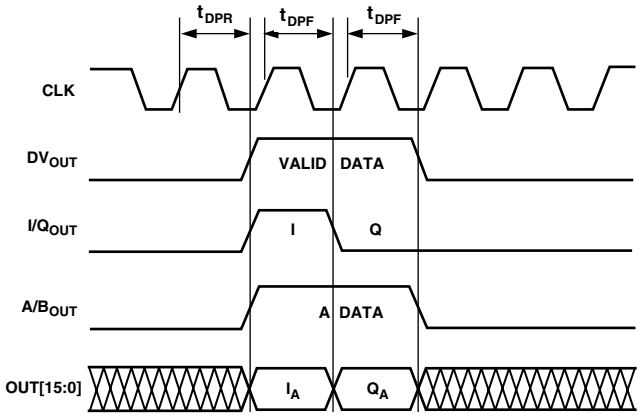


Figure 28. Parallel Output Data Timing (Single-Channel Mode)

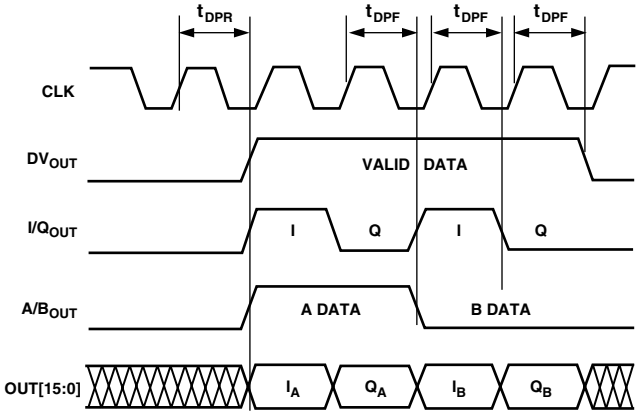


Figure 29. Parallel Output Data Timing (Diversity Channel Mode)

Serial Output Data Port

The AD6620 provides a choice of two output ports: a 16-bit parallel port and a synchronous serial port. The advantage of using the serial port is that all 23 bits of available data can be output in the 24-bit or 32-bit mode. The serial output port shares some of the same pins used by the parallel output port. As a result, one or the other mode of output may be utilized, but not both. The output mode must be set with a hard reset generated by at least a 30 ns low time on the $\overline{\text{RESET}}$ pin. If the PAR/SER line is low (Logic "0") upon reset, then serial output data is activated. The PAR/SER pin should remain static after the output mode has been set (i.e., PAR/SER should only change when $\overline{\text{RESET}}$ is low).

Note that the AD6620 cannot be booted through the serial port. The microport must be used to initialize the device, then serial operation is supported.

Figure 30 shows the typical interconnections between an AD6620 in serial master mode and a DSP. Refer to the Serial Control Port section for a detailed description of pin functions and procedures for writing and reading with relation to the serial port. Note the 10 kΩ resistors connected to SDI and SDO. These prevent the lines from toggling when the AD6620 or DSP three-states these pins.

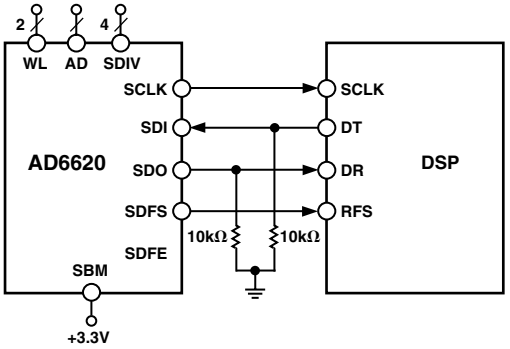


Figure 30. Typical Serial Data Output Interface to DSP (Serial Master Mode, SBM = 1)

Figure 31 shows two AD6620s illustrating the cascade capability for the chip. The first is connected as a serial master and the second is configured in serial cascade mode. The SDFE signal of the master is connected to the SDFS of the slave. This allows the master AD6620 data to be obtained first by the DSP, followed by the cascaded AD6620 data.

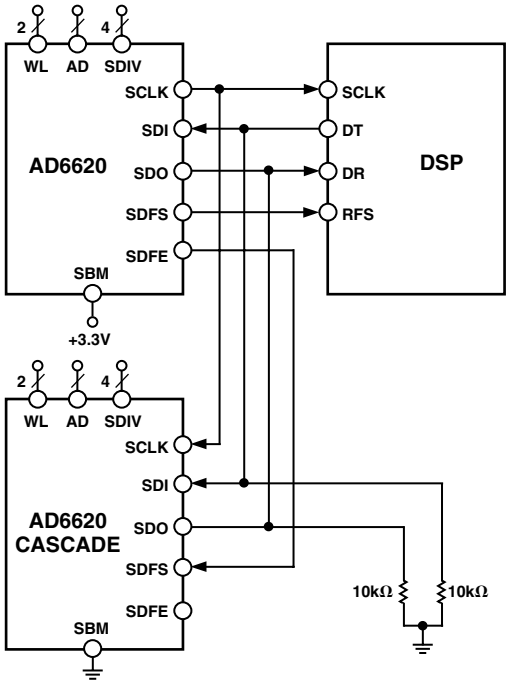


Figure 31. Typical Serial Data Output Interface to DSP (Serial Cascade Mode, SBM = 0)

The AD6620 also supports a serial slave mode, where the serial clock and interface is provided by a DSP or ASIC that is set to operate in the master mode. Note that the AD6620 cannot be booted through the serial port. The microport must be used to initialize the device, then serial operation is supported.

In the serial slave mode, DV_{OUT} is valid and indicates the presence of a new word in the output buffers of the shift register. This pin may thus be used by the DSP to generate an interrupt to service the serial port. The DSP then generates an SFDS pulse to drive the AD6620. The first serial clock rising edge after SDFS makes the first bit available at SDO. The falling edge of serial clock can be used to sample the data. The total number of bits are then read from the AD6620 (determined by the serial port word length). If the DSP has the ability to count bits, the DSP will know when the complete frame is read. If not, the DSP can monitor the SDFE pin to determine that the complete frame is read. The serial clock provided by the DSP can be asynchronous with the AD6620 clock and input data.

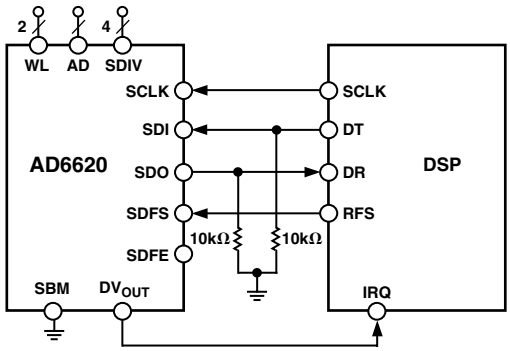


Figure 32. Typical Serial Data Output Interface to DSP (Serial Slave Mode, SBM = 0)

In either the serial master or slave mode, there are two constraints that must be observed. The first is that the clock must be fast enough to read the serial frame prior to the next frame becoming available. Since the AD6620 output is synchronous with its input sample rate, the output update rate can be determined by the user-programmed decimation rate. The timing diagram in Figure 33 details how serial slave mode is implemented. The second constraint is that the time between serial frames may be either zero SCLK periods (the end of one frame adjoins the beginning of the next) or two or more SCLK periods. One SCLK period between frames is not allowed.

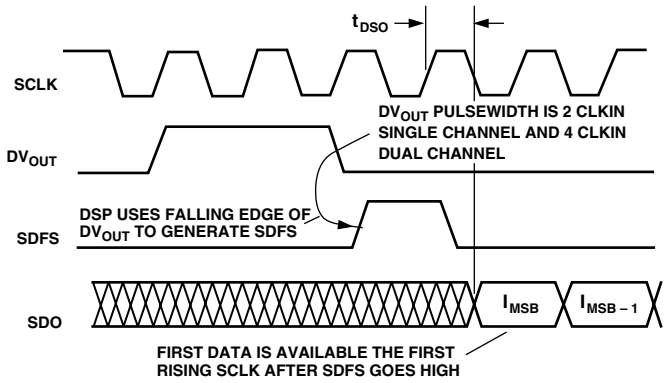


Figure 33. Timing for Serial Slave Mode (SBM = 0)

FREQUENCY TRANSLATOR

The first signal processing stage is a frequency translator consisting of two multipliers and a 32-bit complex numerically controlled oscillator (NCO). The NCO serves as a quadrature local oscillator capable of producing any analytic frequency between $-f_{SAMP}/2$ and $+f_{SAMP}/2$ with a resolution of $f_{SAMP}/2^{32}$. In the Single Channel Real input mode, f_{SAMP} is equal to f_{CLK} multiplied by the fraction of CLK cycles that A/B is high. In the Diversity Channel Real and Single Channel Complex input

modes, f_{SAMP} is equal to f_{CLK} multiplied by the fraction of CLK cycles on which A/B has been toggled. The NCO worst case discrete spur is better than –100 dBc for all output frequencies.

The control word, NCO_FREQ is interpreted as a 32-bit unsigned integer. To translate a channel centered at f_{CH} to dc, calculate NCO_FREQ using the equation below. The mod function is used here to allow for Super Nyquist sampling where the IF carrier (fCH) is larger than the sample rate (fSAMP). The mod removes the integer portion of the number and forces it into the 32-bit NCO Frequency Register. If the fraction remaining is larger than 0.5, the NCO will be tuning above the Nyquist rate. The corresponding signal is then aliased back into the first Nyquist Zone as a negative frequency.

$$NCO\_FREQ = 2^{32} \times mod\left(\frac{f_{CH}}{f_{SAMP}}, 1\right)$$

In both Single and Diversity Channel Real Input modes, the output of the translation stage is the complex product of the real input samples and the complex samples from the NCO. It is necessary for the subsequent decimating filters to reject the unwanted image of the channel of interest, as well as any unwanted neighboring signals (and their images) not rejected by previous analog filters.

In the Diversity Channel Real Input mode, the same NCO output words are used for both channel A and B streams, resulting in identical phase shifts. In Single Channel Complex mode both I and Q inputs are multiplied by the quadrature outputs of the NCO. The I and Q products of the multiply are then processed in the AD6620 filter stages.

In single channel real or dual channel real operation, the frequency translation and filtering processes provide a gain of –6 dB. This can be visualized since the input data is usually a real sampled signal consisting of both positive and negative frequency components (Figure 2a). After being mixed with the complex NCO, the normal filtering of the AD6620 will remove one component or the other resulting in an analytic signal (Figure 2b). This filtering thus removes one-half or 6 dB of the signal keeping consistent with the mathematics involved. If however, the filtering of the device allows both the positive and negative frequency components to pass (i.e., the original signal is near dc), the gain of the frequency translation is 0 dB. Finally, if the NCO is bypassed, the gain of the frequency translation block is –12 dB.

Phase Dither

The AD6620 provides a phase dither option for improving the spurious performance of the NCO. This is controlled via the NCO Control Register at address 301 hex. When phase dither is enabled by setting Bit 1 of this register high, spurs due to phase truncation in the NCO are randomized. The energy from these spurs is spread into the noise floor and Spurious Free Dynamic Range is increased at the expense of very slight decreases in the SNR. Phase dither should be experimented with for each desired NCO frequency and if it is seen to reduce spurs, it should be considered. The choice of whether Phase Dither is used in a system will ultimately be decided by the system goals. If lower spurs are desired at the expense of a slightly raised noise floor, it should be employed. If a low noise floor is desired and the higher spurs can be tolerated or filtered by subsequent stages, then Phase Dither is not needed.

Amplitude Dither

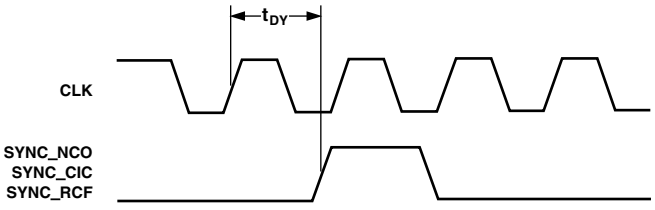
The second dither option is Amplitude Dither or "Complex Dither." Amplitude Dither is enabled by setting Bit 2 of the NCO Control Register at address 0x301 high. Amplitude Dither improves performance by randomizing the amplitude quantization errors within the angular to Cartesian conversion of the NCO. This dither will be particularly useful when the NCO frequency is close to an integer submultiple of the Input Data Rate. However, this option may reduce spurs at the expense of a slightly raised noise floor. Amplitude Dither and Phase Dither can be used together, separately or not at all.

Phase Offset

The phase offset register adds an offset to the phase accumulator of the NCO. This is a 16-bit register and is interpreted as a 16-bit unsigned integer. A 0 in this register corresponds to a 0 Radian offset and an FFFF hex corresponds to an offset of 2 π (1 – 1/(2^16)) Radians. This register can be used to allow multiple AD6620s whose NCOs are synchronized to produce sine waves with a known and steady phase difference.

NCO Synchronization

In order to achieve phase coherence between several AD6620s, a SYNC_NCO pin is provided. When the internal register bit, SYNC_M/S (Bit 3 of internal register 0x300), is set high, SYNC_NCO provides a synchronization pulse on the rising edge of CLK. When the SYNC_M/S bit is low, SYNC_NCO accepts an external synchronization signal sampled on the rising edge of CLK. When the AD6620 is a slave, the SYNC_NCO signal need not be a short pulse. It may be taken high and held for more than a CLK cycle in which case the NCO will be held inactive until this pin is again lowered. If the device is run as a sync slave in Single Channel Mode, the SYNC_NCO pin must be held low for one sample period, usually one clock cycle. If the device is run in Diversity Channel Real mode, the SYNC_NCO must be high for two sample periods (clock cycles). In a system with an array of AD6620s it is not necessary to use one as a master. It may be desirable to generate a synchronization signal elsewhere in the system and use that to control the AD6620. An example of this may be in systems that receive packets of data. In this case, the NCO may be resynchronized prior to the beginning of the packet, thus giving a consistent phase relationship on each burst. This allows for ease of use in a large system where many AD6620s need be synchronized accurately across a large backplane or installation.



NOTE:
IN THE SLAVE MODE WITH SINGLE CHANNEL OPERATION, THE WIDTH OF THE SYNC_NCO SHOULD BE ONE SAMPLE CLOCK CYCLE. IN DUAL CHANNEL MODE, THE PULSEWIDTH SHOULD BE TWO SAMPLE CLOCK CYCLES. IF A PULSE LONGER THAN SPECIFIED IS USED, THE NCO WILL BE INHIBITED AND NOT INCREMENT PROPERLY.

Figure 34. SYNC_NCO Pin

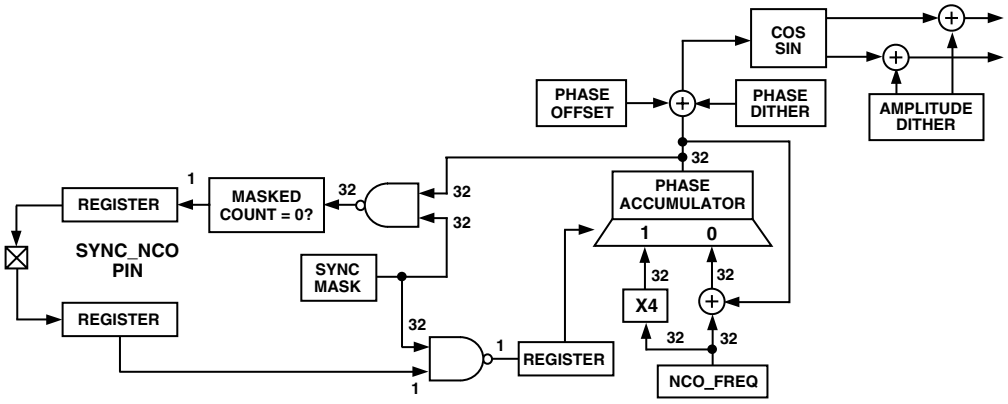


Figure 35. NCO Block Diagram

The frequency of the SYNC_NCO pulses, and therefore the accuracy of the synchronization, is determined by the value of the NCO Sync Control Register at address 302 hex. The value in this register is the SYNC_MASK and is interpreted as a 32-bit unsigned integer. This value controls the window around the zero crossing of the NCO output sine wave in which the NCO will output a SYNC_NCO pulse as a master. As a slave, the value in this register will determine the number of MSBs of the output sine wave that are synchronized with the master. The Master and all slaves should use the same SYNC_MASK word. This value should almost always be written as all 1s (FFFFFFFF hex).

Effects of A/B Input on the NCO

If the AD6620 is run in Single Channel Real mode using fractional rate input timing, the A/B input is used to enable the NCO advancement. If the A/B line is held high longer than one clock period, the NCO will advance for each rising edge of the CLK while A/B is high. This is not normally the desired result and thus A/B must be taken low after the first CLK period to prevent anomalous NCO results. See additional details under Fractional Rate Timing.

Phase Continuous Tuning with the AD6620

For synchronization purposes, the AD6620 NCO phase is reset each time the NCO frequency register is either written to or read from. This is accomplished by forcing an NCO Sync to occur. Normally, phase-continuous tuning is required on the transmit path to control spectral leakage. On the receive path this in not usually a constraint. However, if phase-continuous tuning is required with the AD6620, it can be accomplished by configuring the AD6620 as a Sync Slave. In this manner, no internal NCO sync is generated when the NCO frequency register is written to. If multiple AD6620s are synchronized together, a common external sync pulse can be used to lock each of the receivers together at the appropriate point in time. It is also possible to reconfigure the AD6620 after the NCO frequency register has been written so that the chip is once again a Sync Master. The next time the NCO phase cycles through 0 degrees, the NCO sync is exerted and the chip is again synchronized.

2ND ORDER CASCADED INTEGRATOR COMB FILTER

The CIC2 filter is a fixed-coefficient, decimating filter. It is constructed as a second order CIC filter whose characteristics are defined only by the decimation rate chosen. This filter can process signals at the full rate of the input port (67 MHz) in all input modes. The output rate of this stage is given by the equation below.

$$f_{SAMP2} = \frac{f_{SAMP}}{M_{CIC2}}$$

The decimation ratio, MCIC2, is an unsigned integer that may be between 1 and 16. This stage may be bypassed under certain conditions by setting, M_{CIC2} equal to 1. For this to happen the processing clock rate, f_{CLK} must be two or more times the input data rate, f_{SAMP}. This is because the I and Q data is processed in parallel within the CIC2 filter, and the I and Q output data is then multiplexed through the same data pipe before it enters the CIC5 filter.

The frequency response of the CIC2 filter is given by the following equations.

$$H(z) = \frac{1}{2^{S_{CIC2}}} \times \left(\frac{1 - z^{-M_{CIC2}}}{1 - z^{-1}} \right)^2$$

$$H(f) = \frac{1}{2^{S_{CIC2}}} \times \left(\frac{\sin\left(\pi \frac{M_{CIC2} \times f}{f_{SAMP}} \right)}{\sin\left(\pi \frac{f}{f_{SAMP}} \right)} \right)^2$$

The scale factor, S_{CIC2} is a programmable unsigned integer between 0 and 6. This serves as an attenuator that can reduce the gain of the CIC2 in 6 dB increments. For the best dynamic range, S_{CIC2} should be set to the smallest value possible (i.e., lowest attenuation) without creating an overflow condition. This can be safely accomplished using the equation below, where *input_level* is the largest fraction of full scale possible at the input to this AD6620 (normally 1). The CIC2 scale factor is not ignored when the CIC2 is bypassed.

$$S_{CIC2} = ceil\left(\log_2(M_{CIC2}{}^2 \times input\_level)\right)$$

$$OL_{CIC2} = \frac{1}{2^{S_{CIC2}}} \times input\_level$$

The equations for calculating CIC2 output level is correct when stage is not bypassed (normal operation). However, when bypassed, the following equations should be used instead.

$$OL_{CIC2} = Input\ Level$$

The gain and pass band droop of the CIC2 should be calculated by the equations above, as well as the filter transfer equations that follow. If these are unacceptable, they can be compensated for in subsequent stages.

CIC2 Rejection

The table below illustrates the amount of bandwidth in percent of the data rate into the CIC2 stage. The data in this table may be scaled to any allowable sample rate up to 67 MHz in Single Channel Mode or 33.5 MHz in Diversity Channel Mode. The table can be used as a tool to decide how to distribute the decimation between CIC2, CIC5 and the RCF.

The data in this table may be scaled to any allowable sample rate up to 67 MHz in Single Channel Mode or 33.5 MHz in Diversity Channel Mode.

Table III. SSB CIC2 Alias Rejection Table (f_{SAMP} = 1) Bandwidth Shown in Percentage of f_{SAMP}

M_{CIC2}	–50 dB	–60 dB	–70 dB	–80 dB	–90 dB	–100 dB
2	1.79	1.007	0.566	0.318	0.179	0.101
3	1.508	0.858	0.486	0.274	0.155	0.087
4	1.217	0.696	0.395	0.223	0.126	0.071
5	1.006	0.577	0.328	0.186	0.105	0.059
6	0.853	0.49	0.279	0.158	0.089	0.05
7	0.739	0.425	0.242	0.137	0.077	0.044
8	0.651	0.374	0.213	0.121	0.068	0.038
9	0.581	0.334	0.19	0.108	0.061	0.034
10	0.525	0.302	0.172	0.097	0.055	0.031
11	0.478	0.275	0.157	0.089	0.05	0.028
12	0.439	0.253	0.144	0.082	0.046	0.026
13	0.406	0.234	0.133	0.075	0.043	0.024
14	0.378	0.217	0.124	0.07	0.04	0.022
15	0.353	0.203	0.116	0.066	0.037	0.021
16	0.331	0.19	0.109	0.061	0.035	0.02

Example Calculations

Goal: Implement a filter with an Input Sample Rate of 10 MHz requiring 100 dB of Alias Rejection for a ±7 kHz pass band.

Solution: First determine the percentage of the sample rate that is represented by the pass band.

$$BW_{FRACTION} = 100 \times \frac{7\ kHz}{10\ MHz} = 0.07\%$$

Find the –100 dB column on the right of the table and look down this column for a value greater than or equal to your pass band percentage of the clock rate. Then look across to the extreme left column and find the corresponding decimation rate. Referring to the table, notice that for a decimation of 4, the frequency having –100 dB of alias rejection is 0.071 percent which is slightly greater than the 0.07 percent calculated. Therefore, the maximum bound on CIC2 decimation for this condition is four. Additional decimation means less alias rejection than the 100 dB required.

Note that although an M_{CIC2} less then four would still yield the required rejection, overall power consumption is reduced by decimating as much as possible in this stage. Decimation in CIC2 lowers the data rate and thus reduces power consumed in subsequent stages.

The plot below shows the CIC2 transfer function using a decimation of four. The first plot is referenced to the input sample rate, the complex spectrum from $-f_{SAMP}/2$ to $f_{SAMP}/2$. The second plot is referenced to the CIC2 output rate, the complex spectrum from $-f_{SAMP2}/2$ to $f_{SAMP2}/2$. The aliases of the CIC2 can be seen to be "folding back" in toward the edge of the desired filter pass band. It is the level of these aliases as they move into the desired pass band that are important.

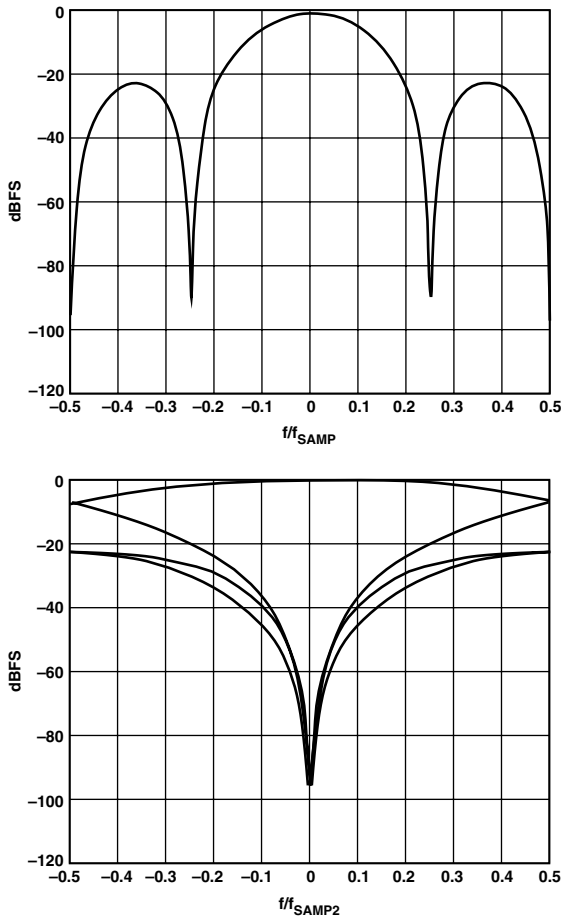


Figure 36. CIC2 Alias Rejection, M_{CIC2} = 4

The set of plots below show a decimation of 16 in the CIC2 filter. The lobes of the filter drop as the decimation rate increases, but the amplitudes of the aliased frequencies increase because the output rate has been reduced.

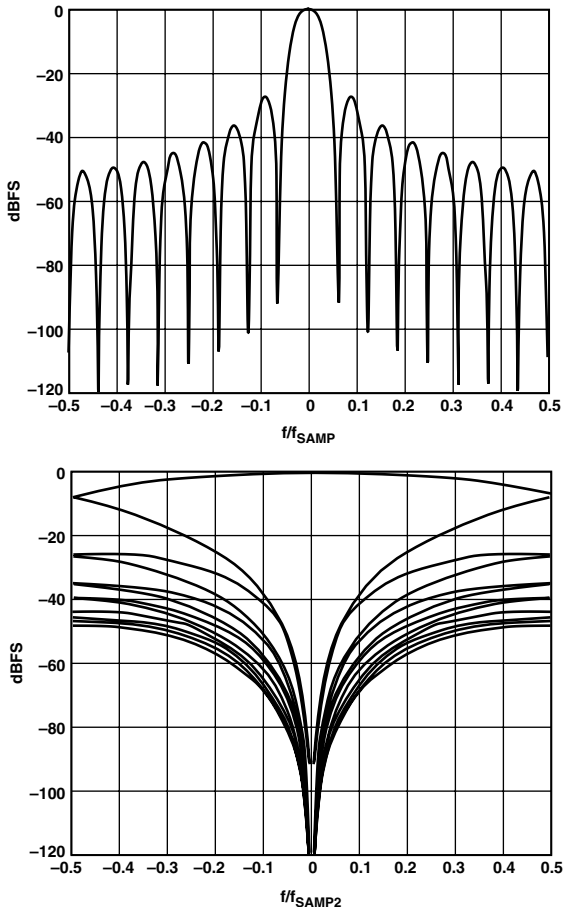


Figure 37. CIC2 Alias Rejection, M_{CIC2} = 16

5TH ORDER CASCADED INTEGRATOR COMB FILTER

The third signal processing stage, CIC5, implements a sharper fixed-coefficient, decimating filter than CIC2. The input rate to this filter is f_{SAMP2}. The maximum input rate is given by the equation below. N_{CH} equals two for Diversity Channel Real input mode; otherwise N_{CH} equals one. In order to satisfy this equation, M_{CIC2} can be increased, N_{CH} can be reduced, or f_{CLK} can be increased (reference fractional rate input timing described in the Input Timing section).

$$f_{SAMP2} \le \frac{f_{CLK}}{2 \times N_{CH}}$$

The decimation ratio, M_{CIC5}, may be programmed from 1 to 32 (all integer values). When M_{CIC5} = 1, this stage is bypassed and the CIC5 scale factor is ignored.

The frequency response of the filter is given by the following equations. The gain and pass band droop of CIC5 should be calculated by these equations. Both parameters may be compensated for in the RCF stage.

$$H(z) = \frac{1}{2^{S_{CIC5}+5}} \times \left(\frac{1 - z^{-M_{CIC5}}}{1 - z^{-1}} \right)^5$$

$$H(f) = \frac{1}{2^{S_{CIC5}+5}} \times \left(\frac{\sin\left(\pi \frac{M_{CIC5} \times f}{f_{SAMP2}} \right)}{\sin\left(\pi \frac{f}{f_{SAMP2}} \right)} \right)^5$$

The scale factor, S_{CIC5} is a programmable unsigned integer between 0 and 20. It serves to control the attenuation of the data into the CIC5 stage in 6 dB increments. For the best dynamic range, S_{CIC5} should be set to the smallest value possible (lowest attenuation) without creating an overflow condition. This can be safely accomplished using the equation below, where OL_{CIC2} is the largest fraction of full scale possible at the input to this filter stage. This value is output from the CIC2 stage then pipelined into the CIC5. S_{CIC5} is ignored when this filter is bypassed by setting M_{CIC5} = 1.

$$S_{CIC5} = ceil\left(\log_2 \left({M_{CIC5}}^5 \times OL_{CIC2} \right) \right) - 5$$

$$OL_{CIC5} = \frac{\left({M_{CIC5}}^5 \right)}{2^{S_{CIC5}+5}} \times OL_{CIC2}$$

when CIC5 is bypassed;

$$OL_{CIC5} = OL_{CIC2}$$

The output rate of this stage is given by the equation below.

$$f_{SAMP5} \le \frac{f_{SAMP2}}{M_{CIC5}}$$

CIC5 Rejection

The table below illustrates the amount of bandwidth in percentage of the clock rate that can be protected with various decimation rates and alias rejection specifications. The maximum input rate into the CIC5 is 32.5 MHz. As in the previous table, these are the 1/2 bandwidth characteristics of the CIC5. Note that the CIC5 stage can protect a much wider band than the CIC2 for any given rejection.

Table IV. SSB CIC5 Alias Rejection Table (f_{SAMP2} = 1) Bandwidth Shown in Percentage of f_{SAMP2}

M_{CIC5}	–50 dB	–60 dB	–70 dB	–80 dB	–90 dB	–100 dB
2	10.227	8.078	6.393	5.066	4.008	3.183
3	7.924	6.367	5.11	4.107	3.297	2.642
4	6.213	5.022	4.057	3.271	2.636	2.121
5	5.068	4.107	3.326	2.687	2.17	1.748
6	4.267	3.463	2.808	2.27	1.836	1.48
7	3.68	2.989	2.425	1.962	1.588	1.281
8	3.233	2.627	2.133	1.726	1.397	1.128
9	2.881	2.342	1.902	1.54	1.247	1.007
10	2.598	2.113	1.716	1.39	1.125	0.909
11	2.365	1.924	1.563	1.266	1.025	0.828
12	2.17	1.765	1.435	1.162	0.941	0.76
13	2.005	1.631	1.326	1.074	0.87	0.703
14	1.863	1.516	1.232	0.998	0.809	0.653
15	1.74	1.416	1.151	0.932	0.755	0.61
16	1.632	1.328	1.079	0.874	0.708	0.572
17	1.536	1.25	1.016	0.823	0.667	0.539
18	1.451	1.181	0.96	0.778	0.63	0.509
19	1.375	1.119	0.91	0.737	0.597	0.483
20	1.307	1.064	0.865	0.701	0.568	0.459
21	1.245	1.013	0.824	0.667	0.541	0.437
22	1.188	0.967	0.786	0.637	0.516	0.417
23	1.137	0.925	0.752	0.61	0.494	0.399
24	1.09	0.887	0.721	0.584	0.474	0.383
25	1.046	0.852	0.692	0.561	0.455	0.367
26	1.006	0.819	0.666	0.54	0.437	0.353
27	0.969	0.789	0.641	0.52	0.421	0.34
28	0.934	0.761	0.618	0.501	0.406	0.328
29	0.902	0.734	0.597	0.484	0.392	0.317
30	0.872	0.71	0.577	0.468	0.379	0.306
31	0.844	0.687	0.559	0.453	0.367	0.297
32	0.818	0.666	0.541	0.439	0.355	0.287

This table helps to calculate an upper bound on decimation, M_{CIC5}, given the desired filter characteristics.

The plots following (Figure 38) represent the CIC5 transfer function with respect to the CIC5 output rate for a decimation of 4. The first plot is referenced to the input sample rate and shows the complex spectrum from $-f_{SAMP}/2$ to $+f_{SAMP}/2$. The second plot is referenced to the CIC5 output rate; the complex spectrum ranges from $-f_{SAMP5}/2$ to $+f_{SAMP5}/2$. Aliased images in CIC5 "fold back" toward the edge of the desired filter pass band. It is the level of these aliases as they move into the desired pass band that are of concern. The improved roll-off of CIC5 over CIC2 can be seen when these plots are compared to those previously shown for CIC2.

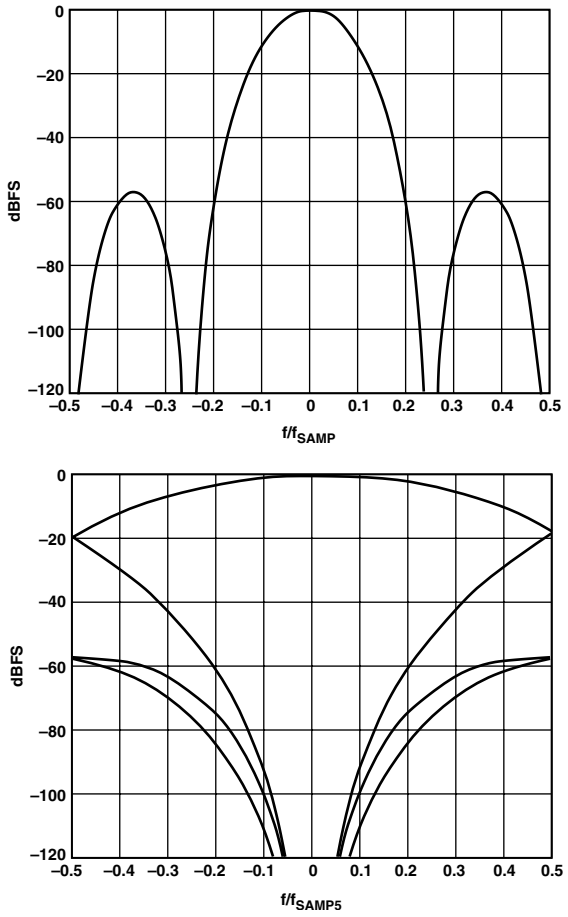


Figure 38. CIC5 Alias Rejection, M_{CIC5} = 4