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4-Channel, 104 MSPS Digital Transmit Signal Processor (TSP)

AD6623

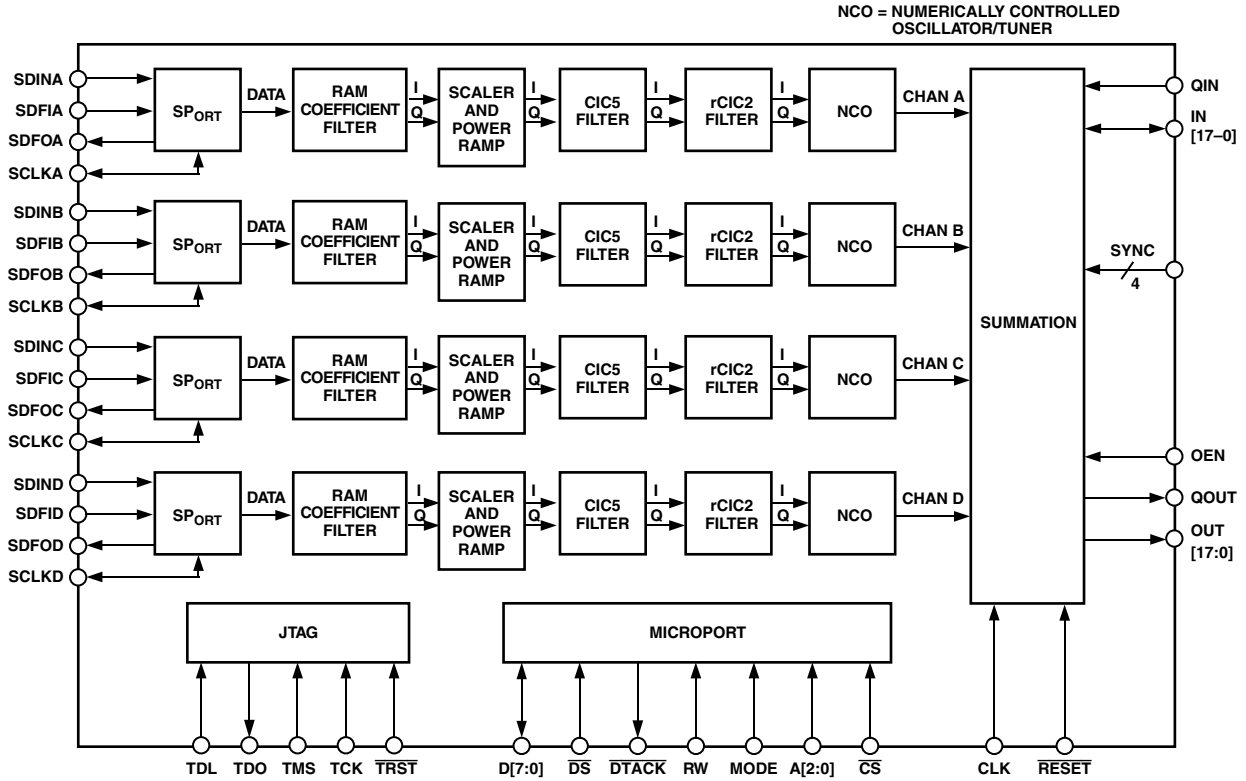
FEATURES

- Pin Compatible to the AD6622
- 18-Bit Parallel Digital IF Output
  - Real or Interleaved Complex
- 18-Bit Bidirectional Parallel Digital IF Input/Output
  - Allows Cascade of Chips for Additional Channels
  - Clipped or Wrapped Over Range
  - Two's Complement or Offset Binary Output
- Four Independent Digital Transmitters in Single Package
- RAM Coefficient Filter (RCF)
  - Programmable IF and Modulation for Each Channel
  - Programmable Interpolating RAM Coefficient Filter
  - $\pi/4$-DQPSK Differential Phase Encoder
  - $3\pi/8$-PSK Linear Encoder
  - 8-PSK Linear Encoder
  - Programmable GMSK Look-Up Table
  - Programmable QPSK Look-Up Table
  - All-Pass Phase Equalizer
  - Programmable Fine Scaler
  - Programmable Power Ramp Unit
- High Speed CIC Interpolating Filter
- Digital Resampling for Noninteger Interpolation Rates
- NCO Frequency Translation
  - Carrier Output from DC to 52 MHz
  - Spurious Performance Better than –100 dBc
- Separate 3-Wire Serial Data Input for Each Channel
  - Bidirectional Serial Clocks and Frames
- Microprocessor Control
- 2.5 V CMOS Core, 3.3 V Outputs, 5 V Inputs
- JTAG Boundary Scan

APPLICATIONS

- Cellular/PCS Base Stations
- Micro/Pico Cell Base Stations
- Wireless Local Loop Base Stations
- Multicarrier, Multimode Digital Transmit
  - GSM, EDGE, IS136, PHS, IS95, TDS CDMA, UMTS, CDMA2000
- Phased Array Beam Forming Antennas
- Software Defined Radio
  - Tuning Resolution Better than 0.025 Hz
  - Real or Complex Outputs

FUNCTIONAL BLOCK DIAGRAM



REV. A

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COMPARABLE PARTS

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DOCUMENTATION

Application Notes

- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design

Data Sheet

- AD6623: 4-Channel, 104 MSPS Digital Transmit Signal Processor (TSP) Data Sheet

Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

TOOLS AND SIMULATIONS

- AD6623 IBIS Models

REFERENCE MATERIALS

Technical Articles

- Basics of Designing a Digital Radio Receiver (Radio 101)
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Smart Partitioning Eyes 3G Basestation

DESIGN RESOURCES

- ad6623 Material Declaration
- PCN-PDN Information
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PRODUCT DESCRIPTION

The AD6623 is a 4-channel Transmit Signal Processor (TSP) that creates high bandwidth data for Transmit Digital-to-Analog Converters (TxDACs) from baseband data provided by a Digital Signal Processor (DSP). Modern TxDACs have achieved sufficiently high sampling rates, analog bandwidth, and dynamic range to create the first Intermediate Frequency (IF) directly. The AD6623 synthesizes multicarrier and multistandard digital signals to drive these TxDACs. The RAM-based architecture allows easy reconfiguration for multimode applications. Modulation, pulse-shaping and anti-imaging filters, static equalization, and tuning functions are combined in a single, cost-effective device. Digital IF signal processing provides repeatable manufacturing, higher accuracy, and more flexibility than comparable high dynamic range analog designs.

The AD6623 has four identical digital TSPs complete with synchronization circuitry and cascadable wideband channel summation. AD6623 is pin compatible to AD6622 and can operate in AD6622-compatible control register mode.
The AD6623 utilizes a 3.3 V I/O power supply and a 2.5 V core power supply. All I/O pins are 5 V tolerant. All control registers and coefficient values are programmed through a generic microprocessor interface. Intel and Motorola microprocessor bus modes are supported. All inputs and outputs are LVCMOS compatible.

FUNCTIONAL OVERVIEW

Each TSP has five cascaded signal processing elements: a programmable interpolating RAM Coefficient Filter (RCF), a programmable Scale and Power Ramp, a programmable fifth order Cascaded Integrator Comb (CIC5) interpolating filter, a flexible second order Resampling Cascaded Integrator Comb filter (rCIC2), and a Numerically Controlled Oscillator/Tuner (NCO).

The outputs of the four TSPs are summed and scaled on-chip. In multicarrier wideband transmitters, a bidirectional bus allows the Parallel (wideband) IF Input/Output to drive a second DAC. In this operational mode two AD6623 channels drive one DAC and the other two AD6623 channels drive a second DAC. Multiple AD6623s may be combined by driving the INOUT[17:0] of the succeeding with the OUT[17:0] of the preceding chip. The INOUT[17:0] can alternatively be masked off by software to allow preceding AD6623's outputs to be ignored.

Each channel accepts input data from independent serial ports that may be connected directly to the serial port of Digital Signal Processor (DSP) chips.

The RCF implements any one of the following functions: Interpolating Finite Impulse Response (FIR) filter, $\pi/4$-DQPSK modulator, 8-PSK modulator, or $3\pi/8$-8-PSK modulator, GMSK modulator, and QPSK modulator. Each AD6623 channel can be dynamically switched between the GMSK modulation mode and the $3\pi/8$-8-PSK modulation mode in order to support the GSM/EDGE standard. The RCF also implements an Allpass Phase Equalizer (APE) which meets the requirements of IS-95-A/B standard (CDMA transmission).

The programmable Scale and Power Ramp block allows power ramping on a time-slot basis as specified for some air-interface standards (e.g., GSM, EDGE). A fine scaling unit at the programmable FIR filter output allows an easy signal amplitude level adjustment on time slot basis.

The CIC5 provides integer rate interpolation from 1 to 32 and coarse anti-image filtering. The rCIC2 provides fractional rate interpolation from 1 to 4096 in steps of 1/512. The wide range of interpolation factors in each CIC filter stage and a highly flexible resampler incorporated into rCIC2 makes the AD6623 useful for creating both narrowband and wideband carriers in a high-speed sample stream.

The high resolution 32-bit NCO allows flexibility in frequency planning and supports both digital and analog air interface standards. The high speed NCO tunes the interpolated complex signal from the rCIC2 to an IF channel. The result may be real or complex. Multicarrier phase synchronization pins and phase offset registers allow intelligent management of the relative phase of independent RF channels. This capability supports the requirements for phased array antenna architectures and management of the wideband peak/power ratio to minimize clipping at the DAC.

The wideband Output Ports can deliver real or complex data. Complex words are interleaved into real (I) and imaginary (Q) parts at half the master clock rate.

AD6623–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Test Level	AD6623 Min	AD6623 Typ	AD6623 Max	Unit
VDD	IV	2.25	2.5	2.75	V
VDDIO	IV	3.0	3.3	3.6	V
$T_{AMBIENT}$	IV	–40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
LOGIC INPUTS (5 V TOLERANT)						
Logic Compatibility	Full			3.3 V CMOS		
Logic "1" Voltage	Full	IV	2.0		5.0	V
Logic "0" Voltage	Full	IV	–0.3		+0.8	V
Logic "1" Current	Full	IV		1	10	µA
Logic "0" Current	Full	IV		0	10	µA
Input Capacitance	25°C	V		4		pF
LOGIC OUTPUTS						
Logic Compatibility	Full			3.3 V CMOS/TTL		
Logic "1" Voltage (I_{OH} = 0.25 mA)	Full	IV	2.0	VDD – 0.2		V
Logic "0" Voltage (I_{OL} = 0.25 mA)	Full	IV		0.2	0.4	V
IDD SUPPLY CURRENT						
GSM Example: CORE		V		232		mA
I/O				56		mA
IS-136 Example: CORE		V		207		mA
I/O				55		mA
WBCDMA Example		V		TBD		mA
Sleep Mode	Full	IV		TBD		mA
POWER DISSIPATION						
GSM Example		V		740		mW
IS-136 Example		V		700		mW
WBCDMA Example		V		TBD		mW
Sleep Mode	Full	IV		TBD		mW

See the Thermal Management section of the data sheet for further details.

GENERAL TIMING CHARACTERISTICS[1, 2]

Parameter (Conditions)		Temp	Test Level	AD6623AS Min	Typ	Max	Unit
CLK Timing Requirements:							
t_{CLK}	CLK Period	Full	I	9.6			ns
t_{CLKL}	CLK Width Low	Full	IV	3			ns
t_{CLKH}	CLK Width High	Full	IV	3	$0.5 \times t_{CLK}$		ns
$\overline{RESET}$ Timing Requirement:							
t_{RESL}	$\overline{RESET}$ Width Low	Full	I	30.0			ns
Input Data Timing Requirements:							
t_{SI}	INOUT[17:0], QIN to ↑CLK Setup Time	Full	IV	1			ns
t_{HI}	INOUT[17:0], QIN to ↑CLK Hold Time	Full	IV	2			ns
Output Data Timing Characteristics:							
t_{DO}	↑CLK to OUT[17:0], INOUT[17:0], QOUT Output Delay Time	Full	IV	2		6	ns
t_{DZO}	OEN HIGH to OUT[17:0] Active	Full	IV	3		7.5	ns
SYNC Timing Requirements:							
t_{SS}	SYNC(0, 1, 2, 3) to ↑CLK Setup Time	Full	IV	1			ns
t_{HS}	SYNC(0, 1, 2, 3) to ↑CLK Hold Time	Full	IV	2			ns
Master Mode Serial Port Timing Requirements (SCS = 0): Switching Characteristics[3]							
t_{DSCLK1}	↑CLK to ↑SCLK Delay (divide by 1)	Full	IV	4		10.5	ns
t_{DSCLKH}	↑CLK to ↑SCLK Delay (for any other divisor)	Full	IV	5		13	ns
t_{DSCLKL}	↑CLK to ↓SCLK Delay (divide by 2 or even number)	Full	IV	3.5		9	ns
$t_{DSCLKLL}$	↓CLK to ↓SCLK Delay (divide by 3 or odd number)	Full	IV	4		10	ns
	Channel is Self-Framing						
t_{SSDI0}	SDIN to ↑SCLK Setup Time	Full	IV	1.7			ns
t_{HSDI0}	SDIN to ↑SCLK Hold Time	Full	IV	0			ns
t_{DSFO0A}	↑SCLK to SDFO Delay	Full	IV	0.5		3.5	ns
	Channel is External-Framing						
t_{SSFI0}	SDFI to ↑SCLK Setup Time	Full	IV	2			ns
t_{HSFI0}	SDFI to ↑SCLK Hold Time	Full	IV	0			ns
t_{SSDI0}	SDIN to ↑SCLK Setup Time	Full	IV	2			ns
t_{HSDI0}	SDIN to ↑SCLK Hold Time	Full	IV	0			ns
t_{DSFO0B}	↑SCLK to SDFO Delay	Full	IV	0.5		3	ns
Slave Mode Serial Port Timing Requirements (SCS = 1): Switching Characteristics[3]							
t_{SCLK}	SCLK Period	Full	IV		$2 \times t_{CLK}$		ns
t_{SCLKL}	SCLK Low Time	Full	IV	3.5			ns
t_{SCLKH}	SCLK High Time	Full	IV	3.5			ns
	Channel is Self-Framing						
t_{SSDH}	SDIN to ↑SCLK Setup Time	Full	IV	1			ns
t_{HSDH}	SDIN to ↑SCLK Hold Time	Full	IV	2.5			ns
t_{DSFO1}	↑SCLK to SDFO Delay	Full	IV	4		10	ns
	Channel is External-Framing						
t_{SSFI1}	SDFI to ↑SCLK Setup Time	Full	IV	2			ns
t_{HSFI1}	SDFI to ↑SCLK Hold Time	Full	IV	1			ns
t_{SSDI1}	SDIN to ↑SCLK Setup Time	Full	IV	1			ns
t_{HSDI1}	SDIN to ↑SCLK Hold Time	Full	IV	2.5			ns
t_{DSFO1}	↓SCLK to SDFO Delay	Full	IV	10			ns

NOTES

[1]All Timing Specifications valid over VDD range of 2.375 V to 2.675 V and VDDIO range of 3.0 V to 3.6 V.

[2]C_{LOAD} = 40 pF on all outputs (unless otherwise specified).

[3]The timing parameters for SCLK, SDIN, SDFI, SDFO, and SYNC apply to all four channels (A, B, C, and D).

Specifications subject to change without notice.

MICROPROCESSOR PORT TIMING CHARACTERISTICS[1, 2]

Parameter (Conditions)		Temp	Test Level	AD6623AS Min	Typ	Max	Unit
MICROPROCESSOR PORT, MODE INM (MODE = 0)							
MODE INM Write Timing:							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	4.5			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{HWR}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address/Data to $\overline{WR}$(RW) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RDY($\overline{DTACK}$) Hold Time	Full	IV	2.0			ns
t_{DRDY}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) Delay	Full	IV	4.0			ns
t_{ACC}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) High Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE INM Read Timing:							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	4.5			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{SAM}	Address to $\overline{RD}$($\overline{DS}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	2.0			ns
t_{ZOZ}	Data Three-State Delay	Full	IV				ns
t_{DD}	RDY($\overline{DTACK}$) to Data Delay	Full	IV				ns
t_{DRDY}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) Delay	Full	IV	4.0			ns
t_{ACC}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) High Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns
MICROPROCESSOR PORT, MOTOROLA (MODE = 1)							
MODE MNM Write Timing:							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	4.5			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{HRW}	RW($\overline{WR}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address/Data to RW($\overline{WR}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RW($\overline{WR}$) Hold Time	Full	IV	2.0			ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay						ns
t_{ACC}	RW($\overline{WR}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE MNM Read Timing:							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	4.0			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address to $\overline{DS}$($\overline{RD}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	2.0			ns
t_{ZD}	Data Three-State Delay	Full	IV				ns
t_{DD}	$\overline{DTACK}$(RDY) to Data Delay	Full	IV				ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay	Full	IV				ns
t_{ACC}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns

NOTES
[1]All Timing Specifications valid over VDD range of 2.375 V to 2.675 V and VDDIO range of 3.0 V to 3.6 V.
[2]C_{LOAD} = 40 pF on all outputs (unless otherwise specified).
[3]Specification pertains to control signals: RW, ($\overline{WR}$), $\overline{DS}$, ($\overline{RD}$), $\overline{CS}$.

Specifications subject to change without notice.

TIMING DIAGRAMS

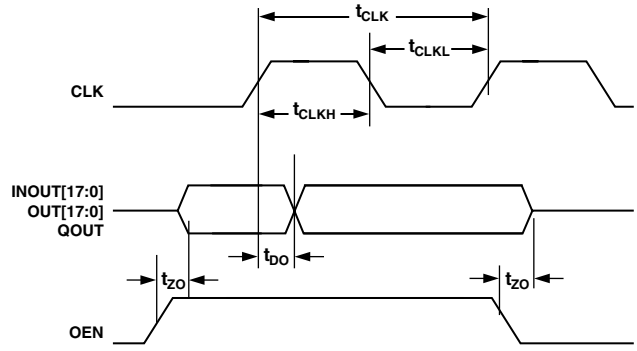


Figure 1. Parallel Output Switching Characteristics

Figure 4. $\overline{RESET}$ Timing Requirements

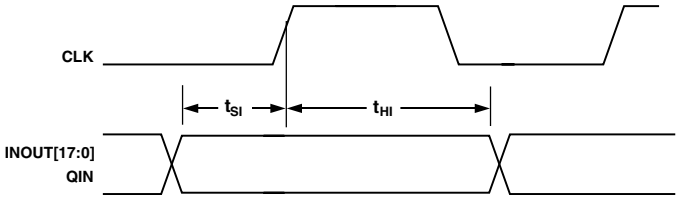


Figure 2. Wideband Input Timing

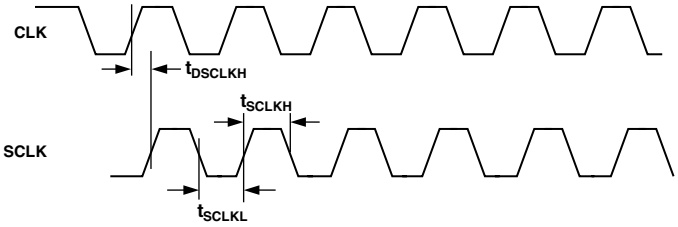


Figure 5. SCLK Switching Characteristics (Divide by 1)

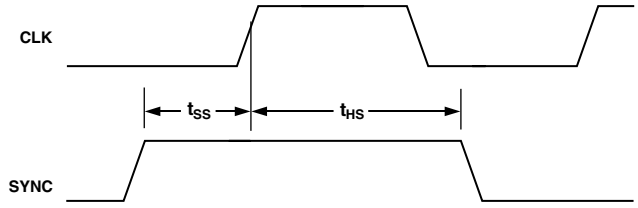


Figure 3. SYNC Timing Inputs

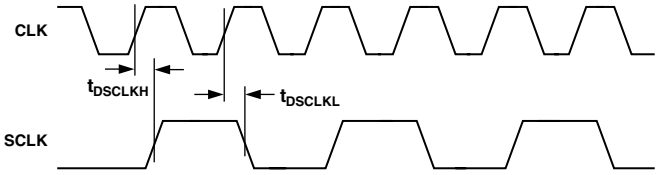


Figure 6. SCLK Switching Characteristic (Divide by 2 or EVEN Integer)

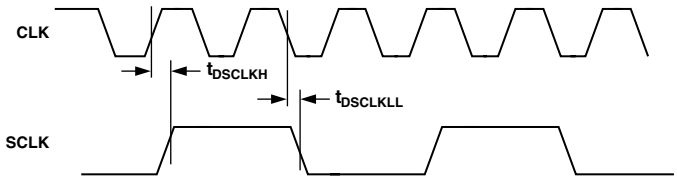


Figure 7. SCLK Switching Characteristic (Divide by 3 or ODD Integer)

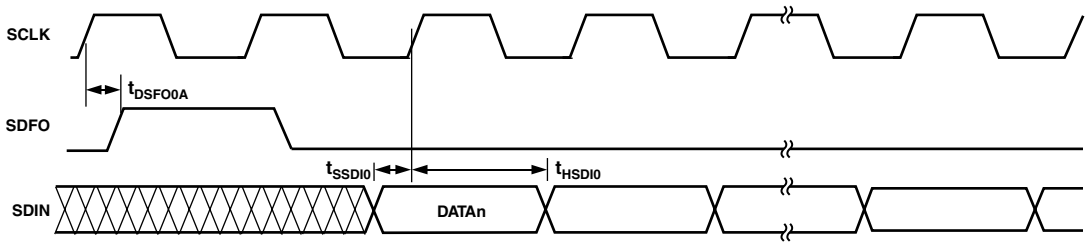


Figure 8. Serial Port Timing, Master Mode (SCS = 0), Channel is Self-Framing

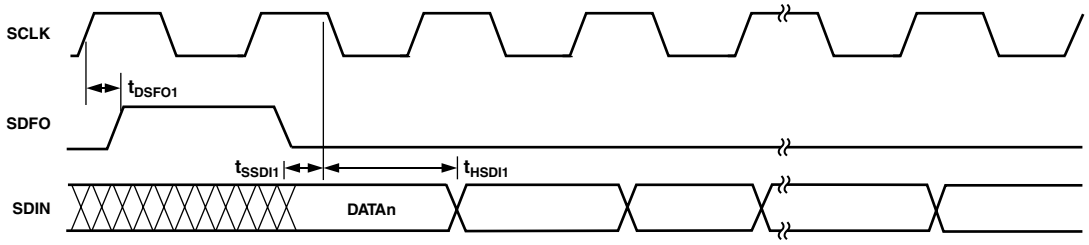


Figure 9. Serial Port Timing, Slave Mode (SCS = 1), Channel is Self-Framing

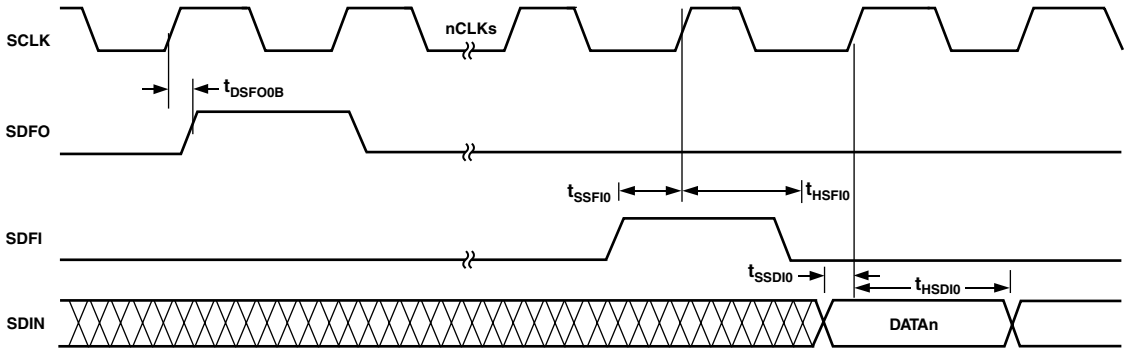


Figure 10. Serial Port Timing, Master Mode (SCS = 0), Channel is External-Framing

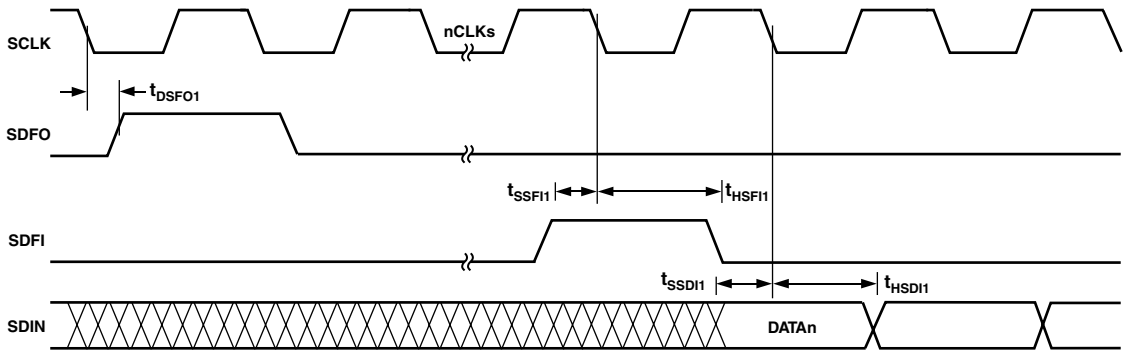
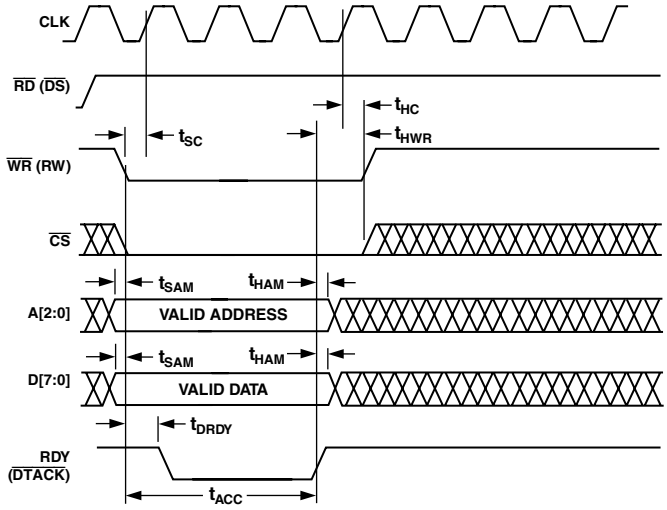


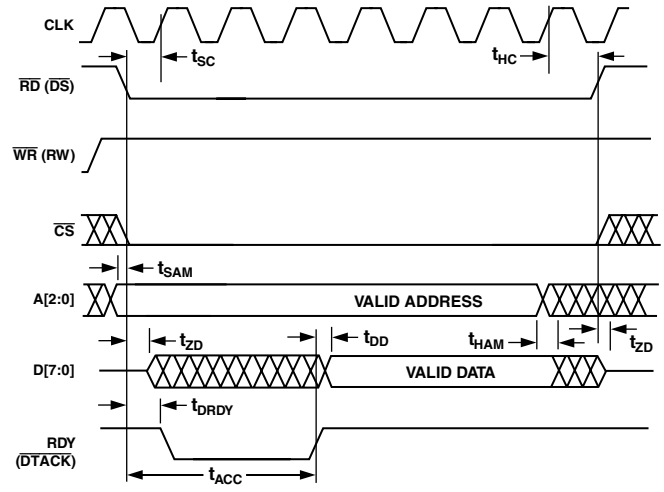
Figure 11. Serial Port Timing, Slave Mode (SCS = 1), Channel is External-Framing

TIMING DIAGRAMS—INM MICROPORT MODE



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{WR}$ TO THE RE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM 9 CLK PERIODS.

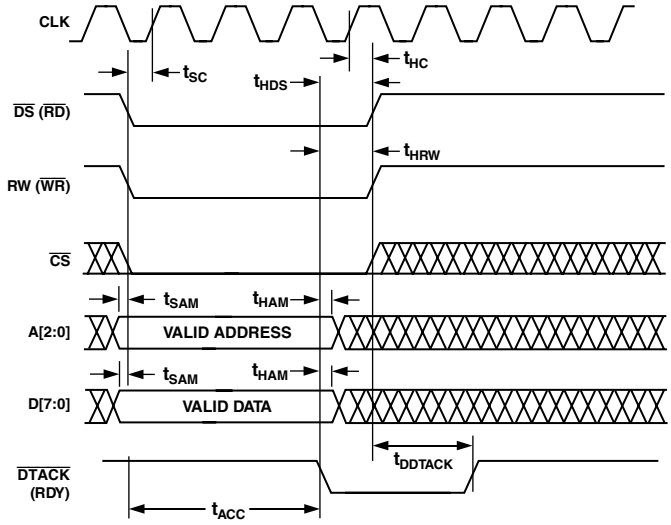
Figure 12. INM Microport Write Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{WR}$ TO THE RE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS AND APPLIES TO A[2:0] = 7, 6, 5, 3, 2, 1

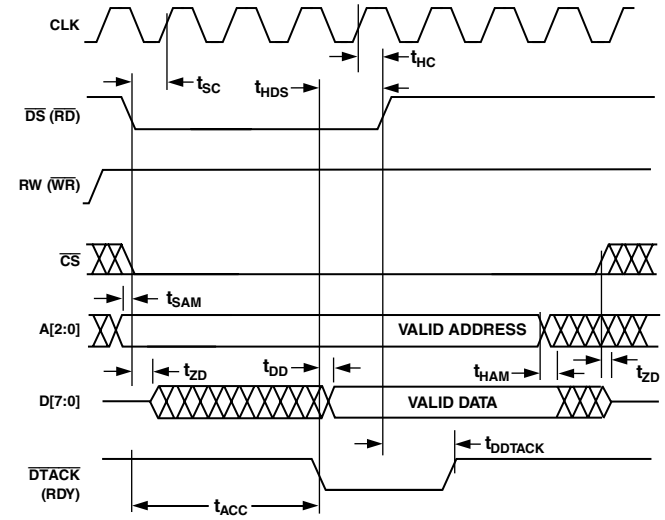
Figure 13. INM Microport Read Timing Requirements

TIMING DIAGRAMS—MNM MICROPORT MODE



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{DS}$ TO THE FE OF $\overline{DTACK}$.
2. t_{ACC} REQUIRES A MAXIMUM 9 CLK PERIODS.

Figure 14. MNM Microport Write Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{DS}$ TO THE FE OF $\overline{DTACK}$.
2. t_{ACC} REQUIRES A MAXIMUM 13 CLK PERIODS.

Figure 15. MNM Microport Read Timing Requirements

ABSOLUTE MAXIMUM RATINGS*

VDDIO . . . . . –0.3 V to +3.6 V
VDD . . . . . –0.3 V to +2.75 V
Input Voltage . . . . . –0.3 V to +5 V (5 V Tolerant)
Output Voltage Swing . . . . . –0.3 V to VDDIO + 0.3 V
Load Capacitance . . . . . 200 pF
Junction Temperature Under Bias . . . . . 125°C
Operating Temperature . . . . . –40°C to +85°C (Ambient)
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) . . . . . 280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the devices at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

128-Lead MQFP with Internal Heat Spreader:
θ_{JA} = 28.1°C/W, no airflow
θ_{JA} = 22.6°C/W, 200 lfpm airflow
θ_{JA} = 20.5°C/W, 400 lfpm airflow

196-Lead BGA:
θ_{JA} = 26.3°C/W, no airflow
θ_{JA} = 22°C/W, 200 lfpm airflow

Thermal measurements made in the horizontal position on a 4-layer board.

EXPLANATION OF TEST LEVELS

I. 100% Production Tested
II. 100% Production Tested at 25°C, and Sample Tested at Specified Temperatures
III. Sample Tested Only
IV. Parameter Guaranteed by Design and Analysis
V. Parameter is Typical Value Only

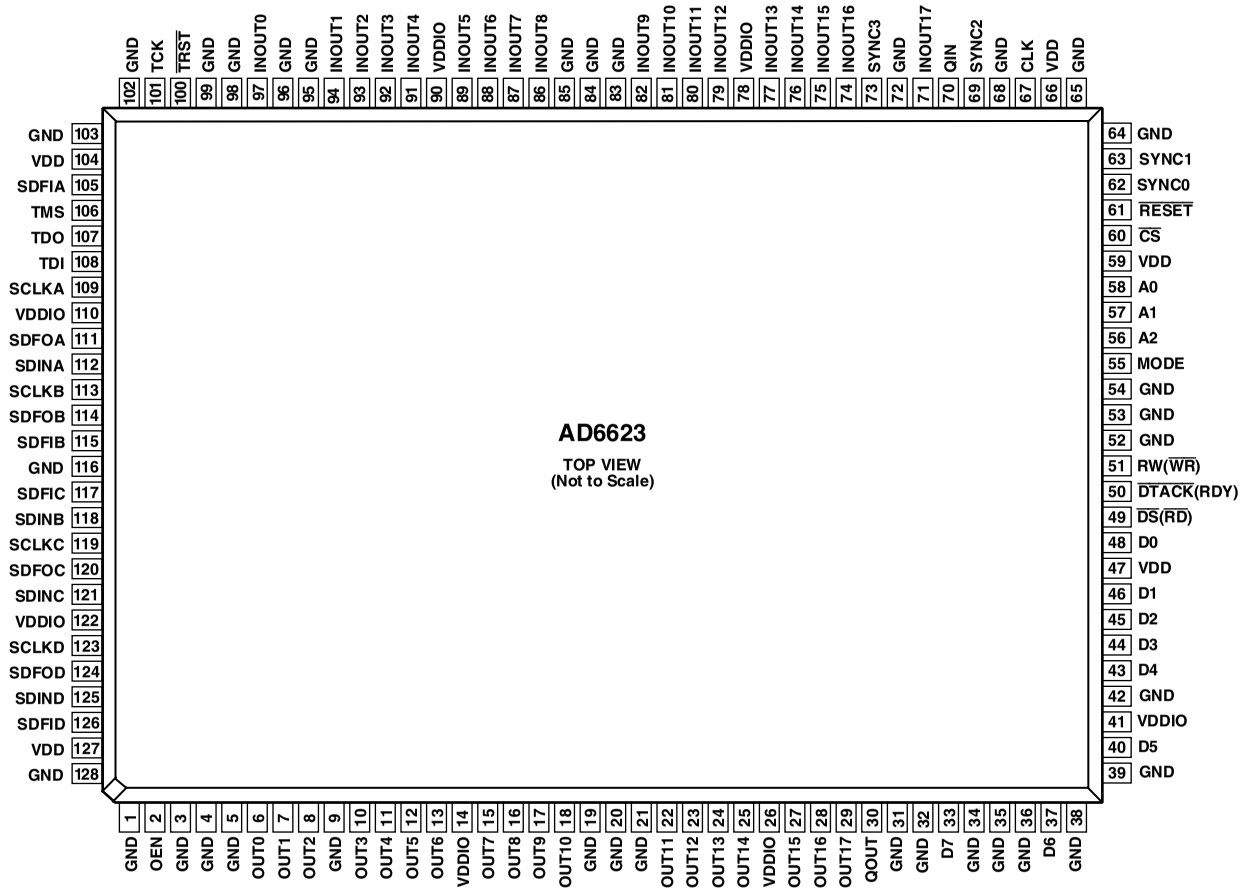
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6623AS	–40°C to +85°C (Ambient)	128-Lead MQFP (Plastic Quad Flatpack)	S-128
AD6623ABC	–40°C to +85°C (Ambient)	196-Lead CSPBGA (Chip Scale Package Ball Grid Array)	BC-196
AD6623S/PCB		MQFP Evaluation Board with AD6623 and Software	
AD6623BC/PCB		CSPBGA Evaluation Board with AD6623 and Software	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6623 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
128-Lead MQFP

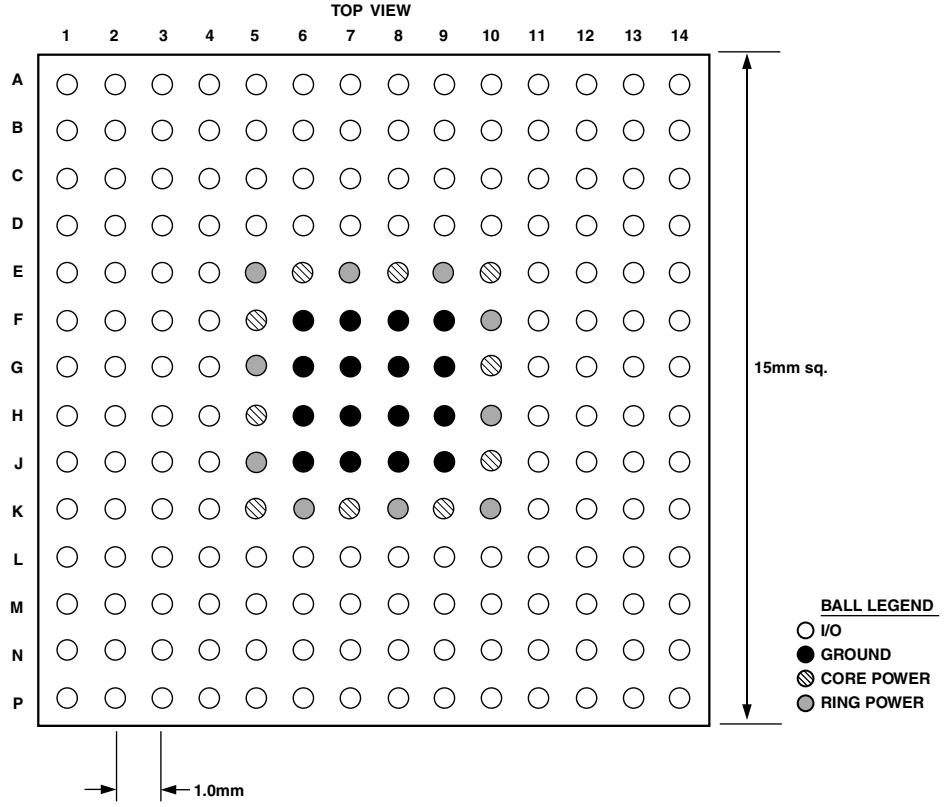


128-LEAD FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Type	Description
1, 3–5, 9, 19–21, 31, 32, 34–36, 38, 39, 42, 52–54, 64–65, 68, 72, 83–85, 95, 96, 98, 99, 102, 103, 116, 128	GND	P	Ground Connection
2	OEN[1]	I	Active High Output Enable Pin
29, 28, 27, 25, 24, 23, 22, 18, 17, 16, 15, 13, 12, 11, 10, 8, 7, 6	OUT[17:0]	O/T	Parallel Output Data
47, 59, 66, 104, 127	VDD	P	2.5 V Supply
14, 26, 41, 78, 90, 110, 122	VDDIO	P	3.3 V Supply
30	QOUT	O/T	When HIGH indicates Q Output Data (Complex Output Mode)
33, 37, 40, 43, 44, 45, 46, 48	D[7:0]	I/O/T	Bidirectional Microport Data
49	$\overline{\text{DS}}$ ($\overline{\text{RD}}$)	I	INM Mode: Read Signal, MNM Mode: Data Strobe Signal
50	$\overline{\text{DTACK}}$ (RDY)	O	Acknowledgment of a Completed Transaction (Signals when µP Port Is Ready for an Access) Open Drain, Must Be Pulled Up Externally
51	RW ($\overline{\text{WR}}$)	I	Active HIGH Read, Active Low Write
55	MODE	I	Sets Microport Mode: MODE = 1, MNM Mode; MODE = 0, INM Mode
56, 57, 58	A[2:0]	I	Microport Address Bus
60	$\overline{\text{CS}}$	I	Chip Select, Active low enable for µP Access
61	$\overline{\text{RESET}}$[2]	I	Active Low Reset Pin
62	SYNC0[1]	I	SYNC Signal for Synchronizing Multiple AD6623s
63	SYNC1[1]	I	SYNC Signal for Synchronizing Multiple AD6623s
67	CLK[1]	I	Input Clock
69	SYNC2[1]	I	SYNC Signal for Synchronizing Multiple AD6623s
70	QIN[1]	I	When HIGH indicates Q input data (Complex Input Mode)
71, 74–77, 79–82, 86–89, 91–94, 97	INOUT[17:0][1]	I/O	Wideband Input/Output Data (Allows Cascade of Multiple AD6623 Chips In a System)
73	SYNC3[1]	I	SYNC Signal for Synchronizing Multiple AD6623s
100	$\overline{\text{TRST}}$[2]	I	Test Reset Pin
101	TCK[1]	I	Test Clock Input
105	SDFIA	I	Serial Data Frame Input—Channel A
106	TMS[2]	I	Test Mode Select
107	TDO	O	Test Data Output
108	TDI[1]	I	Test Data Input
109	SCLKA	I/O	Bidirectional Serial Clock—Channel A
111	SDFOA	O	Serial Data Frame Sync Output—Channel A
112	SDINA[1]	I	Serial Data Input—Channel A
113	SCLKB	I/O	Bidirectional Serial Clock—Channel B
114	SDFOB	O	Serial Data Frame Sync Output—Channel B
115	SDFIB	I	Serial Data Frame Input —Channel B
117	SDFIC	I	Serial Data Frame Input—Channel C
118	SDINB[1]	I	Serial Data Input—Channel B
119	SCLKC	I/O	Bidirectional Serial Clock—Channel C
120	SDFOC	O	Serial Data Frame Sync Output—Channel C
121	SDINC[1]	I	Serial Data Input—Channel C
123	SCLKD	I/O	Bidirectional Serial Clock—Channel D
124	SDFOD	O	Serial Data Frame Sync Output—Channel D
125	SDIND[1]	I	Serial Data Input—Channel D
126	SDFID	I	Serial Data Frame Input—Channel D

NOTES
[1]Pins with a Pull-Down resistor of nominal 70 kΩ.
[2]Pins with a Pull-Up resistor of nominal 70 kΩ.

PIN CONFIGURATION
196-Lead CSPBGA



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC			SDFID	SDINC	SDINB	SDFOB	SCLKB	SCLKA	TDO	SDFIA	TCK		NC
B				OEN	SDIND	SDFOC	SDFIC	SDINA	TDI		$\overline{\text{TRST}}$			
C				SDFOD		SCLKD	SCLKC	SDFIB	SDFOA	TMS				IN0
D	OUT2		OUT0									IN2		IN1
E		OUT1	OUT3		VDDIO	VDD	VDDIO	VDD	VDDIO	VDD				IN4
F	OUT5	OUT4	OUT6		VDD	GND	GND	GND	GND	VDDIO		IN3	IN5	IN7
G	OUT8	OUT7			VDDIO	GND	GND	GND	GND	VDD		IN6	IN8	IN9
H	OUT9	OUT10	OUT12		VDD	GND	GND	GND	GND	VDDIO			IN11	IN10
J	OUT11	OUT13			VDDIO	GND	GND	GND	GND	VDD		IN12	IN14	IN13
K	OUT14		OUT17		VDD	VDDIO	VDD	VDDIO	VDD	VDDIO		IN16	IN17	IN15
L	OUT16		OUT15									QIN		SYNC3
M	QOUT		D7	D4	D1	$\overline{\text{DTACK}}$ (RDY)	MODE (ALE)	A1	$\overline{\text{RESET}}$					SYNC2
N				D5	D3	D0	RW($\overline{\text{WR}}$)		A0	SYNC0				
P	NC	D6		D2		$\overline{\text{DS}}$($\overline{\text{RD}}$)			A2	$\overline{\text{CS}}$	SYNC1		CLK	NC

NC = NO CONNECT

196-LEAD FUNCTION DESCRIPTIONS

Mnemonic	Type	Function
POWER SUPPLY		
VDD	P	2.5 V Supply
VDDIO	P	3.3 V IO Supply
GND	G	Ground
INPUTS		
INOUT[17:0][1]	I/O	A Input Data (Mantissa)
QIN[1]	I	When HIGH Indicates Q Input Data (Complex Input Mode)
$\overline{\text{RESET}}$[2]	I	Active LOW Reset Pin
CLK[1]	I	Input Clock
SYNC0[1]	I	All Sync Pins Go to All Four Output Channels
SYNC1[1]	I	All Sync Pins Go to All Four Output Channels
SYNC2[1]	I	All Sync Pins Go to All Four Output Channels
SYNC3[1]	I	All Sync Pins Go to All Four Output Channels
SDINA[1]	I	Serial Data Input—Channel A
SDINB[1]	I	Serial Data Input—Channel B
SDINC[1]	I	Serial Data Input—Channel C
SDIND[1]	I	Serial Data Input—Channel D
$\overline{\text{CS}}$	I	Active LOW Chip Select
CONTROL		
SCLKA	I/O	Bidirectional Serial Clock—Channel A
SCLKB	I/O	Bidirectional Serial Clock—Channel B
SCLKC	I/O	Bidirectional Serial Clock—Channel C
SCLKD	I/O	Bidirectional Serial Clock—Channel D
SDFOA	O	Serial Data Frame Sync Output—Channel A
SDFOB	O	Serial Data Frame Sync Output—Channel B
SDFOC	O	Serial Data Frame Sync Output—Channel C
SDFOD	O	Serial Data Frame Sync Output—Channel D
SDFIA	I	Serial Data Frame Input—Channel A
SDFIB	I	Serial Data Frame Input—Channel B
SDFIC	I	Serial Data Frame Input—Channel C
SDFID	I	Serial Data Frame Input—Channel D
OEN[1]	I	Active High Output Enable Pin
MICROPORT CONTROL		
D[7:0]	I/O/T	Bidirectional Microport Data
A[2:0]	I	Microport Address Bus
$\overline{\text{DS}}$ ($\overline{\text{RD}}$)	I	Active Low Data Strobe (Active Low Read)
$\overline{\text{DTACK}}$ (RDY)[2]	O/T	Active Low Data Acknowledge (Microport Status Bit)
RW ($\overline{\text{WR}}$)	I	Read Write (Active Low Write)
MODE	I	Intel or Motorola Mode Select
OUTPUTS		
OUT[17:0]	O	Wideband Output Data
QOUT	O	When HIGH Indicates Q Output Data (Complex Output Mode)
JTAG AND BIST		
$\overline{\text{TRST}}$[2]	I	Test Reset Pin (Active Low)
TCK[1]	I	Test Clock Input
TMS[2]	I	Test Mode Select Input
TDO	O/T	Test Data Output
TDI[1]	I	Test Data Input

NOTES
[1]Pins with a Pull-Down resistor of nominal 70 kΩ.
[2]Pins with a Pull-Up resistors of nominal 70 kΩ.

CONTROL REGISTER ADDRESS NOTATION

Register address notation and bit assignment referred to throughout this data sheet are as follows: There are eight, one-digit "External" register addresses in decimal format. "Internal" address notation (read from left to right) begins with "0x", meaning the address that follows is hexadecimal. The next three characters represent the address. The first number or character is the MSB of the address. If an "n" is present, its value can be 1, 2, 3, or 4 and it depends upon the channel that is being addressed (A, B, C, or D). The remaining two digits preceding the colon (if present) are the LSBs of the address. If a colon follows the address, then the succeeding digits tell the user what bit number(s) is/are involved in decimal format. For example, 0xn24:7-0.

SERIAL DATA PORT

The AD6623 has four independent Serial Ports (A, B, C, and D), and each accepts data to its own channel (A, B, C, or D) of the device. Each Serial Port has four pins: SCLK (Serial CLocK), SDFO (Serial Data Frame Out), SDFI (Serial Data Frame In), and SDIN (Serial Data INput). SDFI and SDIN are inputs, SDFO is an output, and SCLK is either input or output depending on the state of SCS (Serial Clock Slave: 0xn16, Bit 4). Each channel can be operated either as a Master or Slave channel depending upon SCS. The Serial Port can be self-framing or accept external framing from the SFDI pin or from the previous adjacent channel (0xn16, Bits 7 and 6).

Serial Master Mode (SCS = 0)

In master mode, SCLK is created by a programmable internal counter that divides CLK. When the channel is "sleeping," SCLK is held low. SCLK becomes active on the first rising edge of CLK after Channel sleep is removed (D0 through D3 of external address 4). Once active, the SCLK frequency is determined by the CLK frequency and the SCLK divider, according to the equations below.

AD6623 mode:

$$f_{SCLK} = \frac{f_{CLK}}{SCLKdivider + 1} \quad (1)$$

AD6622 mode:

$$f_{SCLK} = \frac{f_{CLK}}{2 \times (SCLKdivider + 1)} \quad (2)$$

The SCLK divider is a 5-bit unsigned value located at Internal Channel Address 0xn0D (Bits 4–0), where "n" is 1, 2, 3, or 4 for the chosen channel A, B, C, or D, respectively. The user must select the SCLK divider to insure that SCLK is fast enough to accept full input sample words at the input sample rate. See the design example at the end of this section. The maximum SCLK frequency is equal to the CLK when operating in AD6623 mode serial clock master. When operating in AD6622 compatible mode, the maximum SCLK frequency is one-half the CLK. The minimum SCLK frequency is 1/32 of the CLK frequency in AD6623 mode or 1/64 of the CLK frequency when in AD6622 mode. SDFO changes on the positive edge of SCLK when in master mode. SDIN is captured on positive edge when SCLK is in master mode.

Serial Slave Mode (SCS = 1)

Any of the AD6623 serial ports may be operated in the serial slave mode. In this mode, the selected AD6623 channel requires that an external device such as a DSP to supply the SCLK. This is done to synchronize the serial port to meet an external timing requirement. SDIN is captured on negative edge of SCLK when in slave mode.

Serial Data Framing

The SDIN input pin of each transmit channel of the AD6623 receives data from an external DSP to be digitally filtered, interpolated, and then modulated by the NCO-generated carrier. Serial data from the DSP to the AD6623 is sent as a series of blocks or frames. The length of each block is a function of the desired output format that is supported by the AD6623. Block length may range from 1 bit (MSK) to 32 bits of I and Q data.

The flow of data to the SDIN input is regulated either by the AD6623 (in Self-Framing Mode) or by the external DSP (using AD6623 External Framing Mode). This is accomplished by generating a pulse, SDFO or SDFI, to indicate that the next frame or serial data block is ready to be input or sent to the AD6623. Functions of the two pins, SDFO and SDFI, are fully described in the framing modes that follow.

Self-Framing Mode

In this mode Bit 7 of register 0xn16 is set low. The serial data frame output, SDFO, generates a self-framing data request and is pulsed high for one SCLK cycle at the input sample rate. In this mode, the SDFI pin is not used, and the SDFO signal would be programmed to be a serial data frame request (0xn16, Bit 5 = 0). SDFO is used to provide a sync signal to the host. The input sample rate is determined by the CLK divided by channel interpolation factor. If the SCLK rate is not an integer multiple of the input sample rate, then the SDFO will continually adjust the period by one SCLK cycle to keep the average SDFO rate equal to the input sample rate. When the channel is in sleep mode, SDFO is held low. The first SDFO is delayed by the channel reset latency after the Channel Reset is removed. The channel reset latency varies dependent on channel configuration.

External Framing Mode

In this mode Bit 7 of register 0xn16 is set high. The external framing can come from either the SDFI pin (0xn16, Bit 6 = 0) or the previous adjacent channel (0xn16, Bit 6 = 1). In the case of external framing from a previous channel, it uses the internal frame end signal for serial data frame synchronizing. When in master mode, SDFO and SDFI transition on the positive edge of SCLK, and SDIN is captured on the positive edge of SCLK. When in slave mode, SDFO and SDFI transition on the negative edge of SCLK, and SDIN is captured on the negative edge of SCLK.

Serial Port Cascade Configuration

In this case the SDFO signal from the last channel of the first chip would be programmed to be a serial data frame end (SFE:0xn16, Bit 5 = 1). This SDFO signal would then be fed as an input for the second cascaded chip's SDFI pin input. The second chip would be programmed to accept external framing from the SDFI pin (0xn16, Bit 7 = 1, Bit 6 = 0).

Serial Data Format

The format of data applied to the serial port is determined by the RCF mode selected in Control Register 0xn0C. Below is a table showing the RCF modes and input data format that it sets.

Table I. Serial Data Format

0xn0C Bit 6	0xn0C Bit 5	0xn0C Bit 4	Serial Data Word Length	RCF Mode
0	0	0	32	FIR
0	0	1		π/4-DQPSK
0	1	0		GMSK
0	1	1		MSK
1	0	0	24 (Bit 9 is high)	FIR,
			16 (Bit 9 is low)	compact
1	0	1		8-PSK
1	1	0		3π/8-8-PSK
1	1	1		QPSK

The serial data input, SDIN, accepts 32-bit words as channel input data. The 32-bit word is interpreted as two 16-bit two's complement quadrature words, I followed by Q, MSB first. This results in linear I and Q data being provided to the RCF. The first bit is shifted into the serial port starting on the next rising edge of SCLK after the SDFO pulse. Figure 16 shows a timing diagram for SCLK master (SCS = 0) and SDFO set for frame request (SFE = 0).

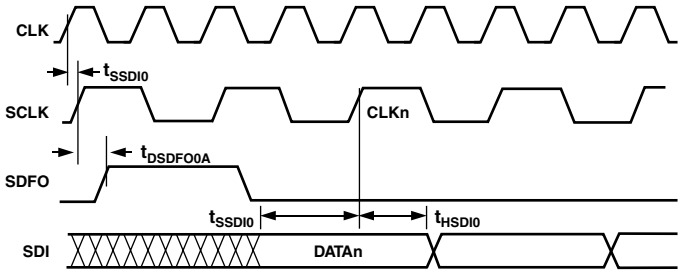


Figure 16. Serial Port Switching Characteristics

As an example of the Serial Port operation, consider a CLK frequency of 62.208 MHz and a channel interpolation of 2560. In that case, the input sample rate is 24.3 kSPS (62.208 MHz/2560), which is also the SDFO rate. Substituting, $f_{SCLK} \geq 32\ 3\ f_{SDFO}$ into the equation and solving for SCLKdivider, we find the minimum value for SCLKdivider according to the equation below.

$$SCLKdivider \leq \frac{f_{CLK}}{32 \times f_{SDFO}} \quad (3)$$

Evaluating this equation for our example, SCLKdivider must be less than or equal to 79. Since the SCLKdivider channel register is a 5-bit unsigned number it can only range from 0 to 31. Any value in that range will be valid for this example, but if it is important that the SDFO period is constant, then there is another restriction. For regular frames, the ratio f_{SCLK}/f_{SDFO} must be equal to an integer of 32 or larger. For this example, constant SDFO periods can only be achieved with an SCLK divider of 31 or less.

See Table II for usable SCLK divider values and the corresponding SCLK and f_{SCLK}/f_{SDFO} ratio for the example of L = 2560.

In conclusion, SDFO rate is determined by the AD6623 CLK rate and the interpolation rate of the channel. The SDFO rate is equal to the channel input rate. The channel interpolation is equal to RCF interpolation times CIC5 interpolation, times CIC2 interpolation:

$$\left(L = L_{RCF} \times L_{CIC5} \times \frac{L_{CRIC2}}{M_{CRIC2}} \right) \quad (4)$$

The SCLK divide ratio is determined by SCLKdivider as shown in equation 3. The SCLK must be fast enough to input 32 bits of data prior to the next SDFO. Extra SCLKs are ignored by the serial port.

Table II. Example of Usable SCLK Divider Values and f_{SCLK}/f_{SDFO} Ratios for L = 2560

SCLKdivider	f_{SCLK}/f_{SDFO}
0	2560
1	1280
3	640
4	512
7	320
9	256
15	160
19	128
31	80

PROGRAMMABLE RAM COEFFICIENT FILTER (RCF)

Each channel has a fully independent RAM Coefficient Filter (RCF). The RCF accepts data from the Serial Port, processes it, and passes the resultant I and Q data to the CIC filter. A variety of processing options may be selected individually or in combination, including PSK and MSK modulation, FIR filtering, all-pass phase equalization, and scaling with arbitrary ramping. See Table III.

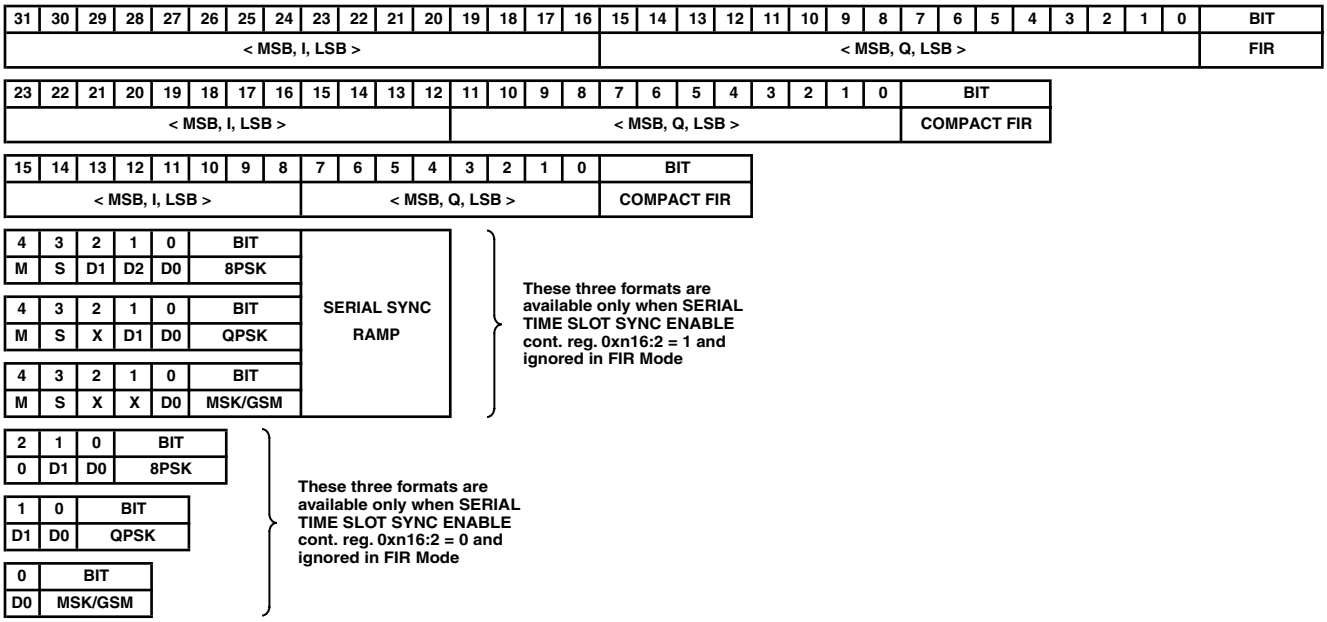
Table III. Data Format Processing Options

Processing Block	Input Data	Output Data
Interpolating FIR Filter	I and Q	I and Q
PSK Modulator	2 or 3 bits per symbol	Unfiltered I and Q: π/4-QPSK, 8-PSK, or 3π/8-8-PSK
MSK Modulator	1 bit per symbol	Filtered MSK or GSM I and Q
QPSK	2 bits per symbol	Filtered QPSK I and Q
All-pass Phase Equalizer	I and Q	I and Q
Scale and Ramp	I and Q	I and Q

OVERVIEW OF THE RCF BLOCKS

The Serial Port passes data to the RCF with the appropriate format and bit precision for each RCF configuration, see Figure 17. The data may be modulated vectors or unmodulated bits. I and Q vectors are sent directly to the Interpolating Fir Filter. Unmodulated bits may be sent to the PSK Modulator, the Interpolating MSK Modulator, or the Interpolating QPSK Modulator. The PSK Modulator produces unfiltered I and Q vectors at the symbol rate which are then passed through the Interpolating FIR Filter. The Interpolating MSK Modulator and the Interpolating QPSK Modulator produce oversampled, pulse-shaped vectors directly without employing the Interpolating FIR Filter. When possible, the MSK and QPSK modulators are recommended for increased throughput and decreased power consumption compared to Interpolating FIR Filter. In addition, the Interpolating MSK Modulator can realize filters with nonlinear inter-symbol interference, achieving excellent accuracy for GMSK applications.

After interpolation, an optional Allpass Phase Equalizer (APE) can be inserted into the signal path. The APE can realize any real, stable, two-pole, two-zero all-pass filter at the RCF's interpolated rate. This is especially useful to precompensate for nonlinear phase responses of receive filters in terminals, as specified by IS-95. When active, the APE utilizes shared hardware with the interpolating modulators and filter, which may reduce the allowed RCF throughput, inter-symbol interference, or both. See Figure 18.



M = mode bit. If M = 0, then the MSB of 3-bit mode select word at 0xn0C:6 is set to 0 (this is also called MODE 0). If M = 1, then the MSB is set to 1 and this is MODE 1. Mode allows quick format changes via the serial port, for example, 010 = GMSK and 110 = 3pi/8PSK. The value m should be held for the duration of the time slot since the value of m will only be updated after the RCF Scale Holdoff Counter reaches a value of 1 (see below).

S = serial time slot sync bit. If S = 0, then no sync is generated. If S = 1, a "Serial Time Slot Sync" occurs that loads the RCF Scale Hold-off Counter with a user programmed value and commences a backwards count of CLK cycles. When the counter reaches one, an automatic sequence occurs as follows: Power Ramp Down occurs, m (above) is updated, serial input is suspended for a REST or QUIET time and any control register with a 2 superscript is updated. After REST, the serial input becomes active and the power level is ramped up to the Fine Scale multiplier value or any lesser power level. Ramp enable bit, 0xn16:0, must be set to logic 1 for the ramp functions to occur. See the RCF Power Ramping and Time Slot Synchronization sections for more detail.

X = don't care

D = payload data bit

Important notes: The sync pulse, s, should be held at Logic 1 for only one serial frame since every frame with Logic 1 in the s position will cause the RCF Scale Hold-off Counter to reload its beginning count and begin counting again. The RCF Scale Hold-off Counter counts master CLK cycles. The REST time period is a programmable 5-bit value that counts interpolated RCF output samples before resuming serial input to the channel. The succeeding actions of any hold-off counter in the AD6623 can be defeated by setting its count value to 0.

Figure 17. Data Formats Supported by the AD6623 when SCLK Master (SCS = 0), and SFDO Set for Frame Request (SFE = 0)

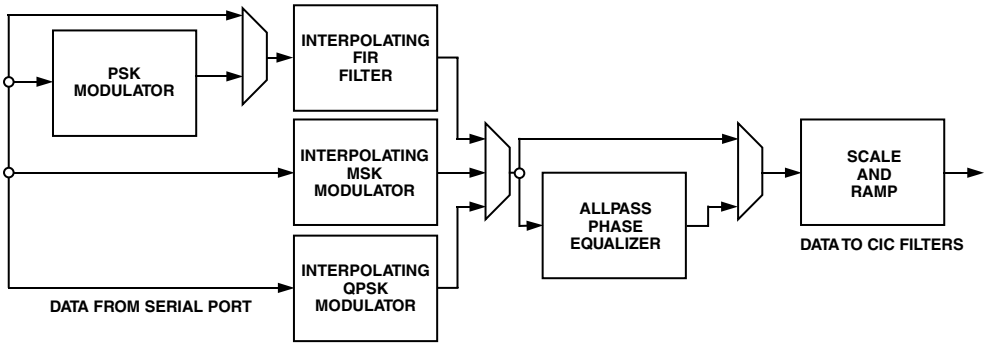


Figure 18. RCF Block Diagram

Table IV. FIR Filter Internal Precision

Signal	x × y Notation	Minimum		Maximum	
		Decimal	Hexadecimal (h)	Decimal	Hexadecimal (h)
I and Q Inputs	1.15	–1.00000	+1.00000	0.999969	0.FFFE
Coefficients	1.15	–1.00000	+1.00000	0.999969	0.FFFE
Product	2.18	–0.99969	+3.00020	1.000000	1.00000
Sum	4.18	–7.00000	+8.00000	7.999996	7.FFFFC
FIR Output	1.17	–1.00000	+1.00000	0.999992	0.FFFF8

The Scale and Ramp block adjusts the final magnitude of the modulated RCF output. A synchronization pulse from the SYNC0–3 pins or serial words can be used to command this block to ramp down, pause, and ramp up to a new scale factor. The shape of the ramp is stored in RAM, allowing complete sample by sample control at the RCF interpolated rate. This is particularly useful for time division multiplexed standards such as GSM/EDGE. Modulator configurations can be updated while the ramp is quiet, allowing for GSM and EDGE timeslots to be multiplexed together without resetting or reconfiguring the channel. Each of the RCF processing blocks is discussed in greater detail in the following sections.

INTERPOLATING FIR FILTER

The Interpolating FIR Filter realizes a real, sum-of-products filter on I and Q inputs using a single interleaved Multiply-Accumulator (MAC) running at the CLK rate. The input signal is interpolated by integer factors to produce arbitrary impulse responses up to 256 output samples long.

Each bus in the data path carries bipolar two's complement values. For the purpose of discussion, we will arbitrarily consider the radix point positioned so that the input data ranges from –1 to just below 1. In Figure 19, the data buses are marked x × y to denote finite precision limitations. A bus marked x × y has x bits above the radix and y bits below the radix, which implies a range from -2^{x-1} to $2^{x-1} - 2^{-y}$ in 2^{-y} steps. The range limits are tabulated in Table IV for each bus. The hexadecimal values are bit-exact and each MSB has negative weight. Note that the Product bus range is limited by result of the multiplication and the two most significant bits are the same except in one case.

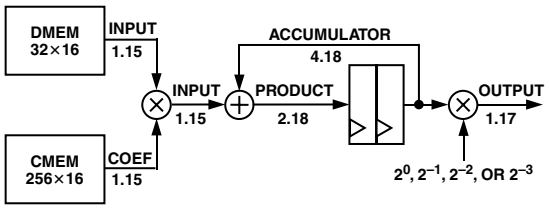


Figure 19. Interpolating FIR Filter Block Diagram

The RCF realizes a FIR filter with optional interpolation. The FIR filter can produce impulse responses up to 256 output samples long. The FIR response may be interpolated up to a factor of 256, although the best filter performance is usually achieved when the RCF interpolation factor (L_{RCF}) is confined to eight or below. The 256 × 16 coefficient memory (CMEM) can be divided among an arbitrary number of filters, one of which is selected by the Coefficient Offset Pointer (channel address 0x0B). The polyphase implementation is an efficient equivalent to an integer up-sampler followed FIR filter running at the interpolated rate.

The AD6623 RCF realizes a sum-of-products filter using a polyphase implementation. This mode is equivalent to an interpolator followed by a FIR filter running at the interpolated rate. In the functional diagram below, the interpolating block increases the rate by the RCF interpolation factor (L_{RCF}) by inserting L_{RCF}–1 zero valued samples between every input sample. The next block is a filter with a finite impulse response length (N_{RCF}) and an impulse response of h[n], where n is an integer from 0 to N_{RCF}–1.

The difference equation for Figure 20 is written below, where h[n] is the RCF impulse response, b[n] is the interpolated input sample sequence at point 'b' in the diagram above, and c[n] is the output sample sequence at point 'c' in Figure 20.

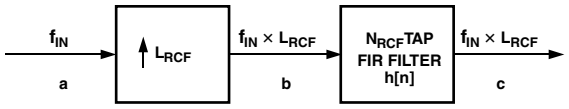


Figure 20. RCF Interpolation

$$c[n] = \sum_{k=0}^{N_{RCF}-1} h[n] \times b[n-k] \quad (5)$$

This difference equation can be described by the transfer function from point 'b' to 'c' as:

$$H_{bc}(z) = \sum_{k=0}^{N_{RCF}-1} h[n] \times z^{-1} \quad (6)$$

The actual implementation of this filter uses a polyphase decomposition to skip the multiply-accumulates when b[n–k] is zero. Compared to the diagram above, this implementation has the benefits of reducing by a factor of L_{RCF} both the time needed to calculate an output and the required data memory (DMEM). The price of these benefits is that the user must place the coefficients into the coefficient memory (CMEM) indexed by the interpolation phase. The process of selecting the coefficients and placing them into the CMEM is broken into three steps shown below.

The FIR accepts two's complement I and Q samples from the serial port with a fixed-point resolution of 16 bits each. When the serial port provides data with less precision, the LSBs are padded with zeroes.

The Data-Mem stores the most recent 16 I and Q pairs for a total of 32 words. The size of the Data-Mem limits the RCF impulse response to 16 × L_{RCF} output samples. When the data words from the Serial Port have fewer than 16 bits, the LSBs are padded with zeroes. The Data-Mem can be accessed through the Microport from 0x20 to 0x5F above the processing channel's base internal address, while the channel's Prog bit is set (external address 4). In order to avoid start-up transients, the Data-Mem should be cleared before operation. The Prog bit must then be reset to enable normal operation.

The Coef-Mem stores up to 256 16-bit filter coefficients. The Coef-Mem can be accessed through the Microport from 0x800 to 0x8FF above the processing channel's base internal address, while the channel's Prog bit is set (external address 4). For AD6622 compatibility, the lower 128 words are also mirrored from 0x080 to 0x0FF above the processing channel's base internal address, while the Prog bit is set.

There is a single Multiply-Accumulator (MAC) on which both the I and Q operations must be interleaved. Two CLK cycles are required for the MAC to multiply each coefficient by an I and Q pair. The MAC is also used for four additional CLK cycles if the All-pass Phase Equalizer is active.

The size of the Data-Mem and Coef-Mem combined with the speed of the MAC determine the total number of the taps per phase (T_{RCF}) that may be calculated. T_{RCF} is the number of RCF input samples that influence each RCF output sample. The maximum available T_{RCF} is calculated by the equation below.

$$T_{RCF} \le least\ of\left(16, floor\left(\frac{256}{L_{RCF}}\right), floor\left(\frac{f_{CLK}}{2 \times f_{SDFO}} - 2 \times APE\right)\right) \quad (7)$$

Where APE = 1 (allpass phase equalizer enabled) or 0 (allpass phase equalizer disabled) and f_{SDFO} = [Output Data Rate/Total Interpolation Rate] in Hz. "*floor()*" indicates that the value within the parenthesis should be reduced to the lowest integer, e.g., floor(9.9999) = 9.

The impulse response length at the output of the RCF is determined by the product of the number of interfering input samples (T_{RCF}) and the RCF interpolation factor (L_{RCF}), as shown by equation (8) below. The values of N_{RCF} and T_{RCF} are programmed into control registers. L_{RCF} is not a control register, but N_{RCF} and T_{RCF} must be set so that L_{RCF} is an integer. If the integer interpolation by the RCF results in an inconvenient sample rate at the output of the RCF, the desired output rate can usually be achieved by selecting non-integer interpolation in the resampling CIC^2 filter.

$$N_{RCF} = T_{RCF} \times L_{RCF} \quad (8)$$

Table V. Channel A RCF Control Registers

Channel Address	Bit Width	Description
0x10A	16	15–8: N_{RCF} –1 B; 7–0: N_{RCF} –1 A
0x10B	8	7–0: O_{RCF}
0x10C	10	9: Ch. A Compact FIR Input Word Length 0: 16 bits–8 I followed by 8 Q 1: 24 bits–12 I followed by 12 Q 8: Ch. A RCF PRBS Enable 7: Ch A RCF PRBS Length 0: 15 1: 8,388,607 6–4: Ch. A RCF Mode Select 000 = FIR 001 = π/4-DQPSK Modulator 010 = GMSK Look-Up Table 011 = MSK Look-Up Table 100 = FIR compact mode 101 = 8-PSK 110 = 3π/8-8PSK Modulator 111 = QPSK Look-Up Table 3–0: Ch. A RCF Taps per Phase
0x10D	8	7–6: RCF Coarse Scale (g): 00 = 0 dB 01 = –6 dB 10 = –12 dB 11 = –18 dB 5: Ch. A Allpass Ph. Eq. Enable 4–0: Serial Clock Divider (1, ..., 32)
0x10E	16	15–2: Ch. A Unsigned Scale Factor 1–0: Reserved
0x10F	18	17–16: Ch. A Time Slot Sync Select 00: Sync0 (See 0x001 Time Slot) 01: Sync1 10: Sync2 11: Sync3 15–0: Ch. A RCF Scale Hold-Off Counter 1) Ramp Down (if Ramp is enabled) 2) Update Scale and Mode 3) Ramp Up (if Ramp is enabled)
0x110	16	15–0: Ch. A RCF Phase EQ Coef1
0x111	16	15–0: Ch. A RCF Phase EQ Coef2
0x112	16	15–0: Ch. A RCF MPSK Magnitude 0
0x113	16	15–0: Ch. A RCF MPSK Magnitude 1
0x114	16	15–0: Ch. A RCF MPSK Magnitude 2
0x115	16	15–0: Ch. A RCF MPSK Magnitude 3
0x116	8	7: Reserved 6: Ch. A Serial Data Frame Select 0: Serial Data Frame Request 1: Serial Data Frame End 5: Ch. A External SDFI Select 0: Internal SDFI 1: External SDFI 4: Ch. A SCLK Slave Select 0: Master 1: Slave 3: Ch. A Serial Fine Scale Enable 2: Ch. A Serial Time Slot Sync Enable (ignored in FIR mode) 1: Ch. A Ramp Interpolation Enable 0: Ch. A Ramp Enable
0x117	6	5–0: Ch. A Mode 0 Ramp Length, R0–1
0x118	6	5–0: Ch. A Mode 1 Ramp Length, R1–1
0x119	5	4–0: Ch. A Ramp Rest Time, Q
0x11A–0x11F		Reserved
0x120–0x13F	16	15–0: Ch. A Data Memory
0x140–0x17F	16	15–14: Reserved 13–0: Ch. A Power Ramp Memory
0x180–0x1FF	16	15–0: Ch. A Coefficient Memory This address is mirrored at 0x900–0x97F and contiguously extended at 0x980–0x9FF

PSK MODULATOR

The PSK Modulator is an AD6623 extension feature that is only available when the control register bit 0x000:7 is high. The PSK Modulator creates 32-bit complex inputs to the Interpolating FIR Filter from two or three data bits captured by the serial port. The FIR Filter operates exactly as if the 32-bit word came directly from the serial port. There are three PSK modulation options to choose from: π/4-DQPSK, 8-PSK, and 3π/8-8-PSK. Every symbol of any of these modulations can be represented by one of the 16 phases shown in Figure 21.

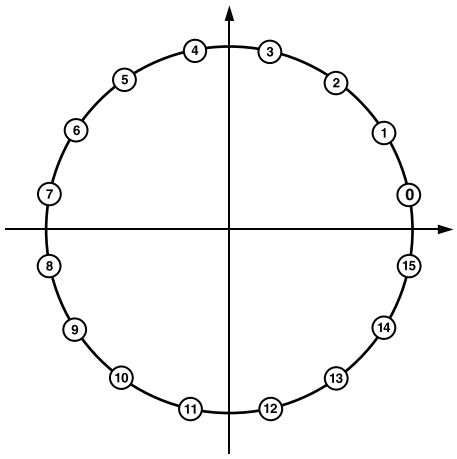


Figure 21. 16-Phase Modulations

All of these phase locations are represented in rectangular coordinates by only four unique magnitudes in the positive and negative directions. These four values are read from four channel registers that are programmed according to the following table, which gives the generic formulas and a specific example. The example is notable because it is only 0.046 dB below full-scale and the 16-bit quantization is so benign at that magnitude, that the rms error is better than –122 dBc. It is also worth noting that because none of the phases are aligned with the axes, magnitudes slightly beyond 0.16 dB above full-scale are achievable.

Table VI. Program Registers

Channel Register	Magnitude M	Magnitude E 0x7F53
0x12	M 3 cos(π/16)	0x7CE1
0x13	M 3 cos(3π/16)	0x69DE
0x14	M 3 cos(5π/16)	0x46BD
0x15	M 3 cos(7π/16)	0x18D7

Using the four channel registers from the preceding table, the PSK Modulator assembles the 16 phases according to Table VII.

Table VII. PSK Modulator Phase

Phase	I Value	Q Value
0	0x12	0x15
1	0x13	0x14
2	0x14	0x13
3	0x15	0x12
4	–0x15	+0x12
5	–0x14	+0x13
6	–0x13	+0x14
7	–0x12	+0x15
8	–0x12	–0x15
9	–0x13	–0x14
10	–0x14	–0x13
11	–0x15	–0x12
12	+0x15	–0x12
13	+0x14	–0x13
14	+0x13	–0x14
15	+0x12	–0x15

The following three sections show how the phase values are created for each PSK modulation mode.

π/4-DQPSK Modulation

IS-136 compliant π/4-DQPSK modulation is selected by setting the channel register 0xn0C: 6–4 to 001b. The phase word is calculated according to the following diagram. The two LSBs of the serial input word update the payload bits once per symbol. The QPSK Mapper creates a data dependent static phase word (Sph) which is added to a time dependent rotating phase word (Rph). The Rph starts at zero when the RCF is reset or switches modes via a sync pulse. Otherwise, the Rph increments by two on every symbol.

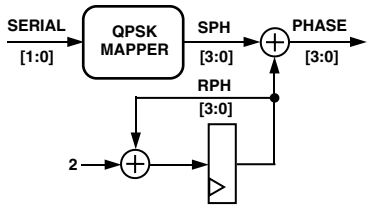


Figure 22. QPSK Mapper

The Sph word is calculated by the QPSK Mapper according to the following truth table.

Table VIII. QPSK Mapper Truth Table

Serial [1:0]	Sph [3:0]
00b	0
01b	4
11b	8
10b	12

8-PSK Modulation

IS-136+ compliant 8-PSK modulation is selected by setting the channel register 0xn0C: 6–4 to 101b. The Phase word is calculated according to the following diagram. The three LSBs of the serial input word update the payload bits once per symbol.

Figure 23. 8-PSK Mapper

The Phase word is calculated by the 8-PSK Mapper according to the following truth table:

Table IX. 8-PSK Mapper Truth Table

Serial [2:0]	Sph [3:0]
111b	0
011b	2
010b	4
000b	6
001b	8
101b	10
100b	12
110b	14

3π/8-8-PSK Modulation

EDGE compliant 3π/8-8-PSK modulation is selected by setting the channel register 0xn0C: 6–4 to 110b. The phase word is calculated according to the following diagram. The three LSBs of the serial input word update the payload bits once per symbol. The 8-PSK Mapper creates a data-dependent static phase word (Sph) which is added to a time-dependent rotating phase word (Rph). The 8-PSK Mapper operates exactly as described in the preceding 8-PSK Modulation section. The Rph starts at zero when the RCF is reset or switches modes via a sync pulse. Otherwise, the Rph increments by three on every symbol.

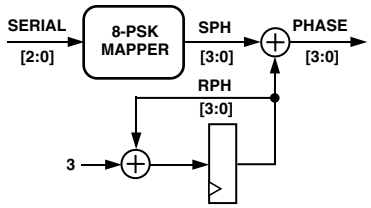


Figure 24. 3 π/8-8-PSK Mapper

MSK Look-Up Table
The MSK Look-Up Table mode for the RCF is selected in Control Register 0xn0C. In the MSK Mode, the RCF performs arbitrary pulse-shaping based on four symbols of impulse response. For the MSK Mode, the serial input format is 1 bit of data.

GMSK Look-Up Table
The GMSK Look-Up Table mode for the RCF is selected in Control Register 0xn0C. In the GMSK Mode, the RCF performs arbitrary pulse-shaping based on four symbols of impulse response. For the GMSK Mode, the serial input format is 1 Bit of data.

QPSK Look-Up Table
The QPSK Filter mode for the RCF is selected in Control Register 0xn0C. In the QPSK Mode, the RCF performs baseband linear pulse-shaping based on filter impulse response up to 12 symbols. For the QPSK Mode, the serial input format is 1 Bit I followed by 1 Bit Q.

PHASE EQUALIZER
The IS-95 Standard includes a phase equalizer after matched filtering at the baseband transmit side of a base station. This filter pre-distorts the transmitted signal at the base station in order to compensate for the distortion introduced to the received signal by the analog baseband filtering in a handset. The AD6623 includes this functionality in the form of an Infinite Impulse Response (IIR) all-pass filter in the RCF. This Phase Equalizer pre-distort filter has the following transfer function:

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1 + b1z + b2z^2}{z^2 + b1z + b2} \quad (9)$$

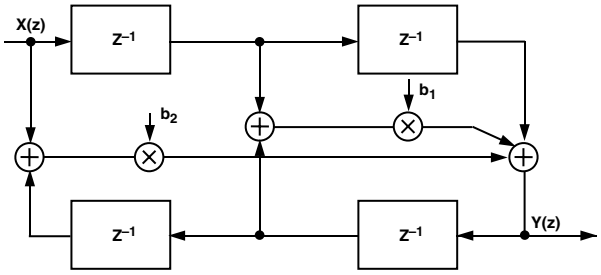


Figure 25. Second Order All-Pass IIR Filter

The Allpass Phase Equalizer (APE) is enabled (logic 1) or disabled (logic 0) in Control Register 0xn0D:5. The value of Bit 5 then becomes the value of the APE term in Equation 7. The coefficients b_1 and b_2 are located in Control Registers 0xn10 and 0xn11 respectively.

The format for b_1 and b_2 is two's complement fractional binary with a range of [–2, 2). With one bit for sign at most significant bit position there are 15 bits for magnitude. The value of one bit is $(2^{-15}) \times 2$, or 0.00006103515625. The register values, in hexadecimal, and the corresponding coefficient weight from positive full-scale through zero to negative full-scale is illustrated in Table X.

Table X. Coefficient Weights

Register Value	Coefficient Weight
0x7FFF	+1.999938964844
..	
0x0001	+0.00006103515625
0x0000	0
0xFFFF	–0.00006103515625
..	
0x8001	–1.999938964844
0x8000	–2

Table XI shows the recommended b_1 and b_2 coefficients for the respective oversampling rate.

Table XI. b_1 and b_2 Coefficients

Over-sampling	b_0	b_1	b_2
1	1	–0.25421 (0.efbbh)	+0.11188 (0.0729h)
2	1	–0.96075 (0.c283h)	+0.33447 (0.1568h)
3	1	–1.28210 (0.adf2h)	+0.48181 (0.1ed6h)
4	1	–1.45514 (0.a2dfh)	+0.57831 (0.2503h)
5	1	–1.56195 (0.9c09h)	+0.64526 (0.294ch)
6	1	–1.63409 (0.976bh)	+0.69415 (0.2c6dh)
7	1	–1.68604 (0.9418h)	+0.73132 (0.2eceh)
8	1	–1.72516 (0.9197h)	+0.76050 (0.30ach)

FINE SCALE AND POWER RAMP
Fine Scale multiplier factors in the range [0, 2) with a step resolution of 2^{-16}. Power Ramp multiplier factors in the range [0, 1) with a step resolution of 2^{-14}.

FINE SCALING
Fine Scale multiplier factors range from [0, 2) with a step resolution of 2^{-15} in the AD6622 emulation mode and 2^{-16} in the AD6623 emulation mode. Scaling values for each channel are programmed at register 0xn0E in the AD6623 internal memory using the Microport interface.

RCF POWER RAMPING
When the output of the AD6623 is programmed to be a rapid series of on/off bursts of data, the DAC used to produce an analog output signal will produce undesirable spectral components that should (or must) be suppressed. Shaping or "ramping" the transition from no power to full power, and vice versa, reduces the amplitude of these spurious signals. To program the ramp function a user must provide, through the Microport, the ramp memory (RMEM) coefficient values (up to 64), number of RMEM coefficients to "construct" the ramp (1 to 64) and selection of a synchronizing signal source as discussed below. The programmable power ramp up/down unit allows power ramping on time-slot basis as specified for some wireless transmission technologies (e.g. TDMA).

The shape of the ramp is stored in RAM. The RAM coefficients (RMEM) allow complete sample-by-sample control at the RCF interpolated rate. This is particularly useful for time division multiplexed standards such as GSM/EDGE. A time slot or "burst" is ramped-up and down by multiplying the Fine Scaled output of the RCF by a series of up to 64 ramp coefficients. If more ramp resolution is required, up to 64 interpolated coefficients can be added if the Ramp Interpolation bit, 0xn16:1, is set to

Logic 1. This extends the maximum ramp length to 128 coefficients. Although the ramp is limited in length, its time duration is a function of the output sample rate of the RCF multiplied by the ramp length. Ramp duration is twice as long with Ramp Interpolation enabled than when it is not enabled.

The channel's Ramp Enable bit at control register address 0xn16: bit 0, must be set to Logic 1 or else the ramp function will be bypassed and the RCF output data is passed unaltered to the CIC interpolation stages. When in use, the maximum signal gain is dependent on what value is stored in the last valid RMEM (ramp memory) location. RMEM words are 14-bits with a range of [0-1).

When the ramp is triggered, the following sequence occurs (see Figures 26 and 27): RAMP-DOWN beginning at the last coefficient of the specified ramp length and proceeding, sample-by-sample, to the first coefficient. Next, a REST or quiet period (from 0 to 32 RCF output samples duration) occurs. During this time, the Mode bit (as shown in Figure 17, AD6623 Data Format and Bit Definition chart) is updated, input sampling is halted and any control register with a superscript 2 is updated. Modulator configurations can be updated while the ramp is "quiet" allowing for GSM and EDGE timeslots to be multiplexed without resetting or reconfiguring the channel. Lastly, RAMP-UP occurs beginning at the first coefficient and ending at the last coefficient of the specified length. The final output level from the ramp stage is equal to the RCF Fine Scale output level multiplied by the last ramp coefficient.

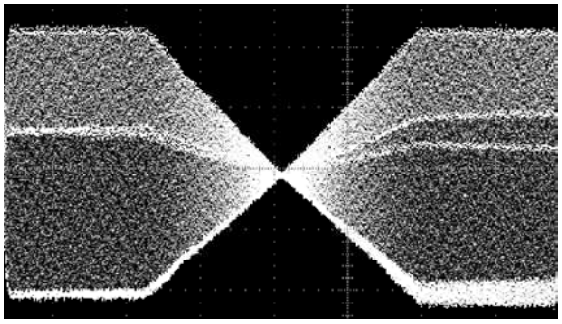


Figure 26. View of an unmodulated carrier with linear ramp-down and ramp-up and rest time between ramps set to 0.

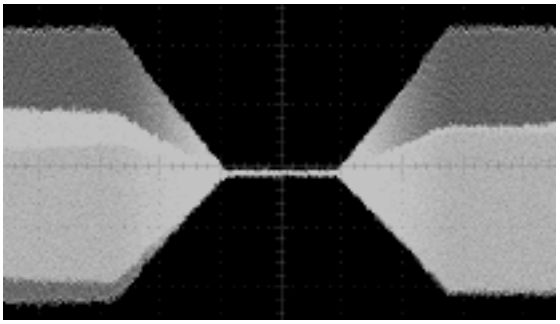


Figure 27. View of an unmodulated carrier with linear ramp-down and ramp-up and rest time between ramps set to 30 (RCF output sample time periods)

Ramp Triggering

The ramp sequence is triggered by the Fine Scale Hold-Off counter. The counter is loaded with a 16-bit user-specified value (>1 and $<2^{16}$) upon receipt of a sync pulse. The counter then counts-down (master CLK cycles) to 1, triggers the Ramp sequence and updates the Fine Scale factor. The counter will then stop at a count of zero. If the counter is initially loaded with 0, then the scale hold-off counter is bypassed and will not trigger any succeeding events. There are three ways to provide the sync pulse that loads the hold-off counter that ultimately triggers the ramp:

1. Serial Input sync. This method is selected when "Serial Time Slot Sync Enable", 0xn16:2, is set to Logic 1 and appropriate serial word input bits are set as described in Figure 17 (AD6623 Data Format and Bit Definition chart). This allows a channel's Fine Scale Hold-Off Counter to be loaded and a power ramp sequence to be triggered by a data word without resorting to hardware or software generated sync pulses. This sync signal is routed to the OR gate following the Time Slot Sync multiplexer shown in the Sync Control block diagram, Figure 37.
2. Hardware Sync. Sync Pins 0, 1, 2, and 3 provide a means to load the fine scale hold-off counter using the channel's "Time Slot Sync" multiplexer. The multiplexer allows selection of the desired hard or "pin"-sync signal using two software controlled select lines at register addresses 0xn0F:17 and 0xn0F:16. Pin-Sync is the most precise method of synchronization. This block shares 2 signals with the Beam Sync block. They are Software Beam Sync and Sync0. This means that whenever a Sync0 or soft beam sync is sent to the Beam Sync block, the same signals are also sent to the Time Slot Sync block.
3. Software Sync. This function allows the user to load Start, Hop, Beam and Fine Scale holdoff counters via software commands through the AD6623 Microport. Sync signals generated in this manner are the least precise means of synchronization. All software sync bits are located at address 5 of the external register (see Table XXI External Registers). The Time Slot soft-sync is derived from the shared Beam Sync soft sync. Setting D6, "Beam", high will generate a soft sync signal that loads the Fine Scale hold-off counter as well as the Beam Sync phase hold-off counter. User must select which channel(s) will receive the soft sync signal(s) using bits D0 through D3 at external address 5 and select what type of sync signal(s) is to be generated (using bits D4, 5 and 6 at address 5). As an example, to generate a Time Slot soft sync for channel C, a user would set bits D2 and D6 high. D6 is the actual sync signal and D2 routes the sync signal only to channel C.

Special Handling Required for SYNC0 Pin-Sync

Proper routing of Sync0 (a hardware sync pulse) for Time Slot Sync may require bits in several registers to be set depending upon the number of active channels. These control bits are located in the Internal "Common Function" Registers (address 0x001) and the Internal "Channel Function" Registers (address 0xn00, 0xn03, 0xn05, 0xn0F). Address 0x001 contains 8 bits that will mask the distribution of pin-sync pulses from Sync0 to all channels and enable which sync multiplexers (start, hop, and beam) receive Sync0 pulses. Furthermore, the MSB at 0x001 is a "First Sync Only" flag that, when high, allows only one Sync0 pulse to be routed to the selected sync block(s). Following this, all 8-bits of register 0x001 are cleared to completely mask off subsequent pulses.

Sync pulses from Sync1, 2, and 3 pins are not masked in any fashion and directly connect to all Sync multiplexers of all channels. The Sync Control Block Diagram, Figure 37, in the Synchronization section of this data sheet provides an overview of all sync signal routing for one channel.

CASCADED INTEGRATOR COMB (CIC) INTERPOLATING FILTERS

The I and Q outputs of the RCF stage are interpolated by two cascaded integrator comb (CIC) filters. The CIC section is separated into three discrete blocks: a fifth order filter (CIC5), a second order resampling filter (rCIC2), and a scaling block (CIC Scaling). The CIC5 and rCIC2 blocks each exhibit a gain that changes with respect to their rate change factors, L_{rCIC2}, M_{rCIC2}, and L_{CIC5}. The product of these gains must be compensated for in a shared CIC Scaling block and can be done to within 6 dB. The remaining compensation can come from the RCF (in the form of coefficient scaling) or the fine scaling unit.

CIC Scaling

The scale factor S_{CIC} is a programmable unsigned integer between 4 and 32. This is a combined scaler for the CIC5 and rCIC2 stages. The overall gain of the CIC section is given by the equation below

$$CIC\_Gain = L_{CIC5}{}^{4} \times L_{rCIC2} \times 2^{-S_{CIC}} \quad (10)$$

CIC5

The first CIC filter stage, the CIC5, is a fifth order interpolating cascaded integrator comb whose impulse response is completely defined by its interpolation factor, L_{CIC5}. The value L_{CIC5}–1 can be independently programmed for each channel at location 0xn09.

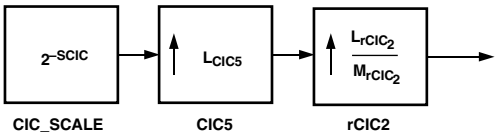


Figure 28. CIC5

While this control register is 8 bits wide, L_{CIC5} should be confined to the range from 1 to 32 to avoid the possibility of internal overflow for full scale inputs. The output rate of this stage is given by the equation below.

$$f_{CIC2} = f_{CIC5} \times L_{CIC5} \quad (11)$$

The transfer function of the CIC5 is given by the following equations with respect to the CIC5 output sample rate, f_{SAMP5}.

$$CIC5(z) = \left(\frac{1 - z^{-L_{CIC5}}}{1 - z^{-1}} \right)^5 \quad (12)$$

The SCIC value can be independently programmed for each channel at Control Register 0xn06. S_{CIC} may be safely calculated according to equation (13) below to ensure the net gain through the CIC stages.

SCIC serves to frame which bits of the CIC output are transferred to the NCO stage. This results in controlling the data out of the CIC stages in 6 dB increments. For the best dynamic range, S_{CIC} should be set to the smallest value possible (lowest attenuation) without creating an overflow condition. This can be safely accomplished using the equation below. To ensure the CIC output data is in range, Equation 13 must always be met. The maximum total interpolation rate may be limited by the amount of scaling available.

$$S_{CIC} \geq ceil\left(4 \times \log_2\left(L_{CIC5}\right) + \log_2\left(L_{CIC2}\right)\right) \quad (13)$$

$$0 \leq S_{CIC} \leq 58 \quad (14)$$

This polynomial fraction can be completely reduced as follows demonstrating a finite impulse response with perfect phase linearity for all values of L_{CIC5}.

$$CIC5(z) = \left(\sum_{k=0}^{L_{CIC5}-1} z^{-k} \right)^5 = \sum_{k=1}^{L_{CIC5}-1} \left(z^{-1} - e^{j2\pi \frac{k}{L_{CIC5}}} \right)^5 \quad (15)$$

The frequency response of the CIC5 can be expressed as follows. The initial $1/L_{CIC5}$ factor normalizes for the increased rate, which is appropriate when the samples are destined for a DAC with a zero order hold output. The maximum gain is $L_{CIC5}{}^{4}$ at baseband, but internal registers peak in response to various dynamic inputs. As long as L_{CIC5} is confined to 32 or less, there is no possibility of overflow at any register.

$$CIC5(f) = \frac{1}{L_{CIC5}} \left(\frac{sin\left(\pi \frac{L_{CIC5} \times f}{f_{CIC5}} \right)}{sin\left(\pi \frac{f}{f_{CIC5}} \right)} \right)^5 \quad (16)$$

The pass band droop of CIC5 should be calculated using this equation and can be compensated for in the RCF stage. The gain should be calculated from the CIC scaling section above.

As an example, consider an input from the RCF whose bandwidth is 0.141 of the RCF output rate, centered at baseband. Interpolation by a factor of five reveals five images, as shown below.

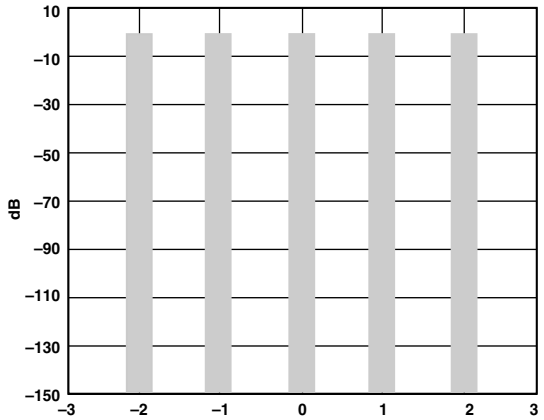


Figure 29. Unfiltered CIC5 Images

The CIC5 rejects each of the undesired images while passing the image at baseband. The images of a pure tone at channel center (DC) are nulled perfectly, but as the bandwidth increases the rejection is diminished. The lower band edge of the first image always has the least rejection. In this example, the CIC5 is interpolating by a factor of five and the input signal has a bandwidth of 0.141 of the RCF output sample rate. The plot below shows –110 dBc rejection of the lower band edge of the first image. All other image frequencies have better rejection.