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Multichannel Digital Upconverter with VersaCREST™ Crest Reduction Engine

AD6633

FEATURES

- 4 or 6 wideband digital upconverter channels
- VersaCREST crest reduction engine reduces demands on external power amplifiers
- One 20-bit complex input port (I, Q interleaved), shared among 4 or 6 processing channels
- Two 18-bit output ports for parallel I and Q or a single 18-bit output port for interleaved I and Q
- All-pass phase equalizer filters (meets IS-95 requirements)
- Programmable RAM coefficient FIR filters (RCF) with resampling
- FIR interpolating filters, 2 per channel
- Fifth-order interpolating CIC filter, 1 per channel
- Full complex NCO, 32-bit tuning resolution (fine), worst spur better than −105 dBc, 1 per channel
- Complex FIR filter for frequency equalization or additional filtering
- Output automatic gain control
- Full complex composite NCO, 6-bit tuning resolution
- 16-bit/8-bit MicroPort (Intel® or Motorola® mode)
- Serial control port (SPI®- or SPORT-compatible)
- 3.3 V I/O and 1.8 V core supplies
- JTAG boundary scan
- User-configurable, built-in, self-test (BIST) capability

APPLICATIONS

- Cellular/PCS basestations
- Micro/pico cell basestations
- Multicarrier cdma2000®, WCDMA, TD-SCDMA basestations
- Broadband wireless access head ends (LMDS, MMDS)
- Software defined radios
- High speed signal processing applications

GENERAL DESCRIPTION

The AD6633 is a multichannel, wide bandwidth digital upconverter (DUC) with crest factor reduction (CFR) technology, which is available in 4-channel or 6-channel versions. It processes 20-bit baseband input data and generates 18-bit, wideband, real, or complex output data at up to 125 MSPS. This rate is suitable for driving digital-to-analog converters (DACs) at the first intermediate frequency (IF) directly.

The AD6633 synthesizes multicarrier and multistandard digital signals to drive the DAC(s) with up to six wideband modulated carriers from a single output port. Each channel includes an internal peak-to-average power reduction block that reduces power amplifier (PA) power dissipation. The user-configurable interpolating filter (RCF) provides multirate processing (including resampling) and malleable FIR filter characteristics. An all-pass phase equalizer designed to comply with the cdma2000 standard follows the RCF. Each channel has its own 32-bit numerically-controlled oscillator (NCO) to up-convert the filtered/interpolated data to the first IF. Interpolation, anti-image filtering, all-pass equalization, and NCO tuning functions are combined in a single, cost-effective device.

Digital IF signal processing provides repeatable manufacturing, higher accuracy, and more flexibility than comparable high dynamic range analog designs. The AD6633 uses a 3.3 V I/O power supply and a 1.8 V core power supply. Typical power consumption is 75 mW per channel or 1.4 W for the complete device. All I/O pins are 5 V tolerant. All control registers and coefficient values are programmed through a generic 16-bit microprocessor interface or a SPI/SPORT-compatible serial port. Intel and Motorola microprocessor bus modes are supported. All inputs and outputs are LVCMOS-compatible.

For more information about the AD6633, contact Analog Devices via email at versaCOMM@analog.com.

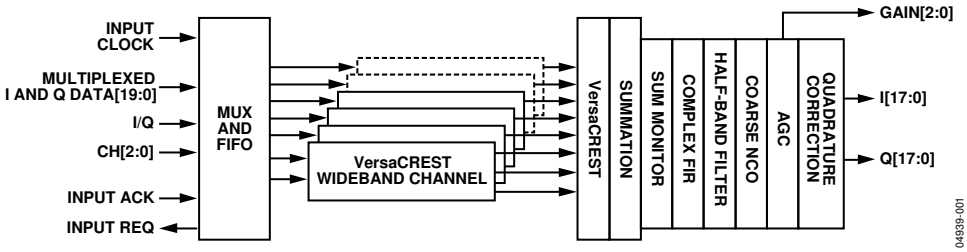

Figure 1. Functional Block Diagram

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Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

AD6633* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-0974: Multicarrier TD-SCMA Feasibility
- AN-835: Understanding High Speed ADC Testing and Evaluation

Data Sheet

- AD6633: Multichannel Digital UpConverter with VersaCREST™ Crest Reduction Engine Data Sheet

TOOLS AND SIMULATIONS

- AD6633 IBIS Model

REFERENCE MATERIALS

Technical Articles

- Design A Clock-Distribution Strategy With Confidence

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- AD6633 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD6633 EngineerZone Discussions.

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Visit the product page to see pricing options.

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PRODUCT OVERVIEW

The AD6633 is a multichannel, wide bandwidth DUC with a VersaCREST crest reduction engine. It processes digital baseband input data and generates wideband, real, or complex IF output data. It drives DACs up to any IF sampled at up to 125 MSPS. Up to six wideband modulated carriers per package can be achieved from a single output port. Devices may be connected together for additional channels by using multiple packages. Interpolation, anti-image filtering, all-pass equalization, and NCO tuning functions are combined in a single, cost-effective device that includes the VersaCREST crest factor reduction engine.

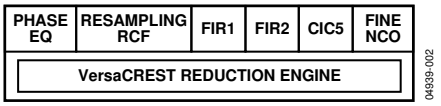

Figure 2. Wideband Channel

Each VersaCREST wideband channel contains a peak-to-average compensation block that reduces PA requirements. By minimizing infrequent peaks in code-division, multiple-access (CDMA) signals, a PA with one-half to one-quarter the previously necessary power capacity can be used. This is done within standard signal quality requirements and significantly lowers system cost.

The input data is time-multiplexed among the active channels for processing through a 20-bit input port. Each channel has a number of elements available to interpolate, resample, and filter the data while tuning to an IF for further upconversion within a radio frequency (RF) system.

An all-pass phase equalizer, designed to comply with IS-95, including cdma2000 standards, is the first available block. A user-configurable, interpolating RAM coefficient filter (RCF) is the first general-purpose filter stage in the channel. It provides multirate processing, including resampling and malleable finite impulse response (FIR) filter characteristics. Further filtering can be accomplished with two additional, fixed-coefficient, FIR, half-band stages. A fifth-order, cascade integrator comb (CIC5) is the final filter stage available.

Each channel has its own 32-bit NCO to upconvert the filtered/interpolated data to a first IF.

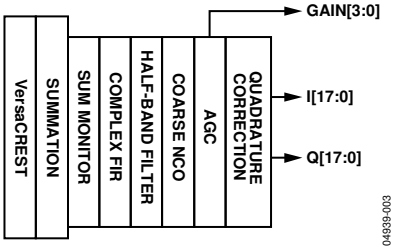

Figure 3. Summation and Post-Sum Blocks

Post-processing after channel summation includes power monitoring, filtering, composite NCO, digital automatic gain control (AGC) output, and quadrature correction stages. The output may be real or complex, and complex output may be parallel on two 18-bit ports or interleaved on one 18-bit port.

Control registers and coefficient values are programmed through a generic 16-bit microprocessor interface or a SPI-/SPORT-compatible serial port. Intel and Motorola microprocessor bus modes are supported.

The AD6633 uses a 3.3 V I/O power supply and a 1.8 V core power supply. Typical power consumption is 75 mW per channel or 1.4 W for the complete device. All inputs and outputs are LVCMOS-compatible and are 5 V tolerant.

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