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80 MSPS, Dual-Channel WCDMA Receive Signal Processor (RSP)

AD6634

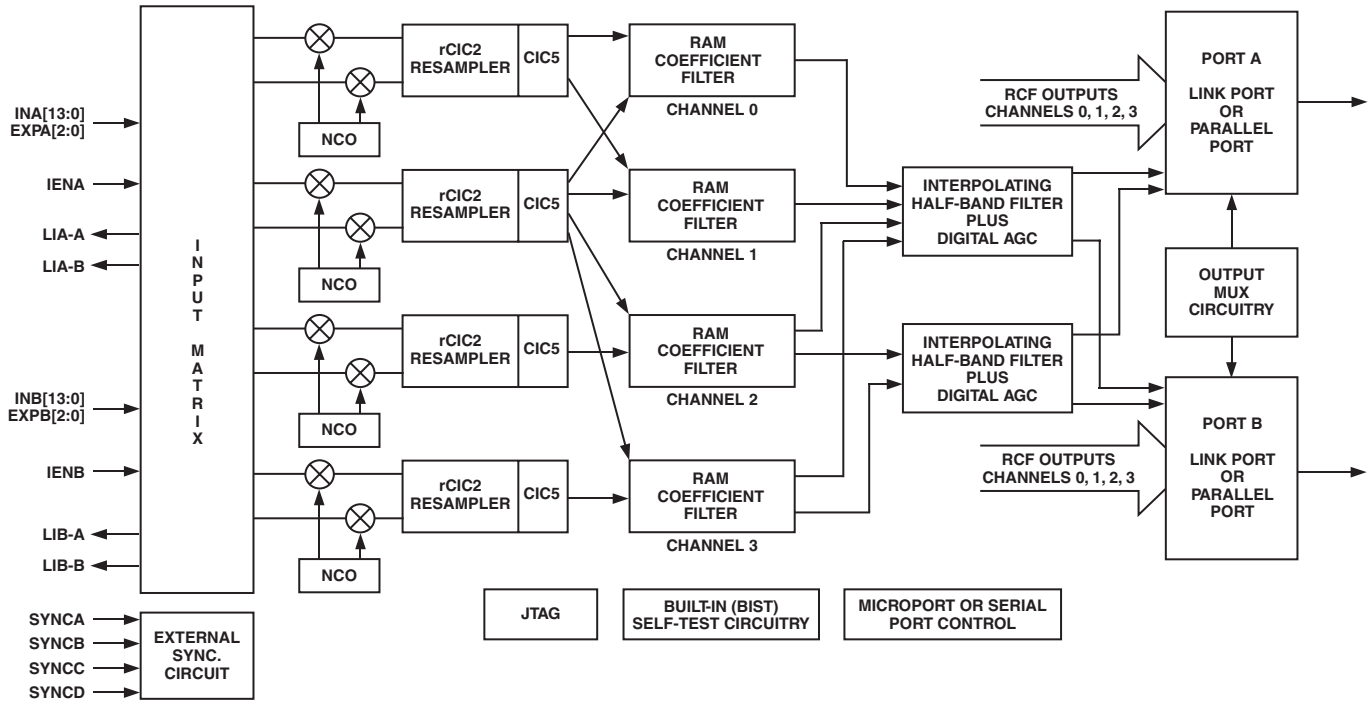
FEATURES

80 MSPS Wideband Inputs (14 Linear Bits Plus Three RSSI)
Processes Two WCDMA Channels (UMTS or CDMA2000 1×) or Four GSM/EDGE, IS136 Channels
Four Independent Digital Receivers in a Single Package
Dual 16-Bit Parallel Output Ports
Dual 8-Bit Link Ports
Programmable Digital AGC Loops with 96 dB Range
Digital Resampling for Noninteger Decimation Rates
Programmable Decimating FIR Filters
Interpolating Half-Band Filters
Programmable Attenuator Control for Clip Prevention and External Gain Ranging via Level Indicator
Flexible Control for Multicarrier and Phased Array
3.3 V I/O, 2.5 V CMOS Core
User Configurable Built-In Self-Test (BIST) Capability
JTAG Boundary Scan

APPLICATIONS

Multicarrier, Multimode Digital Receivers
GSM, IS136, EDGE, PHS, IS95, UMTS, CDMA2000
Micro and Pico Cell Systems, Software Radios
Wireless Local Loop
Smart Antenna Systems
In Building Wireless Telephony

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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Tel: 781/329-4700
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Last Content Update: 02/23/2017

COMPARABLE PARTS

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DOCUMENTATION

Application Notes

- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design

Data Sheet

- AD6634: Dual-Channel, 80MSPS WCDMA Receive Signal Processor (RSP) Data Sheet

Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

TOOLS AND SIMULATIONS

- AD6634 BSDL File
- AD6634 IBIS Models

REFERENCE MATERIALS

Technical Articles

- Basics of Designing a Digital Radio Receiver (Radio 101)
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Smart Partitioning Eyes 3G Basestation

DESIGN RESOURCES

- AD6634 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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GENERAL DESCRIPTION

The AD6634 is a multimode 4-channel digital receive signal processor (RSP) capable of processing up to two WCDMA channels. Each channel consists of four cascaded signal processing elements: a frequency translator, two fixed coefficient decimating filters, and a programmable coefficient decimating filter. Each input port has input level threshold detection circuitry and an AGC controller for accommodating large dynamic ranges or situations where gain ranging converters are used. Dual 16-bit parallel output ports accommodate high data rate WBCDMA applications. On-chip interpolating half-band can also be used to further increase the output rate. In addition, each parallel output port has a digital AGC for output data scaling. Link port outputs are provided to enable glueless interfaces to ADI's TigerSHARC® DSP core.

The AD6634 is part of Analog Devices' SoftCell® Multicarrier transceiver chipset designed for compatibility with Analog Devices' family of high sample rate IF sampling ADCs (AD9238/AD6645 12- and 14-bit). The SoftCell receiver comprises a digital receiver capable of digitizing an entire spectrum of carriers and digitally selecting the carrier of interest for tuning and channel selection. This architecture eliminates redundant radios in wireless base station applications.

High dynamic range decimation filters offer a wide range of decimation rates. The RAM-based architecture allows easy reconfiguration for multimode applications.

The decimating filters remove unwanted signals and noise from the channel of interest. When the channel of interest occupies less bandwidth than the input signal, this rejection of out-of-band noise is called *processing gain*. By using large decimation factors, this processing gain can improve the SNR of the ADC by 30 dB or more. In addition, the programmable RAM coefficient filter allows antialiasing, matched filtering, and static equalization functions to be combined in a single, cost-effective filter. Half-band interpolating filters at the output are used in WCDMA applications to increase the output rate from 2× to 4× of the chip rate. The AD6634 is also equipped with two independent automatic gain control (AGC) loops for direct interface to a RAKE receiver.

The AD6634 is compatible with standard ADC converters such as the AD664x, AD923x, AD943x, and the AD922x families of data converters. The AD6634 is also compatible with the AD6600 diversity ADC, providing a cost and size reduction path.

ARCHITECTURE

The AD6634 has four signal processing stages: a frequency translator, second order resampling cascaded integrator comb FIR filters (rCIC2), a fifth order cascaded integrator comb FIR filter (CIC5), and a RAM coefficient FIR filter (RCF). Multiple modes are supported for clocking data into and out of the chip and provide flexibility for interfacing to a wide variety of digitizers. Programming and control are accomplished via serial and/or microprocessor interfaces.

Frequency translation is accomplished with a 32-bit, complex, numerically controlled oscillator (NCO). Real data entering this stage is separated into inphase (I) and quadrature (Q) components. This stage translates the input signal from a digital intermediate frequency (IF) to digital baseband. Phase and amplitude dither may be enabled on-chip to improve spurious performance of the NCO. A phase-offset word is available to create a known phase relationship among multiple AD6634s or between channels.

Following frequency translation is a resampling, fixed coefficient, high speed, second order, resampling cascade integrator comb (rCIC2) filter that reduces the sample rate based on the ratio between the decimation and interpolation registers.

The next stage is a fifth order cascaded integrator comb (CIC5) filter whose response is defined by the decimation rate. The purpose of this filter is to reduce the data rate to the final filter stage so that it can calculate more taps per output.

The final stage is a sum-of-products FIR filter with programmable 20-bit coefficients, and decimation rates programmable from 1 to 256 (1–32 in practice). The RAM coefficient FIR filter (RCF in the Functional Block Diagram) can handle a maximum of 160 taps.

The next stage is a fixed coefficient half-band interpolation filter where data from different channels is combined together and interpolated by a factor of 2. Next, an AGC section with a gain range of 96.3 dB is available. This AGC section is completely programmable in terms of its response. Two each of half-band filters and AGCs are present in the AD6634, as shown in the Functional Block Diagram. These half-band filters and AGC sections can be bypassed independent of each other.

The overall filter response for the AD6634 is the composite of all decimating and interpolating stages. Each successive filter stage is capable of narrower transition bandwidths but requires a greater number of CLK cycles to calculate the output. More decimation in the first filter stage will minimize overall power consumption. Data from the chip is interfaced to the DSP via either a high speed parallel port or a TigerSHARC compatible link port.

Figure 1a illustrates the basic function of the AD6634: to select and filter a single channel from a wide input spectrum. The frequency translator tunes the desired carrier to baseband. Figure 1b shows the combined filter response of the rCIC2, CIC5, and RCF.

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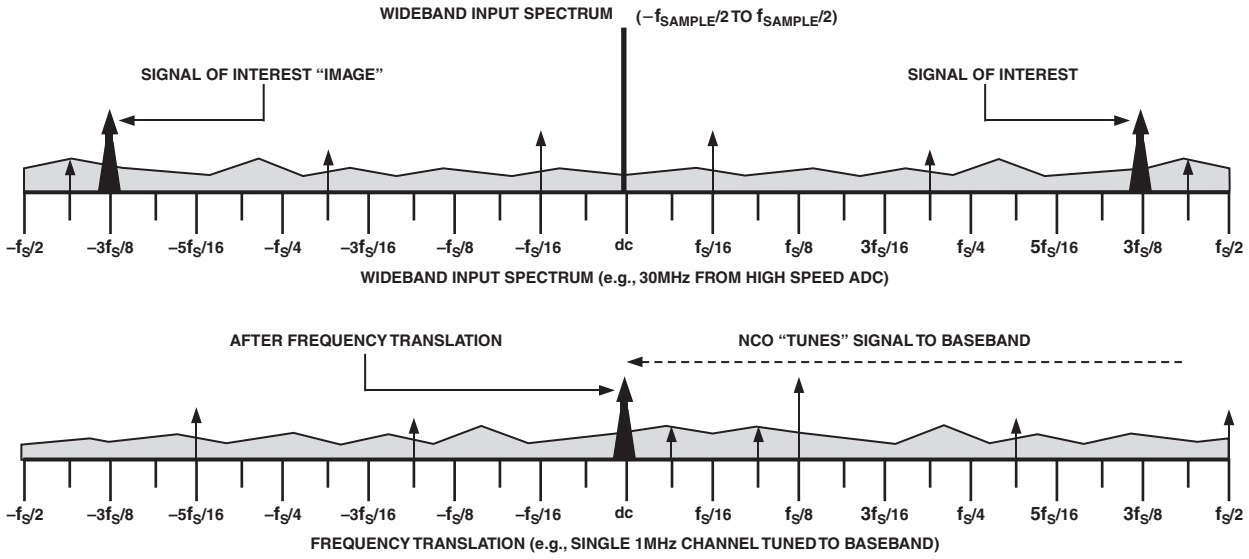


Figure 1a. Frequency Translation of Wideband Input Spectrum

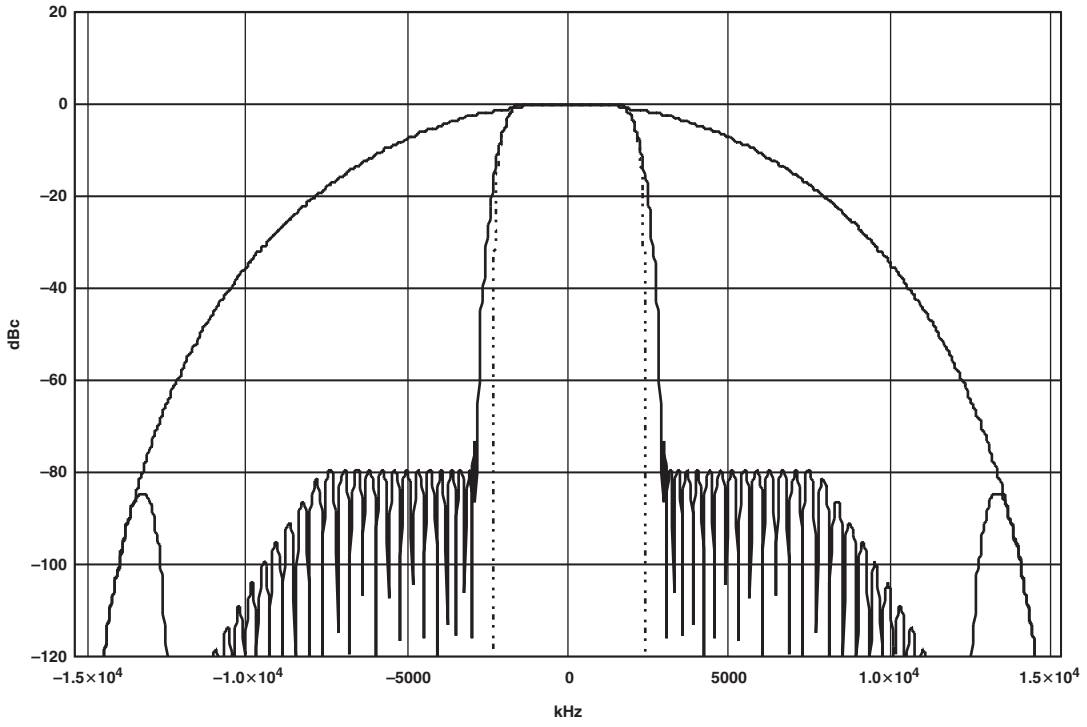


Figure 1b. Composite Filter Response of rCIC2, CIC5, and RCF

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 3.6 V
Input Voltage . . . . . –0.3 V to +5.3 V (5 V Tolerant)
Output Voltage Swing . . . . . –0.3 V to VDDIO +0.3 V
Load Capacitance . . . . . 200 pF
Junction Temperature Under Bias . . . . . 125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) . . . . . 280°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the devices at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

196-Lead BGA:
θ_{JA} = 41°C/W, No Airflow
θ_{JA} = 39°C/W, 200-lfpm Airflow
θ_{JA} = 37°C/W, 400-lfpm Airflow
Thermal measurements made in the horizontal position on a 4-layer board.

EXPLANATION OF TEST LEVELS

I. 100% Production Tested.
II. 100% Production Tested at 25°C, and Sampled Tested at Specified Temperatures.
III. Sample Tested Only
IV. Parameter Guaranteed by Design and Analysis
V. Parameter is Typical Value Only
VI. 100% Production Tested at 25°C, and Sampled Tested at Temperature Extremes

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6634BBC	–40°C to +85°C (Ambient)	196-Lead CSPBGA (Ball Grid Array)	BC-196
AD6634BC/PCB		Evaluation Board with AD6634 and Software	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6634 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Temp	Test Level	AD6634BBC Min	Typ	Max	Unit
VDD		IV	2.25	2.5	2.75	V
VDDIO		IV	3.0	3.3	3.6	V
$T_{AMBIENT}$		IV	–40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter (Conditions)	Temp	Test Level	AD6634BBC Min	Typ	Max	Unit
LOGIC INPUTS (5 V Tolerant)						
Logic Compatibility	Full	IV		3.3 CMOS		V
Logic "1" Voltage	Full	IV	2.0		5.0	V
Logic "0" Voltage	Full	IV	–0.3		+0.8	V
Logic "1" Current	Full	IV		1	10	µA
Logic "0" Current	Full	IV		1	10	µA
Logic "1" Current (Inputs with Pull-Down)	Full	IV				
Logic "0" Current (Inputs with Pull-Up)	Full	IV				
Input Capacitance	25°C	V		4		pF
LOGIC OUTPUTS						
Logic Compatibility	Full	IV		3.3 CMOS/TTL		V
Logic "1" Voltage (I_{OH} = 0.25 mA)	Full	IV	2.4	VDD–0.2		V
Logic "0" Voltage (I_{OL} = 0.25 mA)	Full	IV		0.2	0.4	V
IDD SUPPLY CURRENT						
CLK = 80 MHz, (VDD = 2.75 V, VDDIO = 3.6 V)	Full	IV				
I_{VDD}			397		443	mA
I_{VDDIO}			50		58	mA
CLK = GSM Example (65 MSPS, VDD = 2.5 V, VDDIO = 3.3 V, Dec = 2/10/6 120 Taps Four Channels)	25°C	V				
I_{VDD}				TBD		mA
I_{VDDIO}				TBD		mA
CLK = WBCDMA Example (76.8 MSPS, VDD = 2.5 V, VDDIO = 3.3 V, Dec = 2/10/6 120 Taps Four Channels)	25°C	V				
I_{VDD}				TBD		mA
I_{VDDIO}				TBD		mA
POWER DISSIPATION						
CLK = 80 MHz	Full	IV	1.05		1.45	W
CLK = 65 MHz GSM/EDGE Example		V		840		mW
CLK = 76.8 MHz WBCDMA Example		V		1.2		W
Sleep Mode	Full	IV		287		µW

Specifications subject to change without notice.

GENERAL TIMING CHARACTERISTICS[1, 2]

Parameter (Conditions)		Temp	Test Level	AD6634BBC Min	Typ	Max	Unit
CLK TIMING REQUIREMENTS							
t_{CLK}	CLK Period	Full	I	12.5			ns
t_{CLKL}	CLK Width Low	Full	IV	5.6	$0.5 \times t_{CLK}$		ns
t_{CLKH}	CLK Width High	Full	IV	5.6	$0.5 \times t_{CLK}$		ns
$\overline{\text{RESET}}$ TIMING REQUIREMENTS							
t_{RESL}	$\overline{\text{RESET}}$ Width Low	Full	I	30.0			ns
INPUT WIDEBAND DATA TIMING REQUIREMENTS							
t_{SI}	Input to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HI}	Input to ↑CLK Hold Time	Full	IV	1.0			ns
LEVEL INDICATOR OUTPUT SWITCHING CHARACTERISTICS							
t_{DLI}	↑CLK to LI (A–A, B; B–A, B) Output Delay Time	Full	IV	3.3		10.0	ns
SYNC TIMING REQUIREMENTS							
t_{SS}	SYNC (A, B, C, D) to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HS}	SYNC (A, B, C, D) to ↑CLK Hold Time	Full	IV	1.0			ns
SERIAL PORT CONTROL TIMING REQUIREMENTS SWITCHING CHARACTERISTICS[2]							
t_{SCLK}	SCLK Period	Full	IV	16			ns
t_{SCLKL}	SCLK Low Time	Full	IV	3.0			ns
t_{SCLKH}	SCLK High Time	Full	IV	3.0			ns
INPUT CHARACTERISTICS							
t_{SSI}	SDI to ↓SCLK Setup Time	Full	IV	1.0			ns
t_{HSI}	SDI to ↓SCLK Hold Time	Full	IV	1.0			ns
PARALLEL PORT TIMING REQUIREMENTS (MASTER MODE) SWITCHING CHARACTERISTICS[3]							
$t_{DPOCLKL}$	↓CLK to ↑PCLK Delay (Divide by 1)	Full	IV	6.5		10.5	ns
$t_{DPOCLKLL}$	↓CLK to ↑PCLK Delay (Divide by 2, 4, or 8)	Full	IV	8.3		14.6	ns
t_{DPREQ}	↑CLK to ↑PxREQ Delay					1.0	ns
t_{DPP}	↑CLK to Px[15:0] Delay					0.0	ns
INPUT CHARACTERISTICS							
t_{SPA}	PxACK to ↓PCLK Setup Time			+7.0			ns
t_{HPA}	PxACK to ↓PCLK Hold Time			–3.0			ns
PARALLEL PORT TIMING REQUIREMENTS (SLAVE MODE) SWITCHING CHARACTERISTICS[3]							
t_{POCLK}	PCLK Period	Full	I	12.5			ns
t_{POCLKL}	PCLK Low Period (when PCLK Divisor = 1)	Full	IV	2.0	$0.5 \times t_{POCLK}$		ns
t_{POCLKH}	PCLK High Period (when PCLK Divisor = 1)	Full	IV	2.0	$0.5 \times t_{POCLK}$		ns
t_{DPREQ}	↑CLK to ↑PxREQ Delay					10.0	ns
t_{DPP}	↑CLK to Px[15:0] Delay					11.0	ns
INPUT CHARACTERISTICS							
t_{SPA}	PxACK to ↓PCLK Setup Time			1.0			ns
t_{HPA}	PxACK to ↓PCLK Hold Time			1.0			ns
LINK PORT TIMING REQUIREMENTS SWITCHING CHARACTERISTICS[3]							
t_{RDLCLK}	↑PCLK to ↑LxCLKOUT Delay	Full	IV			2.5	ns
t_{FDLCLK}	↓PCLK to ↓LxCLKOUT Delay	Full	IV			0	ns
$t_{RLCLKDAT}$	↑LCLKOUT to Lx[7:0] Delay	Full	IV	0		2.9	ns
$t_{FLCLKDAT}$	↓LCLKOUT to Lx[7:0] Delay	Full	IV	0		2.2	ns

NOTES
[1]All Timing Specifications valid over VDD range of 2.25 V to 2.75 V and VDDIO range of 3.0 V to 3.6 V.
[2]C_{LOAD} = 40 pF on all outputs unless otherwise specified
[3]The timing parameters for Px[15:0], PxREQ, PxACK, LxCLKOUT, Lx[7:0] apply for port A and B (x stands for A or B).

Specifications subject to change without notice.

MICROPROCESSOR PORT TIMING CHARACTERISTICS[1, 2]

Parameter (Conditions)		Temp	Test Level	AD6634BBC Min	Typ	Max	Unit
MICROPROCESSOR PORT, MODE INM (MODE = 0)							
MODE INM WRITE TIMING							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.5			ns
t_{HWR}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) Hold Time	Full	IV	7.0			ns
t_{SAM}	Address/Data to $\overline{WR}$(RW) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RDY($\overline{DTACK}$) Hold Time	Full	IV	5.0			ns
t_{DRDY}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) High Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE INM READ TIMING							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	5.0			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{SAM}	Address to $\overline{RD}$($\overline{DS}$) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	5.0			ns
t_{DRDY}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) High Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns
MICROPROCESSOR PORT, MODE MNM (MODE = 1)							
MODE MNM WRITE TIMING							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.5			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{HRW}	RW($\overline{WR}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	7.0			ns
t_{SAM}	Address/Data to RW($\overline{WR}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RW($\overline{WR}$) Hold Time	Full	IV	5.0			ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay	Full	IV	8.0			ns
t_{ACC}	RW($\overline{WR}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE MNM READ TIMING							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	5.0			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address to $\overline{DS}$($\overline{RD}$) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	5.0			ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns

NOTES
[1]All Timing Specifications valid over VDD range of 2.25 V to 2.75 V and VDDIO range of 3.0 V to 3.6 V.
[2]C_{LOAD} = 40 pF on all outputs, unless otherwise specified.
[3]Specification pertains to control signals: R/W, ($\overline{WR}$), $\overline{DS}$ ($\overline{RD}$), $\overline{CS}$.

Specifications subject to change without notice.

TIMING DIAGRAMS

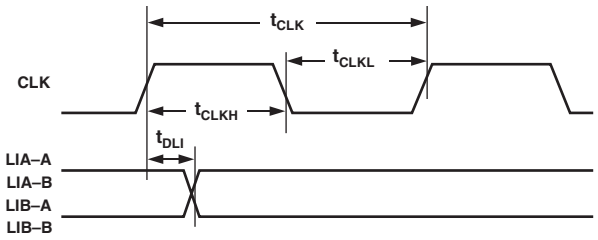


Figure 2. Level Indicator Output Switching Characteristics

Figure 3. $\overline{RESET}$ Timing Requirements

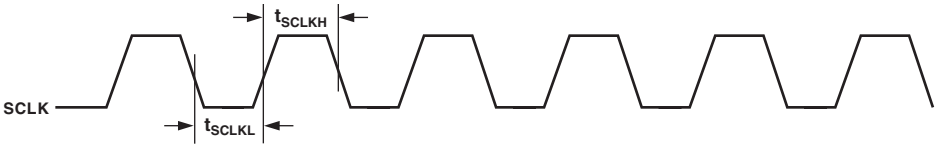


Figure 4. SCLK Switching Characteristics

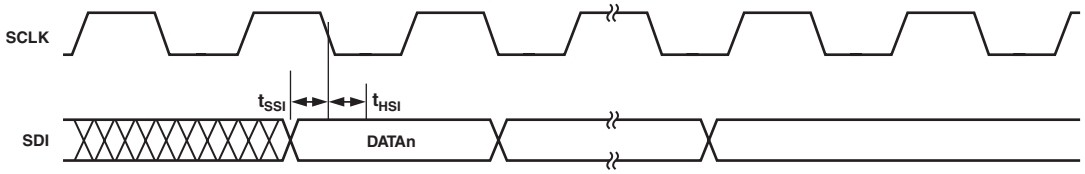


Figure 5. Serial Port Input Timing Characteristics

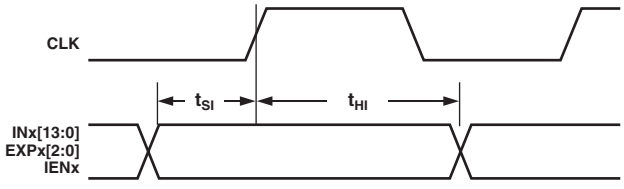


Figure 6. Input Timing for A and B Channels

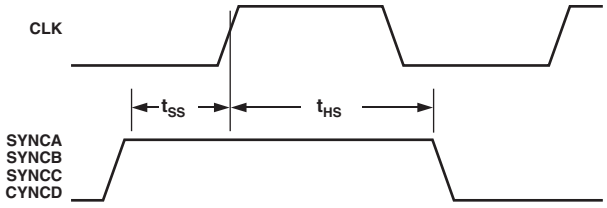


Figure 7. SYNC Timing Inputs

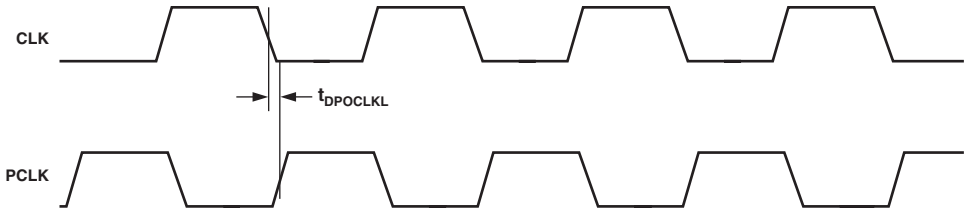


Figure 8. PCLK to CLK Switching Characteristics Divide by 1

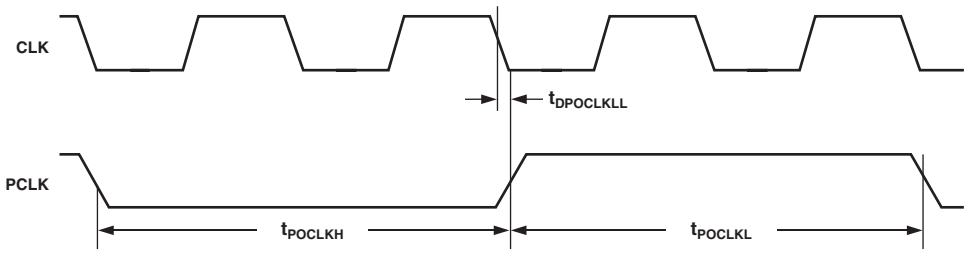


Figure 9. PCLK to CLK Switching Characteristics Divide by 2, 4, or 8

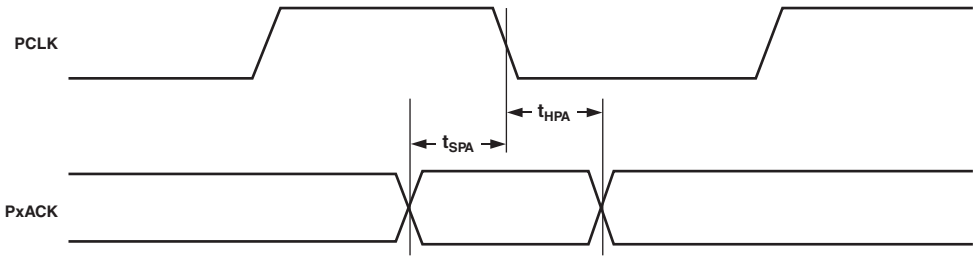


Figure 10. Master Mode PxACK to PCLK Setup and Hold Characteristics

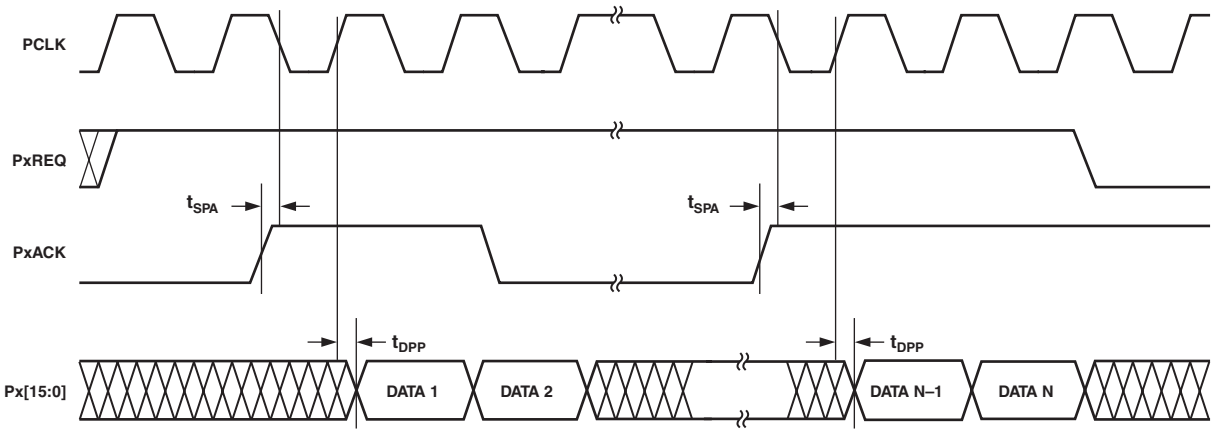


Figure 11. Master Mode PxACK to PCLK Switching Characteristics

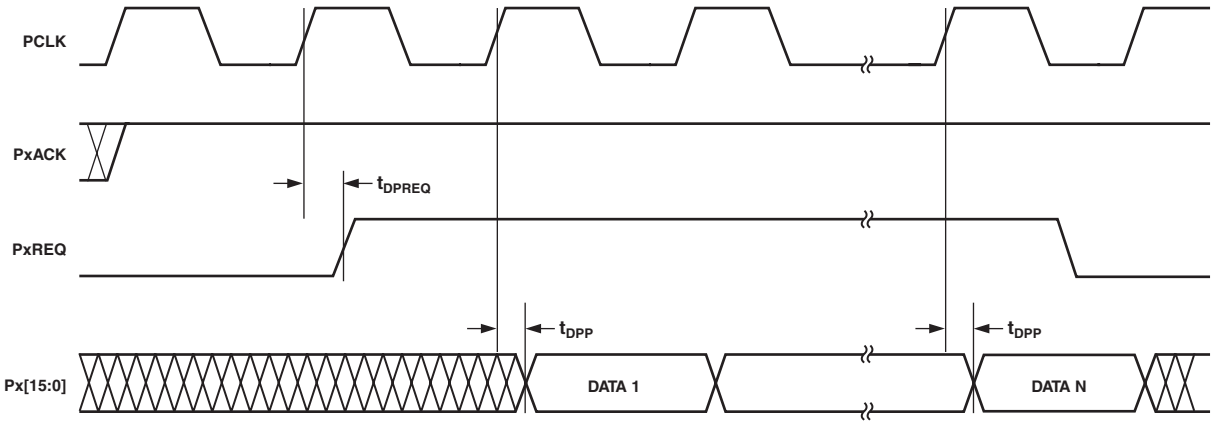


Figure 12. Master Mode PxREQ to PCLK Switching Characteristics

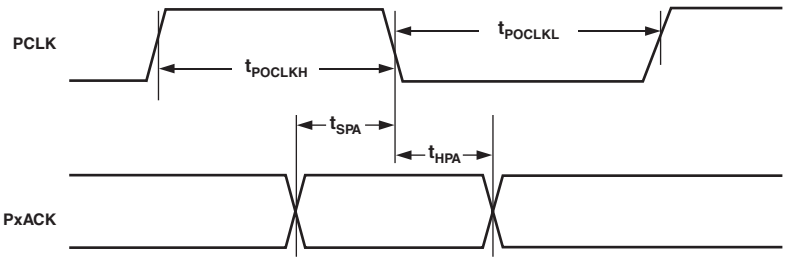


Figure 13. Slave Mode PxACK to PCLK Setup and Hold Characteristics

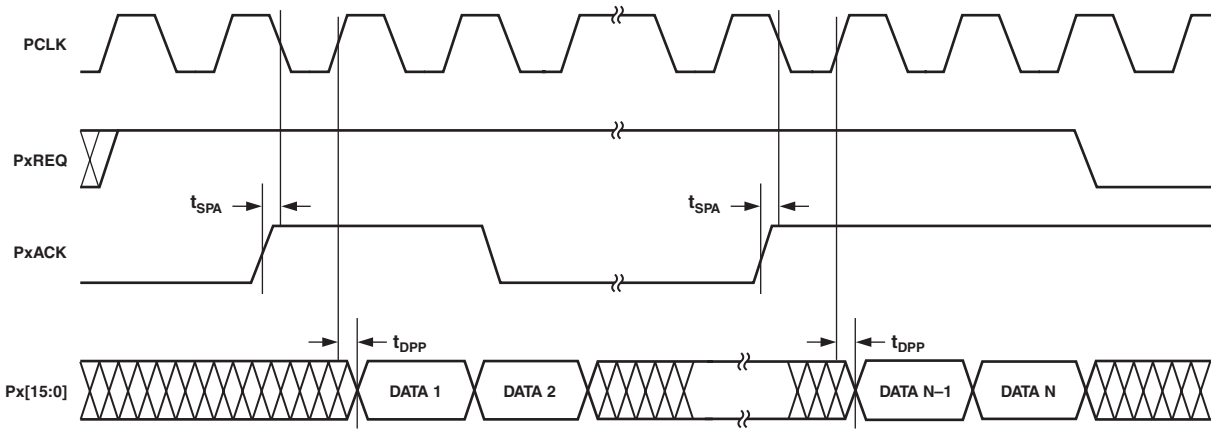


Figure 14. Slave Mode PxACK to PCLK Switching Characteristics

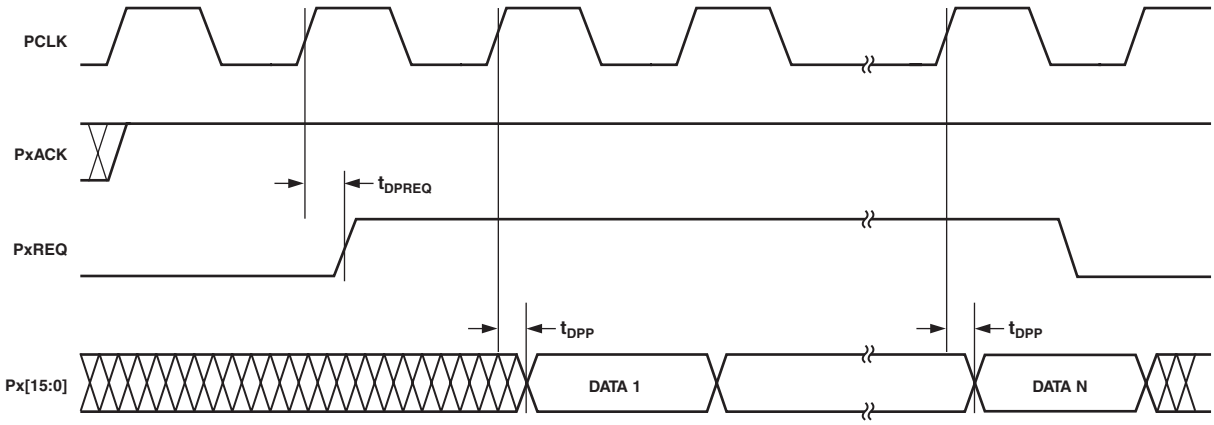


Figure 15. Slave Mode PxREQ to PCLK Switching Characteristics

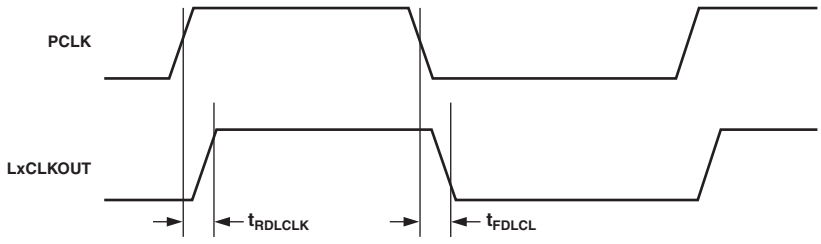


Figure 16. LxCLKOUT to PCLK Switching Characteristics

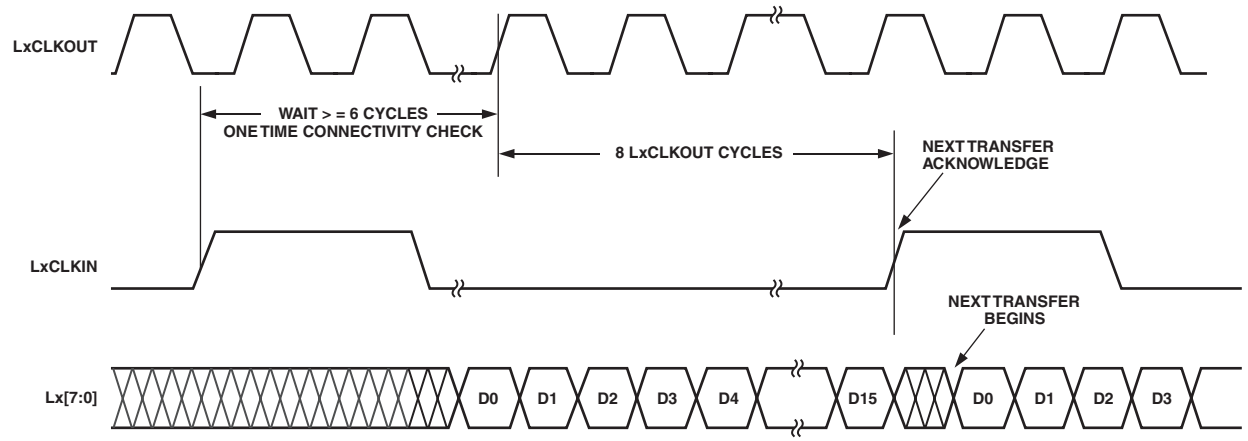


Figure 17. LxCLKIN to LxCLKOUT Data Switching Characteristics

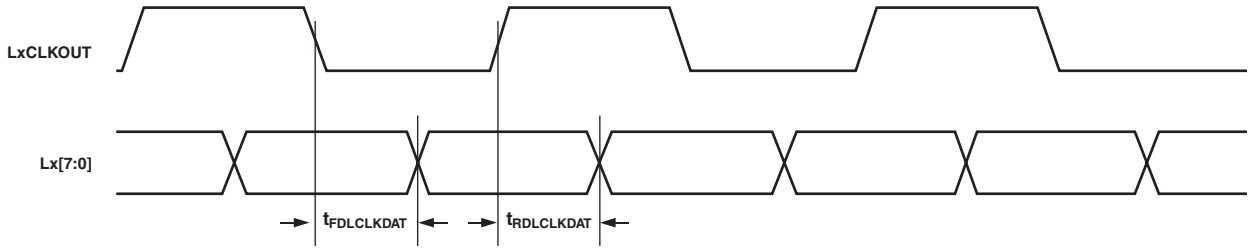
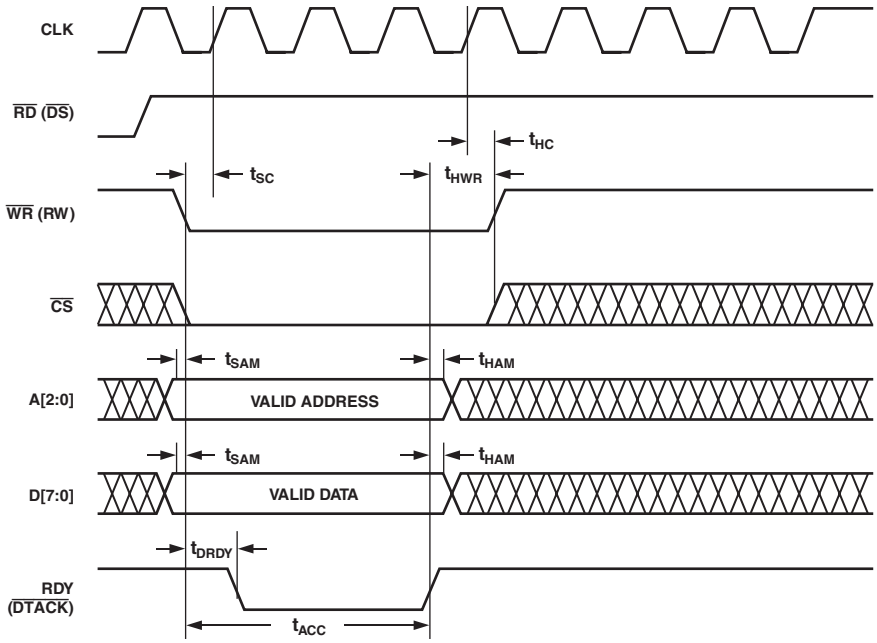


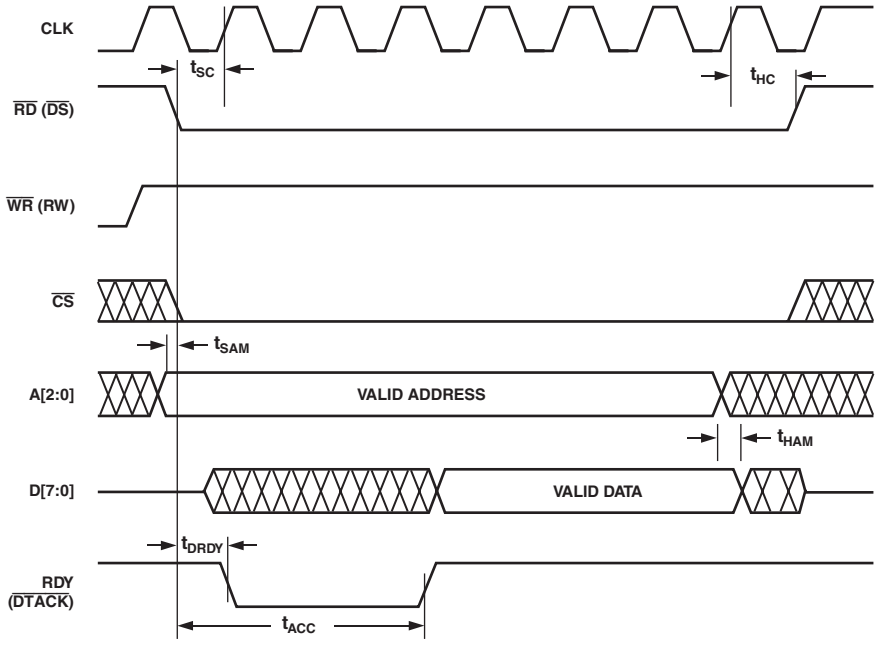
Figure 18. LxCLKOUT to Lx[7:0] Data Switching Characteristics

TIMING DIAGRAMS—INM MICROPORT MODE



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{WR}$ TO RE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF 9 CLK PERIODS.

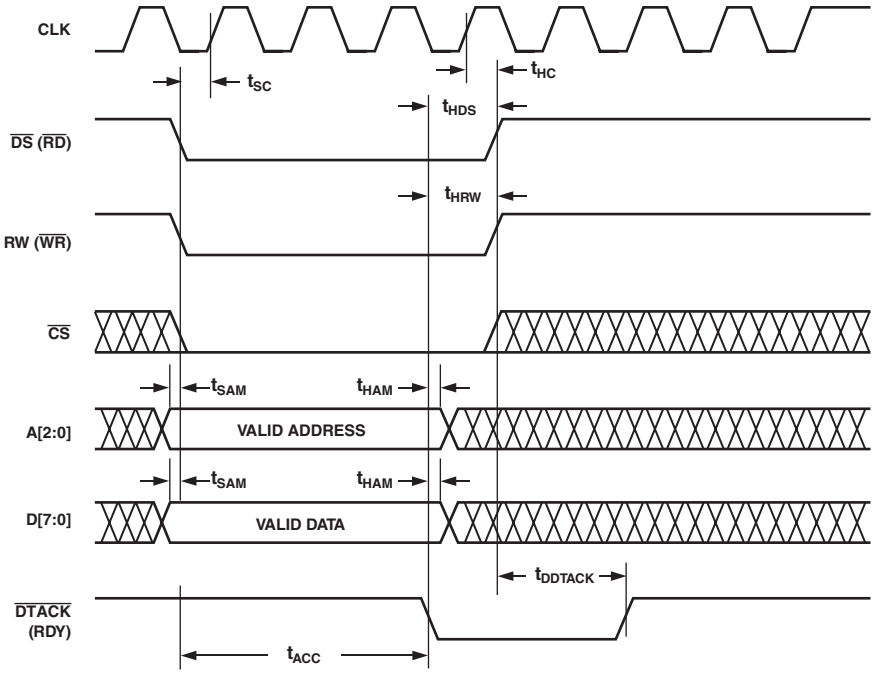
Figure 19. INM Microport Write Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{WR}$ TO RE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS.

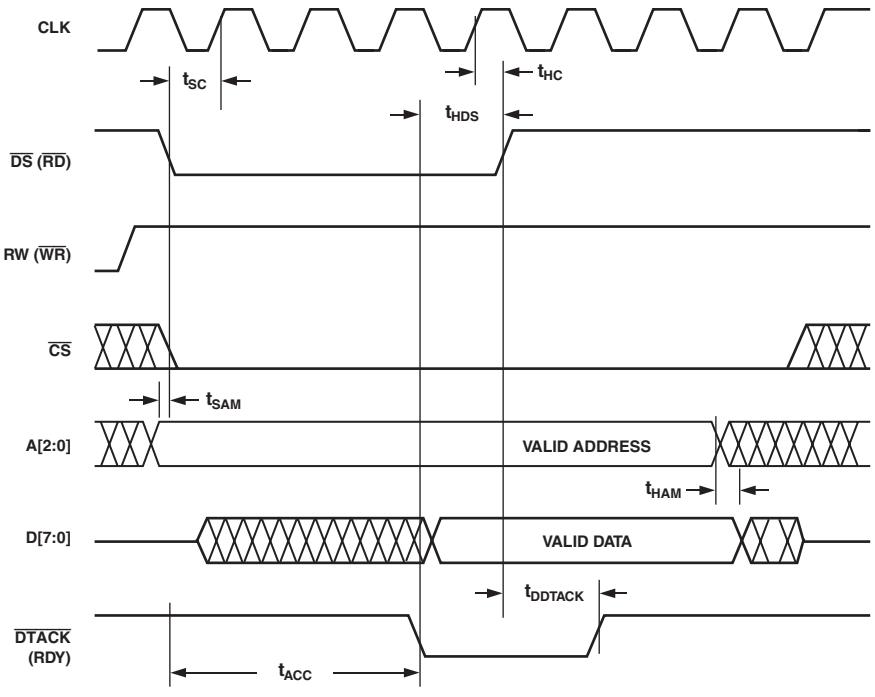
Figure 20. INM Microport Read Timing Requirements

TIMING DIAGRAMS—MNM MICROPORT MODE



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{DS}$ TO THE FE OF $\overline{DTACK}$.
2. t_{ACC} REQUIRES A MAXIMUM OF 9 CLK PERIODS.

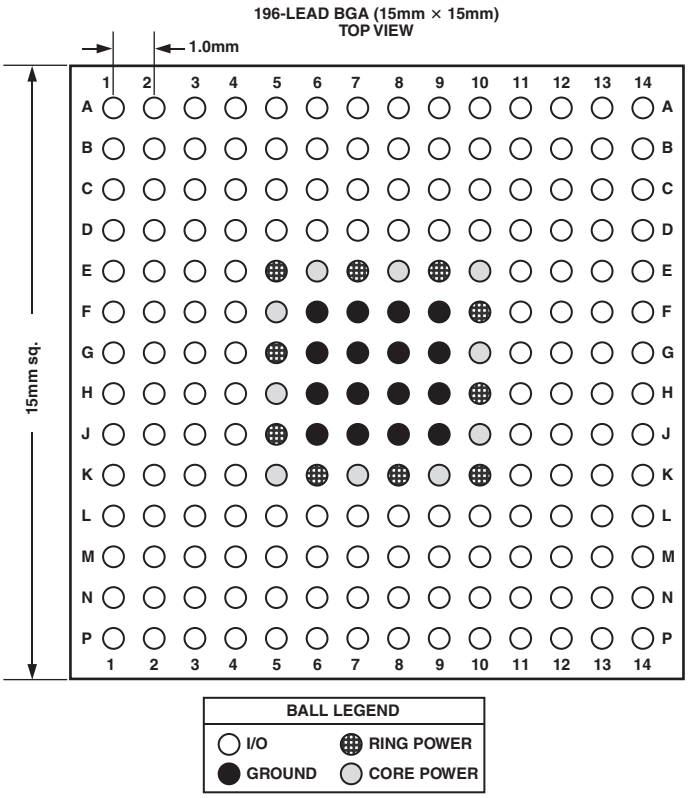
Figure 21. MNM Microport Write Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM THE FE OF $\overline{DS}$ TO THE FE OF $\overline{DTACK}$.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS.

Figure 22. MNM Microport Read Timing Requirements

PIN CONFIGURATION



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NO CONNECT	INB6	INB9	INB11	EXPB1	VDDIO (RESERVED)	PB14	PB12	PB10	PB1 | LB1	PB2 | LB2	PB5 | LB5	PBCH1 | LBCLKIN	NO CONNECT	A
B	INB2	INB4	INB5	INB8	INB12	EXPB0	PB15	PB13	PB11	PB4 | LB4	PB0 | LB0	PB3 | LB3	PBCH0 | LBCLKOUT	PB7 | LB7	B
C	INB0	INB3	INB7	INB13	INB10	EXPB2	PBACK	PBREQ	PB9	PB8		PBIQ	PCLK	PB6 | LB6	C
D	LIB-B	INB1										PAACK	SDI	PAIQ	D
E	CLK	IENB			VDDIO	VDD	VDDIO	VDD	VDDIO	VDD		SCLK	CHIP_ID2	CHIP_ID3	E
F	EXPA1	EXPA0	EXPA2		VDD	GND	GND	GND	GND	VDDIO			CHIP_ID0	CHIP_ID1	F
G	INA12	INA13	INA10		VDDIO	GND	GND	GND	GND	VDD			TDI	TMS	G
H	INA11	INA9	INA7		VDD	GND	GND	GND	GND	VDDIO			PA14	PA15	H
J	INA8	INA6			VDDIO	GND	GND	GND	GND	VDD		PAREQ	PA12	PA13	J
K	INA5	INA4			VDD	VDDIO	VDD	VDD	VDD	VDDIO		TDO	PA10	PA11	K
L	INA3	INA1										TCLK	PA8	PA9	L
M	INA2	IENA		$\overline{\text{DTACK}}$ (RDY)	MODE	$\overline{\text{CS}}$	RW ($\overline{\text{WR}}$)	$\overline{\text{TRST}}$	$\overline{\text{DS}}$($\overline{\text{RD}}$)	A1	A0	PA4 | LA4	PA2 | LA2	PA0 | LA0	M
N	INA0	LIB-A	LIA-B	SYNCB	SYNCD	D7	D5	D3	D1	A2	PCHA1 | LACLKIN	PA5 | LA5	PA3 | LA3	PA1 | LA1	N
P	NO CONNECT	LIA-A	SYNCA	SYNCC	$\overline{\text{RESET}}$	D6	D4	D2	D0	PA6 | LA6	PCHA0 | LACLKOUT	PA7 | LA7		NO CONNECT	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PIN FUNCTION DESCRIPTIONS

	Mnemonic	Type	Function
POWER SUPPLY			
	VDD	P	2.5 V Supply
	VDDIO	P	3.3 V IO Supply
	GND	G	Ground
INPUTS			
	INA[13:0][1]	I	A Input Data (Mantissa)
	EXPA[2:0][1]	I	A Input Data (Exponent)
	IENA[2]	I	Input Enable—Input A
	INB[13:0][1]	I	B Input Data (Mantissa)
	EXPB[2:0][1]	I	B Input Data (Exponent)
	$\overline{\text{IENB}}$[2]	I	Input Enable—Input B
	$\overline{\text{RESET}}$	I	Active Low Reset Pin
	CLK	I	Input Clock
	PCLK	I/O	Link/Parallel Port Clock
	LACLKIN	I	Link Port A Data Ready
	LBCLKIN	I	Link Port B Data Ready
	SYNCA[1]	I	All Sync pins go to all four output channels.
	SYNCB[1]	I	All Sync pins go to all four output channels.
	SYNCC[1]	I	All Sync pins go to all four output channels.
	SYNCD[1]	I	All Sync pins go to all four output channels.
	$\overline{\text{CS}}$[1]	I	Chip Select
	CHIP_ID[3:0][1]	I	Chip ID Selector
CONTROL			
	PAACK	I	Parallel Port A Acknowledge
	PAREQ	O	Parallel Port A Request
	PBACK	I	Parallel Port B Acknowledge
	PBREQ	O	Parallel Port B Request
MICROPORT CONTROL			
	D[7:0]	I/O/T	Bidirectional Microport Data
	A[2:0]	I	Microport Address Bus
	$\overline{\text{DS}}$($\overline{\text{RD}}$)	I	Active Low Data Strobe (Active Low Read)
	$\overline{\text{DTACK}}$(RDY)[2]	O/T	Active Low Data Acknowledge (Microport Status Bit)
	R/$\overline{\text{W}}$($\overline{\text{WR}}$)	I	Read Write (Active Low Write)
	MODE	I	Intel or Motorola Mode Select
SERIAL PORT CONTROL			
	SDI[1]	I	Serial Port Control Data Input
	SCLK[1]	I	Serial Port Control Clock
OUTPUTS			
	LIA–A	O	Level Indicator—Input A, Interleaved–Data A
	LIA–B	O	Level Indicator—Input A, Interleaved–Data B
	LIB–B	O	Level Indicator—Input B, Interleaved–Data B
	LIB–A	O	Level Indicator—Input B, Interleaved–Data A
	LACLKOUT	O	Link Port A Clock Output
	LBCLKOUT	O	Link Port B Clock Output
	LA[7:0]	O	Link Port A Output Data
	LB[7:0]	O	Link Port B Output Data
	PA[15:0]	O	Parallel Output Data Port A
	PB[15:0]	O	Parallel Output Data Port B
	PACH[1:0]	O	Parallel Output Port A Channel Indicator
	PBCH[1:0]	O	Parallel Output Port B Channel Indicator
	PAIQ	O	Parallel Port A I/Q Data Indicator
	PBIQ	O	Parallel Port B I/Q Data Indicator
JTAG AND BIST			
	$\overline{\text{TRST}}$[2]	I	Test Reset Pin
	TCLK[1]	I	Test Clock Input
	TMS[2]	I	Test Mode Select Input
	TDO	O/T	Test Data Output
	TDI[2]	I	Test Data Input

NOTES
[1]Pins with a pull-down resistor of nominal 70 kΩ.
[2]Pins with a pull-up resistor of nominal 70 kΩ.

EXAMPLE FILTER RESPONSE

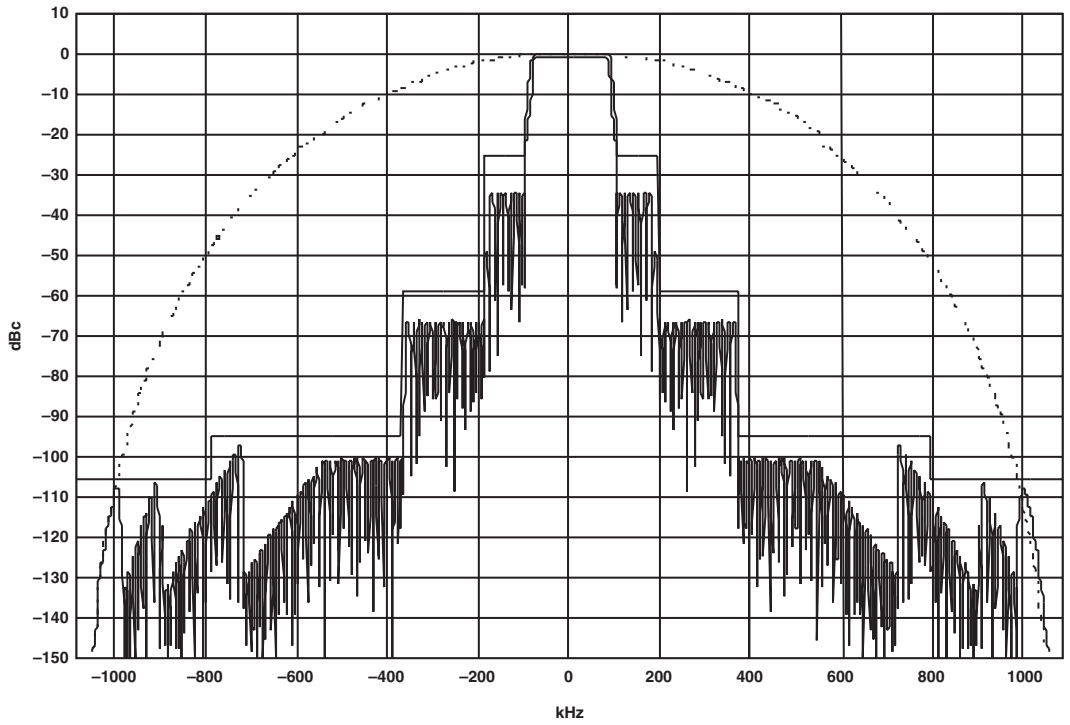


Figure 23. The Filter Above Is Based on a 65 MSPS Input Data Rate and an Output Rate of 541.6666 kSPS (Two Samples per Symbol for EDGE). Total decimation rate is 120, distributed between the rCIC2, CIC5, and RCF.

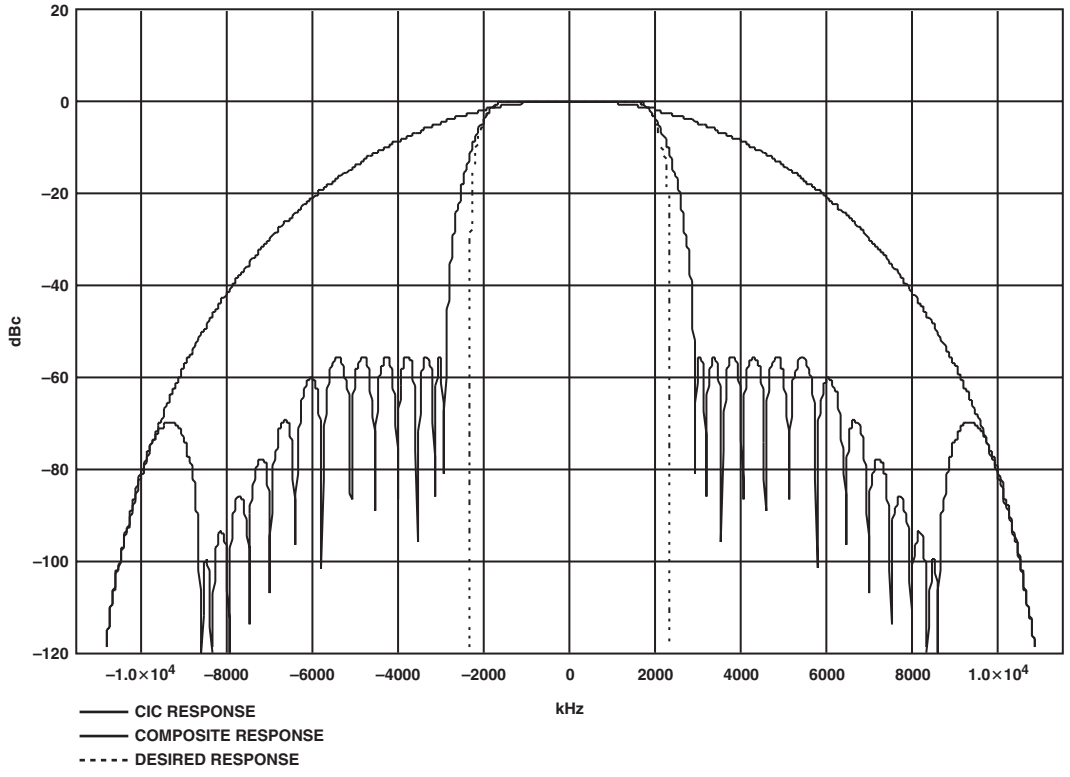


Figure 24. The Filter Above Is Designed to Meet UMTS Specifications. For this configuration, the clock is set to 76.8 MSPS with 20× chip rate (3.84 MCPS) and a 2× output data rate of 7.68 MCPS using two channels of the AD6634.

INPUT DATA PORTS

The AD6634 features dual high speed ADC input ports, input port A and input port B. The dual input ports allow for the most flexibility with a single tuner chip. These can be diversity inputs or truly independent inputs such as separate antenna segments. Either ADC port can be routed to one of four tuner channels. For added flexibility, each input port can be used to support multiplexed inputs such as those found on the AD6600 or other ADCs with multiplexed outputs. This added flexibility can allow for up to four different analog sources to be processed simultaneously by the four internal channels.

In addition, the front end of the AD6634 contains circuitry that enables high speed signal level detection and control. This is accomplished with a unique high speed level detection circuit that offers minimal latency and maximum flexibility to control up to four analog signal paths. The overall signal path latency from input to output on the AD6634 can be expressed in high speed clock cycles. The following equation can be used to calculate the latency.

$$T_{LATENCY} = M_{rCIC2}\left(M_{CIC5} + 7\right) + N_{TAPS} + 26$$

M_{rCIC2} and M_{CIC5} are decimation values for the rCIC2 and CIC5 filters, respectively. N_{TAPS} is the number RCF taps chosen.

Input Data Format

Each input port consists of a 14-bit mantissa and 3-bit exponent. If interfacing to a standard ADC is required, the exponent bits can be grounded. If connected to a floating point ADC such as the AD6600, the exponent bits from that product can be connected to the input exponent bits of the AD6634. The mantissa data format is two's complement and the exponent is unsigned binary.

Input Timing

The data from each high speed input port is latched on the rising edge of CLK. This clock signal is used to sample the input port and clock the synchronous signal processing stages that follow in the selected channels.

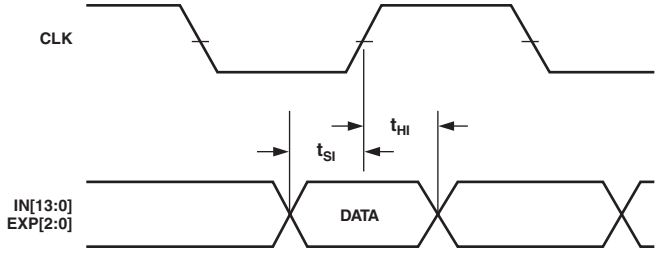


Figure 25. Input Data Timing Requirements

The clock signals can operate up to 80 MHz and have a 50% duty cycle. In applications using high speed ADCs, the ADC sample clock or data valid strobe is typically used to clock the AD6634.

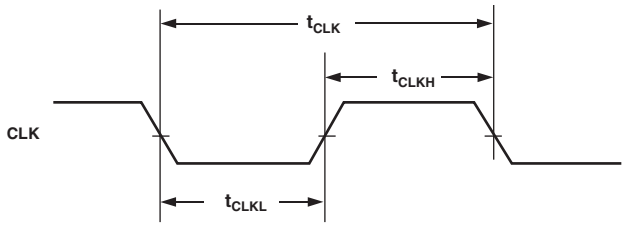


Figure 26. CLK Timing Requirements

Input Enable Control

There is an IENA and an IENB pin for Input Port A and Input Port B, respectively. There are four modes of operation possible while using each IEN pin. Using these modes, it is possible to emulate operation of the other RSPs, such as the AD6620, which offer dual channel modes normally associated with diversity operations. These modes are: IEN transition to Low, IEN transition to High, IEN High, and Blank on IEN low.

In the IEN High mode, the inputs and normal operations occur when the input enable is high. In the IEN transition to Low mode, normal operations occur on the first rising edge of the clock after the IEN transitions to low. Likewise in the IEN transition to High mode, operations occur on the rising edge of the clock after the IEN transitions to High. (See the Numerically Controlled Oscillator section for more details on configuring the Input Enable Modes.) In Blank on IEN low mode, the input data is interpreted as zero when IEN is low.

A typical application for this feature would be to take the data from an AD6600 Diversity ADC to one of the inputs of the AD6634. The A/B_OUT from that chip would be tied to the IEN. Then one channel within the AD6634 would be set so that IEN transition to Low is enabled. Another channel would be configured so that IEN transition to High is enabled. This would allow two of the AD6634 channels to be configured to emulate that AD6620 in diversity mode. Of course the NCO frequencies and other channel characteristics would need to be set similarly, but this feature allows the AD6634 to handle interleaved data streams such as those found on the AD6600.

The difference between the IEN transition to high and the IEN high is found when a system clock is provided that is higher than the data rate of the converter. It is often advantageous to supply a clock that runs faster than the data rate so that additional filter taps can be computed. This naturally provides better filtering. In order to ensure that other parts of the circuit properly recognize the faster clock in the simplest manner, the IEN transition to low or high should be used. In this mode, only the first clock edge that meets the setup and hold times will be used to latch and process the input data. All other clock pulses are ignored by front end processing. However, each clock cycle will still produce a new filter computation pair.

Gain Switching

The AD6634 includes circuitry that is useful in applications where either large dynamic ranges exist or where gain ranging converters are employed. This circuitry allows digital thresholds to be set such that an upper and a lower threshold can be programmed.

One such use of this may be to detect when an ADC is about to reach full scale with a particular input condition. The results would be to provide a flag that could be used to quickly insert an attenuator that would prevent ADC overdrive. If 18 dB (or any arbitrary value) of attenuation (or gain) is switched in, the signal dynamic range of the system will have been increased by 18 dB. The process begins when the input signal reaches the upper programmed threshold. In a typical application, this may be set 1 dB (user-definable) below full scale. When this input condition is met, the appropriate LI (LIA-A, LIA-B, LIB-A, or LIB-B) signal associated with either the A or B input port is made active. This can be used to switch the gain or attenuation of the external circuit. The LI line stays active until the input condition falls below the lower programmed threshold. In order to provide hysteresis, a dwell time register (see Memory Map for Input Control Registers) is available to hold off switching of the control line for a predetermined number of clocks. Once the input condition is below the lower threshold, the programmable counter begins counting high speed clocks. As long as the input signal stays below the lower threshold for the number of high speed clock cycles programmed, the attenuator will be removed on the terminal count. However, if the input condition goes above the lower threshold with the counter running, it will be reset and must fall below the lower threshold again to initiate the process. This will prevent unnecessary switching between states and is illustrated in Figure 27.

When the input signal goes above the upper threshold, the appropriate LI signal becomes active. Once the signal falls below the lower threshold, the counter begins counting. If the input condition goes above the lower threshold, the counter is reset and starts again as shown in Figure 27. Once the counter has terminated to 0, the LI line goes inactive.

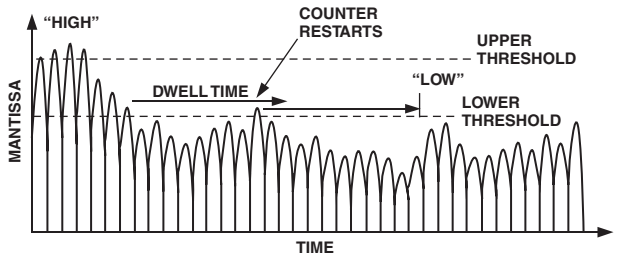


Figure 27. Threshold Settings for LI

The LI line can be used for a variety of functions. It can be used to set the controls of an attenuator, DVGA, or integrated and used with an analog VGA. To simplify the use of this feature, the AD6634 includes two separate gain settings, one when this line is inactive (rCIC2_QUIET[4:0] stored in bits 9:5 of 0x92 register) and the other when active (rCIC2_LOUD[4:0] stored in bits 4:0 of 0x92 register). This allows the digital gain to be adjusted to the external changes. In conjunction with the gain setting, a variable hold-off is included to compensate for the pipeline delay of the ADC and the switching time of the gain control element. Together, these two features provide seamless gain switching.

Another use of this pin is to facilitate a gain range hold-off within a gain ranging ADC. For converters that use gain ranging to increase total signal dynamic range, it may be desirable to prohibit internal gain ranging from occurring in some instances. For such converters, the LI (A or B) line can be used to hold this off. For this application, the upper threshold would be set based on similar criteria. However, the lower threshold would be set to a level consistent with the gain ranges of the specific converter. The hold-off delay can then be set appropriately for any of a number of factors such as fading profile, signal peak to average ratio, or any other time-based characteristics that might cause unnecessary gain changes.

Since the AD6634 has a total of four gain control circuits that can be used if both A and B input ports have interleaved data. Each respective LI pin is independent and can be set to different set points. It should be noted that the gain control circuits are wideband and are implemented prior to any filtering elements to minimize loop delay. Any of the four channels can be set to monitor any of the possible four input channels (two in normal mode and four when the inputs are time multiplexed).

The chip also provides appropriate scaling of the internal data based on the attenuation associated with the LI signal. In this manner, data to the DSP maintains a correct scale value throughout the process, making it totally independent. Since there are often finite delays associated with external gain switching components, the AD6634 includes a variable pipeline delay that can be used to compensate for external pipeline delays or gross settling times associated with gain/attenuator devices. This delay may be set up to seven high speed clocks. These features ensure smooth switching between gain settings.

Input Data Scaling

The AD6634 has two data input ports, an A input port and a B input port. Each accepts 14-bit mantissa (two's complement integer) IN[13:0], a 3-bit exponent (unsigned integer) EXP[2:0] and the Input Enable(IEN). Both inputs are clocked by CLK. These pins allow direct interfacing to both standard fixed-point ADCs such as the AD9238 and AD6645, as well as to gain-ranging ADCs such as the AD6600. For normal operation with ADCs having fewer than 14 bits, the active bits should be MSB justified and the unused LSBs should be tied low.

The 3-bit exponent, EXP[2:0] is interpreted as an unsigned integer. The exponent will subsequently be modified by either of rCIC2_LOUD[4:0] or rCIC2_QUIET[4:0] depending on whether LI line is active or not. These 5-bit scale values are stored in the rCIC2 scale register (0x92) and the scaling is applied before the data enters the rCIC2 resampling filter. These 5-bit registers contain scale values to compensate for the rCIC2 gain, external attenuator (if used) and the exponent offset (Expoff). If no external attenuator is used, both the rCIC2_QUIET and rCIC2_LOUD registers would contain the same value. A detailed explanation and equation for setting the attenuating scale register is given in the Scaling with Floating-Point or Gain-Ranging ADCs section.

Scaling with Fixed-Point ADCs

For fixed-point ADCs, the AD6634 exponent inputs EXP[2:0] are typically not used and should be tied low. The ADC outputs are tied directly to the AD6634 Inputs, MSB-justified. The ExpOff bits in 0x92 should be programmed to 0. Likewise, the Exponent Invert bit should be 0. Thus for fixed-point ADCs, the exponents are typically static and no input scaling is used in the AD6634.

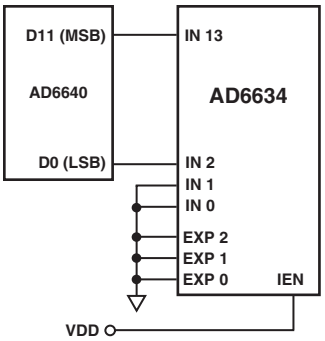


Figure 28. Typical Interconnection of the AD6640 Fixed Point ADC and the AD6634

Scaling with Floating-Point or Gain-Ranging ADCs

An example of the exponent control feature combines the AD6600 and the AD6634. The AD6600 is an 11-bit ADC with three bits of gain ranging. In effect, the 11-bit ADC provides the mantissa, and the three bits of relative signal strength indicator (RSSI) for the exponent. Only five of the eight available steps are used by the AD6600. See the AD6600 data sheet for additional details.

For gain-ranging ADCs such as the AD6600,

$$SCALED\_INPUT = IN \times 2^{-MOD(7-EXP+rCIC2,\ 32)},$$
$$EXPINV = 1, EXPWEIGHT = 0$$

where, *IN* is the value of IN[13:0], *EXP* is the value of EXP[2:0], and rCIC2 is the rCIC scale register value (0x92 Bits 9–5 and 4–0).

The RSSI output of the AD6600 numerically grows with increasing signal strength of the analog input (RSSI = 5 for a large signal, RSSI = 0 for a small signal). When the Exponent Invert Bit (ExpInv) is set to zero, the AD6634 will consider the smallest signal at the IN[13:0] to be the largest and as the EXP word increases, it shifts the data down internally (EXP = 5 will shift a 14-bit word right by five internal bits before passing the data to the rCIC2). In this example where ExpInv = 0, the AD6634 regards the largest signal possible on the AD6600 as the smallest signal. Thus, we can use the Exponent Invert Bit to make the AD6634 exponent agree with the AD6600 RSSI. By setting ExpInv = 1, this forces the AD6634 to shift the data up (left) for growing EXP instead of down. The exponent invert bit should always be set high for use with the AD6600.

The exponent offset is used to shift the data up. For example, Table I shows that with no rCIC2 scaling, 12 dB of range is lost when the ADC input is at the largest level. This is undesirable because it lowers the dynamic range and SNR of the system by reducing the signal of interest relative to the quantization noise floor.

To avoid this automatic attenuation of the full-scale ADC signal the ExpOff is used to move the largest signal (RSSI = 5) up to the point where there is no down shift. In other words, once the Exponent Invert bit has been set, the exponent offset should be adjusted so that mod(7–5 + ExpOff, 32) = 0. This is the case when exponent offset is set to 30 since mod(32, 32) = 0. Table II illustrates the use of ExpInv and ExpOff when used with the AD6600 ADC.

Table I. AD6600 Transfer Function with AD6634 ExpInv = 1, and No ExpOff

ADC Input Level	AD6600 RSSI[2:0]	AD6634 Data	Signal Reduction (dB)
Largest	101 (5)	/4 (>> 2)	–12
	100 (4)	/8 (>>3)	–18
	011 (3)	/16 (>> 4)	–24
	010 (2)	/32 (>> 5)	–30
	001 (1)	/64 (>> 6)	–36
Smallest	000 (0)	/128 (>> 7)	–42

(ExpInv = 1, rCIC2 Scale = 0)

Table II. AD6600 Transfer Function with AD6620 ExpInv = 1, and ExpOff = 6

ADC Input Level	AD6600 RSSI[2:0]	AD6634 Data	Signal Reduction (dB)
Largest	101 (5)	/1 (>> 0)	0
	100 (4)	/2 (>> 1)	–6
	011 (3)	/4 (>> 2)	–12
	010 (2)	/8 (>> 3)	–18
	001 (1)	/16 (>> 4)	–24
Smallest	000 (0)	/32 (>> 5)	–30

(ExpInv = 1, ExpOff = 30, ExpWeight = 0)

This flexibility in handling the exponent allows the AD6634 to interface with gain-ranging ADCs other than the AD6600. The Exponent Offset can be adjusted to allow up to seven RSSI(EXP) ranges to be used as opposed to the AD6600's five. It also allows the AD6634 to be tailored in a system that employs the AD6600 but does not utilize all of its signal range. For example, if only the first four RSSI ranges are expected to occur, the ExpOff could be adjusted to 29, which would then make RSSI = 4 correspond to the 0 dB point of the AD6634.

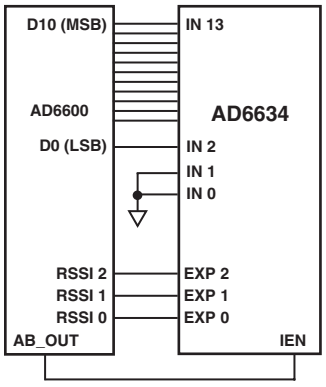


Figure 29. Typical Interconnection of the AD6600 Gain-Ranging ADC and the AD6634

NUMERICALLY CONTROLLED OSCILLATOR

Frequency Translation

This processing stage comprises a digital tuner consisting of two multipliers and a 32-bit complex NCO. Each channel of the AD6634 has an independent NCO. The NCO serves as a quadrature local oscillator capable of producing an NCO frequency between –CLK/2 and +CLK/2 with a resolution of CLK/2^{32} in the complex mode. The worst-case spurious signal from the NCO is better than –100 dBc for all output frequencies.

The NCO frequency value in registers 0x85 and 0x86 is interpreted as a 32-bit unsigned integer. The NCO frequency is calculated using the equation below.

$$NCO\_FREQ = 2^{32} \times MOD\left(\frac{f_{CHANNEL}}{CLK}\right)$$

where, *NCO_FREQ* is the 32-bit integer (registers 0x85 and 0x86), $f_{CHANNEL}$ is the desired channel frequency, and *CLK* is the AD6634 master clock rate or input data rate depending on the Input Enable mode used. See Input Enable Control section.

NCO Frequency Hold-Off Register
When the NCO Frequency registers are written, data is actually passed to a shadow register. Data may be moved to the main registers by one of two methods: when the channel comes out of sleep mode or when a SYNC Hop occurs. In either event a counter can be loaded with NCO Frequency Hold-Off register value. The 16-bit unsigned integer counter (0x84) starts counting down clocked by the master clock and when it reaches zero, the new frequency value in the shadow register is written to the NCO Frequency register. The NCO could also be set up to SYNC immediately, in which case the Frequency Hold-off counter is bypassed and new frequency values are updated immediately.

Phase Offset
The phase offset register (0x87) adds an offset to the phase accumulator of the NCO. This is a 16-bit register and is interpreted as a 16-bit unsigned integer. A 0x0000 in this register corresponds to a 0 Radian offset and a 0xFFFF corresponds to an offset of 2π $(1\text{-}1/(2^{16}))$ Radians. This register allows multiple NCOs to be synchronized to produce sine waves with a known and steady phase difference.

NCO Control Register
The NCO control register located at 0x88 is used to configure the features of the NCO. These are controlled on a per-channel basis, and are described below.

Bypass
The NCO in the front end of the AD6634 can be bypassed. Bypass mode is enabled by setting Bit 0 of 0x88 high. When it is bypassed, down conversion is not performed and the AD6634 channel functions simply as a real filter on complex data. This is useful for baseband sampling applications where the A input is connected to the I signal path within the filter and the B input is connected to the Q signal path. This may be desired if the digitized signal has already been converted to baseband in prior analog stages or by other digital preprocessing.

Phase Dither
The AD6634 provides a phase dither option for improving the spurious performance of the NCO. Phase dither is enabled by setting Bit 1. When phase dither is enabled by setting this bit high, spurs due to phase truncation in the NCO are randomized. The energy from these spurs is spread into the noise floor and spurious-free dynamic range is increased at the expense of very slight decreases in the SNR. The choice of whether phase dither is used in a system will ultimately be decided by the system goals. It should be employed if lower spurs are desired at the expense of a slightly raised noise floor. If a low noise floor is desired, and the higher spurs can be tolerated or filtered by subsequent stages, phase dither is not needed.

Amplitude Dither
Amplitude dither can also be used to improve spurious performance of the NCO. Amplitude dither is enabled by setting Bit 2. Amplitude dither improves performance by randomizing the amplitude quantization errors within the angular to Cartesian conversion of the NCO. This option may reduce spurs at the expense of a slightly raised noise floor. Amplitude dither and phase dither can be used together, separately, or not at all.

Clear Phase Accumulator on HOP
When Bit 3 is set, the NCO phase accumulator is cleared prior to a frequency hop. This ensures a consistent phase of the NCO on each hop. The NCO phase offset is unaffected by this setting and is still in effect. If phase continuous hopping is desired, this bit should be cleared and the last phase in the NCO phase register will be the initiating point for the new frequency.

Input Enable Control
There are four different modes of operation for the input enable. Each of the high speed input ports includes an IEN line. Any of the four filter channels can be programmed to take data from either of the two A or B input ports. (See WB Input Select section.) Along with data is the IEN(A,B) signal. Each filter channel can be configured to process the IEN signal in one of four modes. Three of the modes are associated with when data is processed based on a time division multiplexed data stream. The fourth mode is used in applications that employ time division duplex such as radar, sonar, ultrasound, and communications that involve TDD.

Mode 00: Blank on IEN Low
In this mode, data is blanked while the IEN line is low. During the period of time when the IEN line is high, new data is strobed on each rising edge of the input clock. When the IEN line is lowered, input data is replaced with zero values. During this period, the NCO continues to run such that when the IEN line is raised again, the NCO value will be at the value it would have been otherwise had the IEN line never been lowered. This mode has the effect of blanking the digital inputs when the IEN line is lowered. Back end processing (rCIC2, CIC5, and RCF) continues while the IEN line is high. This mode is useful for time division multiplexed applications.

Mode 01: Clock on IEN High
In this mode, data is clocked into the chip while the IEN line is high. During the period of time when the IEN line is high, new data is strobed on each rising edge of the input clock. When the IEN line is lowered, input data is no longer latched into the channel. Additionally, NCO advances are halted. However, back end processing (rCIC2, CIC5, and RCF) continues during this period. The primary use for this mode is to allow for a clock that is faster than the input sample data rate to allow more filter taps to be computed than would otherwise be possible. In Figure 30, input data is strobed only during the period of time that IEN is high despite the fact that the CLK continues to run at a rate four times faster than the data.

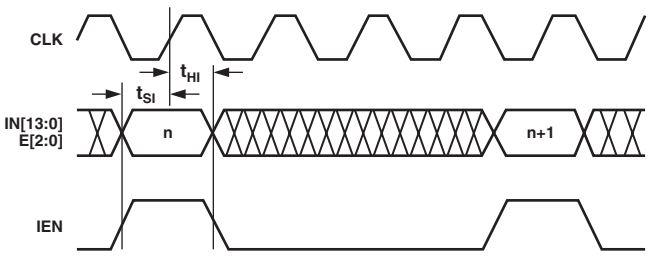


Figure 30. Fractional Rate Input Timing (4x CLK) in Mode 01

Mode 10: Clock on IEN Transition to High
In this mode, data is clocked into the chip only on the first clock edge after the rising transition of the IEN line. Although data is latched only on the first valid clock edge, the back end processing (rCIC2, CIC5, and RCF) continues on each available clock that may be present, similar to Mode 01. The NCO phase accumulator is incremented only once for each new input data sample and not once for each input clock.

Mode 11: Clock on IEN Transition to Low
In this mode, data is clocked into the chip only on the first clock edge after the falling transition of the IEN line. Although data is latched only on the first valid clock edge, the back end processing (rCIC2, CIC5, and RCF) continues one each available clock that may be present, similar to Mode 01. The NCO phase accumulator is incremented only once for each new input data sample and not once for each input clock.

WB Input Select
Bit 6 in this register controls which input port is selected for signal processing. If this bit is set high, input port B (INB, EXPB, and IENB) is connected to the selected filter channel. If this bit is cleared, input port A (INA, EXPA, and IENA) is connected to the selected filter channel.

Sync Select
Bits 7 and 8 of this register determine which external sync pin is associated with the selected channel. The AD6634 has four sync pins named SYNCA, SYNCB, SYNCC, and SYNCD. Any of these sync pins can be associated with any of the four receiver channels within the AD6634. Additionally, if only one sync signal is required for the system, all four receiver channels can reference the same sync pulse. Bit value 00 is channel A, 01 is channel B, 10 is channel C, and 11 is channel D.

SECOND ORDER rCIC FILTER

The rCIC2 filter is a second order cascaded resampling integrator comb filter. The resampler is implemented using a unique technique that does not require the use of a high speed clock, thus simplifying the design and saving power. The resampler allows for noninteger relationships between the master clock and the output data rate, which allows easier implementation of systems that are either multimode or require a master clock that is not a multiple of the data rate to be used.

Interpolation up to 512 and decimation up to 4096 is allowed in the rCIC2. The resampling factor for the rCIC2 (L) is a 9-bit integer. When combined with the decimation factor M, a 12-bit number, the total rate change can be any fraction in the form of:

$$R_{rCIC2} = \frac{L}{M}$$
$$R_{rCIC2} \le 1$$

The only constraint is that the ratio *L*/*M* must be less than or equal to one. This implies that the rCIC2 decimates by 1 or more.

Resampling is implemented by apparently increasing the input sample rate by the factor L, using zero stuffing for the new data samples. Following the resampler is a second order cascaded integrator comb filter. Filter characteristics are determined only by the fractional rate change (L/M).

The filter can process signals at the full rate of the input port, 80 MHz. The output rate of this stage is given by the equation:

$$f_{SAMP2} = \frac{L_{rCIC2}\ f_{SAMP}}{M_{rCIC2}}$$

Both L_{rCIC2} and M_{rCIC2} are unsigned integers. The interpolation rate (L_{rCIC2}) may be from 1 to 512 and the decimation (M_{rCIC2}) may be between 1 and 4096. The stage can be bypassed by setting the decimation to 1/1. The frequency response of the rCIC2 filter is given by the following equations.

$$H(z) = \frac{1}{2^{S_{rCIC2}} \times L_{rCIC2}} \times \left(\frac{1 - z\frac{M_{rCIC2}}{L_{rCIC2}}}{1 - z^1} \right)^2$$

$$H(f) = \frac{1}{2^{S_{rCIC2}} \times L_{rCIC2}} \times \left(\frac{\sin\left(\pi \frac{M_{rCIC2} \times f}{L_{rCIC2} \times f_{SAMP}}\right)}{\sin\left(\pi \frac{f}{f_{SAMP}}\right)} \right)^2$$

The gain and pass-band droop of the rCIC2 should be calculated by the equations above, as well as the filter transfer equations that follow. Excessive pass-band droop can be compensated for in the RCF stage by peaking the pass band by the inverse of the roll-off.

The scale factor, S_{rCIC2} is a programmable unsigned 5-bit between 0 and 31. This serves as an attenuator that can reduce the gain of the rCIC2 in 6 dB increments. For the best dynamic range, S_{rCIC2} should be set to the smallest value possible (i.e., lowest attenuation) without creating an overflow condition. This can be safely accomplished using the equation below, where *input_level* is the largest fraction of full scale possible at the input to the AD6634 (normally 1). The rCIC2 scale factor is always used whether or not the rCIC2 is bypassed.

Moreover, there are two scale registers (rCIC2_LOUD[4:0] Bits 4–0 in x92) and (rCIC2_QUIET[4:0] Bits 9–5 in x92) that are used in conjunction with the computed $S_{rCIC2,}$ which determines the overall rCIC2 scaling. The S_{rCIC2} value must be summed with the values in each respective scale registers and ExpOff to determine the scale value that must be placed in the rCIC2 scale register. This number must be less than 32 or the interpolation and decimation rates must be adjusted to validate this equation. The ceil function denotes the next whole integer and the floor function denotes the previous whole integer. For example, the ceil(4.5) is 5 while the floor(4.5) is 4.

$$scaled\_input = IN \times 2^{-MOD(Exp + rCIC2, 32)},\ ExpInv = 0$$
$$scaled\_input = IN \times 2^{-MOD(7 - Exp + rCIC2, 32)},\ ExpInv = 1$$

$$S_{rCIC2} = ceil\left[\log_2\left(M_{rCIC2} + floor\left(\frac{M_{rCIC2}}{L_{rCIC2}}\right) \times \left(2 \times M_{rCIC2} - L_{rCIC2} \times floor\left(\frac{M_{rCIC2}}{L_{rCIC2}} + 1\right)\right)\right)\right]$$

$$OL_{rCIC2} = \frac{\left(M_{rCIC2}{}^2\right)}{L_{rCIC2} \times 2^{S^{rCIC2}}} \times input\_level$$