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ANALOG DEVICES

4-Channel, 80 MSPS WCDMA Receive Signal Processor (RSP)

AD6635

FEATURES
Four 80 MSPS Wideband Inputs (14 Linear Bits Plus 3 RSSI)
4 Real Input Ports/2 Complex Input Ports
Processes 4 Wideband Channels (UMTS or cdma2000 1x) or 8 GSM/EDGE, IS136 Channels
8 Independent Digital Receivers in a Single Package
Four 16-Bit Parallel Output Ports and Four 8-Bit Link Ports
4 Programmable Digital AGC Loops with 96 dB Range
Digital Resampling for Noninteger Decimation Rates
Programmable Decimating FIR Filters
4 Interpolating Half-Band Filters
Flexible Control for Multicarrier and Phased Array

Programmable Attenuator Control for Clip Prevention and External Gain Ranging via Level Indicator
3.3 V I/O, 2.5 V CMOS Core
User Configurable Built-in Self Test (BIST) Capability

APPLICATIONS
Multicarrier, Multimode Digital Receivers
GSM, IS136, EDGE, PHS, IS95, UMTS, cdma2000
Micro and Pico Cell Systems, Software Radios
Wireless Local Loop
Smart Antenna Systems
In-Building Wireless Telephony

FUNCTIONAL BLOCK DIAGRAM
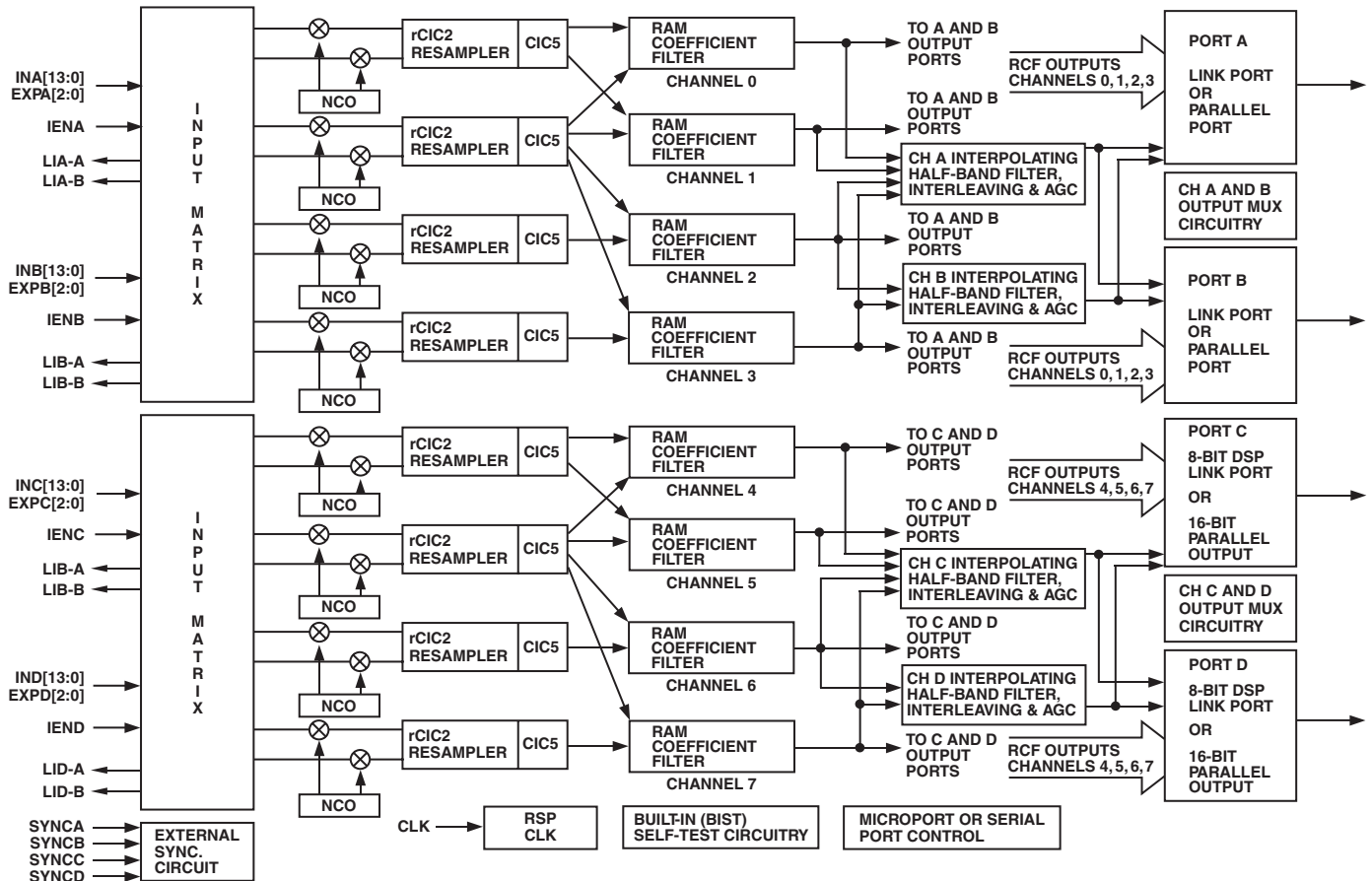
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AD6635

GENERAL DESCRIPTION

The AD6635 is a multimode, 8-channel, digital Receive Signal Processor (RSP) capable of processing up to four WCDMA channels. Each channel consists of four cascaded signal-processing elements: a frequency translator, two CIC decimating filters, and a programmable coefficient-decimating filter. Each input port has input level threshold detection circuitry for accommodating large dynamic ranges or situations where gain ranging converters are used. Quad 16-bit parallel output ports accommodate high data rate WBCDMA applications. On-chip interpolating half-band filters can also be used to further increase the output rate. In addition, each output port has a digital AGC for accommodating large dynamic ranges using smaller bit widths. The AGCs can maintain either signal level or clipping level, depending on their mode. Link port outputs are provided to enable glueless interfaces to Analog Devices' TigerSHARC DSP core.

The AD6635 is part of Analog Devices' SoftCell Multicarrier transceiver chipset designed for compatibility with Analog Devices' family of high sample rate IF sampling ADCs (AD9238/AD6645 12-bit and 14-bit). The SoftCell receiver comprises a digital receiver capable of digitizing an entire spectrum of carriers and digitally selecting the carrier of interest for tuning and channel selection. This architecture eliminates redundant radios in wireless base station applications.

High dynamic range decimation filters offer a wide range of decimation rates. The RAM-based architecture allows easy reconfiguration for multimode applications.

The decimating filters remove unwanted signals and noise from the channel of interest. When the channel of interest occupies less bandwidth than the input signal, this rejection of out-of-band noise is called "processing gain." By using large decimation factors, processing gain can improve the SNR of the ADC by 30 dB or more. In addition, the programmable RAM coefficient filter allows antialiasing, matched filtering, and static equalization functions to be combined in a single, cost-effective filter. Half-band interpolating filters at the output are used in various applications, especially in WCDMA or cdma2000 applications, to increase the output rate from 2× to 4× the chip rate. The AD6635 is equipped with four independent automatic gain control (AGC) loops for direct interface to a RAKE receiver.

The AD6635 is compatible with standard ADC converters, such as the AD664x, AD943x, AD923x, and the AD922x families of data converters. The AD6635 is also compatible with the AD6600 Diversity ADC, and hence can be designed into existing systems that use AD6600 ADCs.

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ARCHITECTURE

Each channel of the AD6635 has four signal processing stages: a Frequency Translator, a second-order Resampling Cascaded Integrator Comb FIR Filter (rCIC2), a fifth-order Cascaded Integrator Comb FIR Filter (CIC5), and a RAM Coefficient FIR Filter (RCF). Multiple modes are supported for clocking data into and out of the chip, and for providing flexibility for interfacing to a wide variety of digitizers. Programming and control is accomplished via serial and/or microprocessor interfaces.

Frequency translation is accomplished with a 32-bit complex Numerically Controlled Oscillator (NCO). Real data entering this stage is separated into inphase (I) and quadrature (Q) components by multiplying with the complex NCO word. This stage translates the input signal from a digital intermediate frequency (IF) to digital baseband. Phase and amplitude dither may be enabled on-chip to improve spurious performance of the NCO. A phase-offset word is available to create a known phase relationship between multiple AD6635s or between channels.

Following frequency translation is a fixed coefficient, high speed, second-order, Resampling Cascade Integrator Comb (rCIC2) filter that reduces the sample rate based on the ratio between the decimation and interpolation registers.

The next stage is a fifth-order Cascaded Integrator Comb (CIC5) filter whose response is defined by the decimation rate. The purpose of these filters is to reduce the data rate to the final filter stage (RCF), so that it can calculate more taps for the same RCF bandwidth. The CIC5 filter has better antialiasing (filtering) compared to rCIC2. In light of this, the user is advised to use this filter only if resampling is required or if the required decimation cannot be handled by CIC5 alone.

The final stage is a sum-of-products FIR filter with programmable 20-bit coefficients, and decimation rates programmable from 1 to 256 (1 to 32 in practice). The RAM Coefficient FIR Filter (RCF) can handle a maximum of 160 taps.

The data coming out of the RCF can be sent to output ports or to an interleaver. This section can interleave data from more than one channel. One carrier can be processed using more than one channel and the interleaver will interleave the data back into the output section. This way, processing power from more than one channel can be used for one carrier.

The interleaved data is sent into a fixed coefficient half-band interpolation filter where data is interpolated by a factor of two. Digital AGC following the half-band filter has a gain range of 96.3 dB. This AGC section is completely programmable in terms of its response. Four each of half-band filters and AGCs are present in the AD6635, as shown in the Functional Block Diagram. These half-band filters and AGC sections can be bypassed independent of each other.

The overall filter response for the AD6635 is the composite of all decimating and interpolating stages. Each successive filter stage is capable of narrower transition bandwidths, but requires a greater number of CLK cycles to calculate the output. More decimation in the first filter stage will minimize overall power consumption. Each independent filter stage can be bypassed in a unique way. Data from the chip is interfaced to the DSP via either a high speed parallel port or a TigerSHARC compatible link port. Each output can be independently configured to use either the parallel port or the link port.

Figure 1 illustrates the tuning function of the AD6635 NCOs to select and filter a single channel from a wide input spectrum. The frequency translator "tunes" the desired carrier to baseband. Figure 2 shows the combined filter response of the rCIC2, CIC5, and RCF filters for a sample filter configuration.
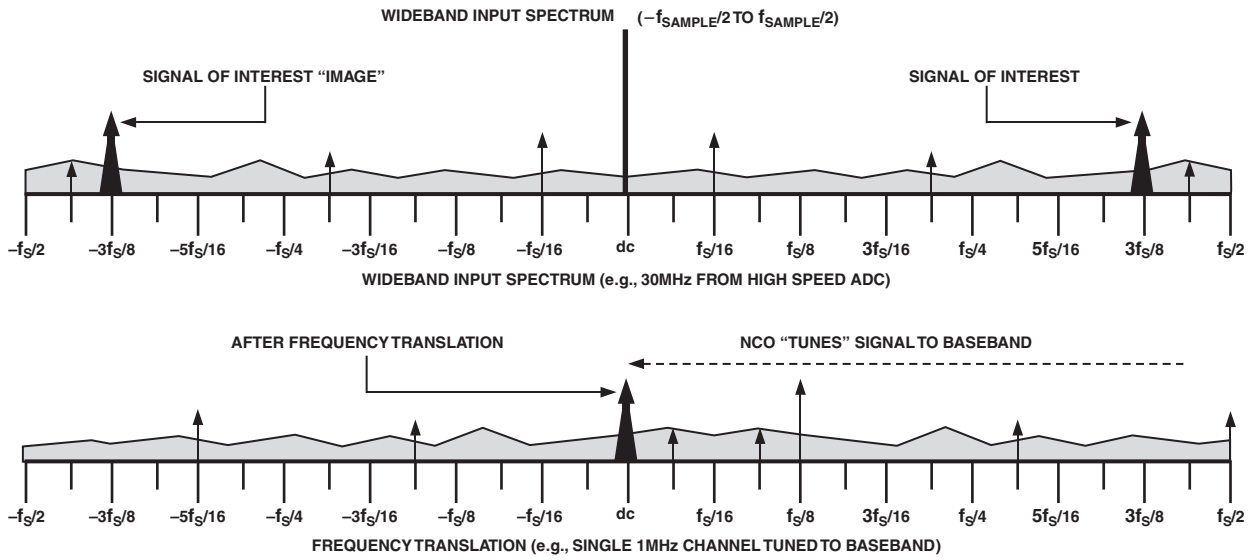
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Figure 1. AD6635 Frequency Translation of Wideband Input Spectrum
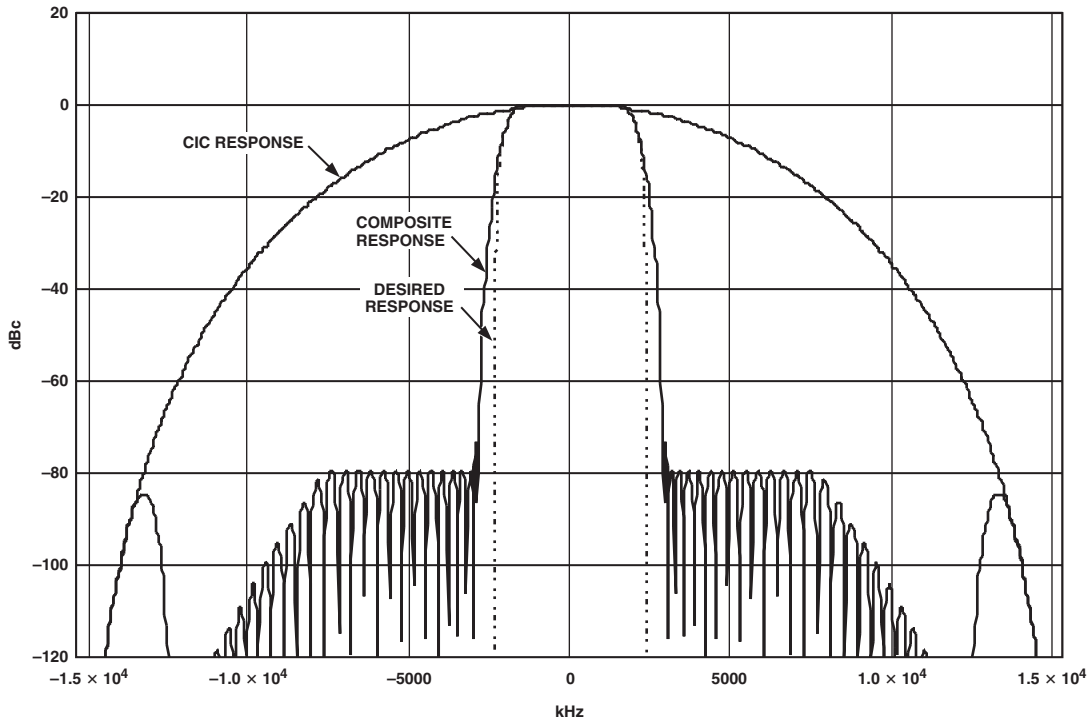
Figure 2. Composite Filter Response of rCIC2, CIC5, and RCF for a Sample Filter Configuration

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Temp	Test Level	AD6635BB Min	Typ	Max	Unit
VDD		IV	2.25	2.5	2.75	V
VDDIO		IV	3.0	3.3	3.6	V
T$_{AMBIENT}$		IV	−40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter (Conditions)	Temp	Test Level	AD6635BB Min	Typ	Max	Unit
LOGIC INPUTS (5 V TOLERANT)						
Logic Compatibility	Full	IV		3.3 V CMOS		
Logic 1 Voltage	Full	IV	2.0		5.0	V
Logic 0 Voltage	Full	IV	−0.3		+0.8	V
Logic 1 Current	Full	IV		1	10	μA
Logic 0 Current	Full	IV		1	10	μA
Logic 1 Current (inputs with pull-down)	Full	IV				
Logic 0 Current (inputs with pull-up)	Full	IV				
Input Capacitance	25°C	V		4		pF
LOGIC OUTPUTS						
Logic Compatibility	Full	IV				
Logic 1 Voltage (I$_{OH}$ = 0.25 mA)	Full	IV	2.4	VDD − 0.2		V
Logic 0 Voltage (I$_{OL}$ = 0.25 mA)	Full	IV		0.2	0.4	V
IDD SUPPLY CURRENT						
CLK = 80 MHz, (VDD = 2.75 V, VDDIO = 3.6 V)	Full	IV				
I$_{VDD}$					880	mA
I$_{VDDIO}$					150	mA
CLK = GSM Example (65 MSPS, VDD = 2.5 V, VDDIO = 3.3 V, 4 Channels)	25°C	V				
I$_{VDD}$				485		mA
I$_{VDDIO}$				60		mA
CLK = WCDMA Example (76.8 MSPS, VDD = 2.5V, VDDIO = 3.3 V, 2 Channels)	25°C	V				
I$_{VDD}$				830		mA
I$_{VDDIO}$				120		mA
POWER DISSIPATION						
CLK = 80 MHz	Full	IV			2.8	W
CLK = 65 MHz GSM/EDGE Example		V		1.4		mW
CLK = 76.8 MHz WCDMA Example		V		2.5		W
CLK = 78.64 MHz cdma2000 Example		V		2.3		W
All Channels in Sleep Mode	Full	IV		570		μW

Specifications subject to change without notice.

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SPECIFICATIONS (continued)

GENERAL TIMING CHARACTERISTICS[1, 2]

Parameter (Conditions)		Temp	Test Level	AD6635BB			Unit
				Min	Typ	Max	
CLKn TIMING REQUIREMENTS							
t_{CLK}	CLKn Period	Full	I	12.5			ns
t_{CLKL}	CLKn Width Low	Full	IV	5.6	$0.5 \times t_{CLK}$		ns
t_{CLKH}	CLKn Width High	Full	IV	5.6	$0.5 \times t_{CLK}$		ns
$\overline{RESET}$ TIMING REQUIREMENTS							
t_{RESL}	$\overline{RESET}$ Width Low	Full	I	30.0			ns
INPUT WIDEBAND DATA TIMING REQUIREMENTS							
t_{SI}	Input to ↑CLKn Setup Time	Full	IV	2.0			ns
t_{HI}	Input to ↑CLKn Hold Time	Full	IV	1.0			ns
LEVEL INDICATOR OUTPUT SWITCHING CHARACTERISTICS							
t_{DLI}	↑CLKn to LIx-y Output Delay Time	Full	IV	3.3		10.0	ns
SYNC TIMING REQUIREMENTS							
t_{SS}	SYNC(A, B, C, D) to ↑CLKn Setup Time	Full	IV	2.0			ns
t_{HS}	SYNC(A, B, C, D) to ↑CLKn Hold Time	Full	IV	1.0			ns
SERIAL PORT CONTROL TIMING REQUIREMENTS SWITCHING CHARACTERISTICS[2]							
t_{SCLK}	SCLKn (n = 0, 4) Period	Full	IV	16			ns
t_{SCLKL}	SCLKn Low Time	Full	IV	3.0			ns
t_{SCLKH}	SCLKn High Time	Full	IV	3.0			ns
INPUT CHARACTERISTICS							
t_{SSI}	SDIn to ↓SCLKn Setup Time	Full	IV	1.0			ns
t_{HSI}	SDIn to ↓SCLKn Hold Time	Full	IV	1.0			ns
PARALLEL PORT TIMING REQUIREMENTS (MASTER MODE) SWITCHING CHARACTERISTICS[3]							
$t_{DPOCLKL}$	↓CLKn to ↑PCLKn Delay (Divide by 1)	Full	IV	6.5		10.5	ns
$t_{DPOCLKLL}$	↓CLKn to ↑PCLKn Delay (Divide by 2, 4, or 8)	Full	IV	8.3		14.6	ns
t_{DPREQ}	↑CLKn to ↑PxREQ Delay					1.0	ns
t_{DPP}	↑CLKn to Px[15:0] Delay					0.0	ns
INPUT CHARACTERISTICS							
t_{SPA}	PxACK to ↓PCLKn Setup Time			7.0			ns
t_{HPA}	PxACK to ↓PCLKn Hold Time			−3.0			ns
PARALLEL PORT TIMING REQUIREMENTS (SLAVE MODE) SWITCHING CHARACTERISTICS[3]							
t_{POCLK}	PCLKn Period	Full	I	12.5			ns
t_{POCLKL}	PCLKn Low Period (when PCLK Divisor = 1)	Full	IV	2.0	$0.5 \times t_{POCLK}$		ns
t_{POCLKH}	PCLKn High Period (when PCLK Divisor = 1)	Full	IV	2.0	$0.5 \times t_{POCLK}$		ns
t_{DPREQ}	↑CLKn to ↑PxREQ Delay					10.0	ns
t_{DPP}	↑CLKn to Px[15:0] Delay					11.0	ns

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GENERAL TIMING CHARACTERISTICS[1, 2]

Parameter (Conditions)		Temp	Test Level	AD6635BB			Unit
				Min	Typ	Max	
INPUT CHARACTERISTICS							
t_{SPA}	PxACK to ↓PCLKn Setup Time			1.0			ns
t_{HPA}	PxACK to ↓PCLKn Hold Time			1.0			ns
LINK PORT TIMING REQUIREMENTS SWITCHING CHARACTERISTICS[3]							
t_{RDLCLK}	↑PCLKn to ↑LxCLKOUT Delay	Full	IV			2.5	ns
t_{FDLCLK}	↓PCLKn to ↓LxCLKOUT Delay	Full	IV			0	ns
$t_{RLCLKDAT}$	↑LxCLKOUT to Lx[7:0] Delay	Full	IV	0		2.9	ns
$t_{FLCLKDAT}$	↓LxCLKOUT to Lx[7:0] Delay	Full	IV	0		2.2	ns

NOTES
[1]All Timing Specifications valid over VDD range of 2.25 V to 2.75 V, and VDDIO range of 3.0 V to 3.6 V.
[2]C_{LOAD} = 40 pF on all outputs unless otherwise specified.
[3]The timing parameters for Px[15:0], PxREQ, PxACK, LxCLKOUT, and Lx[7:0] apply for output ports A, B, C, and D. (x stands for A, B, C, or D.)

Specifications subject to change without notice.

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MICROPROCESSOR PORT TIMING CHARACTERISTICS[1, 2]

Parameter (Conditions)		Temp	Test Level	AD6635BB			Unit
				Min	Typ	Max	
MICROPROCESSOR PORT, MODE MNM (MODE = 0)							
MODE INM WRITE TIMING							
t_{SC}	Control[3] to ↑CLKn Setup Time	Full	IV	2.0			ns
t_{HC}	Control[3] to ↑CLKn Hold Time	Full	IV	2.5			ns
t_{HWR}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) Hold Time	Full	IV	7.0			ns
t_{SAM}	Address/Data to $\overline{WR}$(RW) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RDY($\overline{DTACK}$) Hold Time	Full	IV	5.0			ns
t_{DRDY}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) High Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE INM READ TIMING							
t_{SC}	Control[3] to ↑CLKn Setup Time	Full	IV	5.0			ns
t_{HC}	Control[3] to ↑CLKn Hold Time	Full	IV	2.0			ns
t_{SAM}	Address to $\overline{RD}$($\overline{DS}$) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	5.0			ns
t_{DRDY}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) High Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns
MICROPROCESSOR PORT, MODE MNM (MODE = 1)							
MODE MNM WRITE TIMING							
t_{SC}	Control[3] to ↑CLKn Setup Time	Full	IV	2.0			ns
t_{HC}	Control[3] to ↑CLKn Hold Time	Full	IV	2.5			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{HRW}	RW($\overline{WR}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	7.0			ns
t_{SAM}	Address/Data to RW($\overline{WR}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RW($\overline{WR}$) Hold Time	Full	IV	5.0			ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay	Full	IV	8.0			ns
t_{ACC}	RW($\overline{WR}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE MNM READ TIMING							
t_{SC}	Control[3] to ↑CLKn Setup Time	Full	IV	5.0			ns
t_{HC}	Control[3] to ↑CLKn Hold Time	Full	IV	2.0			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address to $\overline{DS}$($\overline{RD}$) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	5.0			ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns

NOTES

[1]All Timing Specifications valid over VDD range of 2.25 V to 2.75 V, and VDDIO range of 3.0 V to 3.6 V.

[2]C_{LOAD} = 40 pF on all outputs unless otherwise specified.

[3]Specification pertains to control signals: R/W, ($\overline{WR}$), $\overline{DS}$, ($\overline{RD}$), $\overline{CS0}$, $\overline{CS1}$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . 3.6 V
Input Voltage . . . . –0.3 V to +5.3 V (5 V Tolerant)
Output Voltage Swing . . . . –0.3 V to VDDIO + 0.3 V
Load Capacitance . . . . 200 pF
Junction Temperature Under Bias . . . . 150°C
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature (5 sec) . . . . 280°C

*Stresses greater than those listed above may cause permanent damage to the device
These are stress ratings only; functional operation of the devices at these or any
other conditions greater than those indicated in the operational sections of this
specification is not implied. Exposure to absolute maximum rating conditions for
extended periods may affect device reliability.

Thermal Characteristics

324-Lead BGA:

θ_{JA} = 16.87°C/W, no airflow.

Thermal measurements made in the horizontal position on a
4-layer board.

EXPLANATION OF TEST LEVELS

I   100% Production Tested.

II   100% Production Tested at 25°C, and Sample Tested at
       Specified Temperatures.

III   Sample Tested Only.

IV   Parameter Guaranteed by Design and Analysis.

V   Parameter is Typical Value Only.

VI   100% Production Tested at 25°C, and Sample Tested at
       Temperature Extremes.

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Option
AD6635BB AD6635BB/PCB	–40°C to +85°C	324-Lead PBGA (Ball Grid Array) Evaluation Board with AD6635 and Software	B-324

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily
accumulate on the human body and test equipment and can discharge without detection. Although the
AD6635 features proprietary ESD protection circuitry, permanent damage may occur on devices
subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended
to avoid performance degradation or loss of functionality.

AD6635

19mm × 19mm – 18^2 BALL ZAPHOD PACKAGE

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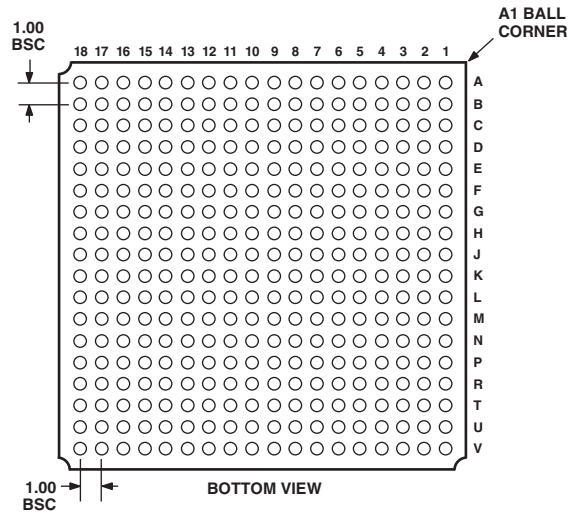
PIN CONFIGURATION (PIN OUT)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A		IENC	INC0	INC7	INC12	IND2	IND3	IND7	IND8	IND11	EXPD1	PDREQ	PD14	PD10	PD8	PD5_LD5	PDCH1_LDCLK_IN		A
B	CLK0	VDDIO (Reserved)	INC1	INC8	INC11	IND1	IND4	IND6	IND9	IND12	EXPD2	PDACK	PD12	PD11	PD4_LD4	PD3_LD3	PD7_LD7	PDCH0_LDCLK_OUT	B
C	CLK1	VDDIO (Reserved)	PAREQ	INC2	INC9	LID-B	IND0	IND5	IND10	IND13	EXPD0	PD15	PD9	PD1_LD1	PD2_LD2	PD0_LD0	SDI4	PDIQ	C
D	PAACK	CHIP0_ID0		LID-A	INC3	INC10	INC13	IEND	EXPC0	VDD	VDD	VDD	PD13	PCACK	CHIP1_ID1	PCIQ	PD6_LD6	PCLK1	D
E	CHIP0_ID1	CHIP0_ID2			INC4	INC5	INC6	EXPC2	EXPC1	VDD	VDD	VDD		VDDIO (Reserved)	DNC	CHIP1_ID0	CHIP1_ID2	SCLK4	E
F	SCLK0	PAIQ		VDD	VDD	VDD	VDDIO	VDDIO	VDDIO	GND	GND	GND	VDDIO	VDDIO	VDDIO	PCREQ	PC14	PC15	F
G	PCLK0	SDI0	PB6_LB6	VDD	VDD	VDD	VDDIO	VDDIO	VDDIO	GND	GND	GND	VDDIO	VDDIO	VDDIO	PC11	PC13	PC12	G
H	PBCH0_LBCLK_OUT	PBIQ	PB7_LB7	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PC10	PC9	DNC	H
J	PBCH1_LBCLK_IN	PB0_LB0	PB3_LB3	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PC8	PC0_LC0	GND (Reserved)	J
K	PB2_LB2	PB4_LB4	PB5_LB5	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PC1_LC1	PC3_LC3	PC2_LC2	K
L	PB11	PB1_LB1	PB8	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	A1	PC5_LC5	PC4_LC4	L
M	PB13	PB9	PB10	VDDIO	VDDIO	VDDIO	VDD	VDD	VDD	VDDIO	VDDIO	VDDIO	VDD	VDD	VDD	PC6_LC6	PC7_LC7	PCCH1_LCCLK_IN	M
N	PB12	PB14	VDDIO (Reserved)	VDDIO	VDDIO	VDDIO	VDD	VDD	VDD	VDDIO	VDDIO	VDDIO	VDD	VDD	VDD	A0	A2	PCCH0_LCCLK_OUT	N
P	PBREQ	PB15	PBACK	PA15	PA14	PA13	PA10	PA12	PA11	PA3_LA3	LIC-A	DNC	DNC	DNC	D7	D0	D1	$\overline{DS}$	P
R	EXPB0	INB10	INB11	INB12	INB13	EXPA0	EXPA2	PA9	PA8	LIC-B	PA5_LA5	$\overline{CS0}$	DNC	D4	D3	$\overline{CS1}$	R/W	VDDIO (Reserved)	R
T	EXPB1	INB9	INB4	INB3	INB0	EXPA1	INA9	INA8	PA0_LA0	PA2_LA2	PA1_LA1	SYNCD	$\overline{DTACK}$	$\overline{RESET}$	PA7_LA7	DNC	D5	D2	T
U	EXPB2	INB8	INB5	INB2	LIB-B	INA13	INA10	INA7	INA5	INA3	INA1	LIA-A	SYNCA	SYNCC	PA6_LA6	PA4_LA4	MODE	D6	U
V		INB7	INB6	INB1	IENB	INA12	INA11	INA6	INA4	INA2	INA0	IENA	LIB-A	LIA-B	SYNCB	PACH0_LACLK_OUT	PACH1_LACLK_IN		V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

AD6635

Name	Type	Function
POWER SUPPLY		
VDD	P	2.5 V Core Supply (also called DVCORE)
VDDIO	P	3.3 V IO Supply (also called DVRING)
GND	G	Ground
INPUTS		
INA[13:0][1]	I	A Input Data (Mantissa)
EXPA[2:0][1]	I	A Input Data (Exponent)
IENA[2]	I	Input Enable—Input A
INB[13:0][1]	I	B Input Data (Mantissa)
EXPB[2:0][1]	I	B Input Data (Exponent)
IENB[2]	I	Input Enable—Input B
INC[13:0][1]	I	C Input Data (Mantissa)
EXPC[2:0][1]	I	C Input Data (Exponent)
IENC[2]	I	Input Enable—Input C
IND[13:0][1]	I	D Input Data (Mantissa)
EXPD[2:0][1]	I	D Input Data (Exponent)
IEND[2]	I	Input Enable—Input D
$\overline{\text{RESET}}$	I	Active Low Reset Pin
CLK0	I	Input Clock 0 (Master Clock for Channels 0–3 and Ports A, B)
CLK1	I	Input Clock 1 (Master Clock for Channels 4–7 and Ports C, D)
PCLK0	I/O	Link/Parallel Port Clock for Output Ports A and B
PCLK1	I/O	Link/Parallel Port Clock for Output Ports C and D
LACLKIN	I	Link Port A Data Ready
LBCLKIN	I	Link Port B Data Ready
LCCLKIN	I	Link Port C Data Ready
LDCLKIN	I	Link Port D Data Ready
SYNCA[1]	I	All Sync Pins Go to All Eight Channels
SYNCB[1]	I	All Sync Pins Go to All Eight Channels
SYNCC[1]	I	All Sync Pins Go to All Eight Channels
SYNCD[1]	I	All Sync Pins Go to All Eight Channels
CHIP0_ID[2:0][1]	I	Chip ID Selector for Channels 0–3 and Ports A, B
CHIP1_ID[2:0][1]	I	Chip ID Selector for Channels 4–7 and Ports C, D
CONTROL		
PAACK	I	Parallel Port A Acknowledge
PAREQ	O	Parallel Port A Request
PBACK	I	Parallel Port B Acknowledge
PBREQ	O	Parallel Port B Request
PCACK	I	Parallel Port C Acknowledge
PCREQ	O	Parallel Port C Request
PDACK	I	Parallel Port D Acknowledge
PDREQ	O	Parallel Port D Request

Name	Type	Function
MICROPORT CONTROL		
D[7:0]	I/O/T	Bidirectional Microport Data
A[2:0]	I	Microport Address Bus
$\overline{DS}$ ($\overline{RD}$)	I	Active Low Data Strobe (Active Low Read)
$\overline{DTACK}$ (RDY)[2]	O/T	Active Low Data Acknowledge (Microport Status Bit)
R/W ($\overline{WR}$)	I	Read Write (Active Low Write)
MODE	I	Intel or Motorola Mode Select
$\overline{CS0}$[1]	I	Chip Select for Channels 0–3 and Ports A, B
$\overline{CS1}$[1]	I	Chip Select for Channels 4–7 and Ports C, D
SERIAL PORT CONTROL		
SDI0[1]	I	Serial Port Control Data Input for Channels 0–3 and Ports A, B
SCLK0[1]	I	Serial Port Control Clock for Channels 0–3 and Ports A, B
SDI4[1]	I	Serial Port Control Data Input for Channels 4–7 and Ports C, D
SCLK4[1]	I	Serial Port Control Clock for Channels 4–7 and Ports C, D
OUTPUTS		
LIA-A	O	Level Indicator—Input A, Interleaved-Data A
LIA-B	O	Level Indicator—Input A, Interleaved-Data B
LIB-A	O	Level Indicator—Input B, Interleaved-Data A
LIB-B	O	Level Indicator—Input B, Interleaved-Data B
LIC-A	O	Level Indicator—Input C, Interleaved-Data A
LIC-B	O	Level Indicator—Input C, Interleaved-Data B
LID-A	O	Level Indicator—Input D, Interleaved-Data A
LID-B	O	Level Indicator—Input D, Interleaved-Data B
LACLKOUT	O	Link Port A Clock Output
LBCLKOUT	O	Link Port B Clock Output
LCCLKOUT	O	Link Port C Clock Output
LDCLKOUT	O	Link Port D Clock Output
LA[7:0]	O	Link Port A Output Data
LB[7:0]	O	Link Port B Output Data
LC[7:0]	O	Link Port C Output Data
LD[7:0]	O	Link Port D Output Data
PA[15:0]	O	Parallel Output Data Port A
PB[15:0]	O	Parallel Output Data Port B
PC[15:0]	O	Parallel Output Data Port C
PD[15:0]	O	Parallel Output Data Port D
PACH[1:0]	O	Parallel Output Port A Channel Indicator
PBCH[1:0]	O	Parallel Output Port B Channel Indicator
PCCH[1:0]	O	Parallel Output Port C Channel Indicator
PDCH[1:0]	O	Parallel Output Port D Channel Indicator
PAIQ	O	Parallel Port A I/Q Data Indicator
PBIQ	O	Parallel Port B I/Q Data Indicator
PCIQ	O	Parallel Port C I/Q Data Indicator
PDIQ	O	Parallel Port D I/Q Data Indicator

NOTES
[1]Pins with a pull-down resistor of nominal 70 kΩ.
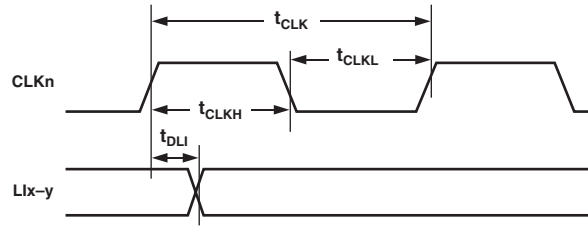[2]Pins with a pull-up resistor of nominal 70 kΩ.

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TIMING DIAGRAMS

*Figure 3. Level Indicator Output Switching Characteristics (x = A, B, C, D; and y = A, B)
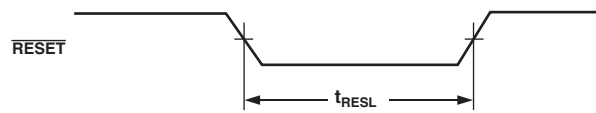(For x = A and B, n = 0; and for x = C or D, n = 1)*

Figure 4. Reset Timing Requirements

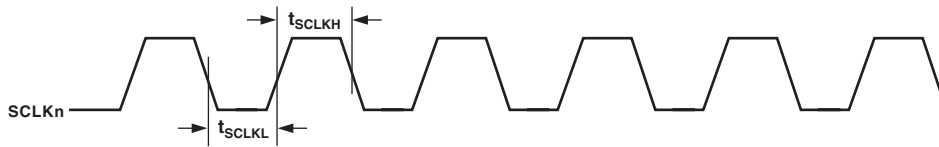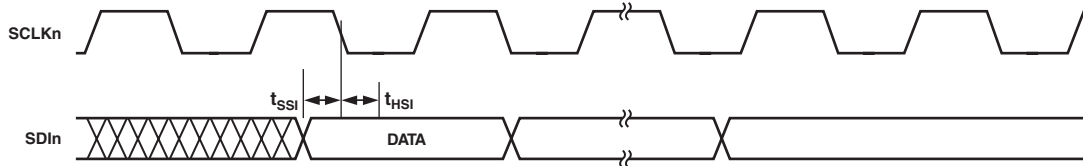*Figure 5. SCLK Switching Characteristics (n = 0, 4)*

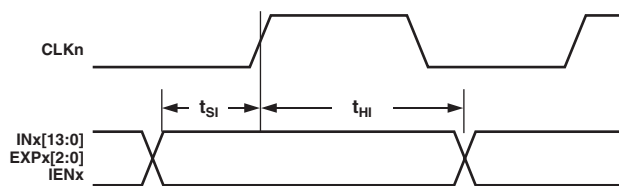*Figure 6. Serial Port Input Timing Characteristics (n = 0, 4)*

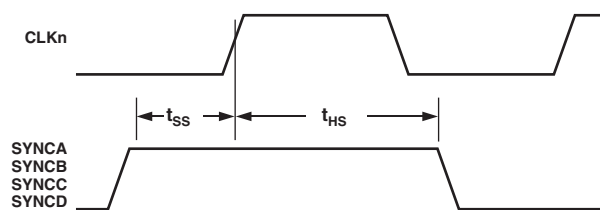REV. 0

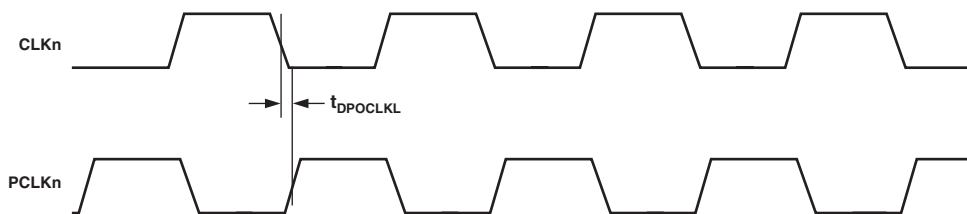Figure 7. Input Timing for A and B Channels

Figure 8. SYNC Timing Inputs

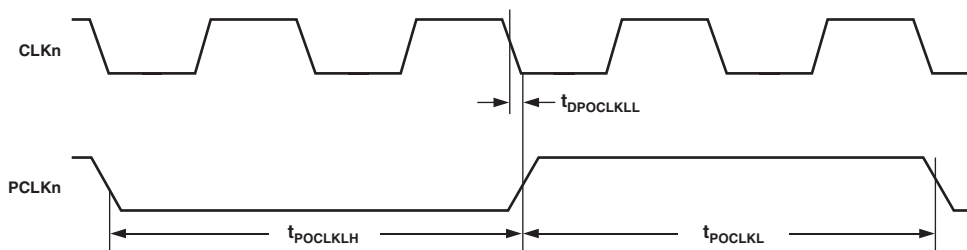Figure 9. PCLKn to CLKn Switching Characteristics Divide by 1

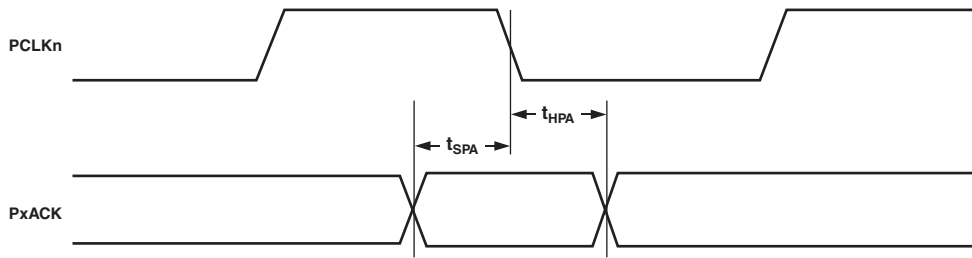Figure 10. PCLKn to CLKn Switching Characteristics Divide by 2, 4, or 8

Figure 11. Master Mode PxACK to PCLKn Setup and Hold Characteristics
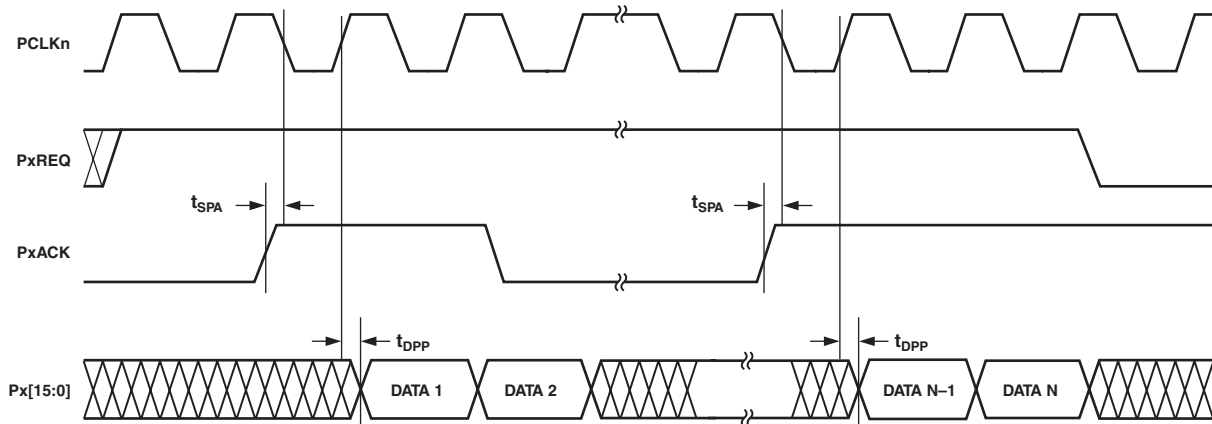(n = 0 and x = A, B; or n = 1 and x = C, D)

Figure 12. Master Mode PxACK to PCLKn Switching Characteristics
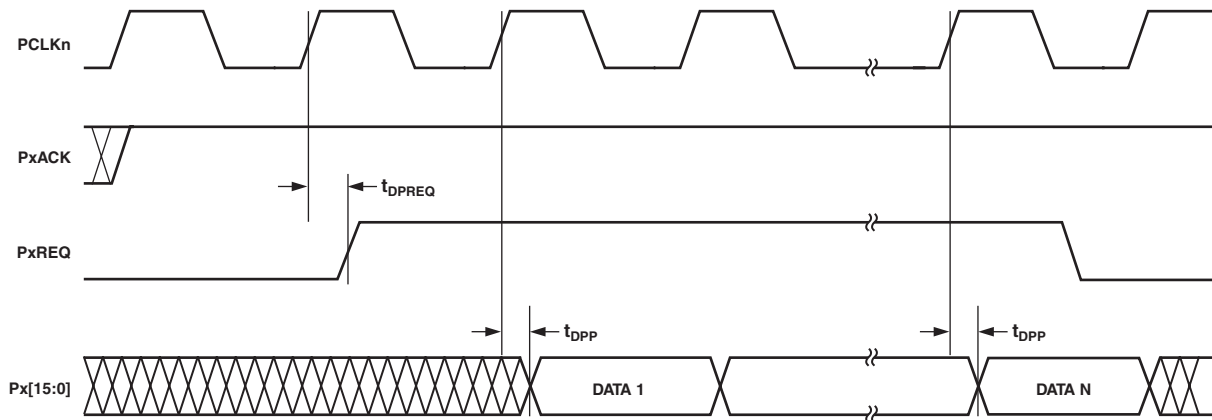(n = 0 and x = A, B; or n = 1 and x = C, D)

Figure 13. Master Mode PxREQ to PCLKn Switching Characteristics
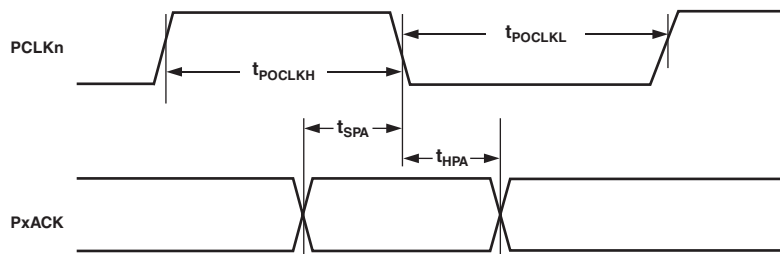(n = 0 and x = A, B; or n = 1 and x = C, D)

Figure 14. Slave Mode PxACK to PCLKn Setup and Hold Characteristics
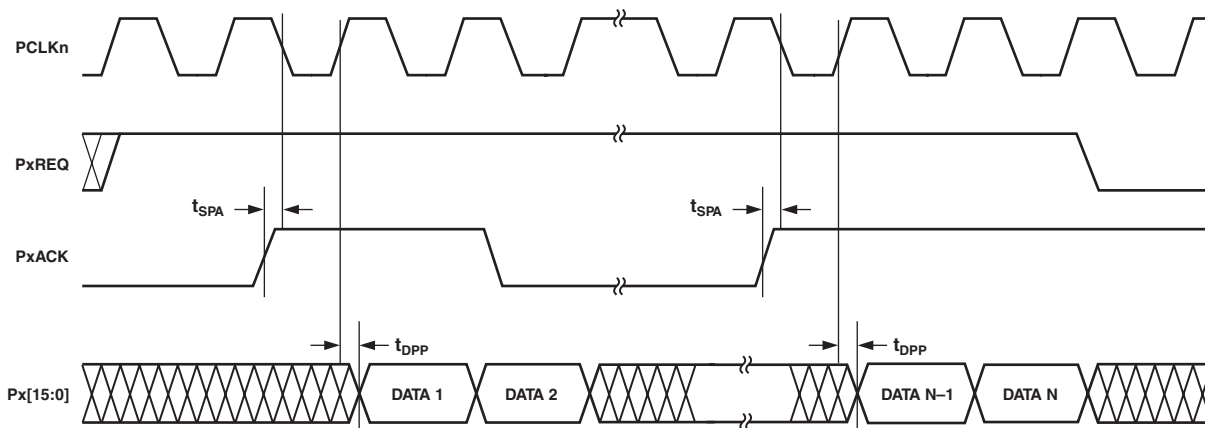(n = 0 and x = A, B; or n = 1 and x = C, D)

Figure 15. Slave Mode PxACK to PCLKn Switching Characteristics
(n = 0 and x = A, B; or n = 1 x = C, D)

Figure 16. Slave Mode PxREQ to PCLKn Switching Characteristics
(n = 0 and x = A, B; or n = 1 and x = C, D)

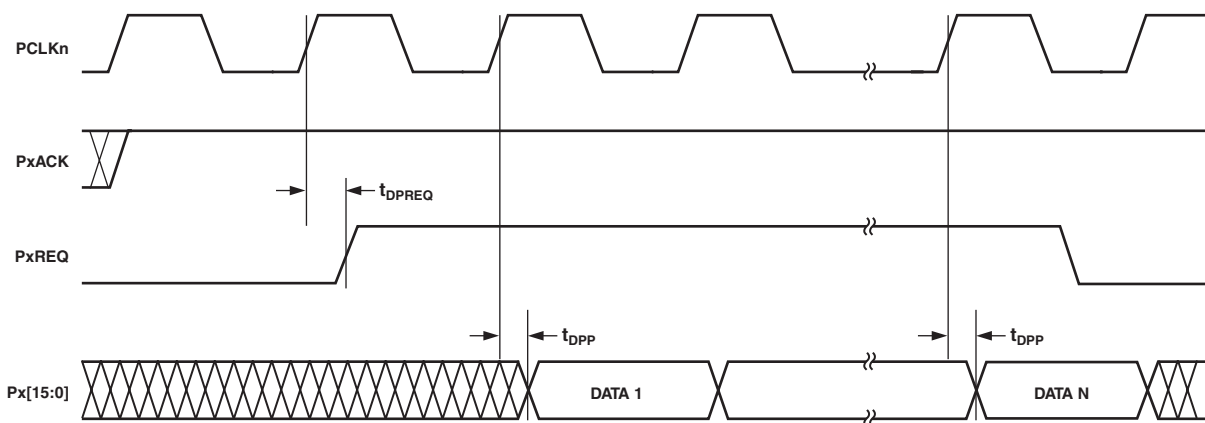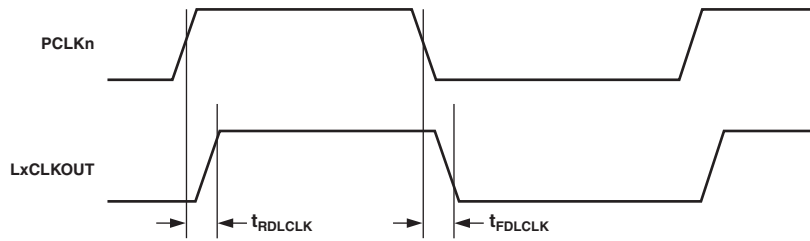# AD6635

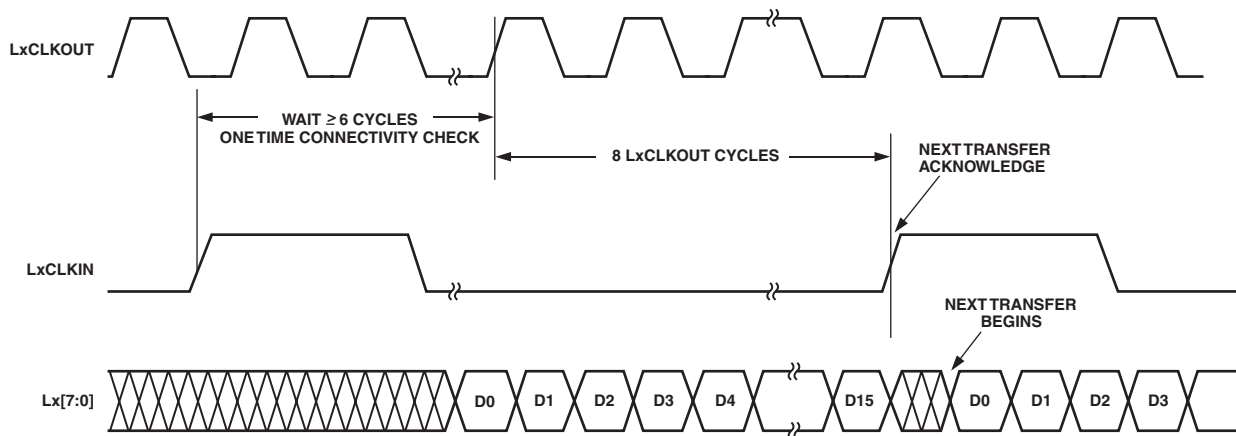Figure 17. LxCLKOUT to PCLKn (n = 0 and x = A, B; or n = 1 and x = C, D) Switching Characteristics

Figure 18. LxCLKIN to LxCLKOUT Data Switching Characteristics
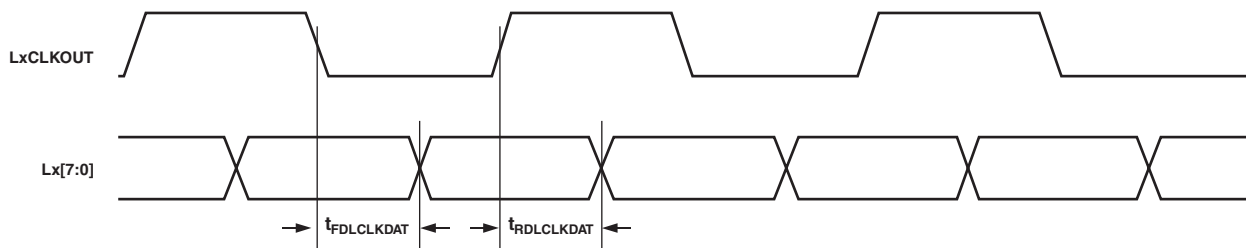
Figure 19. LxCLKOUT to Lx[7:0] Data Switching Characteristics

REV. 0

TIMING DIAGRAMS – INM Microport Mode (MODE = 0)
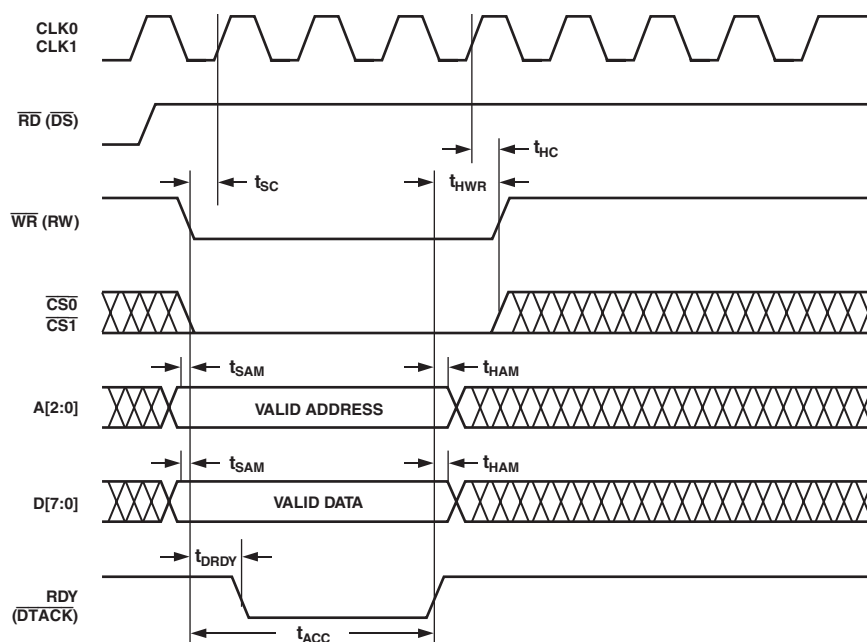
NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED
FROM FE OF $\overline{WR}$ TO RE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF 9 CLK PERIODS.

Figure 20. INM Microport Write Timing Requirements. CLK0 corresponds to $\overline{CS0}$, and CLK1 to $\overline{CS1}$. $\overline{CS0}$ and $\overline{CS1}$ both active (low) at the same time will cause errors in writing.
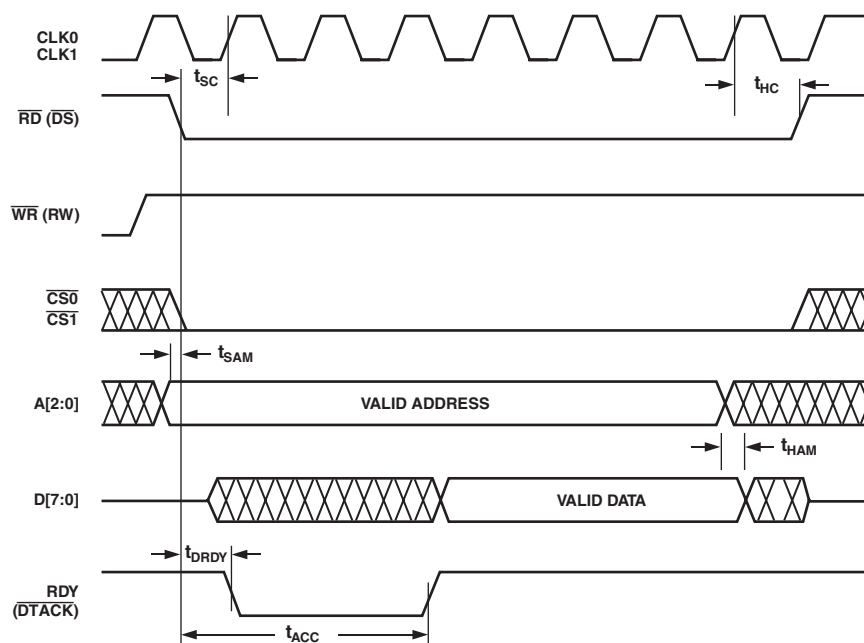
NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED
FROM FE OF $\overline{WR}$ TO RE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS AND APPLIES TO A[2:0] = 7, 6, 5, 3, 2, 1.

Figure 21. INM Microport Read Timing Requirements. CLK0 corresponds to $\overline{CS0}$, and CLK1 to $\overline{CS1}$. $\overline{CS0}$ and $\overline{CS1}$ both active (low) at the same time will cause contention on data bus.

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TIMING DIAGRAMS – MNM Microport Mode (MODE = 1)

NOTES
1. **t$_{ACC}$** ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{DS}$ TO THE FE OF $\overline{DTACK}$.
2. **t$_{ACC}$** REQUIRES A MAXIMUM OF 9 CLK PERIODS.

Figure 22. MNM Microport Write Timing Requirements. CLK0 corresponds to $\overline{CS0}$, and CLK1 to $\overline{CS1}$. $\overline{CS0}$ and $\overline{CS1}$ both active (low) at the same time will cause errors in writing.

NOTES
1. **t$_{ACC}$** ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM THE FE OF $\overline{DS}$ TO THE FE OF $\overline{DTACK}$.
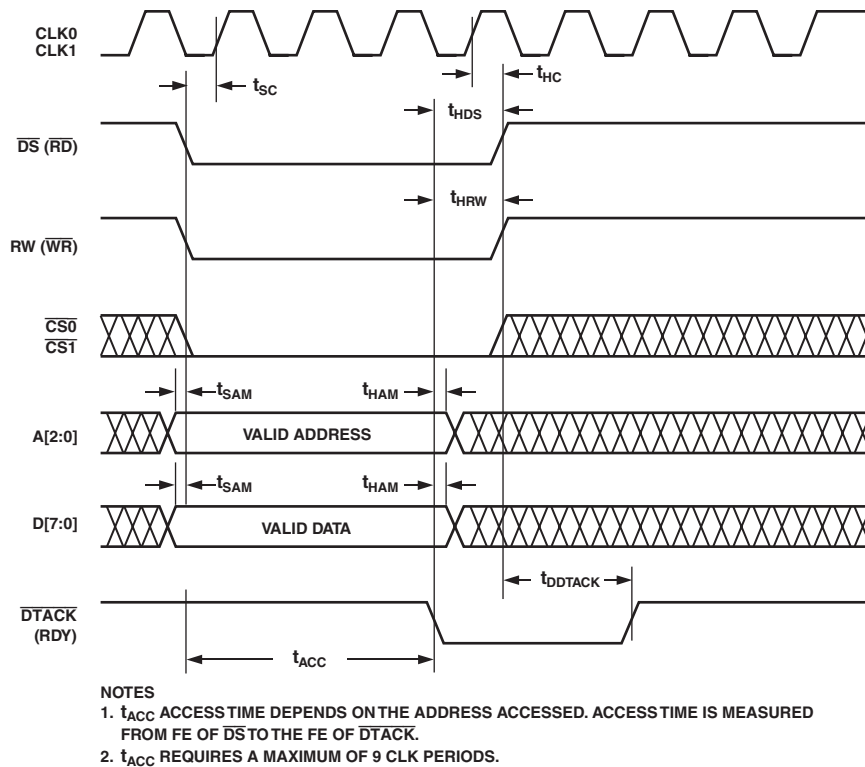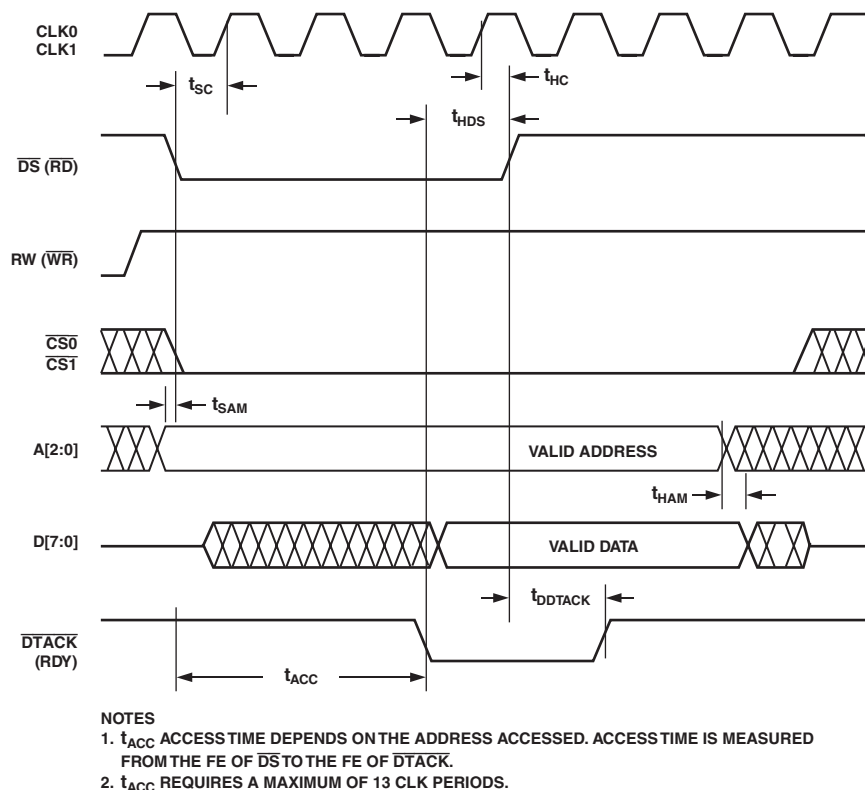2. **t$_{ACC}$** REQUIRES A MAXIMUM OF 13 CLK PERIODS.

Figure 23. MNM Microport Read Timing Requirements. CLK0 corresponds to $\overline{CS0}$, and CLK1 to $\overline{CS1}$. $\overline{CS0}$ and $\overline{CS1}$ both active (low) at the same time will cause contention on data bus.

REV. 0

INPUT DATA PORTS

The AD6635 features four high speed ADC Input Ports, A, B, C, and D. The input ports allow for the most flexibility with a single tuner chip. These can be diversity inputs or truly independent inputs such as separate antenna segments. Channels 0 through 3 can take data from either of the input ports A or B independently. Similarly, Channels 4 through 7 can take data from either of the Input Ports C or D independently. For added flexibility, each input port can be used to support multiplexed inputs, such as found on the AD6600 or other ADCs with multiplexed outputs. This added flexibility allows up to eight different analog sources to be processed simultaneously by the eight internal AD6635 channels.

In addition, the front end of the AD6635 contains circuitry that enables high speed signal level detection and control. This is accomplished with a unique high speed level detection circuit that offers minimal latency and maximum flexibility to control up to four analog signal paths. The overall signal path latency from input to output on the AD6635 can be expressed in high speed clock cycles. The equation below can be used to calculate the latency.

$$T_{LATENCY} = M_{rCIC2}(M_{CIC5} + 7) + N_{TAPS} + 26$$

M_{rCIC2} and M_{CIC5} are decimation values for the rCIC2 and CIC5 filters, respectively. N_{TAPS} is the number of RCF taps chosen.

Input Data Format

Each input port consists of a 14-bit mantissa and 3-bit exponent. If interfacing to a standard ADC, the exponent bits can be grounded. If connected to a floating point ADC, such as the AD6600, the exponent bits from that ADC product can be connected to the input exponent bits of the AD6635. The mantissa data format is twos complement, and the exponent is unsigned binary.

Input Timing

The data from each high speed input port is latched on the rising edge of CLK. This clock signal is used to sample the input port and clock the synchronous signal processing stages that follow in the selected channels.
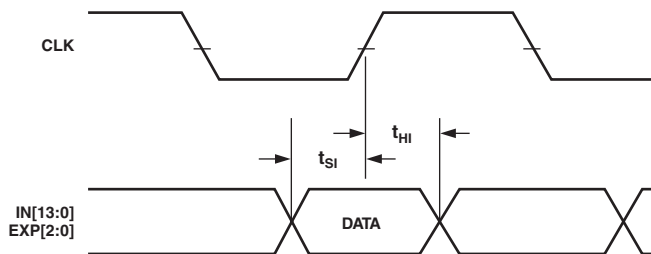

Figure 24. Input Data Timing Requirements

The clock signals can operate up to 80 MHz and have a 50% duty cycle. In applications using high speed ADCs, the ADC sample clock or data valid strobe is typically used to clock the AD6635.
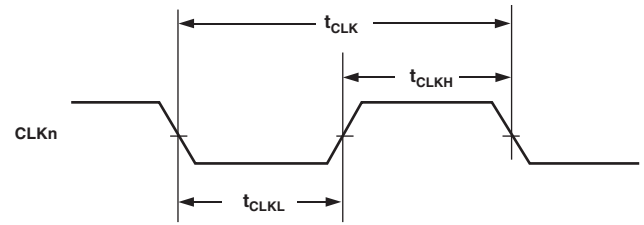

Figure 25. CLKn Timing Requirements (n = 0, 1)

Input Enable Control

There are four Input Enable pins IENx (x = A, B, C, or D) corresponding to individual Input Ports A through D. There are four modes of operation possible while using each IEN pin. Using these modes, it is possible to emulate operation of the other RSPs such as the AD6620, which offer dual channel modes normally associated with diversity operations. These modes are IEN transition to Low, IEN transition to High, IEN High, and Blank on IEN Low.

In the IEN High mode, the inputs and normal operations occur when the Input Enable is High. In the IEN transition to Low mode, normal operations occur on the first rising edge of the clock after the IEN transitions to Low. Likewise in the IEN transition to High mode, operations occur on the rising edge of the clock after the IEN transitions to High. See the numerically Controlled Oscillator section for more details on configuring the Input Enable Modes. In Blank on IEN Low mode, the input data is interpreted as zero when IEN is low.

A typical application for input modes would be to take the data from an AD6600 Diversity ADC to one of the inputs of the AD6635. The A/B_OUT from that chip would be tied to the IEN of the corresponding input port. Then one channel within the AD6635 would be set so that IEN transition to Low is enabled. Another channel would be configured so that IEN transition to High is enabled. This would allow two of the AD6635 channels to be configured to emulate that AD6620 in diversity mode and receive interleaved input data. Though the NCO frequencies and other channel characteristics would need to be set similarly, this feature allows the AD6635 to handle interleaved data streams such as found on the AD6600.

The difference between the IEN transition to High and the IEN High is found when a system clock is provided that is higher than the data rate of the converter. It is often advantageous to supply a clock that runs faster than the data rate so that additional filter taps can be computed. This indeed leads to better filtering. To ensure that other parts of the circuit properly recognize the faster clock in the simplest manner, the IEN transition to Low or High should be used. In this mode, only the first clock edge that meets the setup and hold times will be used to latch and process the input data. All other clocks pulses are ignored by front end processing. However, each clock cycle will still produce a new filter computation pair.

Gain Switching

The AD6635 includes circuitry that is useful in applications where either large dynamic ranges exist, or where gain ranging converters are employed. This circuitry allows digital thresholds to be set such that an upper and a lower threshold can be programmed. One such use of this may be to detect when an ADC is about to reach full scale with a particular input condition. The results

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would be to provide a flag that could be used to quickly insert an attenuator that would prevent ADC overdrive. If 18 dB (or any other arbitrary value) of attenuation is switched in, then the signal dynamic range of the system will have been increased by 18 dB. The process begins when the input signal reaches the upper programmed threshold. In a typical application, this may be set 1 dB (user definable) below full scale. When this input condition is met, the appropriate LI signal (LIA-A, LIB-A, LIC-A, or LID-A) associated with its corresponding input port (A through D) is made active. This can be used to switch the gain or attenuation of the external circuit. The LI line stays active until the input condition falls below the lower programmed threshold. To provide hysteresis, a dwell time register (see Memory Map for Input Control Registers) is available to hold off switching of the control line for a predetermined number of clocks. Once the input condition is below the lower threshold, the programmable counter begins counting high speed clocks. As long as the input signal stays below the lower threshold for the number of high speed clock cycles programmed, the attenuator will be removed on the terminal count. However, if the input condition goes above the lower threshold with the counter running, the counter is reset and input must fall below the lower threshold again to initiate the process. This will prevent unnecessary switching between states.

This is illustrated in Figure 26. When the input signal goes above the upper threshold, the appropriate LI signal becomes active. Once the signal falls below the lower threshold, the counter begins counting. If the input condition goes above the lower threshold, the counter is reset and starts again as shown. Once the counter has terminated to 0, the LI line goes inactive.
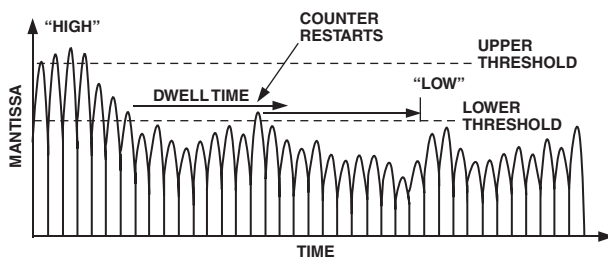

Figure 26. Threshold Settings for LI

The LI line can be used for a variety of functions. It can be used to set the controls of an attenuator, DVGA, or it can be integrated and used with an analog VGA. To simplify the use of this feature, the AD6635 includes two separate gain settings, one when this LI line is inactive (rCIC2_QUIET[4:0] stored in Bits 9:5 of 0x92 register) and the other when active (rCIC2_LOUD[4:0] stored in Bits 4:0 of 0x92 register). This allows the digital gain to be adjusted to the external changes. In conjunction with the gain setting, a variable holdoff is included to compensate for the pipeline delay of the ADC and the switching time of the gain control element. Together, these two features provide seamless gain switching.

Another use of this pin is to facilitate a gain-range holdoff within a gain-ranging ADC. For converters that use gain-ranging to increase total signal dynamic range, it may be desirable to prohibit internal gain ranging from occurring in some instances. For such converters, the LI (A or B) line can be used to hold this off. For this application, the upper threshold would be set based on similar criteria. However, the lower threshold would be set to a level

consistent with the gain ranges of the specific converter. Then the holdoff delay can be set appropriately for any of a number of factors, such as fading profile, signal peak-to-average ratio, or any other time based characteristics that might cause unnecessary gain changes.

The AD6635 has a total of eight gain control circuits to support all channels, and hence can be used even when all input ports have interleaved data. When data is interleaved on a certain input port, the appropriate bit should be set in the Gain Range Control Register. This way both interleaved channel data can be monitored, and LIA-B, LIB-B, LIC-B, or LID-B pins associated with their corresponding Input Ports A through D act as output indicators for the interleaved channel. LIx-A pins act as indicators for input data corresponding to IENx Low, and LIx-B act as indicators for input data corresponding to IENx High in this mode. When interleaved channels are not used, LIx-B pins are complimentary to LIx-A pins acting as indicators with opposite polarity. It should be noted that the gain control circuits are wideband and are implemented prior to any filtering elements to minimize loop delay.

The chip also provides appropriate scaling of the internal data based on the attenuation associated with the LI signal. In this manner, data to the DSP maintains a correct scale value throughout the process, making it entirely independent. Since there often are finite delays associated with external gain switching components, the AD6635 includes a variable pipeline delay that can be used to compensate for external pipeline delays or gross settling times associated with gain/attenuator devices. This delay may be set for up to seven high speed clocks. These features ensure smooth switching between gain settings.

Input Data Scaling
The AD6635 has four data input ports. Each accepts a 14-bit mantissa (twos complement integer) IN[13:0], a 3-bit exponent (unsigned integer) EXP[2:0], and the Input Enable(IEN). Input Ports A and B are clocked by CLK0 and Input Ports C and D are clocked by CLK1. These pins allow direct interfacing to both standard fixed-point ADCs such as the AD9238 and AD6645, as well as to gain-ranging ADCs such as the AD6600. For normal operation with ADCs having fewer than 14 bits, the active bits should be MSB justified and the unused LSBs should be tied low.

The 3-bit exponent, EXP[2:0] is interpreted as an unsigned integer. The exponent will subsequently be modified by either of rCIC2_LOUD[4:0] or rCIC2_QUIET[4:0], depending on whether the LI line is active or not. These 5-bit scale values are stored in the rCIC2 scale register (0x92) and the scaling is applied before the data enters the rCIC2 resampling filter. These 5-bit registers contain scale values to compensate for the rCIC2 gain, external attenuator (if used), and the Exponent Offset (Expoff). If no external attenuator is used, both the rCIC2_QUIET and rCIC2_LOUD registers contain the same value. A detailed explanation and equation for setting the attenuating scale register is given in the Scaling with Floating-Point ADCs section.

Scaling with Fixed-Point ADCs
For fixed-point ADCs the AD6635 exponent inputs, EXP[2:0], are typically not used and should be tied low. The ADC outputs are tied directly to the AD6635 inputs, MSB-justified. The ExpOff bits in 0x92 should be programmed to 0. Likewise, the Exponent Invert bit should be 0. Thus for fixed-point ADCs, the exponents are typically static and no input scaling is used in the AD6635.
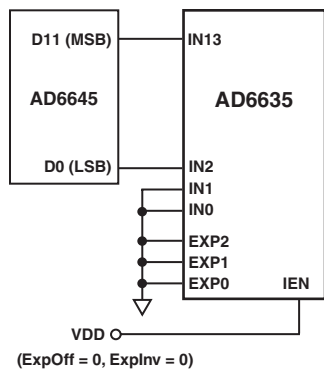
Figure 27. Typical Interconnection of the AD6645
Fixed-Point ADC and the AD6635

Scaling with Floating-Point or Gain-Ranging ADCs

An example of the exponent control feature combines the AD6600 and the AD6635. The AD6600 is an 11-bit ADC with 3 bits of gain ranging. In effect, the 11-bit ADC provides the mantissa, and the 3 bits of relative signal strength indicator (RSSI) for the exponent. Only five of the eight available steps are used by the AD6600. See the AD6600 data sheet for additional details.

For gain-ranging ADCs such as the AD6600,

$$scaled\_input = in \times 2^{-\bmod(7-Exp+rCIC2,\ 32)}$$

ExpInv = 1, ExpWeight = 0

where IN is the value of IN[13:0], Exp is the value of EXP[2:0], and rCIC2 is the rCIC scale register value (0x92 bits 9-5 and 4-0). "mod" is the remainder function. For example, mod(1,32) = 1, mod(2,32) = 2, and mod(34,32) = 2.

The RSSI output of the AD6600 grows numerically with increasing signal strength of the analog input (RSSI = 5 for a large signal, RSSI = 0 for a small signal). When the Exponent Invert Bit (ExpInv) is set to zero, the AD6635 will consider the smallest signal at the IN[13:0] to be the largest, and as the EXP word increases, it shifts the data down internally (EXP = 5 will shift a 14-bit word to the right by 5 internal bits before passing the data to the rCIC2). In this example, if ExpInv = 0, the AD6635 regards the RSSI[2:0] = 5 as smallest signal and RSSI[2:0] = 0 as the largest signal possible on the AD6600. Thus, we can use the Exponent Invert Bit to make the AD6635 exponent agree with the AD6600 RSSI. Setting ExpInv = 1 forces the AD6635 to shift the data up (left) for growing EXP instead of down. The exponent invert bit should always be set high for use with the AD6600.

The Exponent Offset is used to shift the data up. For example, Table I shows that with no rCIC2 scaling, 12 dB of range is lost when the ADC input is at the largest level. This is not desired because it lowers the dynamic range and SNR of the system by reducing the signal of interest relative to the quantization noise floor.

**Table I. AD6600 Transfer Function with
AD6635 ExpInv = 1, and no ExpOff**

ADC Input Level	AD6600 RSSI[2:0]	AD6635 Data	Signal Reduction (dB)
Largest	101 (5)	/4 (>> 2)	–12
	100 (4)	/8 (>>3)	–18
	011 (3)	/16 (>> 4)	–24
	010 (2)	/32 (>> 5)	–30
	001 (1)	/64 (>> 6)	–36
Smallest	000 (0)	/128(>> 7)	–42

ExpInv = 1, rCIC2 Scale = 0)

To avoid this automatic attenuation of the full-scale ADC signal, the ExpOff is used to move the largest signal (RSSI = 5) up to the point where there is no downshift. In other words, once the Exponent Invert bit has been set, the Exponent Offset should be adjusted so that mod(7-5 + ExpOff,32) = 0. This is the case when Exponent Offset is set to 30 since mod(32,32) = 0. Table II illustrates the use of ExpInv and ExpOff when used with the AD6600 ADC.

**Table II. AD6600 Transfer Function with
AD6620 ExpInv = 1, and ExpOff = 30**

ADC Input Level	AD6600 RSSI[2:0]	AD6635 Data	Signal Reduction (dB)
Largest	101 (5)	/1 (>> 0)	0
	100 (4)	/2 (>>1)	–6
	011 (3)	/4 (>> 2)	–12
	010 (2)	/8 (>> 3)	–18
	001 (1)	/16 (>> 4)	–24
Smallest	000 (0)	/32(>> 5)	–30

ExpInv = 1, ExpOff = 30, Exp Weight = 0)

This flexibility in handling the exponent allows the AD6635 to interface with other gain-ranging ADCs besides the AD6600. The Exponent Offset can be adjusted to allow up to seven RSSI(EXP) ranges to be used as opposed to the AD6600's five. It also allows the AD6635 to be tailored in a system that employs the AD6600 but does not utilize all of its signal range. For example, if only the first four RSSI ranges are expected to occur, then the ExpOff could be adjusted to 29, which would make RSSI = 4 correspond to the 0 dB point of the AD6635.

Note that the above scale factor set in the rCIC2 register is only to account for the ExpOff required. This register should also account for compensating rCIC2 filter gain. The value required for this will be given in the CIC2 filter section. Hence the final value set in the rCIC2 register will be the sum total of ExpOff and rCIC2 scale required.