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Dual IF Receiver

AD6642

FEATURES

- 11-bit, 200 MSPS output data rate per channel
- Integrated noise shaping requantizer (NSR)
- Performance with NSR enabled
  - SNR: 75.5 dBFS in 40 MHz band to 70 MHz @ 185 MSPS
  - SNR: 73.7 dBFS in 60 MHz band to 70 MHz @ 185 MSPS
- Performance with NSR disabled
  - SNR: 66.5 dBFS to 70 MHz @ 185 MSPS
  - SFDR: 83 dBc to 70 MHz @ 185 MSPS
- Low power: 0.62 W @ 185 MSPS
- 1.8 V analog supply operation
- 1.8 V LVDS (ANSI-644 levels) output
- 1-to-8 integer clock divider
- Internal ADC voltage reference
- 1.75 V p-p analog input range (programmable to 2.0 V p-p)
- Differential analog inputs with 800 MHz bandwidth
- 95 dB channel isolation/crosstalk
- Serial port control
- User-configurable built-in self-test (BIST) capability
- Energy-saving power-down modes

APPLICATIONS

- Communications
- Diversity radio and smart antenna (MIMO) systems
- Multimode digital receivers (3G)
  - WCDMA, LTE, CDMA2000
  - WiMAX, TD-SCDMA
- I/Q demodulation systems
- General-purpose software radios

FUNCTIONAL BLOCK DIAGRAM

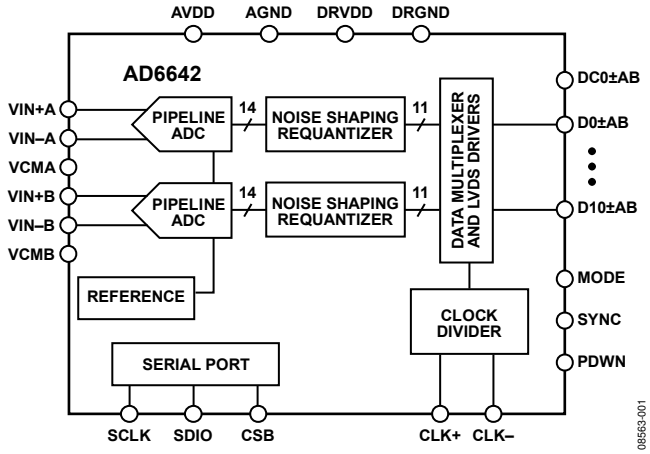

Figure 1.

PRODUCT HIGHLIGHTS

1. Two ADCs are contained in a small, space-saving, 10 mm × 10 mm × 1.4 mm, 144-ball CSP_BGA package.
2. Pin selectable noise shaping requantizer (NSR) function that allows for improved SNR within a reduced bandwidth of up to 60 MHz at 185 MSPS.
3. LVDS digital output interface configured for low cost FPGA families.
4. 120 mW per ADC core power consumption.
5. Operation from a single 1.8 V supply.
6. Standard serial port interface (SPI) that supports various product features and functions, such as data formatting (offset binary or twos complement), NSR, power-down, test modes, and voltage reference mode.
7. On-chip integer 1-to-8 input clock divider and multichip sync function to support a wide range of clocking schemes and multichannel subsystems.

Rev. A

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AD6642* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD6642 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD6642: Dual IF Receiver Data Sheet

User Guides

- UG-232: Evaluating the AD6642/AD6657 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog

DESIGN RESOURCES

- AD6642 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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7/10—Rev. 0 to Rev. A

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10/09—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD6642 is an 11-bit, 200 MSPS, dual-channel intermediate frequency (IF) receiver specifically designed to support multi-antenna systems in telecommunication applications where high dynamic range performance, low power, and small size are desired.

The device consists of two high performance analog-to-digital converters (ADCs) and noise shaping requantizer (NSR) digital blocks. Each ADC consists of a multistage, differential pipelined architecture with integrated output error correction logic. The ADC features a wide bandwidth switched-capacitor sampling network within the first stage of the differential pipeline. An integrated voltage reference eases design considerations. A duty cycle stabilizer (DCS) compensates for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

Each ADC output is connected internally to an NSR block. The integrated NSR circuitry allows for improved SNR performance in a smaller frequency band within the Nyquist bandwidth. The device supports two different output modes selectable via the external MODE pin or the SPI.

With the NSR feature enabled, the outputs of the ADCs are processed such that the AD6642 supports enhanced SNR performance within a limited portion of the Nyquist bandwidth while maintaining an 11-bit output resolution. The NSR block can be programmed to provide a bandwidth of either 22% or 33% of the sample clock. For example, with a sample clock rate of 185 MSPS, the AD6642 can achieve up to 75.5 dBFS SNR for a 40 MHz bandwidth in the 22% mode and up to 73.7 dBFS SNR for a 60 MHz bandwidth in the 33% mode.

With the NSR block disabled, the ADC data is provided directly to the output with a resolution of 11 bits. The AD6642 can achieve up to 66.5 dBFS SNR for the entire Nyquist bandwidth when operated in this mode. This allows the AD6642 to be used in telecommunication applications such as a digital predistortion observation path where wider bandwidths are desired.

After digital signal processing, multiplexed output data is routed into two 11-bit output ports such that the maximum data rate is 400 Mbps (DDR). These outputs are set at 1.8 V LVDS and support ANSI-644 levels.

The AD6642 receiver digitizes a wide spectrum of IF frequencies. Each receiver is designed for simultaneous reception of a separate antenna. This IF sampling architecture greatly reduces component cost and complexity compared with traditional analog techniques or less integrated digital methods.

Flexible power-down options allow significant power savings. Programming for device setup and control is accomplished using a 3-wire SPI-compatible serial interface with numerous modes to support board-level system testing.

The AD6642 is available in a Pb-free/RoHS compliant, 144-ball, 10 mm × 10 mm chip scale package ball grid array (CSP_BGA) and is specified over the industrial temperature range of −40°C to +85°C.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, f_S = 185 MSPS, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and default SPI, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	11			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−4.5	2	7.4	mV
Gain Error	Full		±3	±7	% FSR
Differential Nonlinearity (DNL)[1]	Full		±0.1	±0.5	LSB
Integral Nonlinearity (INL)[1]	Full		±0.2	±0.5	LSB
MATCHING CHARACTERISTIC					
Offset Error	Full	−2.4	2.5	8.3	mV
Gain Error	Full		±1	±3	% FSR
TEMPERATURE DRIFT					
Offset Error	Full		2		ppm/°C
Gain Error	Full		40		ppm/°C
ANALOG INPUT					
Input Range	Full	1.4	1.75	2.0	V p-p
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	Full		20		kΩ
Input Capacitance[2]	Full		5		pF
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
Supply Current					
I_{AVDD}[1]	Full		265	291	mA
I_{DRVDD}[1] (1.8 V LVDS)	Full		79	89	mA
POWER CONSUMPTION					
Sine Wave Input[1]	Full		619	684	mW
Standby Power[3]	Full		83		mW
Power-Down Power	Full		4.5	18	mW

[1] Measured with a 10 MHz, 0 dBFS sine wave, with 100 Ω termination on each LVDS output pair.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Standby power is measured with a dc input and the CLKx pins inactive (set to AVDD or AGND).

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, f_S = 185 MSPS, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and default SPI, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE-RATIO (SNR)—NSR DISABLED					
f_{IN} = 30 MHz	25°C		66.5		dBFS
f_{IN} = 70 MHz	25°C		66.5		dBFS
f_{IN} = 170 MHz	Full	65.7	66.1		dBFS
f_{IN} = 250 MHz	25°C		65.5		dBFS
SIGNAL-TO-NOISE-RATIO (SNR)—NSR ENABLED					
22% BW Mode					
f_{IN} = 70 MHz	25°C		75.5		dBFS
f_{IN} = 170 MHz	Full	72.8	74.4		dBFS
f_{IN} = 230 MHz	25°C		72.8		dBFS
33% BW Mode					
f_{IN} = 70 MHz	25°C		73.7		dBFS
f_{IN} = 170 MHz	Full	71.0	72.6		dBFS
f_{IN} = 230 MHz	25°C		71.0		dBFS
SIGNAL-TO-NOISE-AND DISTORTION (SINAD)					
f_{IN} = 30 MHz	25°C		65.5		dBFS
f_{IN} = 70 MHz	25°C		66.3		dBFS
f_{IN} = 170 MHz	Full	64.1	65.6		dBFS
f_{IN} = 250 MHz	25°C		64.3		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 30 MHz	25°C		10.6		Bits
f_{IN} = 70 MHz	25°C		10.7		Bits
f_{IN} = 170 MHz	Full	10.3	10.6		Bits
f_{IN} = 250 MHz	25°C		10.3		Bits
WORST SECOND OR THIRD HARMONIC					
f_{IN} = 30 MHz	25°C		−90		dBc
f_{IN} = 70 MHz	25°C		−83		dBc
f_{IN} = 170 MHz	Full	−72	−78		dBc
f_{IN} = 250 MHz	25°C		−80		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 30 MHz	25°C		90		dBc
f_{IN} = 70 MHz	25°C		83		dBc
f_{IN} = 170 MHz	Full	72	78		dBc
f_{IN} = 250 MHz	25°C		80		dBc
WORST OTHER HARMONIC (FOURTH THROUGH EIGHTH)					
f_{IN} = 30 MHz	25°C		−100		dBc
f_{IN} = 70 MHz	25°C		−96		dBc
f_{IN} = 170 MHz	Full	−82	−90		dBc
f_{IN} = 250 MHz	25°C		−95		dBc
TWO-TONE SFDR (−7 dBFS)					
f_{IN1} = 169 MHz, f_{IN2} = 172 MHz	25°C		82		dBc
CROSSTALK[2]	Full		95		dB
ANALOG INPUT BANDWIDTH	25°C		800		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 155 MHz with −1 dBFS on one channel and no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, f_S = 185 MSPS, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and default SPI, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.2		3.6	V p-p
Input Voltage Range	Full	AGND – 0.3		AVDD + 0.2	V
High Level Input Voltage	Full	1.2		2.0	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full	8	10	12	kΩ
Input Capacitance	Full		4		pF
SYNC INPUT					
Logic Compliance			CMOS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Resistance	Full	12	16	20	kΩ
Input Capacitance	Full		1		pF
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
LOGIC INPUT (MODE)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA

Parameter	Temperature	Min	Typ	Max	Unit
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (PDWN)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−90		−134	μA
Low Level Input Current	Full	−10		+10	μA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS (LVDS)					
Differential Output Voltage (V_{OD})	Full	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, f_S = 185 MSPS, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and default SPI, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS					
Input Clock Rate	Full			625	MHz
Conversion Rate[1]	Full	40	185	200	MSPS
CLK Pulse Width High (t_{CH})	Full		2.7		ns
Aperture Delay (t_A)	Full		1.3		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.13		ps rms
DATA OUTPUT PARAMETERS					
Data Propagation Delay (t_{PD})	Full	3.0	4.35	5.7	ns
DCO Propagation Delay (t_{DCO})	Full	3.2	4.55	5.9	ns
DCO to Data Skew (t_{SKEW})	Full	−0.4	−0.2	0	ns
Pipeline Delay (Latency)	Full		9		Cycles
With NSR Enabled	Full		12		Cycles
Wake-Up Time[2]	Full		1.2		μs
OUT-OF-RANGE RECOVERY TIME	Full		2		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Wake-up time is dependent on the value of the decoupling capacitors.

TIMING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, f_S = 185 MSPS, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and default SPI, unless otherwise noted.

Table 5.

Parameter	Description	Min	Typ	Max	Unit
SYNC TIMING REQUIREMENTS					
t_{SSYNC}	SYNC to rising edge of CLK setup time		0.24		ns
t_{HSYNC}	SYNC to rising edge of CLK hold time		0.40		ns
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	SCLK pulse width high	10			ns
t_{LOW}	SCLK pulse width low	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

Timing Diagrams

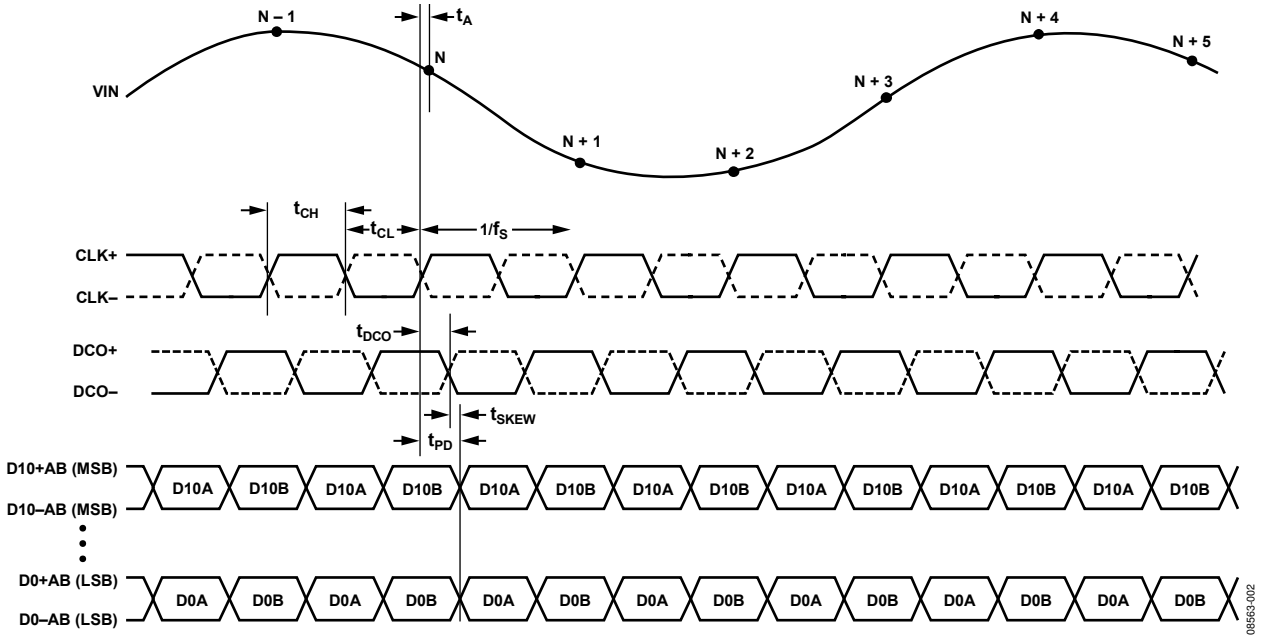

Figure 2. Data Output Timing

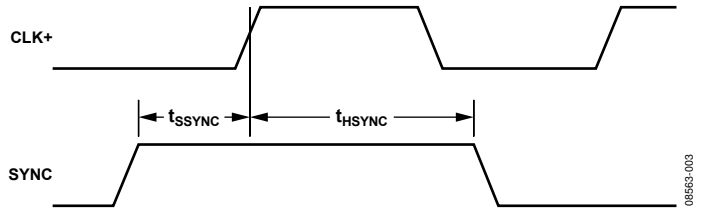

Figure 3. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+x, VIN−x to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to AVDD + 0.2 V
VCMx to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.2 V
SCLK to AGND	−0.3 V to DRVDD + 0.2 V
SDIO to AGND	−0.3 V to DRVDD + 0.2 V
PDWN to AGND	−0.3 V to DRVDD + 0.2 V
MODE to AGND	−0.3 V to DRVDD + 0.2 V
Digital Outputs to AGND	−0.3 V to DRVDD + 0.2 V
DCO+AB, DCO−AB to AGND	−0.3 V to DRVDD + 0.2 V
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The values in Table 7 are per JEDEC JESD51-7 plus JEDEC JESD25-5 for a 2S2P test board. Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown in Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Table 7.

Package Type	Airflow Velocity	θ_{JA}[1]	θ_{JC}[2]	θ_{JB}[3]	Unit
144-Ball CSP_BGA, 10 mm × 10 mm (BC-144-1)	0 m/s	26.9	8.9	6.6	°C/W
	1 m/s	24.2			
	2.5 m/s	23.0			

[1] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[2] Per MIL-STD 883, Method 1012.1.
[3] Per JEDEC JESD51-8 (still air).

The values in Table 8 are from simulations. The PCB is a JEDEC multilayer board. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine whether they are similar to those assumed in these calculations.

Table 8.

Package Type	Airflow Velocity	Ψ_{JB}	Ψ_{JT}	Unit
144-Ball CSP_BGA, 10 mm × 10 mm (BC-144-1)	0 m/s	14.4	0.23	°C/W
	1 m/s	14.0	0.50	
	2.5 m/s	13.9	0.53	

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12
A	AGND	DNC	DNC	AGND	AVDD	CLK–	CLK+	AVDD	AGND	VIN–B	VIN+B	AGND
B	AGND	AGND	DNC	AGND	AVDD	AVDD	AVDD	AVDD	AGND	VCMB	AGND	AGND
C	DNC	AGND	AGND	CSB	SDIO	SCLK	PDWN	SYNC	MODE	AGND	AGND	VIN+A
D	DNC	DNC	AGND	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AGND	VCMA	VIN–A
E	AGND	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AGND
F	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
G	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND
H	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD
J	DNC	DNC	DNC	DNC	DNC	DNC	D0–AB	D2–AB	D4–AB	D6–AB	D8–AB	D10–AB
K	DNC	DNC	DNC	DNC	DNC	DNC	D0+AB	D2+AB	D4+AB	D6+AB	D8+AB	D10+AB
L	DNC	DNC	DNC	DNC	DNC	DNC	D1–AB	D3–AB	D5–AB	D7–AB	D9–AB	DCO–AB
M	DNC	DNC	DNC	DNC	DNC	DNC	D1+AB	D3+AB	D5+AB	D7+AB	D9+AB	DCO+AB

08563-004

Figure 4. Pin Configuration (Top View)

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A5, A8, B5, B6, B7, B8, D4, D5, D6, D7, D8, D9, E2, E3, E4, E5, E6, E7, E8, E9, E10, E11	AVDD	Supply	Analog Power Supply (1.8 V Nominal)
A1, A4, A9, A12, B1, B2, B4, B9, B11, B12, C2, C3, C10, C11, D3, D10, E1, E12, F1, F2, F3, F4, F5, F6, F7, F8, F9, F10, F11, F12	AGND	Ground	Analog Ground
H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal)
G1, G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, G12	DRGND	Ground	Digital Output Driver Ground
A7	CLK+	Input	ADC Clock Input—True
A6	CLK–	Input	ADC Clock Input—Complement
C12	VIN+A	Input	Differential Analog Input Pin (+) for Channel A
D12	VIN–A	Input	Differential Analog Input Pin (–) for Channel A
D11	VCMA	Output	Common-Mode Level Bias Output for Analog Input Channel A
A11	VIN+B	Input	Differential Analog Input Pin (+) for Channel B
A10	VIN–B	Input	Differential Analog Input Pin (–) for Channel B
B10	VCMB	Output	Common-Mode Level Bias Output for Analog Input Channel B
A2, A3, B3, C1, D1, D2, J1 to J6, K1 to K6, L1 to L6, M1 to M6	DNC		Do Not Connect
K7	D0+AB	Output	Channel A and Channel B LVDS Output Data 0—True
J7	D0–AB	Output	Channel A and Channel B LVDS Output Data 0—Complement
M7	D1+AB	Output	Channel A and Channel B LVDS Output Data 1—True
L7	D1–AB	Output	Channel A and Channel B LVDS Output Data 1—Complement

Pin No.	Mnemonic	Type	Description
K8	D2+AB	Output	Channel A and Channel B LVDS Output Data 2—True
J8	D2−AB	Output	Channel A and Channel B LVDS Output Data 2—Complement
M8	D3+AB	Output	Channel A and Channel B LVDS Output Data 3—True
L8	D3−AB	Output	Channel A and Channel B LVDS Output Data 3—Complement
K9	D4+AB	Output	Channel A and Channel B LVDS Output Data 4—True
J9	D4−AB	Output	Channel A and Channel B LVDS Output Data 4—Complement
M9	D5+AB	Output	Channel A and Channel B LVDS Output Data 5—True
L9	D5−AB	Output	Channel A and Channel B LVDS Output Data 5—Complement
K10	D6+AB	Output	Channel A and Channel B LVDS Output Data 6—True
J10	D6−AB	Output	Channel A and Channel B LVDS Output Data 6—Complement
M10	D7+AB	Output	Channel A and Channel B LVDS Output Data 7—True
L10	D7−AB	Output	Channel A and Channel B LVDS Output Data 7—Complement
K11	D8+AB	Output	Channel A and Channel B LVDS Output Data 8—True
J11	D8−AB	Output	Channel A and Channel B LVDS Output Data 8—Complement
M11	D9+AB	Output	Channel A and Channel B LVDS Output Data 9—True
L11	D9−AB	Output	Channel A and Channel B LVDS Output Data 9—Complement
K12	D10+AB	Output	Channel A and Channel B LVDS Output Data 10—True
J12	D10−AB	Output	Channel A and Channel B LVDS Output Data 10—Complement
M12	DCO+AB	Output	Data Clock LVDS Output for Channel A and Channel B—True
L12	DCO−AB	Output	Data Clock LVDS Output for Channel A and Channel B—Complement
C9	MODE	Input	Mode Select Pin (Logic Low Enables NSR; Logic High Disables NSR)
C8	SYNC	Input	Digital Synchronization Pin
C7	PDWN	Input	Power-Down Input (Active High)
C6	SCLK	Input	SPI Clock
C5	SDIO	Input/Output	SPI Data
C4	CSB	Input	SPI Chip Select (Active Low)

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, sample rate = 185 MSPS, 1.75 V p-p differential input, VIN = −1.0 dBFS, 32k sample, T_A = 25°C, unless otherwise noted.

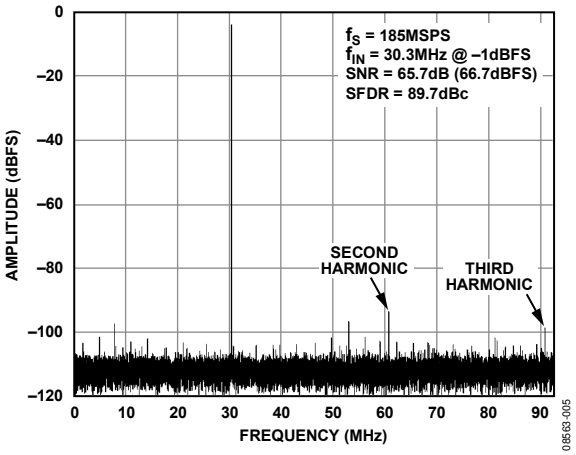

Figure 5. Single-Tone FFT with f_{IN} = 30.3 MHz

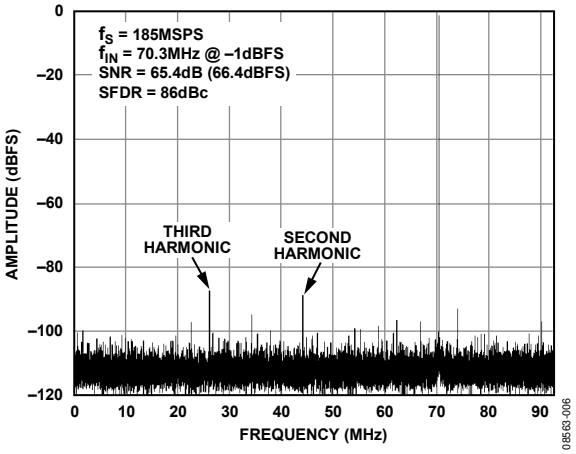

Figure 6. Single-Tone FFT with f_{IN} = 70.3 MHz

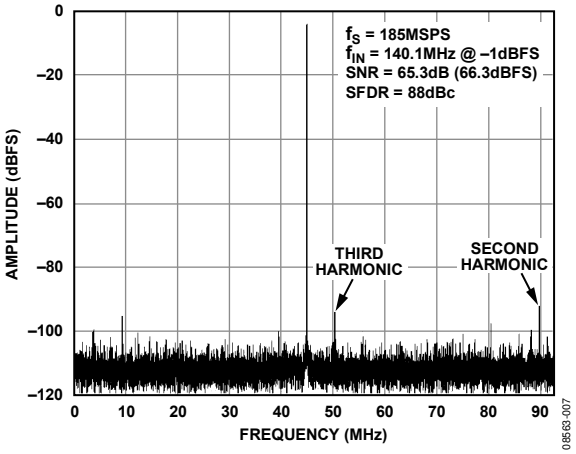

Figure 7. Single-Tone FFT with f_{IN} = 140.1 MHz

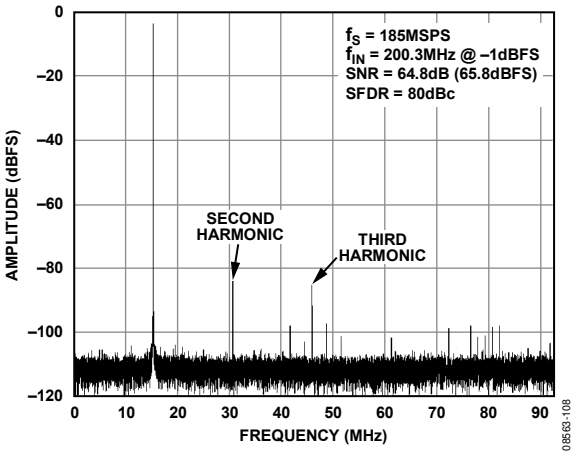

Figure 8. Single-Tone FFT with f_{IN} = 200.3 MHz

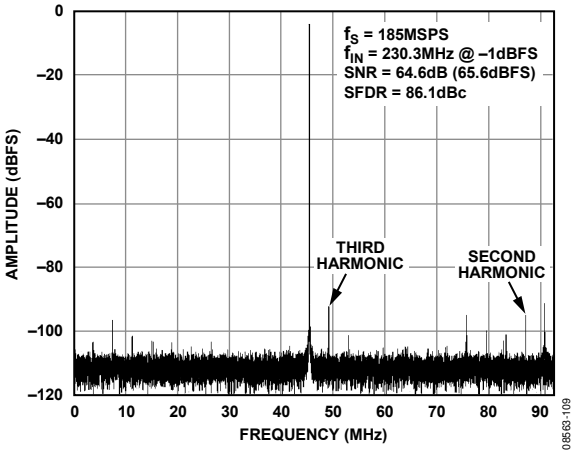

Figure 9. Single-Tone FFT with f_{IN} = 230.3 MHz

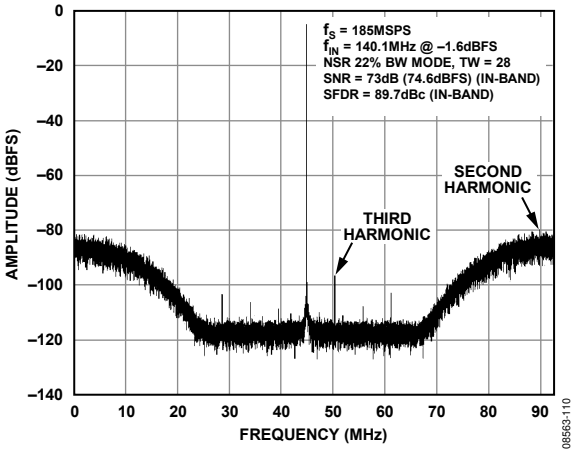

Figure 10. Single-Tone FFT with f_{IN} = 140.1 MHz, NSR Enabled in 22% BW Mode with Tuning Word = 28

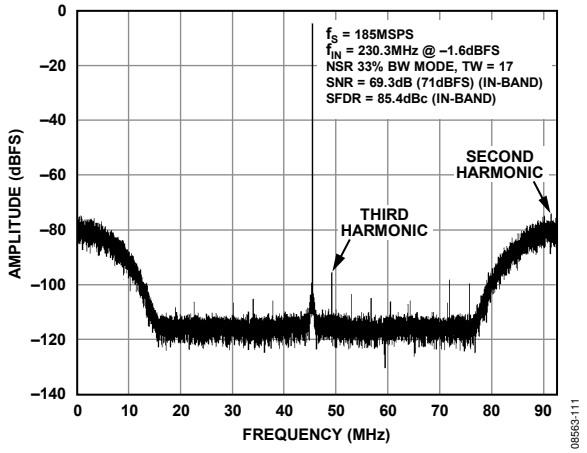

Figure 11. Single-Tone FFT with f_{IN} = 230.3 MHz, NSR Enabled in 33% BW Mode with Tuning Word = 17

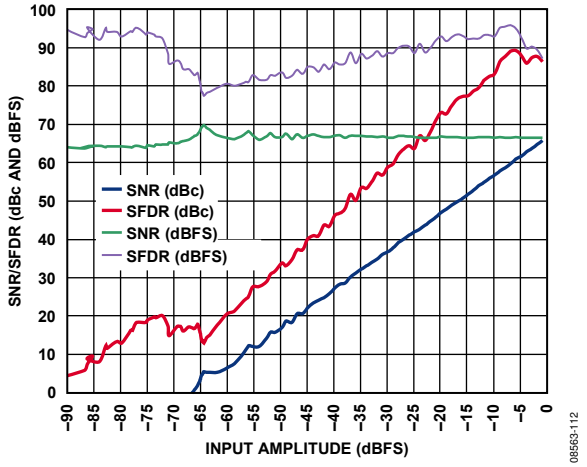

Figure 12. Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 70.3 MHz

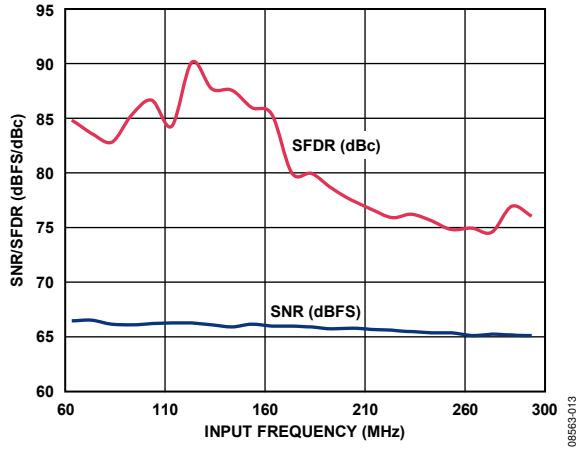

Figure 13. Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) with 1.75 V p-p Full Scale

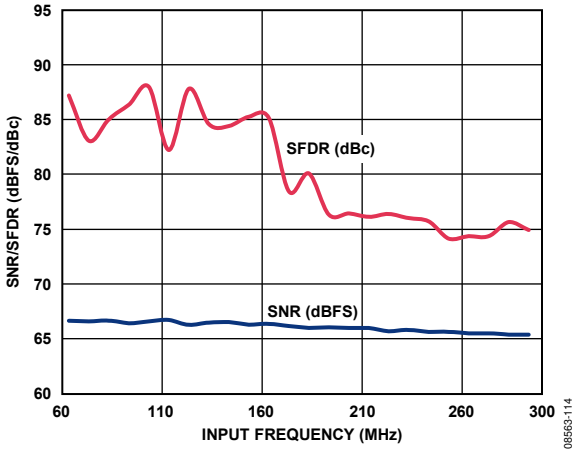

Figure 14. Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) with 2.0 V p-p Full Scale

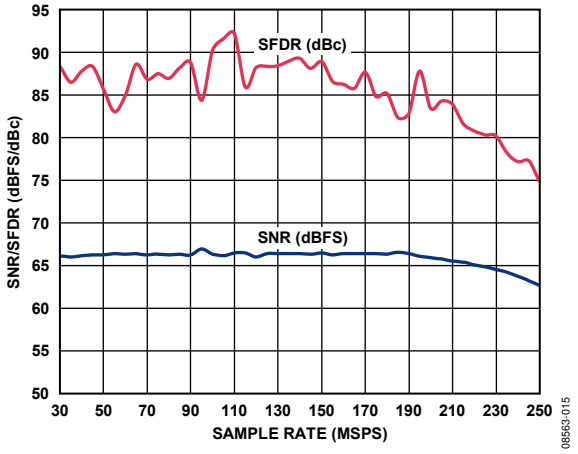

Figure 15. Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 70.1 MHz

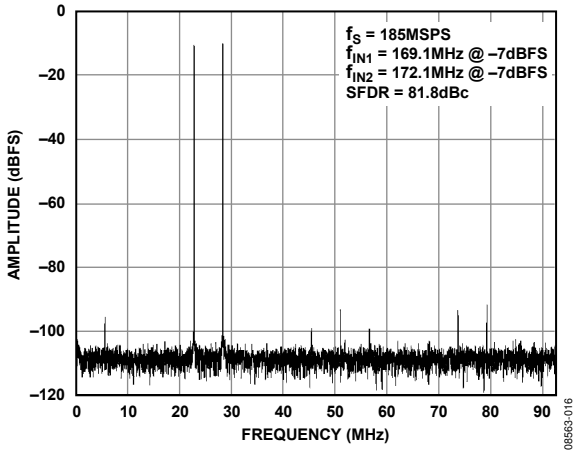

Figure 16. Two-Tone FFT with f_{IN1} = 169.1 MHz and f_{IN2} = 172.1 MHz

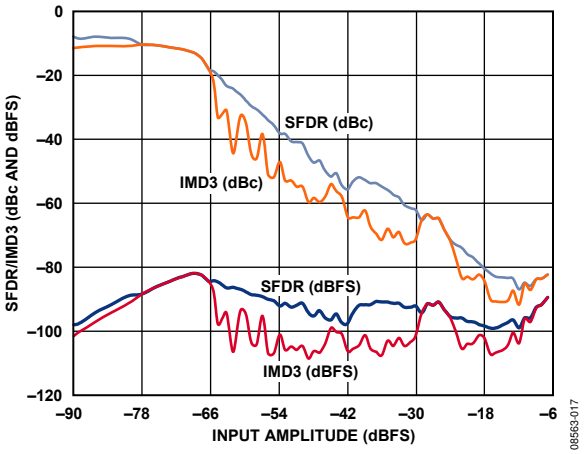

Figure 17. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 169.1 MHz and f_{IN2} = 172.1 MHz

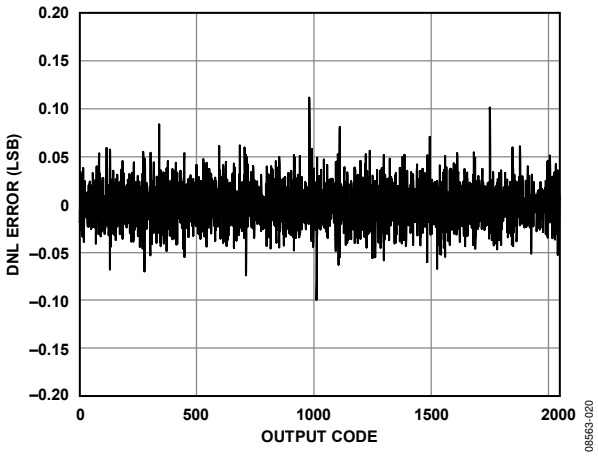

Figure 20. DNL with f_{IN} = 30.3 MHz

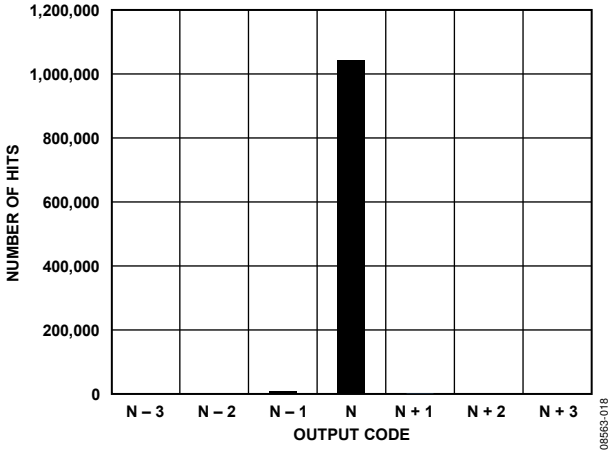

Figure 18. Grounded Input Histogram

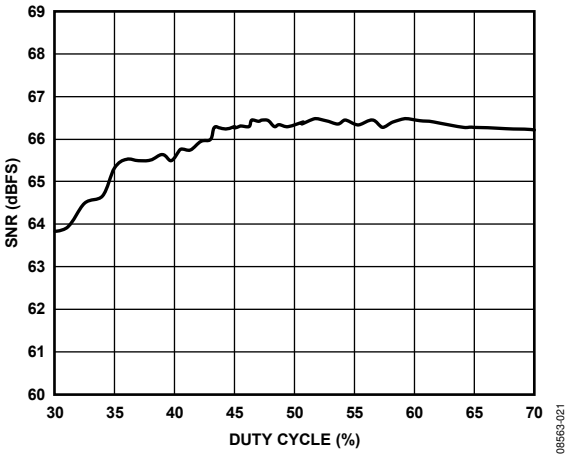

Figure 21. SNR vs. Duty Cycle with f_{IN} = 10.3 MHz

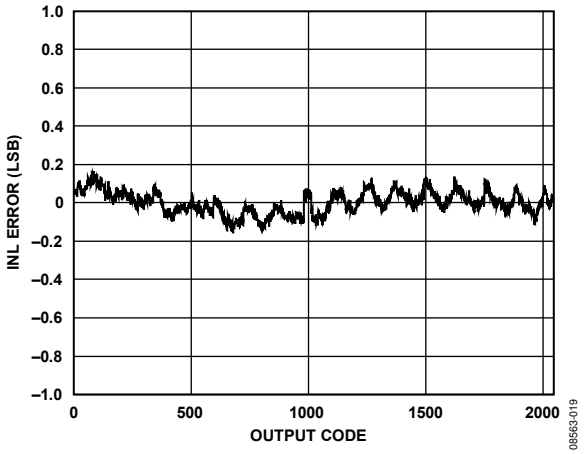

Figure 19. INL with f_{IN} = 30.3 MHz

EQUIVALENT CIRCUITS

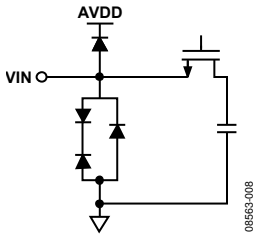

Figure 22. Equivalent Analog Input Circuit

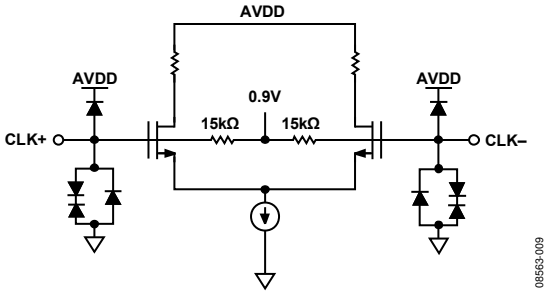

Figure 23. Equivalent Clock Input Circuit

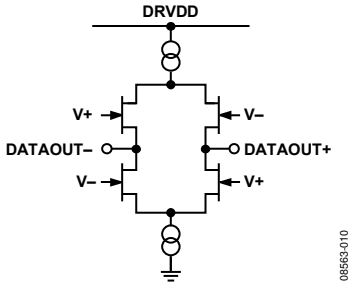

Figure 24. Equivalent LVDS Output Circuit

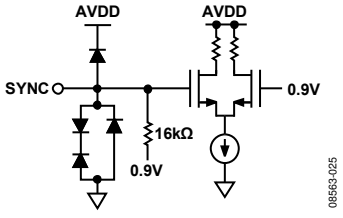

Figure 25. Equivalent SYNC Input Circuit

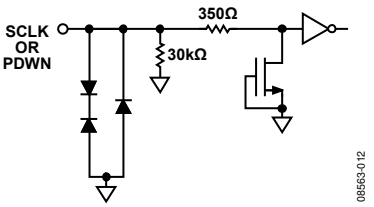

Figure 26. Equivalent SCLK and PDWN Input Circuit

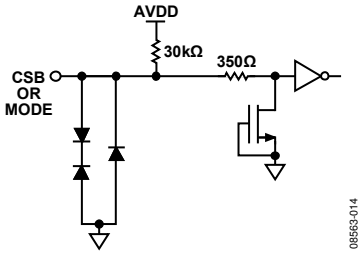

Figure 27. Equivalent CSB and MODE Input Circuit

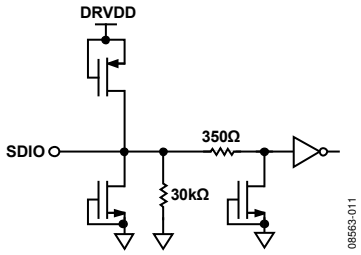

Figure 28. Equivalent SDIO Circuit

THEORY OF OPERATION

ADC ARCHITECTURE

The AD6642 architecture consists of dual front-end sample-and-hold circuits, followed by pipelined, switched-capacitor ADCs. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. Alternately, the 14-bit result can be processed through the noise shaping requantizer (NSR) block before it is sent to the digital correc-tion logic.

The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjust-ment of the output drive current. During power-down, the output buffers go into a high impedance state.

The AD6642 dual IF receiver can simultaneously digitize two channels, making it ideal for diversity reception and digital pre-distortion (DPD) observation paths in telecommunication systems.

Synchronization capability is provided to allow synchronized timing between multiple channels or multiple devices.

Programming and control of the AD6642 are accomplished using a 3-wire SPI-compatible serial interface.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6642 is a differential switched-capacitor circuit that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see Figure 29). When the input is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within 1/2 of a clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, any shunt capacitors should be reduced. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. For more information on this subject, see Application Note AN-742, *Frequency Domain Response of Switched-Capacitor ADCs*; Application Note AN-827, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters" (see www.analog.com).

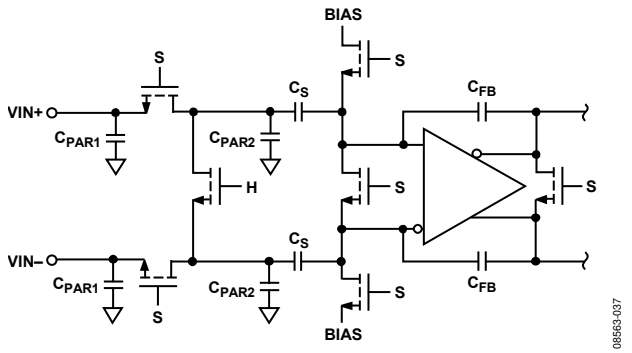

Figure 29. Switched-Capacitor Input

For best dynamic performance, the source impedances driving the VIN+ and VIN− pins should be matched.

An internal differential reference buffer creates positive and negative reference voltages that define the input span of the ADC core. The span of the ADC core is set by this buffer to 2 × V_{REF}.

Input Common Mode

The analog inputs of the AD6642 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. An on-board common-mode voltage reference is included in the design and is available from the VCMx pins. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCMx pin voltage (typically 0.5 × AVDD). The VCMx pins must be decoupled to ground by a 0.1 µF capacitor.

Differential Input Configurations

Optimum performance is achieved when driving the AD6642 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, and ADA4938-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4938-2 is easily set with the VCMx pin of the AD6642 (see Figure 30), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

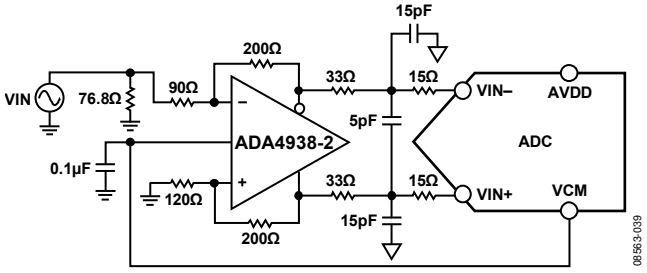

Figure 30. Differential Input Configuration Using the ADA4938-2

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 31. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

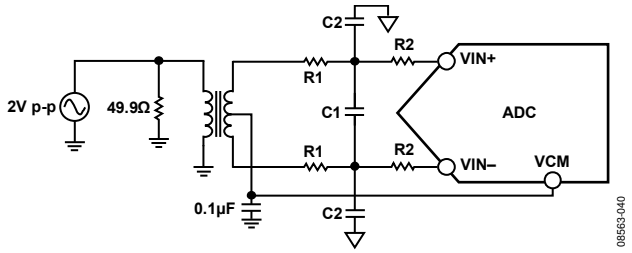

Figure 31. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz (MHz). Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD6642. For applications in which SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 32). In this configuration, the input is ac-coupled and the CML is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 10 lists recommended values to set the RC network. At higher input frequencies, good performance can be achieved by using a ferrite bead in series with a resistor and removing the capacitors. However, these values are dependent on the input signal and should be used only as a starting guide.

Table 10. Example RC Network

Frequency Range (MHz)	R1 Series (Each)	C1 Differential	R2 Series (Each)	C2 Shunt (Each)
0 to 100	33 Ω	5 pF	15 Ω	15 pF
100 to 200	10 Ω	5 pF	10 Ω	10 pF
100 to 300	10 Ω[1]	Remove	66 Ω	Remove

[1] In this configuration, R1 is a ferrite bead with a value of 10 Ω @ 100 MHz.

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use the AD8352 differential driver (see Figure 33). For more information, see the AD8352 data sheet.

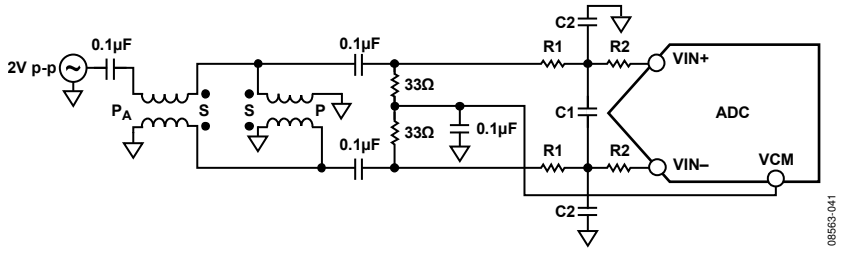

Figure 32. Differential Double Balun Input Configuration

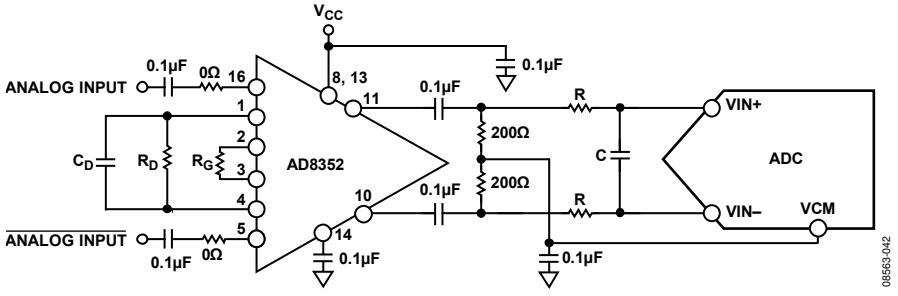

Figure 33. Differential Input Configuration Using the AD8352

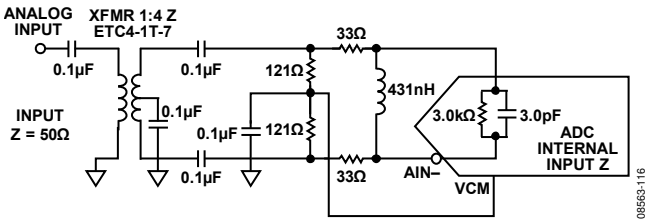

Figure 34. 1:4 Transformer Passive Configuration

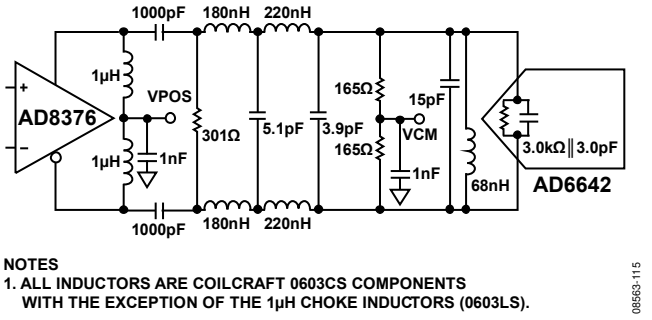

Figure 35. Active Front-End Configuration Using the AD8376

For the popular IF band of 140 MHz, Figure 34 shows an example of a 1:4 transformer passive configuration where a differential inductor is used to resonate with the internal input capacitance of the AD6642. This configuration realizes excellent noise and distortion performance. Figure 35 shows an example of an active front-end configuration using the AD8376 dual VGA. This configuration is recommended when signal gain is required.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD6642 sample clock inputs, CLK+ and CLK–, should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally (see Figure 36) and require no external bias.

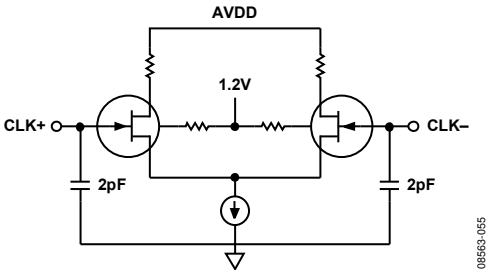

Figure 36. Equivalent Clock Input Circuit

Clock Input Options

The AD6642 has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern (see the Jitter Considerations section).

Figure 37 and Figure 38 show two preferred methods for clocking the AD6642 (at clock rates up to 625 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF balun or an RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 625 MHz, and the RF transformer configuration is recommended for clock frequencies from 10 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer/balun secondary limit clock excursions into the AD6642 to approximately 0.8 V p-p differential.

This limit helps to prevent the large voltage swings of the clock from feeding through to other portions of the AD6642 while preserving the fast rise and fall times of the signal that are critical to a low jitter performance.

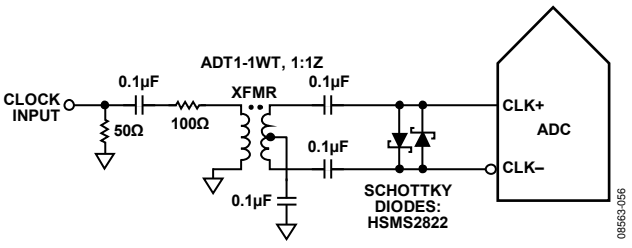

Figure 37. Transformer-Coupled Differential Clock (Up to 200 MHz)

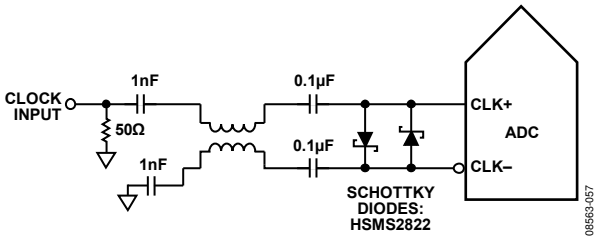

Figure 38. Balun-Coupled Differential Clock (Up to 625 MHz)

If a low jitter clock source is not available, another option is to ac-couple a differential PECL signal to the sample clock input pins, as shown in Figure 39. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516 clock drivers offer excellent jitter performance.

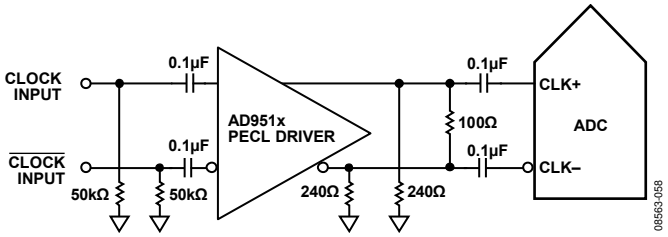

Figure 39. Differential PECL Sample Clock (Up to 625 MHz)

A third option is to ac-couple a differential LVDS signal to the sample clock input pins, as shown in Figure 40. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516 clock drivers offer excellent jitter performance.

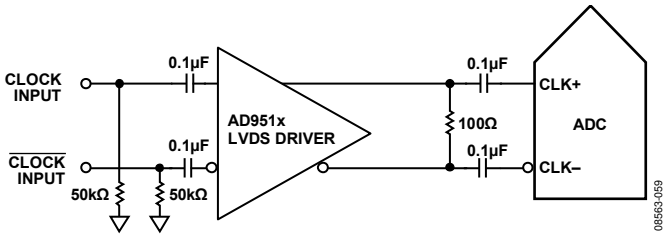

Figure 40. Differential LVDS Sample Clock (Up to 625 MHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, the CLK+ pin should be driven directly from a CMOS gate, and the CLK– pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 41).

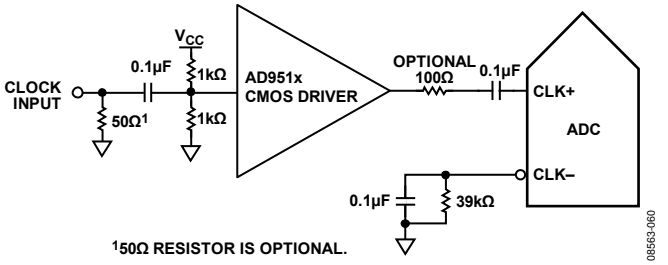

Figure 41. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

CLK+ can be driven directly from a CMOS gate. Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages of up to 3.6 V, making the selection of the drive logic voltage very flexible (see Figure 42).

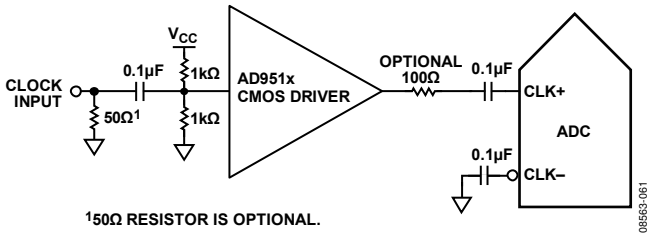

Figure 42. Single-Ended 3.3 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD6642 contains an input clock divider with the ability to divide the input clock by integer values from 1 to 8.

The AD6642 clock divider can be synchronized using the external SYNC input. Bit 1 of Register 0x3A enables the clock divider to be resynchronized on every SYNC signal. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD6642 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD6642. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS enabled.

Jitter in the rising edge of the input is still of paramount concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 40 MHz nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time period that the loop is not locked, the DCS loop is bypassed, and internal device timing is dependent on the duty cycle of the input clock signal.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR from the low frequency SNR (SNR_{LF}) at a given input frequency (f_{IN}) due to jitter (t_{JRMS}) can be calculated by

$$SNR_{HF} = -10\log[(2\pi \times f_{IN} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the clock input jitter specification. IF undersampling applications are particularly sensitive to jitter, as illustrated in Figure 43.

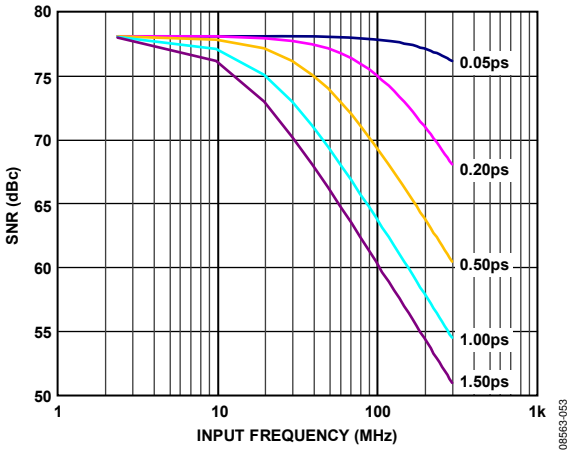

Figure 43. SNR vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases in which aperture jitter may affect the dynamic range of the AD6642. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock at the last step. Refer to Application Note AN-501 and Application Note AN-756 for more information about jitter performance as it relates to ADCs (see www.analog.com).

POWER DISSIPATION AND STANDBY MODE

The power dissipated by the AD6642 is proportional to its clock rate (see Figure 44). The digital power dissipation does not vary significantly because it is determined primarily by the DRVDD supply and the bias current of the LVDS drivers.

Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 44 was taken using the same operating conditions as those used in the Typical Performance Characteristics section, with a 5 pF load on each output driver.

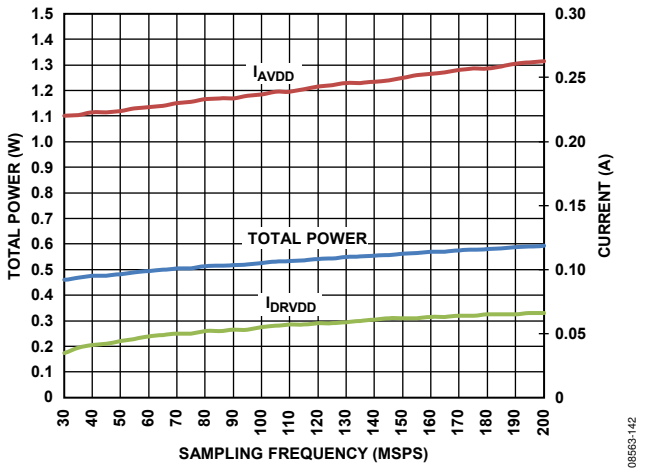

Figure 44. Power and Current vs. Sampling Frequency

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD6642 is placed in power-down mode. In this state, the ADC typically dissipates 4.5 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD6642 to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode; shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map Register Descriptions section for more details.

CHANNEL/CHIP SYNCHRONIZATION

The AD6642 has a SYNC input that offers the user flexible synchronization options for synchronizing the clock divider. The clock divider sync feature is useful for guaranteeing synchronized sample clocks across multiple ADCs.

The SYNC input is internally synchronized to the sample clock; however, to ensure that there is no timing uncertainty between multiple parts, the SYNC input signal should be externally synchronized to the input clock signal, meeting the setup and hold times shown in Table 5. The SYNC input should be driven using a single-ended CMOS-type signal.

DIGITAL OUTPUTS

The AD6642 output drivers are configured to interface with LVDS outputs using a DRVDD supply voltage of 1.8 V. The output bits are DDR LVDS as shown in Figure 2. Applications that require the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

As described in Application Note AN-877, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary or twos complement when using the SPI control.

TIMING

The AD6642 provides latched data with a latency of nine clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD6642. These transients can degrade converter dynamic performance.

The lowest typical conversion rate of the AD6642 is 40 MSPS. At clock rates below 40 MSPS, dynamic performance can degrade.

Data Clock Output (DCO)

The AD6642 provides a data clock output (DCO) signal intended for capturing the data in an external register. The output data for Channel A is valid when DCO is high; the output data for Channel B is valid when DCO is low. See Figure 2 for a graphical timing description.

Table 11. Output Data Format

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode
VIN+ − VIN−	$< -V_{REF} - 0.5$ LSB	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ − VIN−	$= -V_{REF}$	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ − VIN−	= 0	1000 0000 0000 0000	0000 0000 0000 0000
VIN+ − VIN−	$= +V_{REF} - 1.0$ LSB	1111 1111 1111 1111	0111 1111 1111 1111
VIN+ − VIN−	$> +V_{REF} - 0.5$ LSB	1111 1111 1111 1111	0111 1111 1111 1111

NOISE SHAPING REQUANTIZER (NSR)

The AD6642 features a noise shaping requantizer (NSR) to allow higher than 11-bit SNR to be maintained in a subset of the Nyquist band. The harmonic performance of the receiver is unaffected by the NSR feature. When enabled, the NSR contributes an additional 0.6 dB of loss to the input signal, such that a 0 dBFS input is reduced to −0.6 dBFS at the output pins.

The NSR feature can be independently controlled per channel via the SPI or the MODE pin.

Two different bandwidth modes are provided; the mode can be selected from the SPI port. In each of the two modes, the center frequency of the band can be tuned such that IFs can be placed anywhere in the Nyquist band.

22% BW MODE (>40 MHZ @ 184.32 MSPS)

The first bandwidth mode offers excellent noise performance over 22% of the ADC sample rate (44% of the Nyquist band) and can be centered by setting the NSR mode bits in the NSR control register (Address 0x3C) to 000. In this mode, the useful frequency range can be set using the 6-bit tuning word in the NSR tuning register (Address 0x3E). There are 57 possible tuning words (TW); each step is 0.5% of the ADC sample rate. The following three equations describe the left band edge (f_0), the channel center (f_{CENTER}), and the right band edge (f_1), respectively.

$$f_0 = f_{ADC} \times .005 \times TW$$

$$f_{CENTER} = f_0 + 0.11 \times f_{ADC}$$

$$f_1 = f_0 + 0.22 \times f_{ADC}$$

Figure 45 to Figure 47 show the typical spectrum that can be expected from the AD6642 in the 22% BW mode for three different tuning words.

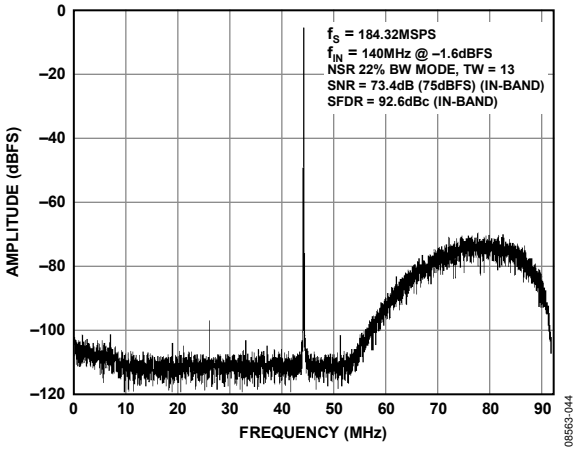

Figure 45. 22% BW Mode, Tuning Word = 13

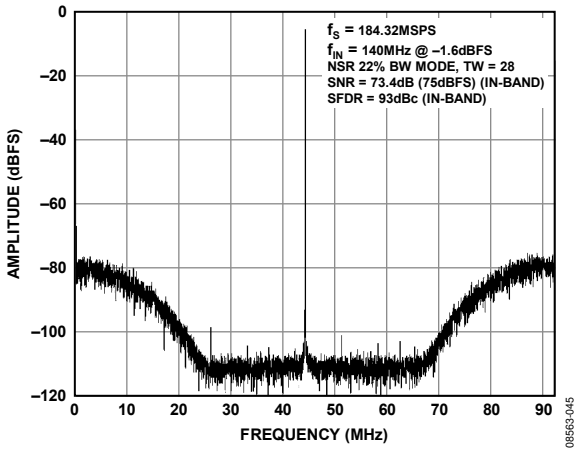

Figure 46. 22% BW Mode, Tuning Word = 28 (f_S/4 Tuning)

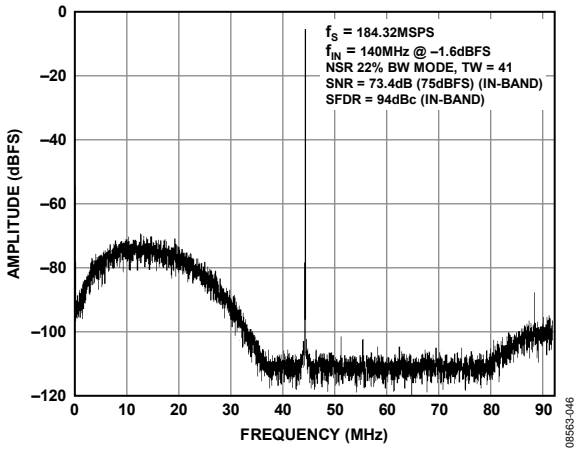

Figure 47. 22% BW Mode, Tuning Word = 41

33% BW MODE (>60 MHZ @ 184.32 MSPS)

The second bandwidth mode offers excellent noise performance over 33% of the ADC sample rate (66% of the Nyquist band) and can be centered by setting the NSR mode bits in the NSR control register (Address 0x3C) to 001. In this mode, the useful frequency range can be set using the 6-bit tuning word in the NSR tuning register (Address 0x3E). There are 34 possible tuning words (TW); each step is 0.5% of the ADC sample rate. The following three equations describe the left band edge (f_0), the channel center (f_{CENTER}), and the right band edge (f_1), respectively.

$$f_0 = f_{ADC} \times .005 \times TW$$

$$f_{CENTER} = f_0 + 0.165 \times f_{ADC}$$

$$f_1 = f_0 + 0.33 \times f_{ADC}$$

Figure 48 to Figure 50 show the typical spectrum that can be expected from the AD6642 in the 33% BW mode for three different tuning words.

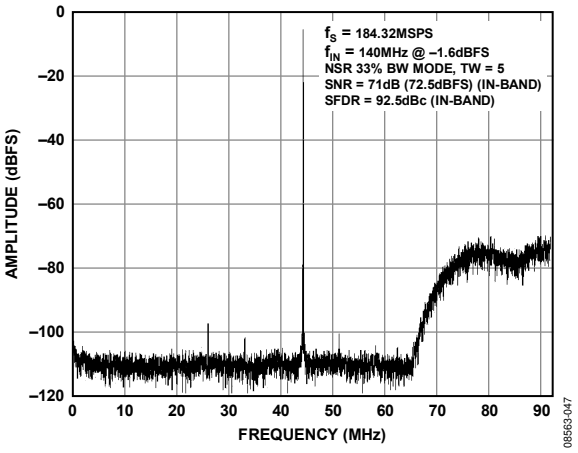

Figure 48. 33% BW Mode, Tuning Word = 5

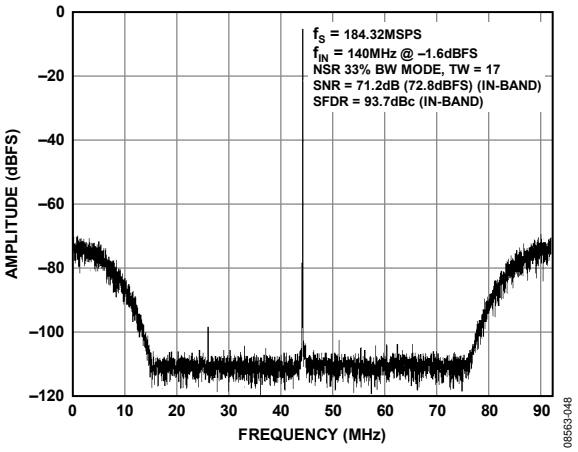

Figure 49. 33% BW Mode, Tuning Word = 17 (f_S/4 Tuning)

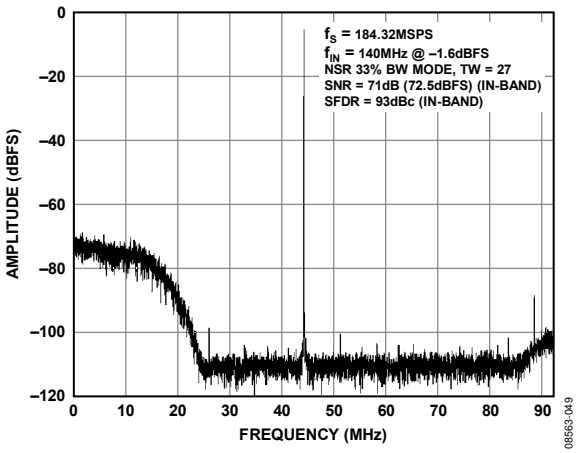

Figure 50. 33% BW Mode, Tuning Word = 27

MODE PIN

The MODE pin input allows convenient control of the NSR feature. A logic low enables NSR mode and a logic high sets the receiver to straight 11-bit mode with NSR disabled. By default, the MODE pin is pulled high internally to disable the NSR. Each channel can be individually configured to ignore the MODE pin state by writing to Bit 4 of the NSR control register at Address 0x3C. Use of the NSR control register in conjunction with the MODE pin allows for very flexible control of the NSR feature on a per-channel basis.

BUILT-IN SELF-TEST (BIST) AND OUTPUT TEST

The AD6642 includes built-in test features designed to verify the integrity of each channel and to facilitate board-level debugging. A BIST (built-in self-test) feature is included that verifies the integrity of the digital datapath of the AD6642. Various output test options are also provided to place predictable values on the outputs of the AD6642.

BUILT-IN SELF-TEST (BIST)

The BIST is a thorough test of the digital portion of the selected AD6642 signal path. When enabled, the test runs from an internal pseudorandom noise (PN) source through the digital datapath starting at the ADC block output. The BIST sequence runs for 512 cycles and stops. The BIST signature value for the selected channel is written to Register 0x24 and Register 0x25. If one channel is selected, its BIST signature is written to the two registers. If Channel A and Channel B are both selected, the results from Channel A are written to the BIST signature registers.

The outputs are not disconnected during this test, so the PN sequence can be observed as it runs. The PN sequence can be continued from its last value or reset from the beginning, based on the value programmed in Register 0x0E, Bit 2. The BIST signature result varies based on the channel configuration.

OUTPUT TEST MODES

The output test options are shown in Table 13. When an output test mode is enabled, the analog section of the receiver is disconnected from the digital back-end blocks, and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting. The seed value for the PN sequence tests can be forced if the PN reset bits are used to hold the generator in reset mode by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they require an encode clock. For more information, see Application Note AN-877, *Interfacing to High Speed ADCs via SPI*.